Features

- **Operates as Host Bridge Between Serial ATA and Parallel ATA interfaces**
- **Ultra ATA100 Mode Supported with Rates up to 100 MB/s**
- **Data is Transferred on Both Edges of the STROBE when in Ultra DMA Mode**
- **16-bit CRC is Calculated on a Per-burst Basis**
- **Ultra DMA5 Compliant Drive Interfaces**
- **Compatible with 48-bit LBA Methods of Addressing**
- **Dual 1024-byte Transmit/Receive FIFO for Overrun Prevention**
- **8B/10B Encoding and Decoding in Serial ATA Link Layer**
- **Low Power: < 380 mW**
- **Supports PIO Modes 0, 1, 2, 3 and 4**
- **Supports UDMA Modes 0, 1, 2, 3, 4, and 5**
- **Supports 80-conductor Cable for UDMA Modes 4, and 5**

Overview

The AT78C5009 SATA Controller bridges the conventional Parallel ATA devices with Serial ATA PHY transceivers. It includes a Serial ATA Link layer, a Transport layer, a Command Layer, two 256 x 32 FIFOs and an IDE Host/Target Controller, a Serial ATA Core and an IDE Controller, and is fully compliant with Serial ATA Gen1. The PHY block is connected to the ATA block by a 20-bit transmit and a 20-bit receive data bus. This host bridge is intended to adapt a Serial ATA Device interface to an Ultra ATA100 Host interface. Ultra DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED, and PACKET commands.

Serial ATA Host Bridge

AT78C5009

Summary

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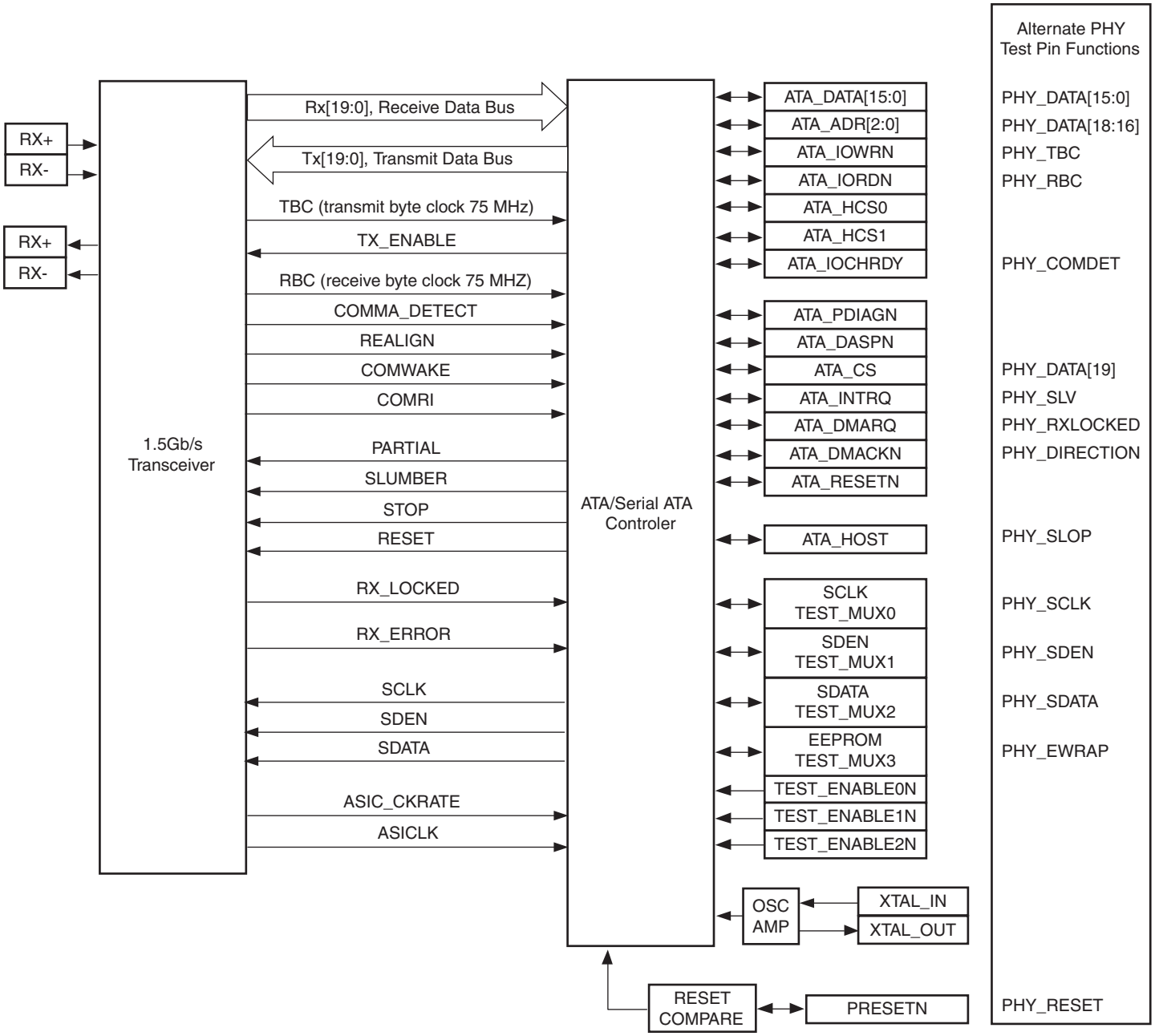
Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

Figure 1. AT78C5009 Block/PAD Interconnect



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