

## Features

- General
  - Serial ATA Rev.1.0a Compliant Gen1 Physical Layer
  - 150 MHz Frequency Synthesizer for ASIC Clock Generation
  - Built-in Transmission PLL Circuits
  - Parallel 10b interface
  - Optional 20-bit Transmit Data (Two 10-bit 8b/10b Encoded Characters)
  - Bi-directional TBC (Transmit Byte Clock)
  - 25 MHz Crystal Oscillator
  - Read/Write Serial Port Interface to Program Transmission and Receive Characteristics
  - Power Monitor for Glitch-free Power Off/On Cycles
  - Power Management Modes: PARTIAL, SLUMBER, STOP
  - Loop-back Test Modes
  - Device Status to Link Layer
  - Low-power Consumption, about 100 mW (Core, Typical)
  - Operates at 1.8V Supply Voltage
- Transmitter
  - Transmission Speed of 1.5 Gb/s Differential NRZ Serial Stream
  - Provides a 100Ω Matched Differential Termination at the Transmitter
  - Serialize 10-bit or 20-bit Parallel Input from Link Layer
  - Spread-spectrum Modulation for TX PLL Clock with +0/-0.5% Slow Frequency Variation Over a 33.33 μs Up/Down Triangular Wave Period
  - DC or AC Coupled to SATA Cable
  - Pre-emphasis Control Via Serport
- Receiver
  - 1.5 Gb/s Differential NRZ Serial Stream
  - 100Ω Matched Differential Termination at Receiver
  - Passive Equalization in Receive Input Buffer
  - Extract Data and Clock from Serial Stream
  - De-serialize Serial Stream into 10-bit or 20-bit Parallel Data
  - Detection of K28.5 Comma Character to Provide Word Aligned 10-bit or 20-bit Parallel Output
  - Squelch Detector
  - OOB Signal Detection for COMWAKE, COMINIT/COMRESET
  - DC or AC Coupled to SATA Cable
  - Built-in Clock Recovery PLL for De-serializer and Decoder Circuits
  - Accommodates Spread Spectrum Clocked Data in CDR (Clock & Data Recovery)

## Overview

The AT78C5081 is a stand-alone Serial ATA physical layer that is designed based on SATA Standard revision 1.0a. The parallel interface to the link layer is based on a 10-bit interface in both rising and falling edges of the clock. The device also accepts two 10-bit 8b/10b encoded transmit characters in parallel and latches them on the rising edge of TBC. The serialized data is transmitted onto the TXP/TXN differential outputs at a baud rate twenty times that of the TBC frequency. The device also samples serial data received on the RXP/RXN differential inputs, recovers the clock and data, de-serializes it into one or two 10-bit receive characters in parallel. The recovered clock is sent out at one twentieth of the incoming data rate. The receiver includes the squelch detector, out of band (OOB) signal detector, and is capable of detecting “Comma” characters. This transceiver contains on-chip PLLs circuitry for synthesis of the transmitting clock and extraction of the clock from the received serial stream. The transmit PLL is also responsible for link layer reference clock generation (ASIC\_CK). The circuit requires only one external component, the reference resistor. An additional on-chip serial port interface is employed to adjust the performance of certain blocks or to



## Serial ATA Physical Layer

### AT78C5081

## Summary

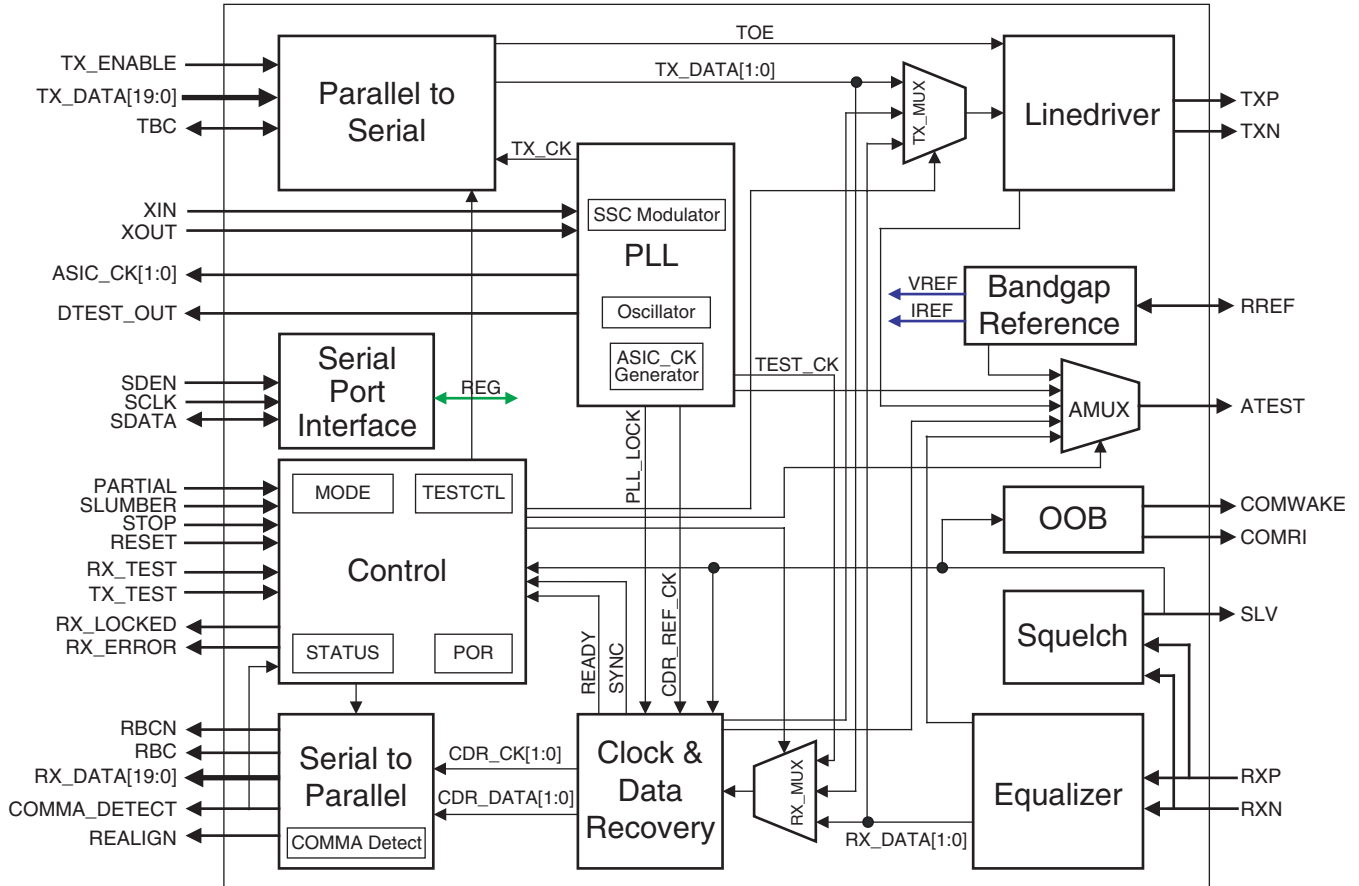
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Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

configure the circuit in certain test modes. The PHY is transparent to SATA traffic and as a result does not perform scrambling/descrambling, encoding/decoding, or run time disparity check. It does not respond to SATA primitives.

## Block Diagram





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