12-bit 500 Msps ADC

AT84AS001

Summary

Features

- **12-bit Resolution**
- **500 Msps Sampling Rate**
- **Full Power Input Bandwidth (–3 dB) > 1.5 GHz**
- **1.1 Vpp Analog Input (Differential Only)**
- **AC or DC Coupled Analog Input with External Control**
- **Differential 100Ω or Single-ended 50Ω PECL/LVDS Compatible Clock Inputs**
- **LVDS Output Compatibility (100Ω)**
- **3-wire Serial Bus Programming Interface**
  - 16-bit Data, 3-bit Address
  - Gain (±1.5 dB Full-scale) Digital Control
  - Offset Digital Control (± 40 LSB)
  - Standby Mode
  - Internal Static Built-In Test (BIST)
- **Synchronous Reset Input**
- **Low Power Consumption: 2.3W**
- **Power Supply: 5V (Analog), 3.3V (Digital, Output)**
- **EBGA 192 Package**

Performances

- **Band Flatness (0.5 dB) from DC up to 250 MHz**
- **10-bit ENOB (at F_{IN} = 250 MHz)**
- **SFDR = 72 dBc, SNR = 62 dBc, at F_S = 500 Msps, F_{IN} = 250 MHz, –1 dB Input Level**
- **2-tone IMD: –70 dBc (240 MHz, 250 MHz) at 500 Msps**
- **DNL = ±0.8 LSB; INL = ±2 LSB (Typical)**

Screening

- **Temperature range:**
  - **Commercial *C* grade 0°C < T_{amb} < 70°C**
  - **Industrial *V* grade –40°C < T_{amb} < 85°C**

Applications

- **Test and Measurement Instrumentation**
- **Radar and Satellite Receiver Subsystems**
- **Wireless and Wired Communications Receivers**
- **High Speed Data Acquisition**
- **Medical Imaging**

For more information, please contact
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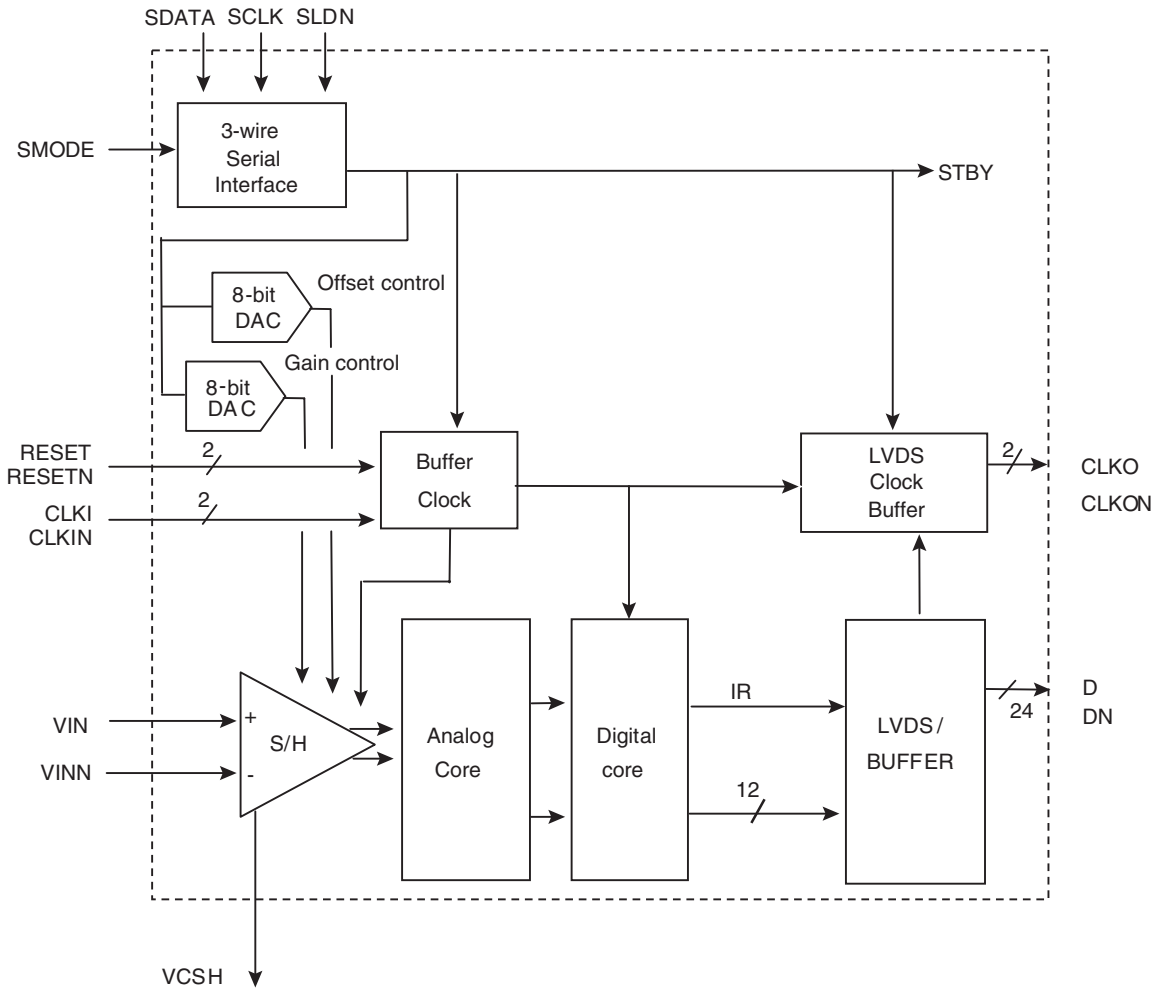
5412BS–BDC–04/06

1. Description

The AT84AS001 is a high performance 12-bit, 500 Msps ADC featuring low power consumption and true 12-bit linearity for IF sampling applications. By using its on-chip S/H circuity and advanced high speed process technology, it allows for sampling rates up to 500 Msps at a center frequency of 150 MHz and IF band of ±100 MHz. Its electrical performance is coupled with ease of integration into new or existing designs by such features as AC or DC coupled analog input, differential LVDS compatible output, 3-wire serial programming interface (gain control, offset control, standby mode and Built-In-Test), Double Data Rate clock output and synchronous reset input.

Figure 1-1. Block Diagram



2. Functional Description

The AT84AS001 is a monolithic 12-bit 500 Msps ADC. The circuit includes an on-chip Sample and Hold (S/H), and a 12-bit analog-to-digital converter core.

The output data is LVDS (100Ω) compliant.

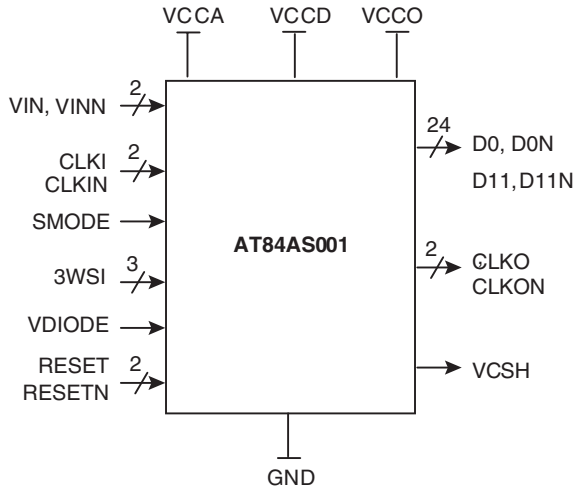
A 3-wire serial interface (3-bit address, 16-bit data) is included to provide several adjustments and controls:

- Gain: ±1.5 dB full-scale digital control (8-bit-control)
- Offset: ±40 LSB digital control (8-bit control)
- Standby mode for power saving

The AT84AS001 features a full-power input bandwidth of 1.5 GHz

Table 2-1. Functional Description

Name	Function
V_{CCA}	Positive analog power supply 5V
V_{CCD}	Positive digital power supply 3.3V
V_{CCO}	Positive output power supply 2.5V or 3.3V
GND	Ground
VIN, VINN	Differential analog inputs
CLKI, CLKIN	Differential clock inputs
CLKO, CLKON	Differential data ready output
<D0:D11>	Positive output data mode LVDS
<D0N:D11N>	Negative output data mode LVDS
RESET; RESETN	Synchronous reset input signal
VDIODE	Diode for die junction temperature monitoring
3WSI	3-wire serial bus interface
VCSH	Common sample and hold voltage
SMODE	3-wire serial bus interface selection

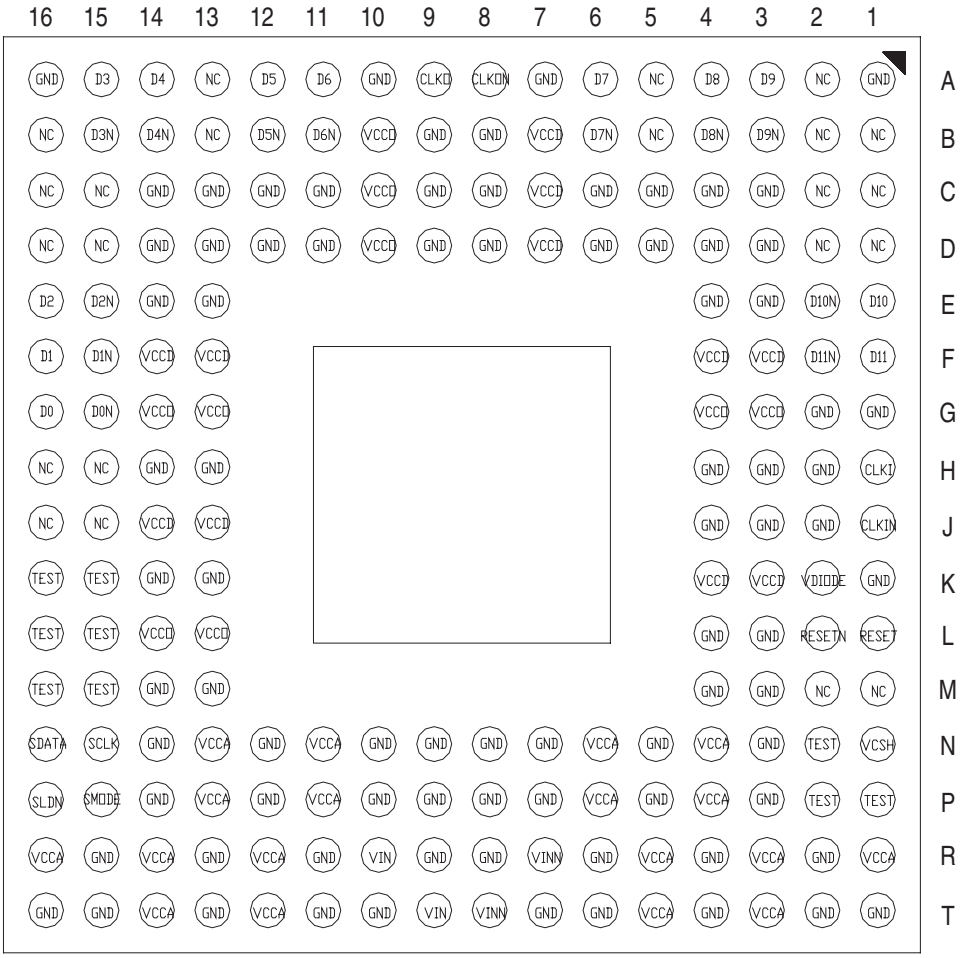


3. AT84AS001 Pinout

Table 3-1. Pinout Table

Pin Number	Symbol	Function
A1, A7, A10, A16, B8, B9, C3, C4, C5, C6, C8, C9, C11, C12, C13, C14, D3, D4, D5, D6, D8, D9, D11, D12, D13, D14, E3, E4, E13, E14, G1, G2, H2, H3, H4, H13, H14, J2, J3, J4, K1, K13, K14, L3, L4, M3, M4, M13, M14, N3, N5, N7, N8, N9, N10, N12, N14, P3, P5, P7, P8, P9, P10, P12, P14, R2, R4, R6, R8, R9, R11, R13, R15, T1, T2, T4, T6, T7, T10, T11, T13, T15, T16	GND	Ground
N4, N6, N11, N13, P4, P6, P11, P13, R1, R3, R5, R12, R14, R16, T3, T5, T12, T14	VCCA	Analog power supply 5V
B7, C7, D7, F3, F4, F13, F14, J13, J14, K3, K4	VCCD	Digital power supply 3.3V
B10, C10, D10, G3, G4, G13, G14, L13, L14	VCCO	Output and 3WSI power supply 3.3V or 2.5V
Inputs		
H1, J1	CLKI, CLKIN	Input clock
T9	VIN	In-phase Analog input (Signal)
T8	VINN	Out-of-phase Analog input (Signal)
R10	VIN	In-phase Analog input (50Ω reverse termination)
R7	VINN	Out-of-phase Analog input (50Ω reverse termination)
Outputs		
G16, F16, E16, A15, A14, A12, A11, A6, A4, A3, E1, F1	D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11	In-phase digital output data (D11 is the MSB)
G15, F15, E15, B15, B14, B12, B11, B6, B4, B3, E2, F2	D0N, D1N, D2N, D3N, D4N, D5N, D6N, D7N, D8N, D9N, D10N, D11N	Out-of-phase digital output data (D11N is the MSB)
A9, A8	CLKO, CLKON	Output clock
N1	VCSH	Input common mode
Function Inputs		
L1, L2	RESET, RESETN	Differential Synchronous RESET signal
K2	VDIODE	Diode for die junction temperature monitoring
P15	SMODE	Selection Bit for 3WSI (SMODE = 1) or normal mode (SMODE = 0)
P16	SLDN	Beginning and End of register line for 3WSI
N16	SDATA	Input data for 3WSI
N15	SCLK	Input clock for 3WSI
Other		
A2, A5, A13, B1, B2, B5, B13, B16, C1, C2, C15, C16, D1, D2, D15, D16, H15, H16, J15, J16, M1, M2	NC	Not connected pins They can be used as thermal pads when connected to ground
K15, K16, L15, L16, M15, M16, N2, P1, P2	TEST	Atmel Internal Test Pins They must be left unconnected (floating)

Figure 3-1. Pinout Diagram (Bottom View)

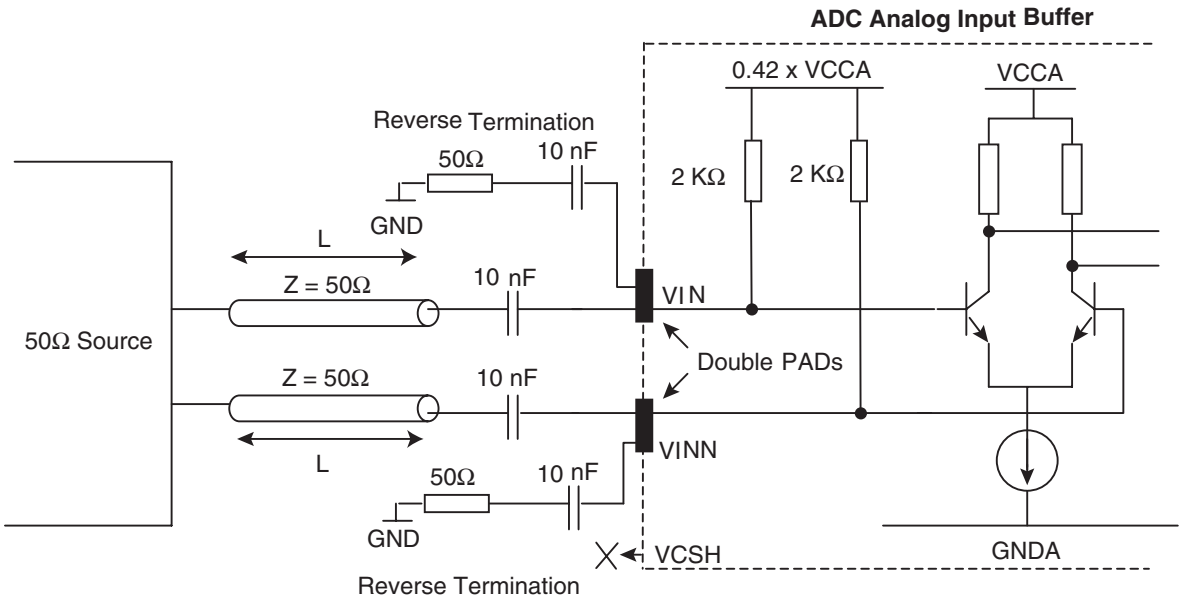


4. Implementing the AT84AS001 ADC

4.1 Analog Input Implementation in AC Coupled Mode

The analog inputs of the ADC were designed with a double pad implementation as illustrated in the following schema, Figure 4-1. The reverse pad for each input should be tied to ground via a capacitor of 10 nF and a 50Ω resistor. In this mode, the VSCH output pin is left open.

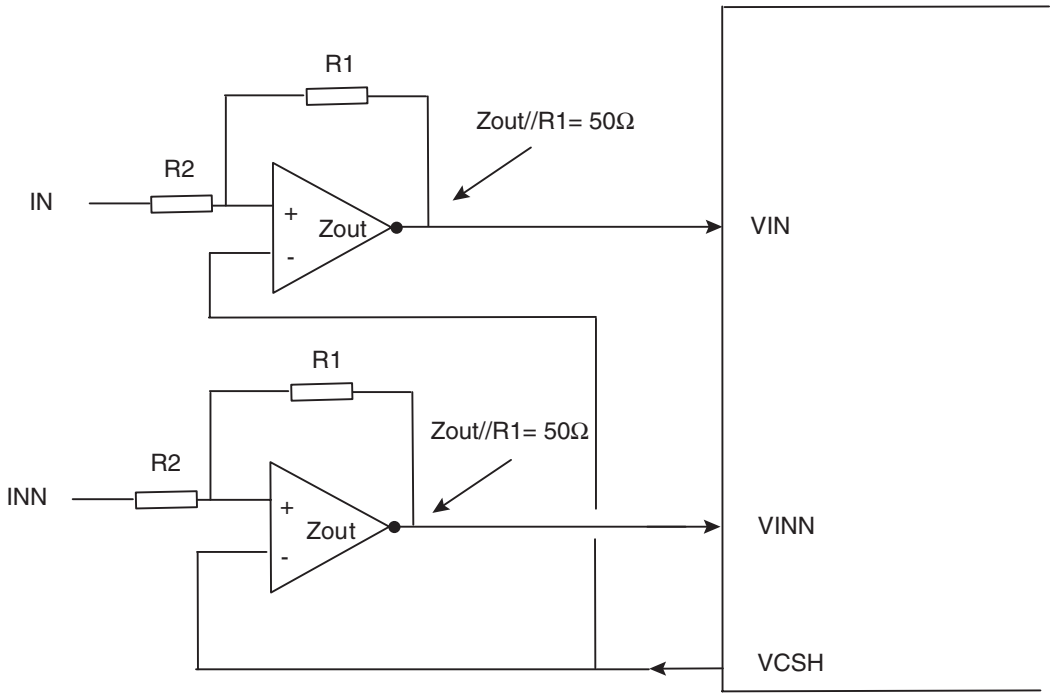
Figure 4-1. AC Analog Inputs Termination Methods



4.2 Analog Input implementation in DC Coupled Mode

In order to set the DC analog input, voltage the VCSH output pin must be used as described in Figure 4-2. The impedance Zout//R1 must be lower than 2 kΩ and equal to 50Ω to guarantee good impedance matching and to apply correct analog input level.

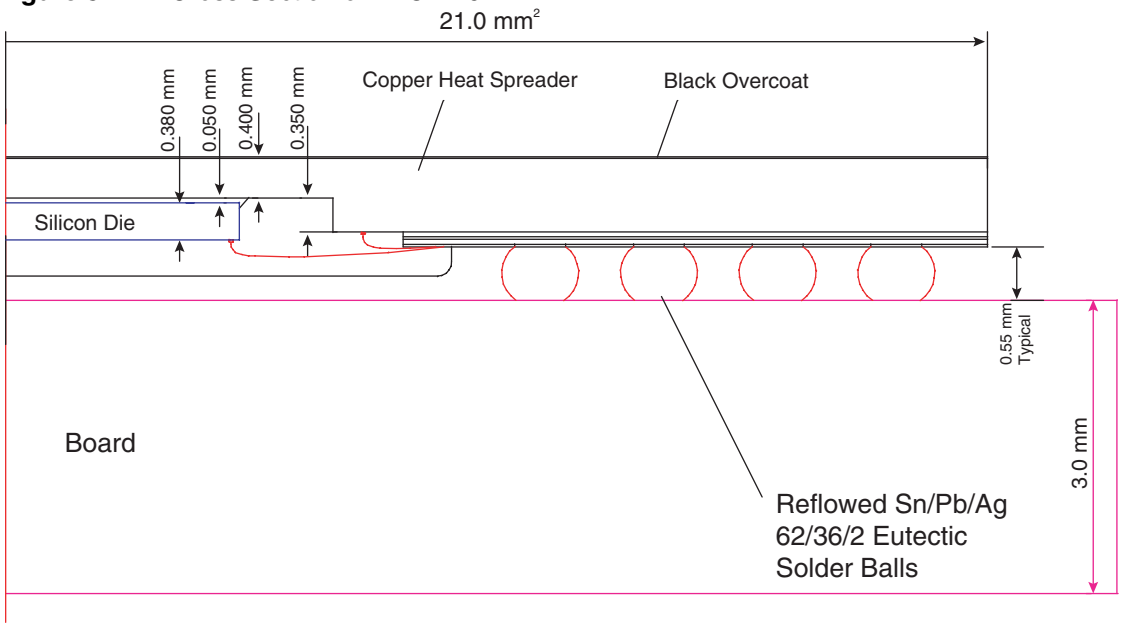
Figure 4-2. DC Analog Inputs Termination Methods



Note: The VCSH is equal to 0.42 x V_{CCA}

5. Package Information

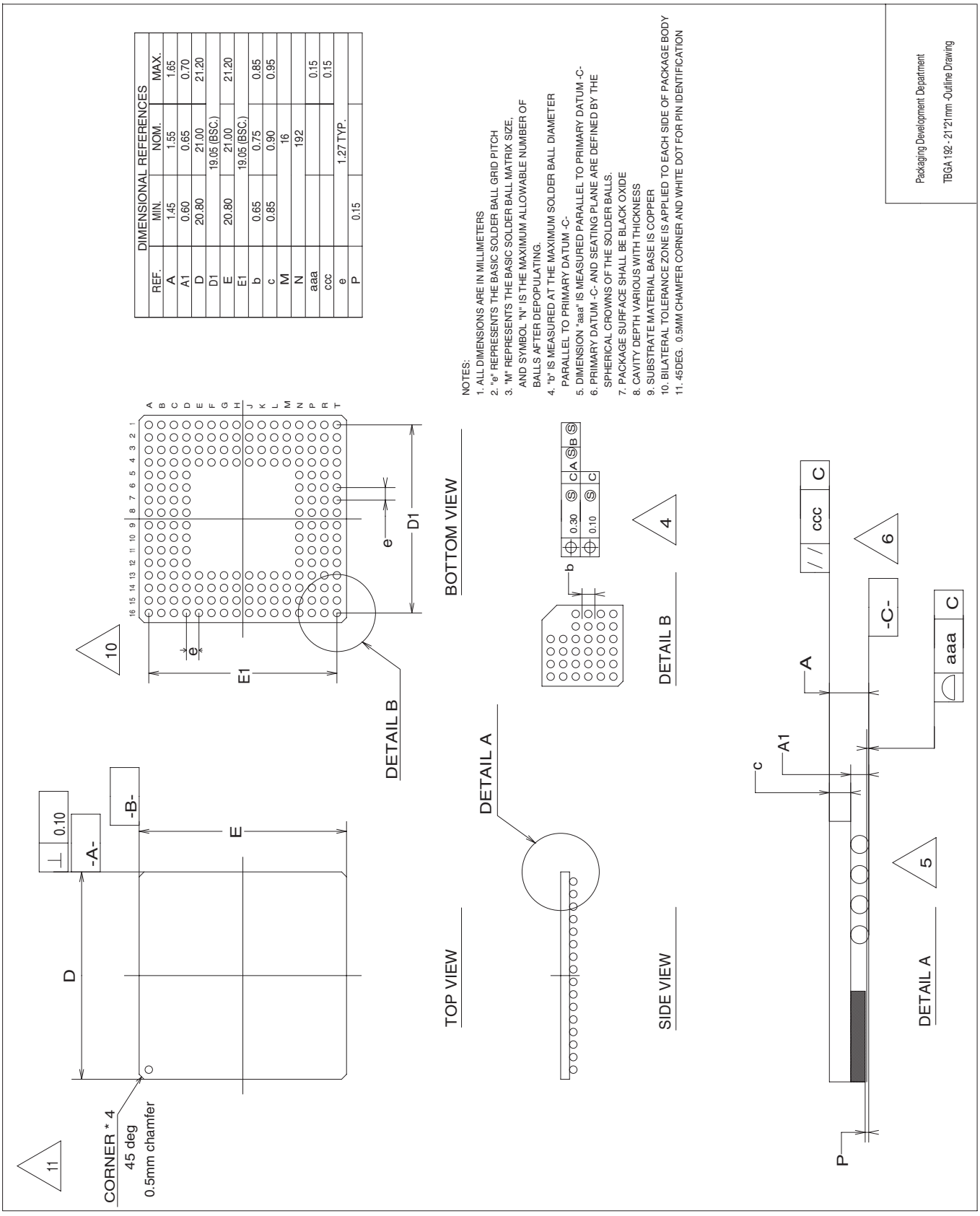
Figure 5-1. Cross Section of TBGA 192



Due to package weight, the balls "collapse" somewhat during reflow, and the height of the balls is reduced by approximately 0.10 mm. The balls increase simultaneously in diameter to compensate.

Notes:
1. The copper heat spreader is connected to the ADC circuit GND through a conductive low resistivity die attach.
2. For RoHS version, please contact your local Atmel Sales Office.

Figure 5-2. Mechanical Drawings of TBGA 192



6. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
AT84XAS001TP	TBGA 192	Ambient	Prototype	
AT84AS001CTPY	EBGA 192	RoHS compliant Commercial *C* grade $0°C < T_{amb} < 70°C$	Standard	For availability please contact your local Atmel sales office
AT84AS001VTPY	EBGA 192	RoHS compliant Industrial *V* grade $-40°C < T_{amb} < 85°C$	Standard	For availability please contact your local Atmel sales office
AT84AS001TP-EB	TBGA 192	Ambient	Prototype	Evaluation board

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