

Features

- 10-bit Resolution ADC
- 2.2 Gsps Sampling Rate
- Seamless ascending Compatibility with Atmel TS83102G0B 10-bit 2 Gsps ADC
- 500 mVpp Full Scale Analog Input Range
- 100Ω Differential or 50Ω Single-ended Analog input and Clock Input
- 100Ω Differential Outputs
- ECL/LVDS Output Compatibility
- Functions:
 - ADC Gain Adjust and Sampling Delay Adjust
 - Data Ready Output with Asynchronous Reset
 - Out-of-range Output Bit
- Power Consumption: 4.2W
- Power supplies:
 - Analog: -5V, 5V
 - Digital: -5V to -2.2V and 1.5V
- Radiation Tolerant (to be confirmed)
- Package: CBGA152 Cavity Down Hermetic Package
- Evaluation Board AT84AS008GL-EB
- Companion Device:
 - DMUX 8/10 bit 1:2/1:4 LVDS 2.2 Gsps AT84CS001

Performances

- 3.3 GHz Full Power Input Bandwidth (-3 dB)
- Gain Flatness: ± 0.2 dB (from DC up to 1.5 GHz)
- Low Input VSWR: 1.2 Maximum from DC to 2.5 GHz
- Single Tone Performances (-1 dBFS):
 - SFDR = -56 dBc; 8.0 ENOB; SNR = 52 dBc at $F_S = 1.7$ Gsps, $F_{IN} = 850$ MHz
 - SFDR = -55 dBc; 7.7 ENOB; SNR = 51 dBc at $F_S = 2.2$ Gsps, $F_{IN} = 1.1$ GHz
 - SFDR = -55 dBc; 7.3 ENOB; SNR = 48 dBc at $F_S = 2.2$ Gsps, $F_{IN} = 2$ GHz
- Dual Tone Performances (IMD3), $F_S = 1.7$ Gps, (-7dBFS tone):
 - ($F_{in1} = 995$ MHz, $F_{in2} = 1005$ MHz): IMD3 = 60 dBFS
 - ($F_{in1} = 1545$ MHz, $F_{in2} = 1555$ MHz): IMD3 = 60 dBFS
 - ($F_{in1} = 1945$ MHz, $F_{in2} = 1955$ MHz): IMD3 = 57 dBFS
- Low Bit Error Rate (10^{-11}) at 2.2 Gsps

Screening

- Temperature Range for Packaged Device:
 - $0^\circ\text{C} < T_c; T_j < 90^\circ\text{C}$ (Commercial “C” Grade)
 - $-20^\circ\text{C} < T_c; T_j < 110^\circ\text{C}$ (Industrial “V” Grade)

Applications

- Broadband Direct RF Down Conversion
- Wide Band Satellite Receivers
- Phased Array Antennas, Radars and ECM
- High-speed Instrumentation and High speed Acquisition Systems
- High Energy Physics
- Automatic Test Equipment



ADC
10-bit 2.2 Gsps

AT84AS008

Summary

5404AS-BDC-05/05



Note: This is a summary document. A complete document is not available at this time. For more information, please contact your local Atmel sales office. www.DataSheet4U.com

1. Description

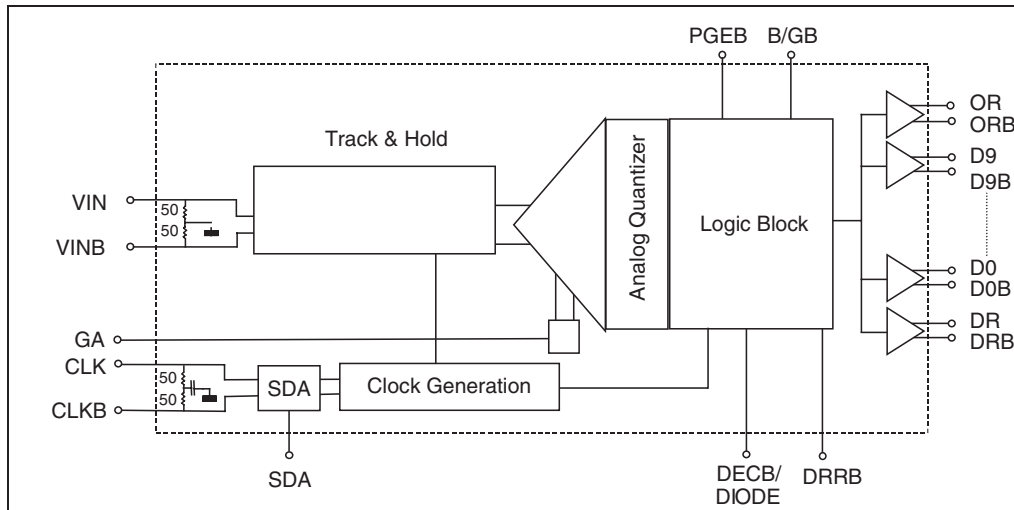
The AT84AS008 10-bit 2.2 Gsps ADC allows accurate digitization of high frequency signals thanks to the 3.3 GHz analog input bandwidth.

The innovative design of the on-chip Track and Hold (T/H) and digitizing core lead to unprecedented dynamic performance at a sampling rate of 2.2 GHz (over the full first Nyquist zone). A 7.7 ENOB is achieved at 2.2 Gps in Nyquist conditions using gray encoded digital outputs for optimum SNR performance.

The AT84AS008 features an enhanced spectral purity and a very low noise floor, independent on frequency and temperature. It is particularly well suited for performance enhancements (i.e., dithering).

The AT84AS008 is fully compatible with Atmel's TS83102G0B 10-bit 2 Gsps ADC, allowing zero-effort system improvement by plug-and-play replacement with the new part.

Figure 1-1. Block Diagram



2. Functional Description

The AT84AS008 is a 10-bit 2.2 Gsps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by 100Ω differential output buffers.

The AT84AS008 works in fully differential mode from the analog inputs up to the digital outputs. A differential Data Ready output (DR/DRB) is available to indicate when the outputs are valid and an Asynchronous Data Ready Reset ensures that the first digitized data corresponds to the first acquisition.

For sampling rates exceeding 2 Gsps, the gray output encoding is recommended for optimum SNR performance.

The control pin B/GB (A11 of the CBGA package) is provided to select either a binary or gray data output format. The gain control pin GA (R9 of the CBGA package) is provided to adjust the ADC gain transfer function.

A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requesting the interleaving of multiple ADCs for example.

A pattern generator is integrated on-chip for debug or acquisition set-up. This function is enabled through the PGEB pin (A9 of the CBGA package).

An Out-of-range Bit (OR/ORB) indicates when the input overrides 0.5 Vpp.

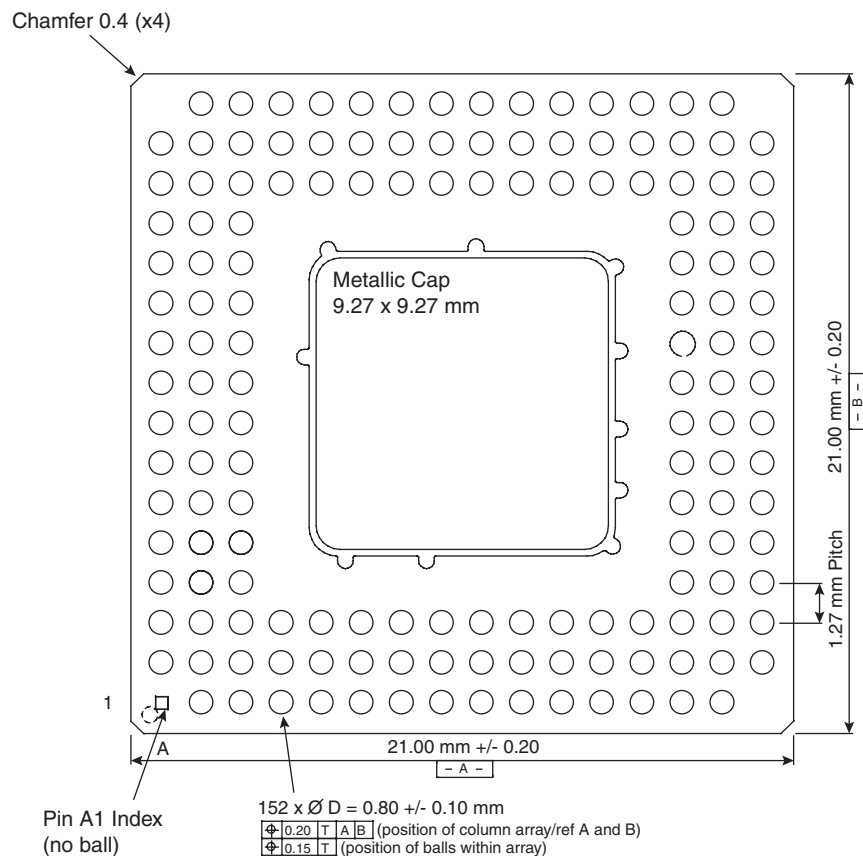
A selectable decimation by 32 function is also available for enhanced testability coverage (A10 of the CBGA package) along with a die junction temperature monitoring function.

The AT84AS008 uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allow enhanced radiation tolerance (over 100kRad (Si) expected total dose).

The AT84AS008 provides full ascending compatibility with the TS83102G0B with enhanced performances.

3. Package Description

Figure 3-1. Hermetic CBGA 152 Outline Dimensions (Bottom View)





4. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
AT84XAS008GL	CBGA152	Ambient	Prototype	Please contact your local Atmel sales office
AT84AS008CGL	CBGA152	Commercial "C" grade 0°C < T _C , T _J < 90°C	Standard	
AT84AS008VGL	CBGA152	Industrial "V" grade -20°C < T _C , T _J < 110°C	Standard	
AT84AS008GL-EB	CBGA152	Ambient	Prototype	Evaluation board (delivered with a heat sink)





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