Features

General

- High-performance, Low-power secureAVR™ Enhanced RISC Architecture
  - 133 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low-power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V
- Operating Ranges: from 2.7V to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules and Industry-standard Packages

Memory

- 256K Bytes of ROM Program Memory
- 72K Bytes of EEPROM, Including 128-byte OTP Area and 384-byte Bit-addressable Bytes
  - 1 to 128-byte Program/Erase
  - 1 ms Program, 1 ms Erase
  - Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
- EEPROM Erase Only Mode
- Write EEPROM With or Without Autoerase
- 6K Bytes of RAM

Peripherals

- ISO 7816 Controller
  - Up to 625 kbps at 5 MHz
  - Compliant with T = 0 and T = 1 Protocols
- One I/O Port
- Programmable Internal Oscillator (Up to 20 MHz on ROM)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 7-vector Interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Checksum Accelerator
- CRC 16 Engine (Compliant with ISO/IEC 3309)

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

Development Tools

- Voyager Emulation Platform (ATV2 Advanced) to Support Software Development
- IAR Systems C-Spy Debugger or Atmel's AVR Studio Version 4.07 or Above
- Software Libraries and Application Notes

Secure Microcontroller for Smart Cards

AT90SC25672R

Summary

Rev. 1585AS–SMIC–06/03

Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Description

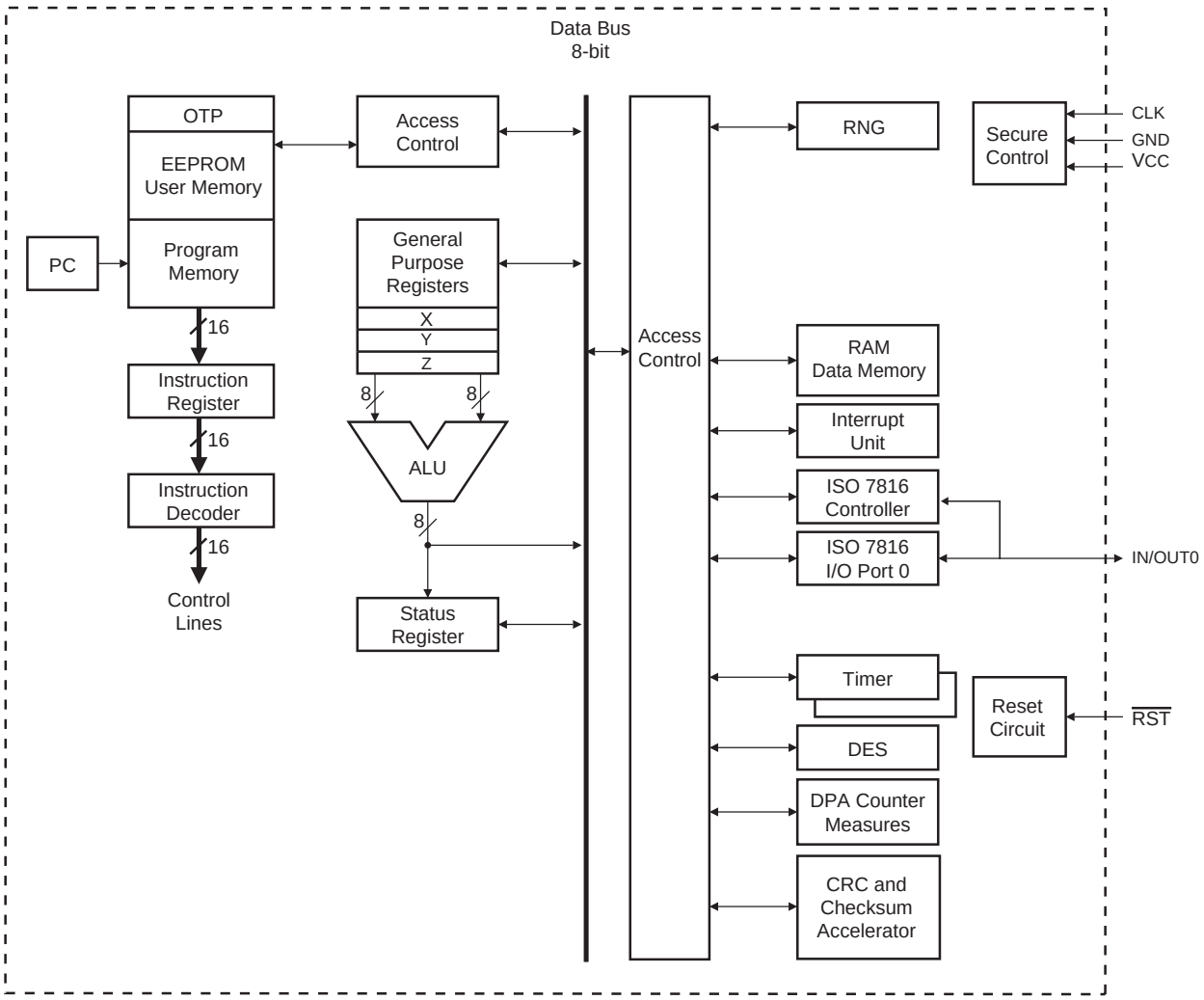
The AT90SC25672R is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90SC25672R achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The AT90SC25672R uses a new AVR architecture, the secureAVR that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications.

Additional security features include power and frequency protection logic, logical scrambling on program data and addresses, Power Analysis countermeasures and memory accesses controlled by a supervisor mode. A block diagram of the AT90SC25672R is shown in Figure 1.

Figure 1. AT90SC25672R secureAVR RISC Architecture



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