

Features

General

- High-performance, Low-power AVR™ RISC Architecture
 - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to $\pm 6000V$
- Operating Ranges: 2.7 to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications
- Available in Wafers, Modules, and Industry-standard Packages

Memory

- 96K Bytes of ROM Program Memory
- 4K Bytes of EEPROM, Including 64 OTP Bytes and 192-byte Bit-addressable Bytes
 - 1 to 64-byte Program / Erase
 - 1.25 ms Program / 1.25 ms Erase
 - Typically 500,000 Write/Erase Cycles at a Temperature of 25°C
 - 10 Years Data Retention
- 2K Bytes of RAM

Peripherals

- ISO 7816 controller
 - Up to 625 kbps at 5 MHz
 - Compliant with T = 0 and T = 1 Protocols
- One I/O Port
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 7-vector Interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Checksum Accelerator
- CRC 16 & 32 Engine (Compliant with ISO/IEC 3309)

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

Development Tools

- Voyager Emulation Platform (ATV2 adv or ATV4) to Support Software Development
- IAR Embedded Workbench® V4.20 Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes

Certification targeted

- EAL4+
- VISA
- CAST



Secure Microcontroller for Smart Cards

AT90SC 9604RU Summary

6540BS-SPD-02May07



Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Description

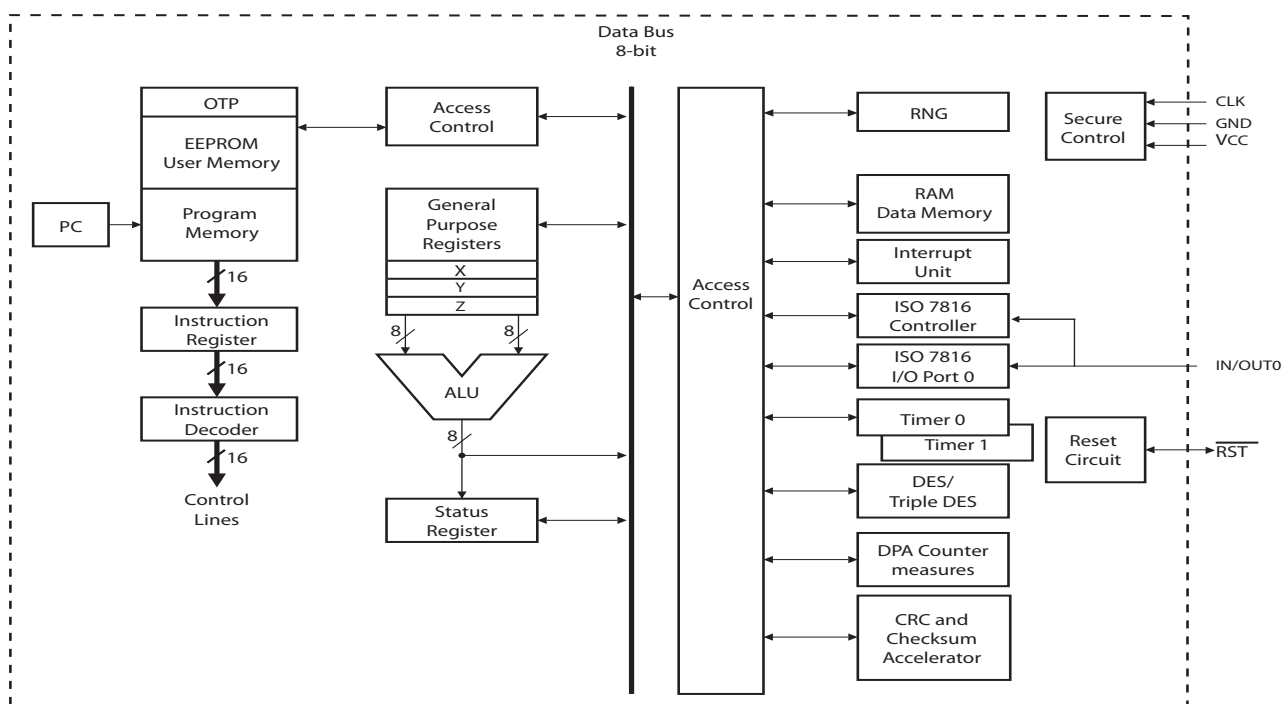
The AT90SC9604RU is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90SC9604RU achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The AT90SC9604RU uses the secureAVR that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications.

Figure 1 shows a block diagram of the AT90SC9604RU

Figure 1. AT90SC9604RU SecureAVR RISC Architecture





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