ATB110x Datasheet

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Revision History

Version	Revision Content	Date
V1.0	Initial version	2018-07-20
V1.1	1. add the describe of security 2. modify the describe of the key mode 3. Correction part describes syntax errors.	2018-10-25

1 Introduction

The ATB110x is an ultra-low power, fully-integrated, single-chip Bluetooth Low Energy solution. It features a low-power physical layer, a link layer with a security engine, a host controller interface and an ARM Cortex-M0 MCU to handle the upper layer protocol. ATB110x supports the latest Bluetooth V4.2 version with LE packet length extension feature. There are two operation modes are supported by ATB110x which are single-chip mode and HCI controller mode. The single-chip mode includes all the BLE layers from Link layer to GATT and Customers can implement the application SW on the embedded Cortex M0. The HCI mode means that ATB110x is just a HCI controller and communicate with the host controller by standard HCI command.

1.1 Key Features

Bluetooth

- Complies with bluetooth ® Low Energy Core Specification V4.2
- Low power and excellent performance 2.4GHz transceiver built-in balun for compact layout area Master and slave mode support
- Industry leading power consumption
  BLE Active Rx: 3.1mA（with DCDC）
  BLE Active Tx: 3.5mA@0dBm（with DCDC）
  BLE Active Rx: 4.2 mA（without DCDC）
  BLE Active Tx: 6.9mA@0dBm（without DCDC）,11mA@5dBm（without DCDC）
  BLE Sleep mode: 700 nA(SW mode)
  Standby mode with all wakeup sources (with SRAM retention) : <20uA
  Standby mode without any wakeup sources (CHIPEN=0) :< 300nA (without flash memory)
- RX sensitivity: -93.5dBm(30.8% PER, Dirty,Mix Mode）
- TX power range: -20 to +5 dBm(2/4 layer PCB)
- BT qualified, FCC & ETSI compliant
- Support standalone mode
- Support HCI mode with standard HCI interface

System

- ARM Cortex-M0 processor,up to 96MHz
- 8K Icache
- 40KB RAM(up to 48KB RAM if Icache unused)
- Integrate 4Mb Flash(Only in ATB1103)
- Build-in EFUSE.
- Security: CHIP unique ID, firmware encryption, firmware tamper proofing.
- Zephyr RTOS, Support OTA (Over the Air) programming mechanism for firmware upgrade
- Support UART0, SWD, OTA upgrade firmware
- Ultra low power consumption with intelligent PMU

- Wide supply voltage range (1.8V to 3.6V)
- Support internal 32KHz OSC or external 32KHz clock input for low power mode
- Support build-in HCL32K (without 32k crystal) for low BOM cost mode
- Supports 1V or 3V Power mode.

Audio

- Ultra low power consumption with intelligent Voice ADC
- Mono Sigma-Delta Voice ADC, 16bit, 16KHz sample rate ,SNR(A-weighted): 83dB
- Configurable high-pass filter with ADC
- Support DMIC IN, DMIC Clock up to 3MHz
- I2S Tx: standard I2S,Support both the master mode and slave mode, sample rate up to 44.1Khz/48Khz
- I2S Rx: standard I2S and TDM4 mode, Support both the master mode and slave mode, sample rate up to 44.1 Khz/48Khz.

Peripheral

- Embed 8-CH 10-bit LRADC(include BATADC and TempADC,up to 64KHz sample in fast mode)
- Real-time counters (RTC)
- Flexible General Purpose IOs (14GPIOs with ATB1103)
- Timer*4(with capture function)
- TWI*2
- UART*3
- SPI*3
- PWM *5
- IRC TX and RX（The RX has both pulse mode (dedicated IRC receiver) and carrier mode (shared IRC transmitter).
- Key scanner:up to Support 35 keys in scan mode with 7 Pins(c_n^2 +2n (n is number of IO))
- Temperature Sensor
- Battery Monitor

Application

- BLE Voice Remote
- BLE Mesh device
- Smart wearable devices(Consumer health, Fitness,activity trackers,Medical monitors.etc)
- Beacon
- Smart Home sensors
- TV ,STB and Toys (connect with the BLE remote controller)
- Home Automation Gateway

1.2 Block Diagram

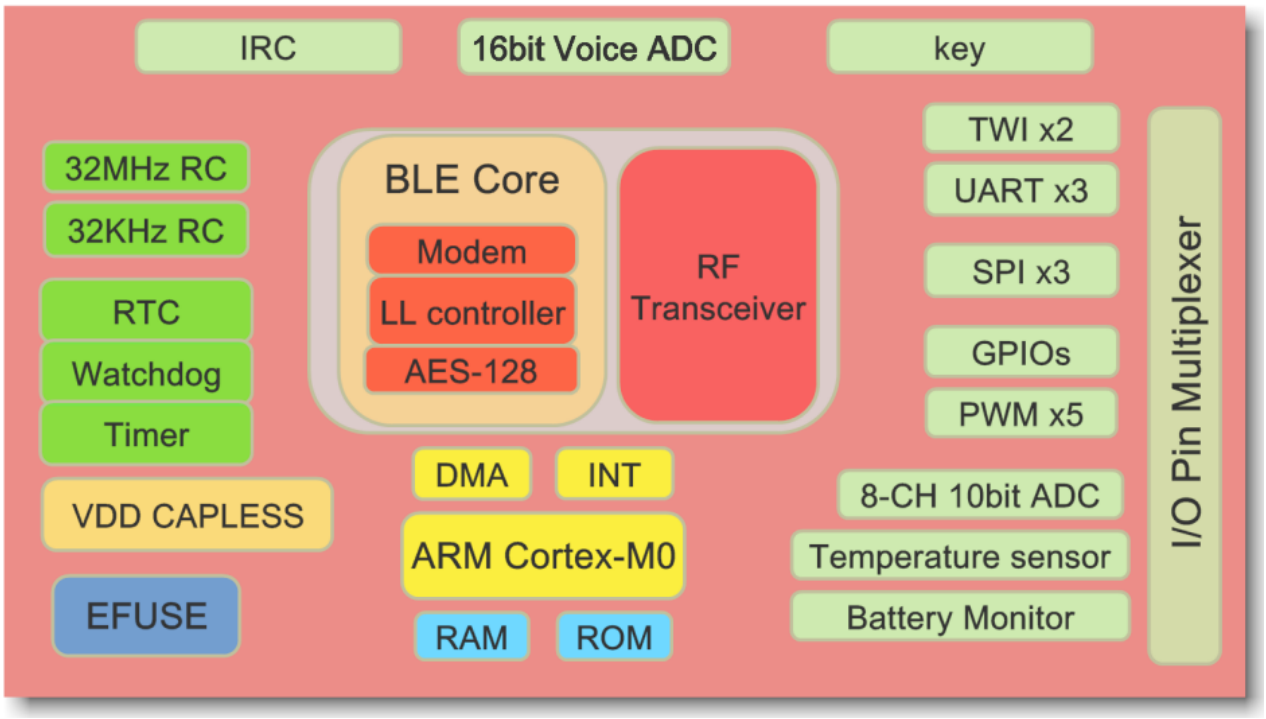


Figure 1-1 ATT110X Block Diagram

1.3 Application Diagram

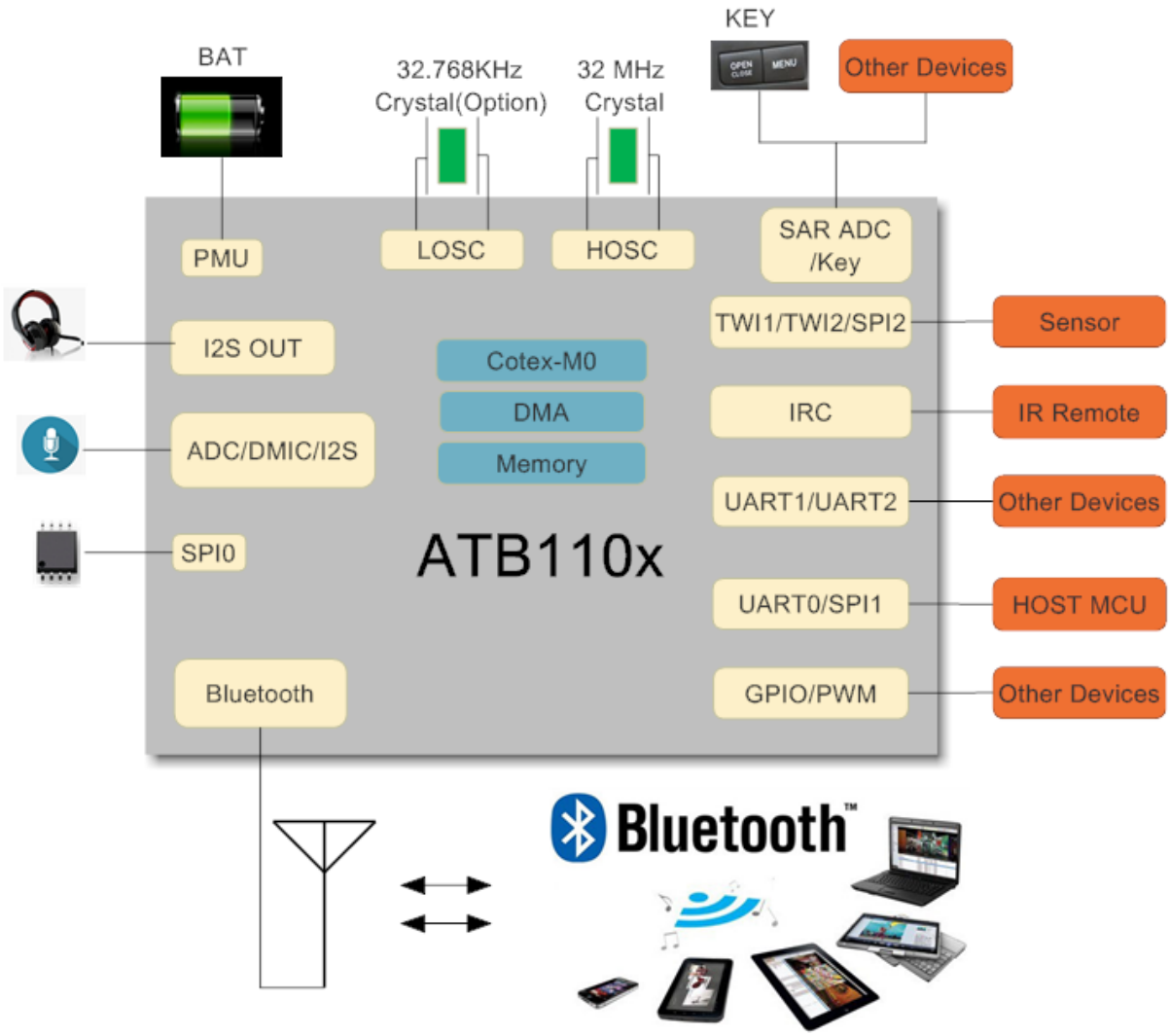


Figure 1-2 ATB110X Typical Application Diagram

1.4 ATB110X Pin Assignment

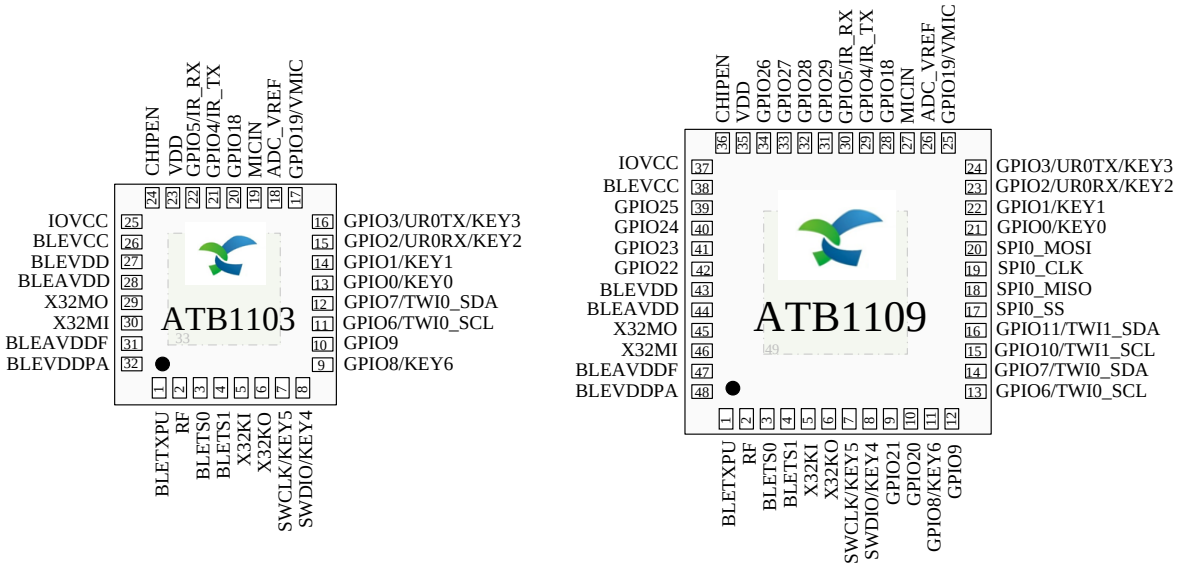


Figure 1-3 ATB110x schematic pin assignment

1.5 ATB1103 Pin Description

Table 1-1 ATB1103 PIN description

Pin No.	ATB1103 PIN Name	MFP	GPIO Initial State
1	BLETXPU	BLETXPU	
2	RF	RF	
3	BLETS1	BLETS1	
4	BLETS2	BLETS2	
5	X32KI	X32KI	
6	X32KO	X32KO	
7	GPIO12	GPIO12/SWCLK/KEY5/IR_TX/IR_RX/Timer2	1*
8	GPIO13	GPIO13/SWDIO/KEY4/IR_TX/IR_RX/Timer3	0*
9	GPIO8	GPIO8/PWM3/TWI0_SCL/UART1_CTS/KEY6/SPI2_SS/Timer2	Z
10	GPIO9	GPIO9/PWM4/TWI0_SDA/UART1_RTS/SPI2_CLK/Timer3	Z
11	GPIO6	GPIO6/PWM1/SPI2_SS/GPIO_BT[0]/TWI0_SCL/I2SRX_MCLK/DMIC_CLK/Timer2	Z
12	GPIO7	GPIO7/PWM2/SPI2_CLK/GPIO_BT[1]/TWI0_SDA/I2SRX_BCLK/DMIC_DAT/KEY0/Timer3	Z
13	GPIO0	GPIO0/ADC0/PWM0/UART0_CTS/SPI1_MISO/TWI0_SCL/	Z

		I2STX_MCLK/KEY0/IR_TX/IR_RX/Timer2	
14	GPIO1	GPIO1/ADC1/PWM1/UART0_RTS/SPI1_MOSI/TWI0_SDA /I2STX_BCLK/KEY1/IR_TX/IR_RX/Timer3	Z
15	GPIO2	GPIO2/ADC2/PWM2/UART0_RX/SPI1_SS/I2STX_LRCLK/ KEY2/Timer2	Z
16	GPIO3	GPIO3/ADC3/PWM3/UART0_TX/SPI1_CLK/I2STX_DOUT /KEY3/Timer3	Z
17	GPIO19	GPIO19/PWM4/SPI2_MISO/TWI0_SDA/UART2_CTS/SWD IO_BT/I2SRX_DIN/VMIC/Timer3	Z
18	ADC_VREF		
19	MICIN	MICIN/DMIC_DAT	
20	GPIO18	GPIO18/PWM3/SPI2_MOSI/TWI0_SCL/UART2_RTS/I2SR X_LRCLK/DMIC_CLK/KEY6/Timer2	Z
21	GPIO4	GPIO4/ADC4/PWM4/TWI1_SCL/UART1_TX/KEY4/IR_TX /IR_RX/Timer2	Z
22	GPIO5	GPIO5/ADC5/PWM0/TWI1_SDA/UART1_RX/KEY5/IR_T X/IR_RX/IR_RX_ANA/Timer3	Z
23	VDD	VDD	
24	CHIPEN	CHIPEN	
25	IOVCC	IOVCC	
26	BLEVCC	BLEVCC	
27	BLEVDD	BLEVDD	
28	BLEAVDD	BLEAVDD	
29	X32MO	X32MO	
30	X32MI	X32MI	
31	BLEAVDDF	BLEAVDDF	
32	BLEVDDPA	BLEVDDPA	
33	EPAD_GND	EPAD_GND	

1.6 ATB1109 Pin Description

Table 1-2 ATB1109 PIN description

PIN No.	ATB1109 PIN Name	MFP	GPIO Initial State
1	BLETXPU	BLETXPU	
2	RF	RF	
3	BLETS1	BLETS1	
4	BLETS2	BLETS2	
5	X32KI	X32KI	
6	X32KO	X32KO	
7	GPIO12	GPIO12/SWCLK/KEY5/IR_TX/IR_RX/Timer2	1*
8	GPIO13	GPIO13/SWDIO/KEY4/IR_TX/IR_RX/Timer3	0*
9	GPIO21	GPIO21/SPI0_IO3/IR_TX/IR_RX/Timer3	Z

10	GPIO20	GPIO20/SPI0_IO2/IR_TX/IR_RX/Timer2	Z
11	GPIO8	GPIO8/PWM3/TWI0_SCL/UART1_CTS/KEY6/SPI2_SS/Timer2	Z
12	GPIO9	GPIO9/PWM4/TWI0_SDA/UART1_RTS/SPI2_CLK/Timer3	Z
13	GPIO6	GPIO6/PWM1/SPI2_SS/GPIO_BT[0]/TWI0_SCL/I2SRX_MCLK/DMIC_CLK/Timer2	Z
14	GPIO7	GPIO7/PWM2/SPI2_CLK/GPIO_BT[1]/TWI0_SDA/I2SRX_BCLK/DMIC_DAT/KEY0/Timer3	Z
15	GPIO10	GPIO10/PWM0/UART0_TX/TWI1_SCL/UART2_TX/KEY1/Timer2	Z
16	GPIO11	GPIO11/PWM1/UART0_RX/TWI1_SDA/UART2_RX/KEY2/Timer3	Z
17	GPIO15	GPIO15/SPI0_SS	X
18	GPIO14	GPIO14/SPI0_MISO/PWM2/KEY5	X
19	GPIO16	GPIO16/SPI0_CLK	X
20	GPIO17	GPIO17/SPI0_MOSI	X
21	GPIO0	GPIO0/ADC0/PWM0/UART0_CTS/SPI1_MISO/TWI0_SCL/I2STX_MCLK/KEY0/IR_TX/IR_RX/Timer2	Z
22	GPIO1	GPIO1/ADC1/PWM1/UART0_RTS/SPI1_MOSI/TWI0_SDA/I2STX_BCLK/KEY1/IR_TX/IR_RX/Timer3	Z
23	GPIO2	GPIO2/ADC2/PWM2/UART0_RX/SPI1_SS/I2STX_LRCLK/KEY2/Timer2	X
24	GPIO3	GPIO3/ADC3/PWM3/UART0_TX/SPI1_CLK/I2STX_DOUT/KEY3/Timer3	X
25	GPIO19	GPIO19/PWM4/SPI2_MISO/TWI0_SDA/UART2_CTS/I2SRX_DIN/VMIC/Timer3	Z
26	ADC_VREF		
27	MICIN	MICIN/DMIC_DAT	
28	GPIO18	GPIO18/PWM3/SPI2_MOSI/TWI0_SCL/UART2_RTS/I2SRX_LRCLK/DMIC_CLK/KEY6/Timer2	Z
29	GPIO4	GPIO4/ADC4/PWM4/TWI1_SCL/UART1_TX/KEY4/IR_TX/IR_RX/Timer2	Z
30	GPIO5	GPIO5/ADC5/PWM0/TWI1_SDA/UART1_RX/KEY5/IR_TX/IR_RX/IR_RX_ANA/Timer3	Z
31	GPIO29	GPIO29/I2SRX_DIN/SPI2_CLK/TWI1_SDA/Timer3	Z
32	GPIO28	GPIO28/KEY6/I2SRX_LRCLK/SPI2_SS/TWI1_SCL/Timer2	Z
33	GPIO27	GPIO27/KEY5/I2SRX_BCLK/SPI2_MOSI/TWI0_SDA/Timer3	Z
34	GPIO26	GPIO26/KEY4/I2SRX_MCLK/SPI2_MISO/TWI0_SCL/PWM4/Timer2	Z
35	VDD	VDD	
36	CHIPEN	CHIPEN	
37	IOVCC	IOVCC	
38	BLEVCC	BLEVCC	

39	GPIO25	GPIO25/KEY3/I2STX_DOUT/SPI1_CLK/UART2_RX/PWM3/Timer3	Z
40	GPIO24	GPIO24/KEY2/I2STX_LRCLK/SPI1_SS/UART2_TX/PWM2/Timer2	Z
41	GPIO23	GPIO23/KEY1/I2STX_BCLK/SPI1_MOSI/UART1_RX/PWM1/Timer3	Z
42	GPIO22	GPIO22/KEY0/I2STX_MCLK/SPI1_MISO/UART1_TX/PWM0/Timer2	Z
43	BLEVDD	BLEVDD	
44	BLEAVDD	BLEAVDD	
45	X32MO	X32MO	
46	X32MI	X32MI	
47	BLEAVDDF	BLEAVDDF	
48	BLEVDDPA	BLEVDDPA	
49	EPAD_GND	EPAD_GND	

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 2-1 Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Storage temperature	Tstg	-55	+150	℃
Supply voltage	IOVCC,BLEVCC	0.3	3.63	V
	VDD	0.3	1.32	V
Input Voltage	+3.3V IO	0.3	3.63	V
Radio RF	input level		+5	dBm
ESD HBM	Human body model	2000		V
ESD CDM	Charged Device Model	500		V
32 kHz Crystal Oscillator	9 pF 32.768 kHz Crystal(-40℃~85℃)		±100	ppm
32 MHz Crystal Oscillator	8 pF 32 MHz Crystal(-40℃~85℃)		±25	ppm

Note:

1) Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
2) All voltage values are with respect to GND

2.2 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 2-2 Recommended Operating Conditions

Supply Voltage	Min	Typ	Max	Unit
IOVCC	1.65	3.3	3.63	V
BLEVCC(1V MODE)	1.00	1.2	1.65	V
BLEVCC(3V MODE)	1.65	3.3	3.63	V
BLEVDD	0.91	0.95	0.99	V
BLEAVDD	0.81	1	1.65	V
VDD	0.65	0.9	1.35	V
Ambient Temperature	-40	25	85	℃

2.3 DC Characteristics

DC Parameters for +3.0V IO PIN

Table 2-3 DC Parameters

Parameter	Symbol	MIN.	MAX.	Unit	Condition
Low-level input voltage	VIL		0.8	V	VCC = 3.0V Tamb = －10 to 70 ℃
High-level input voltage	VIH	2.0		V	
Low-level output voltage	VOL		0.4	V	
High-level output voltage	VOH	2.4		V	

3 MCU

3.1 Overview

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.It is intended for deeply embedded applications that require optimal interrupt response features.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

The required blocks are as follows:

(1) Processor core
(2) A Nested Vectored Interrupt Controller (NVIC)
(3) Data Watchpoint and Trace Unit (DWT)
(4) Wake-up Interrupt Controller (WIC)
(5) Serial-Wire Debug Port (SW-DP), SWDIO has internal 10KOhmpull-up resistor, SWDCLK has internal 10KOhm pull-down resistor. Up to 10MHz
(6) Low power:
Integrated architectural clock gating;
Sleep & deep sleep modes put Cortex-M0 into low-power state
Sleep-on-exit mode to enter sleep mode whenever Cortex-M0 completes all outstanding Interrupt Service Routines (ISRs)
Wakeup Interrupt Controller (WIC) in a separate power domain to wake Cortex-M0 up from deep sleep mode

3.2 NVIC

The ATB110X use Cortex-M0 processor, a Nested vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing.

The NVIC provides configurable interrupt handling abilities to the processor, facilitates low-latency exception and interrupt handling, and controls power management.

The NVIC supports up to 32 interrupts, each with up to 4 levels of priority that can be changed dynamically. The processor and NVIC can be put into a very low-power sleep mode, leaving the Wake Up Controller (WIC) to identify and prioritize interrupts. Also, the processor supports both level and pulse interrupts.

The NVIC and the processor core interface are closely couple, to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts.

Each peripheral device has one interrupt line connected to the NVIC. External interrupt can be programmed to generate an interrupt on rising edge, falling edge, or both.

3.2.1 Vector Table

When an exception takes place and is being handled by the Cortex-M0, the processor will need to locate the starting address of the exception handler. This information is stored in the vector table.

Table 3-1 vector table

Exception Number	Exception Type	Priority	Description	Vector Address
-	-	-	reserved	0x00000000
1	Reset	-3(Highest)	Reset, Watch Dog	0x00000004
2	NMI	-2	Nonmaskable interrupt	0x00000008
3	Hard Fault	-1	All fault conditions, if the corresponding fault handler is not enable	0x0000000C
4-10	Reserved	NA	-	0x0000001C~2B
11	SVCall	Programmable	System Service call	0x0000002C
12-13	NA	-		0x00000030~34
14	PendSV	Programmable	Pendable request for system device	0x00000038
15	SYSTICK	Programmable	System tick timer	0x0000003C

Table 3-2 Peripheral interrupt

Exception Number	Exception Type	Priority	Description	Vector Address
16	Timer0	Programmable	Timer0 interrupt	0x00000040
17	Timer1	Programmable	Timer1 interrupt	0x00000044
18	RTC	Programmable	RTC interrupt	0x00000048
19	WatchDog	Programmable	Watch dog module	0x0000004C
20	BLE0	Programmable	BLE module interrupt RXCMD	0x00000050
21	BLE1	Programmable	BLE module interrupt RXEVT	0x00000054
22	BLE2	Programmable	BLE module interrupt TXCMD	0x00000058
23	BLE3	Programmable	BLE module interrupt TXEVT	0x0000005C
24	BLE4	Programmable	BLE module interrupt TXDMAL	0x00000060
25	BLE5	Programmable	BLE module interrupt RXDMAL	0x00000064
26	BLE6	Programmable	BLE module interrupt TXDMAH	0x00000068
27	BLE7	Programmable	BLE module interrupt RXDMAH	0x0000006C
28	BLE8	Programmable	BLE module interrupt LLCC_CLK_ENABLE_REQ	0x00000070
29	DMA	Programmable	DMA Module interrupt	0x00000074
30	EXTI	Programmable	External Line interrupt	0x00000078
31	UART0	Programmable	UART0 module interrupt	0x0000007C
32	UART1	Programmable	UART1 module interrupt	0x00000080
33	UART2	Programmable	UART2 module interrupt	0x00000084
34	SPI0	Programmable	SPI0 module interrupt	0x00000088
35	SPI1	Programmable	SPI1 module interrupt	0x0000008C

36	SPI2	Programmable	SPI2 module interrupt	0x00000090
37	SARADC	Programmable	SAR ADC module interrupt	0x00000094
38	UART Wakeup	Programmable	UART wake up system interrupt	0x00000098
39	IRC	Programmable	IRC module interrupt	0x0000009C
40	TWI0	Programmable	TWI0 module interrupt	0x000000A0
41	TWI1	Programmable	TWI1 module interrupt	0x000000A4
42	Audio	Programmable	Audio module interrupt	0x000000A8
43	KEY	Programmable	KEY module interrupt	0x000000AC
44	SARADC wakeup	Programmable	SAR ADC wake up interrupt	0x000000B0
45	Timer2	Programmable	Timer2 interrupt	0x000000B4
46	Timer3	Programmable	Timer3 interrupt	0x000000B8
47	KEY wakeup	Programmable	KEY wake up system interrupt	0x000000BC

4 SPI CACHE

4.1 Overview

ATB110X SPI cache module support system code and constant table to run directly in SPI nor.

- Support code runs directly in SPI nor
- Caching data for code and read-only data
- four way associative
- 8k bytes cache size
- Support performance profile

4.2 Register List

SPI Cache Controller Registers Address

Name	Physical Base Address
SPICACHE_Control_Register	0x40014000

SPI Cache Controller Registers

Offset	Register Name	Description
0x0000	SPICACHE_CTL	SPI CACHE Control Register
0x0004	SPICACHE_INVALIDATE	SPI CACHE Invalidate Register
0x0008	SPICACHE_UNCACHE_ADDR_START	SPI CACHE Uncache Start Address Register
0x000C	SPICACHE_UNCACHE_ADDR_END	SPI CACHE Uncache End Address Register
0x0010	SPICACHE_PROFILE_INDEX_START	SPI CACHE Profile Index Start Address Register
0x0014	SPICACHE_PROFILE_INDEX_END	SPI CACHE Profile Index End Address Register
0x0018	SPICACHE_RANGE_INDEX_MISS_COUNT	SPI CACHE Range Index Miss Count Register
0x001C	SPICACHE_RANGE_INDEX_HIT_COUNT	SPI CACHE Range Index Hit Count Register
0x0020	SPICACHE_PROFILE_ADDR_START	SPI CACHE Profile Address Start Address Register
0x0024	SPICACHE_PROFILE_ADDR_END	SPI CACHE Profile Address End Address Register
0x0028	SPICACHE_RANGE_ADDR_MISS_COUNT	SPI CACHE Range Address Miss Count Register
0x002C	SPICACHE_RANGE_ADDR_HIT_COUNT	SPI CACHE Range Address Hit Count Register
0x0030	SPICACHE_TOTAL_MISS_COUNT	SPI CACHE Total Miss Count Register
0x0034	SPICACHE_TOTAL_HIT_COUNT	SPI CACHE Total Hit Count Register

4.3 Register Description

4.3.1 SPICACHE_CTL

SPI CACHE Control Register
Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	0x0
4	PROF_EN	SPI CACHE Profile Enable 0: Disable 1: Enable	R/W	0x0
3	ABORT_EN	SPI CACHE Prefetch About Enable 0: Disable 1:Enable	R/W	0x0
2	UNCACHE_EN	SPI CACHE Local Range Uncache Enable 0: Disable 1: Enable	R/W	0x0
1	PREF_EN	SPI CACHE Prefetch Enable 0: Disable 1: Enable	R/W	0x0
0	EN	SPI CACHE Enable 0: Disable 1: Enable	R/W	0x0

4.3.2 SPICACHE_INVALIDATE

SPI CACHE Invalidate Register
Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:5	CACHELINE_ADDR	Cacheline address: Bit[10:5] indicate cacheline index, bit[12:11] indicate way number (index mode) Bit[23:5] indicate address (address mode)	R/W	0x0
4:3	-	Reserved	R	0x0
2:1	INVALIDATE_MODE	Cache Invalidate mode 00: invalidate all cache 01: invalidate one cacheline (index mode) 10: invalidate one cacheline (address mode)	R/W	0x0
0	INVALIDATE	Cache Invalidate 0: Write 0 is no effect	R/W	0x0

		1: Write 1 to invalidate cpu cache		

Note: During invalidation, this bit remains 1. When invalidation is ok, this bit changes to 0.

4.3.3 SPICACHE_UNCACHE_ADDR_START

SPI CACHE Uncache Start Address Register
Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
30:24	-	Reserved	R	0x0
23:5	START	SPICACHE Uncache Start Address[23:5]	R/W	0x0
4:0	-	Reserved	R	0x0

4.3.4 SPICACHE_UNCACHE_ADDR_END

SPI CACHE Uncache End Address Register
Offset = 0x000C

Bit(s)	Name	Description	R/W	Reset
30:24	-	Reserved	R	0x0
23:5	END	SPICACHE Uncache End Address[23:5]	R/W	0x0
4:0	-	Reserved	R	0x0

4.3.5 SPICACHE_PROFILE_INDEX_START

SPI CACHE Profile Start Index Register
Offset = 0x0010

Bit(s)	Name	Description	R/W	Reset
30:6	-	Reserved	R	0x0
5:0	START	SPICACHE Profile Start Index	R/W	0x0

4.3.6 SPICACHE_PROFILE_INDEX_END

SPI CACHE Profile End Index Register
Offset = 0x0014

Bit(s)	Name	Description	R/W	Reset
30:6	-	Reserved	R	0x0
5:0	END	SPICACHE Profile End Index	R/W	0x0

4.3.7 SPICACHE_RANGE_INDEX_MISS_COUNT

SPI CACHE Range Index Miss Count
Offset = 0x0018

Bit(s)	Name	Description	R/W	Reset
31:0	COUNTER	SPICACHE_RANGE_INDEX_MISS_COUNT	R	0x0

4.3.8 SPICACHE_RANGE_INDEX_HIT_COUNT

SPI CACHE Range Index Hit Count
Offset = 0x001C

Bit(s)	Name	Description	R/W	Reset
31:0	COUNTER	SPICACHE_RANGE_INDEX_HIT_COUNT	R	0x0

4.3.9 SPICACHE_PROFILE_ADDR_START

SPI CACHE Profile Start Address Register
Offset = 0x0020

Bit(s)	Name	Description	R/W	Reset
30:24	-	Reserved	R	0x0
23:5	START	SPICACHE Profile Start Address[23:5]	R/W	0x0
4:0	-	Reserved	R	0x0

4.3.10 SPICACHE_PROFILE_ADDR_END

SPI CACHE Profile End Address Register
Offset = 0x0024

Bit(s)	Name	Description	R/W	Reset
30:24	-	Reserved	R	x
23:5	END	SPICACHE Profile End Address[23:5]	R/W	0x0
4:0	-	Reserved	R	x

4.3.11 SPICACHE_RANGE_ADDR_MISS_COUNT

SPI CACHE Range Address Miss Count
Offset = 0x0028

Bit(s)	Name	Description	R/W	Reset

31:0	COUNTER	SPICACHE_RANGE_ADDR_MISS_COUNT	R	0x0

4.3.12 SPICACHE_RANGE_ADDR_HIT_COUNT

SPI CACHE Range Address Hit Count

Offset = 0x002C

Bit(s)	Name	Description	R/W	Reset
31:0	COUNTER	SPICACHE_RANGE_ADDR_HIT_COUNT	R	0x0

4.3.13 SPICACHE_TOTAL_MISS_COUNT

SPI CACHE Total Miss Count

Offset = 0x0030

Bit(s)	Name	Description	R/W	Reset
31:0	COUNTER	SPICACHE_TOTAL_MISS_COUNT	R	0x0

4.3.14 SPICACHE_TOTAL_HIT_COUNT

SPI CACHE Total Hit Count

Offset = 0x0034

Bit(s)	Name	Description	R/W	Reset
31:0	COUNTER	SPICACHE_TOTAL_HIT_COUNT	R	0x0

5 Memory controller

5.1 Memory Map

Table 5-1 system memory map

Start address	End address	Size	Function
Total Mapping			
0x40000000	0x5fffffff	-	IO device
0x20000000	0x2000bfff	48K	SRAM
0x00000000	0x00027fff	160K	ROM
IO Device			
0x40000000	0x40000fff		Chip Version
0x40001000	0x40001fff		RMU
0x40002000	0x40002fff		CMU
0x40004000	0x40004fff		RTC/2Hz/WD/HCL
0x40008000	0x40008fff		PMU
0x40009000	0x40009fff		Memory controller
0x4000a000	0x4000afff		DMA
0x4000b000	0x4000bfff		TWI0
0x4000c000	0x4000cfff		TWI1
0x4000d000	0x4000dfff		UART0
0x4000e000	0x4000efff		UART1
0x4000f000	0x4000ffff		UART2
0x40010000	0x40010fff		IRC
0x40011000	0x40011fff		SPI0
0x40012000	0x40012fff		SPI1
0x40013000	0x40013fff		SPI2
0x40014000	0x40014fff		SPI Cache
0x40015000	0x40015fff		ADC/DMIC/I2S
0x40016000	0x40016fff		GPIO
0x40017000	0x40017fff		PWM
0x40018000	0x40018fff		KEY
0x40020000	0x4002ffff		BLE IP
SRAM Mapping (total: 48K) (RAM Region)			
0x20000000	0x20001fff	8K	RAM0
0x20002000	0x20003fff	8K	RAM1
0x20004000	0x20004fff	4K	RAM2
0x20005000	0x20005fff	4K	RAM3
0x20006000	0x20006fff	4K	RAM4
0x20007000	0x20007fff	4K	RAM5

0x20008000	0x20009fff	8K	RAM6
0x2000a000	0x2000bfff	8K	RAM7(cache ram)
BROM Mapping (total:160K) (Code Region)			
0x00000000	0x00027fff	160K	BROM
SNOR Mapping (total:16M) (code Region)			
0x01000000	0x01ffffff	16M	SNOR

5.2 Memory control register list

Memory control group base address

Name	Physical Base Address
MEMORYCONTROLLER	0x40009000

memory controller register list

Offset	Register Name	Description
0x0000	MEMCTRL	Memory Control register
0x0004	VECTORBASEADDR	Vector table base address register
0x0100	MAPPING_ADDR0	Mapping Address register 0
0x0104	ADDR0_ENTRY	Address0 Entry register
0x0108	MAPPING_ADDR1	Mapping Address register 1
0x010c	ADDR1_ENTRY	Address1 Entry register
0x0110	MAPPING_ADDR2	Mapping Address register 2
0x0114	ADDR2_ENTRY	Address2 Entry register
0x0118	MAPPING_ADDR3	Mapping Address register 3
0x011c	ADDR3_ENTRY	Address3 Entry register
0x0120	MAPPING_ADDR4	Mapping Address register 4
0x0124	ADDR4_ENTRY	Address4 Entry register
0x0128	MAPPING_ADDR5	Mapping Address register 5
0x012c	ADDR5_ENTRY	Address5 Entry register
0x0130	MAPPING_ADDR6	Mapping Address register 6
0x0134	ADDR6_ENTRY	Address6 Entry register
0x0138	MAPPING_ADDR7	Mapping Address register 7
0x013c	ADDR7_ENTRY	Address7 Entry register
0x0140	ADDR_MISS_STA	Address miss status register

5.3 Register Description

5.3.1 MEMCTRL

Memory control register
Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	x
1	SPI_NOR_CRC_ERROR_RESPONSE	Send SPI NOR CRC error response to create exception: 0: do not create exception 1: create exception	R/W	0x0
0	VTBSEL	Vector table base address select 0: ROM address 0x00000000 1: witch to the value of VECTORBASEADDR register	R/W	0x0

5.3.2 VECTORBASEADDR

Vector table base address register
Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:8	VTBADDR	Vector table base address	R/W	0x200000
7:0	-	Reserved	R	x

5.3.3 MAPPING_ADDR0

Mapping Address register 0
Offset = 0x0100

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR0	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.4 ADDR0_ENTRY

Address0 Entry register
Offset = 0x0104

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x

21:9	ADDR0_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.5 MAPPING_ADDR1

Mapping Address register 1

Offset = 0x0108

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR1	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.6 ADDR1_ENTRY

Address1 Entry register

offset = 0x010C

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR1_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.7 MAPPING_ADDR2

Mapping Address register 2

Offset = 0x0110

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR2	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.8 ADDR2_ENTRY

Address2 Entry registe

Offset = 0x0114

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR2_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.9 MAPPING_ADDR3

Mapping Address register 3

Offset = 0x0118

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR3	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.10 ADDR3_ENTRY

Address3 Entry register

Offset = 0x011c

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR3_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.11 MAPPING_ADDR4

Mapping Address register 4

Offset = 0x0120

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR4	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.12 ADDRz4_ENTRY

Address4 Entry register

Offset = 0x0124

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR4_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.13 MAPPING_ADDR5

Mapping Address register 5

Offset = 0x0128

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR5	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.14 ADDR5_ENTRY

Address5 Entry register

Offset = 0x012c

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR5_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.15 MAPPING_ADDR6

Mapping Address register 6

Offset = 0x0130

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR6	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.16 ADDR6_ENTRY

Address6 Entry register

Offset = 0x0134

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR6_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.17 MAPPING_ADDR7

Mapping Address register 0

Offset = 0x0138

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24:20	MAPPING_ADDR7	The bit 24:20 of mapping address	R/W	0x0
19:0	-	Reserved	R	x

5.3.18 ADDR7_ENTRY

Address7 Entry register
Offset = 0x0000013c)

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	x
21:9	ADDR7_ENTRY	The bit 21:9 of Address entry	R/W	0x0
8:0	-	Reserved	R	x

5.3.19 ADDR_MISS_STA

ADDR miss status register
Offset = 0x00000140)

Bit(s)	Name	Description	R/W	Reset
31:1	-	Reserved	R	x
0	MISS_STA	0: no cache access SNOR address miss 1: cache access SNOR address miss Write 1 to clear this bit	R/W	0x0

6 BLE（Bluetooth Low Energy）

6.1 Overview

The ATB110X BLE product provides the following features:

- Bluetooth Core Specification V4.2 with the Low Energy Core Configuration
  Master and slave mode support
- Fully Integrated Link Layer subsystem
  At the HCI level
- AES-128 encryption engine, NIST validated
- RX sensitivity: - 93.5dBm @ 1V, (RX sensitivity is reduced when using 3v switcher mode)
- TX power range: -20 to +5 dBm
- Single Antenna pin (50 Ohms)
- BT qualified, FCC & ETSI compliant

6.2 BLE Performance

TRM-LE/CA/01/C (Output power)

Bursts: 1, Payload: PRBS 9, Length: 37 Bytes

Channel: 0

Average Power	**-20.00 dBm**	**10.00 dBm**	**5.37 dBm**	✓
Difference (PowPeak - PowAvg)		**3.00 dB**	**0.65 dB**	✓

Channel: 19

Average Power	**-20.00 dBm**	**10.00 dBm**	**5.29 dBm**	✓
Difference (PowPeak - PowAvg)		**3.00 dB**	**0.71 dB**	✓

Channel: 39

Average Power	**-20.00 dBm**	**10.00 dBm**	**4.82 dBm**	✓
Difference (PowPeak - PowAvg)		**3.00 dB**	**0.81 dB**	✓

TRM-LE/CA/01/C (Output power)

Bursts: 1, Payload: PRBS 9, Length: 37 Bytes

Channel: 0

Average Power	-20.00 dBm	10.00 dBm	5.18 dBm	✓
Difference (PowPeak - PowAvg)		3.00 dB	0.68 dB	✓

Channel: 19

Average Power	-20.00 dBm	10.00 dBm	5.10 dBm	✓
Difference (PowPeak - PowAvg)		3.00 dB	0.74 dB	✓

Channel: 39

Average Power	-20.00 dBm	10.00 dBm	4.63 dBm	✓
Difference (PowPeak - PowAvg)		3.00 dB	0.76 dB	✓

TRM-LE/CA/06/C (Carrier frequency offset and drift)

Bursts: 10, Payload: 10101010, Length: 37 Bytes

Channel: 0

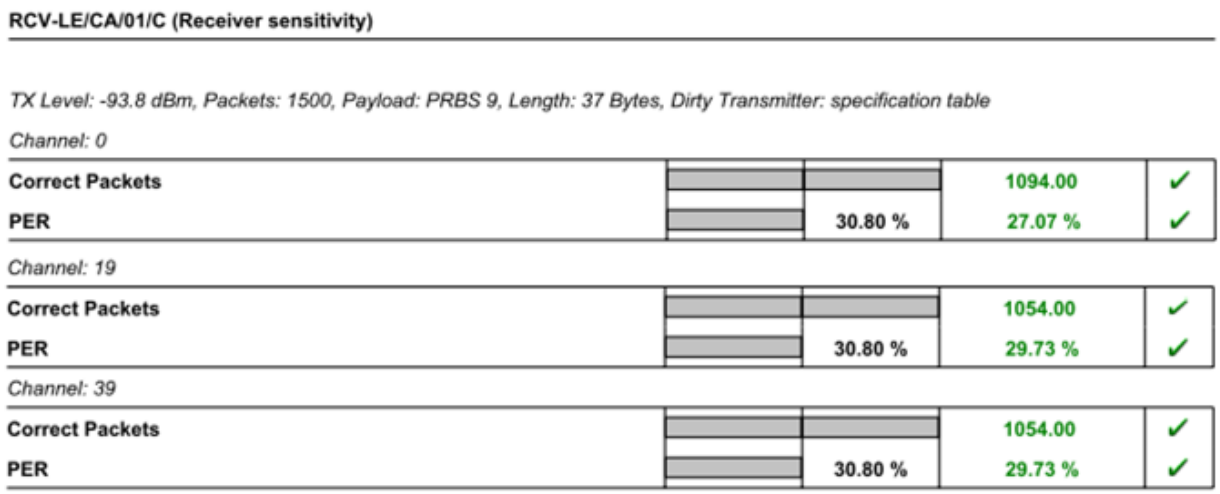
Frequency Accuracy	-150.00 kHz	150.00 kHz	3.20 kHz	✓
Frequency Offset	-150.00 kHz	150.00 kHz	5.30 kHz	✓
Frequency Drift	-50.00 kHz	50.00 kHz	4.15 kHz	✓
Maximum Drift Rate (kHz/50µs)	-20.00 kHz	20.00 kHz	2.97 kHz	✓
Initial Frequency Drift	-20.00 kHz	20.00 kHz	2.71 kHz	✓

Channel: 19

Frequency Accuracy	-150.00 kHz	150.00 kHz	2.78 kHz	✓
Frequency Offset	-150.00 kHz	150.00 kHz	5.03 kHz	✓
Frequency Drift	-50.00 kHz	50.00 kHz	4.59 kHz	✓
Maximum Drift Rate (kHz/50µs)	-20.00 kHz	20.00 kHz	3.42 kHz	✓
Initial Frequency Drift	-20.00 kHz	20.00 kHz	1.96 kHz	✓

Channel: 39

Frequency Accuracy	-150.00 kHz	150.00 kHz	1.88 kHz	✓
Frequency Offset	-150.00 kHz	150.00 kHz	5.97 kHz	✓
Frequency Drift	-50.00 kHz	50.00 kHz	5.50 kHz	✓
Maximum Drift Rate (kHz/50µs)	-20.00 kHz	20.00 kHz	3.49 kHz	✓
Initial Frequency Drift	-20.00 kHz	20.00 kHz	1.58 kHz	✓


RCV-LE/CA/01/C (Receiver sensitivity)

TX Level: -93.8 dBm, Packets: 1500, Payload: PRBS 9, Length: 37 Bytes, Dirty Transmitter: specification table

Channel: 0				
Correct Packets			1094.00	✓
PER		30.80 %	27.07 %	✓
Channel: 19				
Correct Packets			1054.00	✓
PER		30.80 %	29.73 %	✓
Channel: 39				
Correct Packets			1054.00	✓
PER		30.80 %	29.73 %	✓

Figure 6-1 BLE Performance

Note: ATB1109 EVB #26_5db_3V mixmode 25℃

6.3 BLE Register List

BLE Registers Address

Name	Physical Base Address
BLE	0x40008000

BLE Configuration Registers List

Offset	Register Name	Description
0x0048	BLE_CTL	BLE Control Register
0x004c	BLE_STATE	BLE State Register
0x0050	BLE_INT_CTL	BLE Interrupt Enable Register

6.4 Register Description

6.4.1 BLE_CTL

BLE Control Register

Offset=0x0048

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	0x0
5	BLE_SWBLEAVDD_REQ	The BLEAVDD switching regulator enable 0：disable 1：enable Only in 3V mode When the software is configured into mix mode, this bit	R/W	0x0

		must be set to 0. BLE can switch to switching when the Vbat is greater than 2.6V.		
4	BLEVCC_STAT_REQ	BLEVCC state request enable 0：disable 1：enable	R/W	0x0
3	-	Reserved for analog future use	R/W	0x0
2	LLCC_CLK_REQ_WK_EN	LLCC_CLK_REQ wake pmu enable 0：disable 1：enable	R/W	0x1
1	BLE_SLEEP_REQ	Sleep request enable 0：disable 1：enable	R/W	0x1
0	BLE_WAKE_REQ	Wake request enable 0：disable 1：enable	R/W	0x0

6.4.2 BLE_STATE

BLE State Register

Offset=0x004c

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	0x0
4	LLCC_CLK_o	HCLK clock state 0：clock is not required 1：clock is required	R	x
3	BLE_SWBLEAVDD_o	BLEAVDD regulator state 0：linear regulator 1：switching regulator Only in 3V mode	R	x
2	BLE_VCCSTAT_o	BLEVCC state 0：normal condition 1：the low-battery condition	R	x
1	BLE_AWAKE_o	BLE power state 0：sleep 1：BLE power-supply is on	R	x
0	BLE_3V	BLE 3V MODE state 0:not in 3V mode 1:3V mode	R	x

6.4.3 BLE_INT_CTL

BLE Interrupt Enable Register

Offset=0x0050

Bit(s)	Name	Description	R/W	Reset
31:2	--	Reserved	R	0x0
1	-	Reserved for analog future use	R/W	0x0
0	LLCC_CLK_ENABLE_REQ_INT_EN	LLCC_CLK_Enable_REQ interrupt enable 0：Disable 1：Enable	R/W	0x0

7 System Control

7.1 PMU

7.1.1 Overview

- Wide battery（connected IOVCC）supply voltage range：1.65V~3.6V.
- Analog or digital pin wakeup from STANDBY mode.
- Brown out Reset/ Power on Reset.
- ATB110X BLE Supports 1V or 3V Power mode.

7.1.2 Power architecture

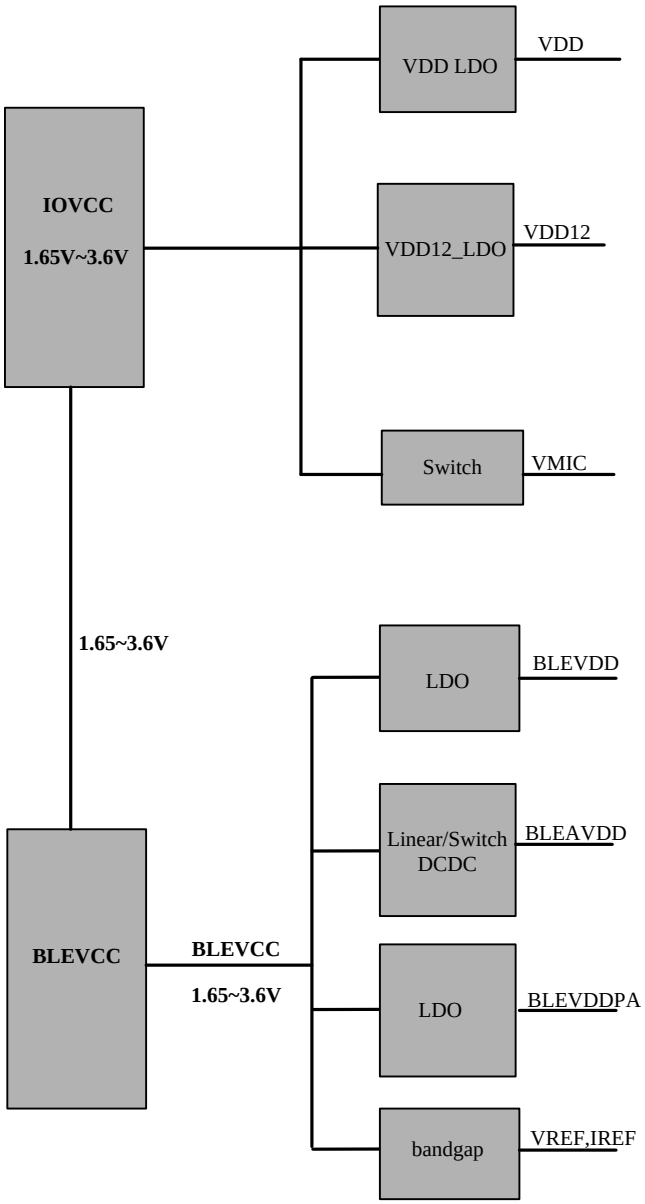


Figure 7-1 Power Supply Block Diagram（BLE 3V MODE）

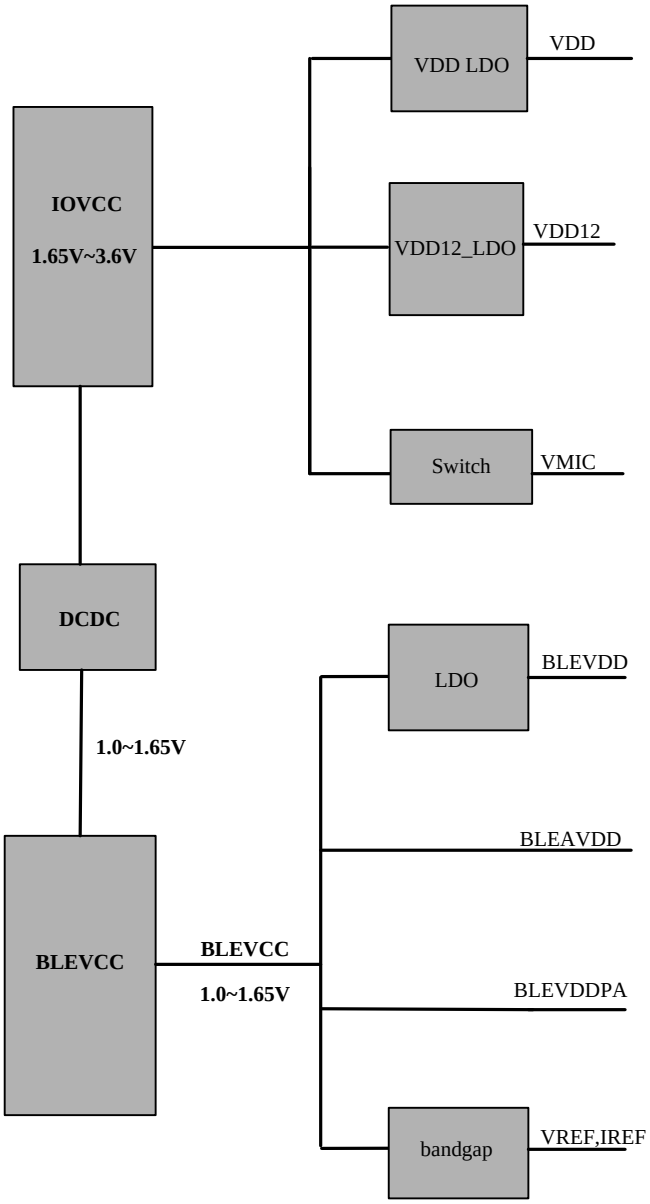


Figure 7-2 Power Supply Block Diagram（BLE 1V MODE）

7.1.2.1 VDD Linear Regulators

The output voltages are highly precise within ±1%, They provide large currents with a significantly small dropout voltage within ±3%. Table 7-1 shows main LDO parameter.

Table 7-1 Main LDO Parameter

LDO	INPUT	OUTPUT	Load
VDD	1.65V~3.6V	0.8V~1.35V	15mA

7.1.2.2 BLE Power

BLEVCC Supports in 1V or 3V domains.

Supply voltage ranges are 1.0V to 1.65V and 1.65V to 3.63V.

For 1V Power mode, BLEVCC, BLEAVDD, BLEVDDPA, and BLEAVDDF must be tied together externally.

- Support 1V linear mode, BLEVCC range: 1.0 – 1.65V

For 3V Power mode, BLEVCC is the primary voltage input. BLEAVDD and BLEVDDPA become outputs. The BLEAVDD output should be filtered off-chip and returned via BLEAVDDF.

- Support 3V linear mode
- Support 3V switcher mode
- Support 3V mixed mode: linear mode during active & switcher mode during sleep

7.1.2.3 BLEAVDD Generating Subsystem

For 3V mode, a switched capacitor DC/DC converter is used to step down battery voltages to 1.0 – 1.1V. It uses a pulse skipping regulation technique in which the converter clock is gated when a voltage comparator detects that the output voltage is above a reference of 1.05V.

A linear regulator is connected in parallel to the DC/DC converter for startup and be switched from switch mode.

7.1.3 A/D Converters

ATB110X integrates one 10-bit ADC module, which can be used to sample battery voltage, temperature and 6 external analog inputs.

The ADC contains 6 external input channels and the input voltage range is 0 to BAT（connected IOVCC） or 0 to 1.2V selected by REG[PMU_ADC_CTL1].

The reference voltage is 1.2V.

The input range of BAT(connected IOVCC) pin is 1.65V to 3.6V.

The range of detectable temperature is -30℃ to 90℃.

Each channel can trigger an interrupt, which will be asserted when data is ready.

7.1.3.1 Mode

The ADC has two operating modes: normal mode and fast mode, the default is normal mode.

The Normal mode can open multiple channels at the same time, optionally working at 2khz/4khz/6khz/8khz. And the Fast mode can only use one channel at a time, raising the sampling frequency to 8 times times the normal mode. Max 64 KHz.

Set REG[PMUADC_CTL2] can be configured as fast Mode, select the channel which to be open.

7.1.3.2 BATADC & TEMPADC

The output data of ADC can be calculated as the following formula：

1.BATADC（Connected IOVCC）

1 LSB= $\frac{3.6}{2^{10}} * \frac{Vref}{1.2}$， When the battery voltage equals V, the ADC data n= $\frac{V}{\frac{3.6}{2^{10}} * \frac{Vref}{1.2}}$

Where Vref is the value of the reference voltage actually value.

For example: Vref=1.2V, 1LSB=3.516mV， So the corresponding data from 0v to 0.0035V is 000h .

V=3600/1024*DATA(mV)

2. TEMPADC

1 LSB= $\frac{Vref}{2^{10}}$， When the voltage of TEMP SENSOR equals V, the ADC data n= $\frac{V}{\frac{Vref}{2^{10}}}$

Where Vref is the value of the reference voltage actually value.

For example: Vref=1.2V, 1LSB=1.17mV， 0~1024 correspondence to -30℃~+90℃

T=120/1024* DATA (decimal)-30℃

7.1.4 Power Mode

7.1.4.1 PMU Mode

Power: STANDBY mode：

IOVCC=3.0V, With XTAL32K, Standby current is 9.3uA (VDD=0.9V).

CHIPEN When pulling down, turn off the power source, in the lowest power state, Iiovcc=200nA (IOVCC =3.0V).

7.1.4.2 PMU_FAULT

BAT (Connected IOVCC) appears low voltage (set), VDD_OK will pull down and reset all registers in VDD domain

7.1.4.3 Wakeup

ATB110x have six wakeup sources:

- GPIO
- UART_Rx
- RTC
- BLE interrupt
- LRADC
- KEY

7.1.5 PMU Register List

PMU Controller Registers Address

Name	Physical Base Address
PMU	0x40008000

PMU Block Configuration Registers List

Offset	Register Name	Description	RESET
0x0000	VD12_CTL	VD12 LDO Set Register	RST_N
0x0004	VDD_CTL	VDD LDO Set Register	VDD_OK
0x0010	PMUADC_CTL0	PMUADC Control Register	RST_N
0x0014	PMUADC_CTL1	PMUADC Input Voltage Control Register	RST_N
0x0018	PMUADC_CTL2	PMUADC Fast Mode Control Register	RST_N
0x001c	PMUADC_INT_CTL	PMUADC Interrupt Enable Register	RST_N
0x0020	PMUADC_INT_PD	PMUADC Interrupt Pending Register	RST_N
0x0024	BATADC_data	BAT（connected IOVCC）ADC DATA Register	RST_N
0x0028	TEMPADC_data	TEMP SENSOR ADC DATA Register	RST_N
0x002c	PMUADC_CH0_data	ADC_CH[0] DATA Register	RST_N
0x0030	PMUADC_CH1_data	ADC_CH[1] DATA Register	RST_N
0x0034	PMUADC_CH2_data	ADC_CH[2] DATA Register	RST_N
0x0038	PMUADC_CH3_data	ADC_CH[3] DATA Register	RST_N
0X003c	PMUADC_CH4_data	ADC_CH[4] DATA Register	RST_N
0x0040	PMUADC_CH5_data	ADC_CH[5] DATA Register	RST_N
0x0044	RAM_CTL	RAM Retention/Power Down Control Register	RST_N
0x0054	WAKE_PD	WAKE UP Source Pending Register	Bit[0]:VDD_OK Bit[1]:RST_N Bit[2]:VDD_OK Bit[3]:RST_N

7.1.6 Register Description

7.1.6.1 VD12_CTL

VD12 LDO Set Register
Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	R	0x0
14	VD12PD_EN	VD12 PD control： 0：Disable 1：Enable	R/W	0x1
13:12	VD12PD_SET	for analog	R/W	0x1
11	-	Reserved for analog future use	R/W	0x0
10:9	VD12_BIAS_SET	for analog	R/W	0x0
8	VD12_LGBIAS_EN	VD12 lgbias control 0：Disable 1：Enable	R/W	0x1
7:5	-	Reserved for analog future use	R/W	0x0
4	VD12_EN	VD12 enable： 0：Disable 1：Enable	R/W	0x1
3	-	Reserved for analog future use	R/W	0x0
2:0	VD12_SET	VD12 voltage level select 000:1.00V 001:1.05V 010:1.10V 011:1.15V 100:1.20V 101:1.25V 110:1.30V 111:1.35V	R/W	0x4

7.1.6.2 VDD_CTL

VDD LDO Set Register
Offset=0x0004

Bit(s)	Name	Description	R/W	Reset

31:6	-	Reserved	R	0x0
5:4	VDD_BIAS_S3	for analog	R/W	0x0
3:0	VDD_SET	VDD voltage level select 0000:0.8V 0001:0.85V 0010:0.9V 0011:0.95V 0100:1.00V 0101:1.05V 0110:1.10V 0111:1.15V 1000:1.2V 1001:1.25V 1010:1.3V 1011:1.35V	R/W	0x2

7.1.6.3 PMUADC_CTL0

PMUADC Control Register

Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31	ADC5_WKEN	ADC_CH[5] wake up enable 0：Disable 1：Enable If the voltage of ADC_CH[5] is small than 0.9*VBAT) or small than 0.9V set by PMUADC_CTL1 bit5 ADC_CH[5]_SET,MCU awake.	R/W	0x0
30	ADC4_WKEN	ADC_CH[4] wake up enable 0：Disable 1：Enable If the voltage of ADC_CH[5] is small than 0.9*VBAT) or small than 0.9V set by PMUADC_CTL1 bit5 ADC_CH[5]_SET,MCU awake.	R/W	0x0
29	ADC3_WKEN	ADC_CH[3] wake up enable 0：Disable 1：Enable If the voltage of ADC_CH[5] is small than 0.9*VBAT) or small than 0.9V set by PMUADC_CTL1 bit5 ADC_CH[5]_SET,MCU awake.	R/W	0x0
28	ADC2_WKEN	ADC_CH[2] wake up enable 0：Disable	R/W	0x0

		1：Enable If the voltage of ADC_CH[5] is small than 0.9*VBAT) or small than 0.9V set by PMUADC_CTL1 bit5 ADC_CH[5]_SET,MCU awake.		
27	ADC1_WKEN	ADC_CH[1] wake up enable 0：Disable 1：Enable If the voltage of ADC_CH[5] is small than 0.9*VBAT) or small than 0.9V set by PMUADC_CTL1 bit5 ADC_CH[5]_SET,MCU awake.	R/W	0x0
26	ADC0_WKEN	ADC_CH[0] wake up enable 0：Disable 1：Enable If the voltage of ADC_CH[5] is small than 0.9*VBAT) or small than 0.9V set by PMUADC_CTL1 bit5 ADC_CH[5]_SET,MCU awake.	R/W	0x0
25:13	-	Reserved	R	x
12	TEST_SARAD	for analog	R/W	0x0
11	I_COMP_SET	for analog	R/W	0x0
10	COMP_TRIM	for analog	R/W	0x1
9:8	FREQ_SET	ADC working frequency set Normal Mode Fast Mode 00： 2 KHz 16KHz 01： 4 KHz 32 KHz 10： 6 KHz 48KHz 11： 8 KHz 64KHz	R/W	0x1
7	ADC_CH5_EN	ADC_CH [5] enable. 0：Disable 1：Enable If ADC5_WKEN=1,should set this bit =1	R/W	0x0
6	ADC_CH4_EN	ADC_CH [4] enable. 0：Disable 1：Enable If ADC4_WKEN=1,should set this bit =1	R/W	0x0
5	ADC_CH3_EN	ADC_CH [3] enable. 0：Disable 1：Enable If ADC3_WKEN=1,should set this bit =1	R/W	0x0
4	ADC_CH2_EN	ADC_CH [2] enable. 0：Disable 1：Enable If ADC2_WKEN=1,should set this bit =1	R/W	0x0
3	ADC_CH1_EN	ADC_CH[1] enable.	R/W	0x0

		0：Disable 1：Enable If ADC1_WKEN=1,should set this bit =1		
2	ADC_CH0_EN	ADC_CH [0] enable. 0：Disable 1：Enable If ADC0_WKEN=1,should set this bit =1	R/W	0x0
1	TEMPADC_EN	TEMP sensor A/D enable 0：Disable, TEMP sensor circuit and output disable 1：Enable, TEMP sensor circuit and output enable	R/W	0x0
0	BATADC_EN	Battery A/D enable 0：Disable 1：Enable	R/W	0x0

7.1.6.4 PMUADC_CTL1

PMUADC Input Voltage Control Register

Offset=0x0014

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	x
5	ADC_CH5_SET	ADC_CH[5] Input Voltage range set: 0：0~VBAT 1：0~1.2V	R/W	0x0
4	ADC_CH4_SET	ADC_CH[4] Input Voltage range set: 0：0~VBAT 1：0~1.2V	R/W	0x0
3	ADC_CH3_SET	ADC_CH[3] Input Voltage range set: 0：0~VBAT 1：0~1.2V	R/W	0x0
2	ADC_CH2_SET	ADC_CH[2] Input Voltage range set: 0：0~VBAT 1：0~1.2V	R/W	0x0
1	ADC_CH1_SET	ADC_CH[1] Input Voltage range set: 0：0~VBAT 1：0~1.2V	R/W	0x0
0	ADC_CH0_SET	ADC_CH[0] Input Voltage range set: 0：0~VBAT 1：0~1.2V	R/W	0x0

7.1.6.5 PMUADC_CTL2

PMUADC Fast Mode Control Register

Offset=0x0018

Bit(s)	Name	Description	R/W	Reset
31:4	--	RESERVED	R	0x0
3:1	FASTMODE_SET	ADC single channel fast mode channel select: 000：BAT 001：TEMP 010：CH[0] 011：CH[1] 100：CH[2] 101：CH[3] 110：CH[4] 111：CH[5]	R/W	0x0
0	FASTMODE_EN	ADC single channel fast mode enable: 0：Disable 1：Enable	R/W	0x0

7.1.6.6 PMUADC_INT_CTL

PMUADC Interrupt Enable Register

Offset=0x001c

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7	ADC_CH5_INT_EN	ADC_CH[5] interrupt enable 0：Disable 1：Enable	R/W	0x0
6	ADC_CH4_INT_EN	ADC_CH[4] interrupt enable 0：Disable 1：Enable	R/W	0x0
5	ADC_CH3_INT_EN	ADC_CH[3] interrupt enable 0：Disable 1：Enable	R/W	0x0
4	ADC_CH2_INT_EN	ADC_CH[2] interrupt enable 0：Disable 1：Enable	R/W	0x0
3	ADC_CH1_INT_EN	ADC_CH[1] interrupt enable 0：Disable 1：Enable	R/W	0x0
2	ADC_CH0_INT_EN	ADC_CH[0] interrupt enable	R/W	0x0

		0：Disable 1：Enable		
1	TEMPADC_INT_EN	TEMPADC interrupt enable 0：Disable 1：Enable	R/W	0x0
0	BATADC_INT_EN	BATADC interrupt enable 0：Disable 1：Enable	R/W	0x0

7.1.6.7 PMUADC_INT_PD

PMUADC Interrupt Pending Register

Offset=0x0020

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7	ADC_CH5_INT_PD	ADC_CH[5] interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0
6	ADC_CH4_INT_PD	ADC_CH[4] interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0
5	ADC_CH3_INT_PD	ADC_CH[3] interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0
4	ADC_CH2_INT_PD	ADC_CH[2] interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0
3	ADC_CH1_INT_PD	ADC_CH[1] interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0
2	ADC_CH0_INT_PD	ADC_CH[0] interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0
1	TEMPADC_INT_PD	TEMPADC interrupt pending	R/W	0x0

		0：not active 1：active Note: Write 1 Clear 0		
0	BATADC_INT_PD	BATADC interrupt pending 0：not active 1：active Note: Write 1 Clear 0	R/W	0x0

7.1.6.8 BATADC_DATA

BATADC DATA Register

Offset=0x0024

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	BATADC	10-bit data，used to indicate Battery voltage（connect IOVCC）。 Input voltage range is: 1.8V~3.6V	R	x

7.1.6.9 TEMPADC_DATA

TEMP SENSOR ADC DATA Register

Offset=0x0028

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	TEMPADC	10-bit data，used to indicate TEMP SENSOR voltage。 Input voltage range is: 0-1.2V	R	x

7.1.6.10 PMUADC_CH0_DATA

ADC_CH0 DATA Register

Offset=0x002c

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	ADC_CH0	10-bit data，used to indicate external analog channel 0 voltage	R	x

7.1.6.11 PMUADC_CH1_DATA

ADC_CH1 DATA Register
Offset=0x0030

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	ADC_CH1	10-bit data，used to indicate external analog channel 1 voltage	R	x

7.1.6.12 PMUADC_CH2_DATA

ADC_CH2 DATA Register
Offset=0x0034

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	ADC_CH2	10-bit data，used to indicate external analog channel 2 voltage	R	x

7.1.6.13 PMUADC_CH3_DATA

ADC_CH3 DATA Register
Offset=0x0038

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	ADC_CH3	10-bit data，used to indicate external analog channel 3 voltage	R	x

7.1.6.14 PMUADC_CH4_DATA

ADC_CH4 DATA Register
Offset=0x003c

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	ADC_CH4	10-bit data，used to indicate external analog channel 4 voltage	R	x

7.1.6.15 PMUADC_CH5_DATA

ADC CH5 DATA Register
Offset=0x0040

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	x
9:0	ADC_CH5	10-bit data，used to indicate external analog channel 5 voltage	R	x

7.1.6.16 RAM_CTL

RAM Retention/Power Down Control Register
Offset=0x0044

Bit(s)	Name	Description	R/W	Reset
32:22	-	Reserved	R	0x0
21:20	-	Reserved for analog future use	R/W	0x0
19	audioRAM_PD_EN	audioRAM block power down enable Write ‘1’ to power down	R/W	0x0
18	audioRAM_RET_EN	audioRAM block retention enable Write ‘1’ to have tagRAM retention	R/W	0x0
17	tagRAM_PD_EN	tagRAM block power down enable Write ‘1’ to power down	R/W	0x0
16	tagRAM_RET_EN	tagRAM block retention enable Write ‘1’ to have tagRAM retention	R/W	0x0
15	RAM7_PD_EN	RAM7 block power down enable Write ‘1’ to power down	R/W	0x0
14	RAM6_PD_EN	RAM6 block power down enable Write ‘1’ to power down	R/W	0x0
13	RAM5_PD_EN	RAM5 block power down enable Write ‘1’ to power down	R/W	0x0
12	RAM4_PD_EN	RAM4 block power down enable Write ‘1’ to power down	R/W	0x0
11	RAM3_PD_EN	RAM3 block power down enable Write ‘1’ to power down	R/W	0x0
10	RAM2_PD_EN	RAM2 block power down enable Write ‘1’ to power down	R/W	0x0
9	RAM1_PD_EN	RAM1 block power down enable Write ‘1’ to power down	R/W	0x0
8	RAM0_PD_EN	RAM0 block power down enable Write ‘1’ to power down	R/W	0x0
7	RAM7_RET_EN	RAM7 block retention enable	R/W	0x0

		Write ‘1’ to have RAM7 retention		
6	RAM6_RET_EN	RAM6 block retention enable Write ‘1’ to have RAM6 retention	R/W	0x0
5	RAM5_RET_EN	RAM5 block retention enable Write ‘1’ to have RAM5 retention	R/W	0x0
4	RAM4_RET_EN	RAM4 block retention enable Write ‘1’ to have RAM4 retention	R/W	0x0
3	RAM3_RET_EN	RAM3 block retention enable Write ‘1’ to have RAM3 retention	R/W	0x0
2	RAM2_RET_EN	RAM2 block retention enable Write ‘1’ to have RAM2 retention	R/W	0x0
1	RAM1_RET_EN	RAM1 block retention enable Write ‘1’ to have RAM1 retention	R/W	0x0
0	RAM0_RET_EN	RAM0 block retention enable Write ‘1’ to have RAM0 retention	R/W	0x0

Note：If RAMx_PD_EN set1, RAMx_RET_EN auto change to1.

7.1.6.17 WAKE_PD

WAKE UP Source Pending Register

Offset=0x0054

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	ADC_WKPD	Any one way ADC wake-up pending 0: No SARADC Wake up Interrupt 1: Any way SARADC occurs wake up Interrupt Write 1 clear 0.	R/W	0x0
2	S3PD	S3 power down pending 0: never entered S3 1: entered S3 Write 1 clear 0.	R/W	0x0
1	LLCC_CLK_ENABLE_REQ_PD	LLCC_CLK_Enable_REQ interrupt pending 0:No LLCC_CLK_Enable_REQ interrupt 1:Occurred LLCC_CLK_Enable_REQ interrupt Write 1 clear 0.	R/W	0x0
0	POWER_ON_PD	First power up or CHIPEN pin wake up pending 0:never 1: first power up or CHIPEN wake up pending Write 1 clear 0.	R/W	0x0

7.2 CMU

7.2.1 Overview

The CMU Controller of ATB110X has following features:

- 32MHz crystal oscillator, using external 8pf 32MHz crystal, crystal demand precision less than ±25ppm(-40℃~85℃).
- 32KHz crystal oscillator, using external 9pf 32KHz crystal,crystal demand precision less than ±100ppm (-40℃~85℃)
- 3MHz RC oscillator，precision accuracy 15%.
- Support build-in HCL32K (without 32k crystal) for low BOM cost mode
- The CMU (Clock Management Unit) can select CLK_32M_O, CLK_32K_O, RC3M, and HCL_32K, HCL_4Hz as the clock of each peripheral.
- The clock divider of all blocks can be selected by CMU.
- The clock of each peripheral can be gated by module to limit current consumption in unused branches of the clock tree
- Two PLLs: AUDIOPLL and COREPLL.
- AUDIOPLL support for fine-tuning,output 24.576M/22.5792M
- COREPLL: 32M/48M/64M/80M/96M output and support the spread function.

7.2.2 Function Description

The CMU (Clock Management Unit) can select CLK_32M_O, CLK_32K_O, RC3M, and HCL_32K, HCL_4Hz, AUDIOPLL and COREPLL. As the clock of each peripheral and select different clock sources to each memory block.If the peripheral clock is disabling, the S_CLK for AHB registers access of this peripheral is also disable.

All modules except the CPU core are driven to DC after power on reset. The CPU core and all the RAM/ROM blocks are driven by the HFCLK at this time.

The clock source and frequency division of each module are shown in the following diagram

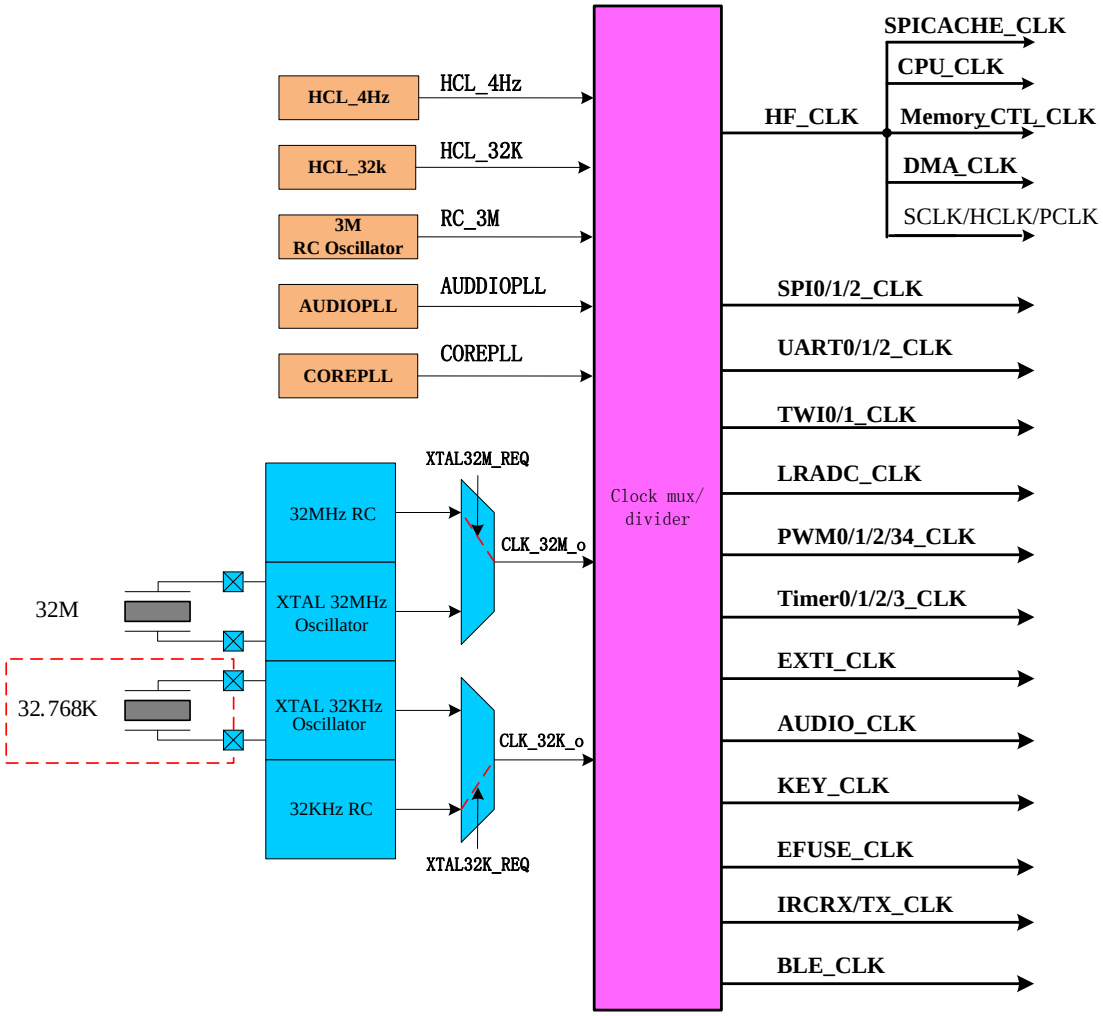


Figure 7-3 Block Diagram of CMU

7.2.3 CMU Register List

CMU Controller Registers Address

Name	Physical Base Address
CMU	0x40002000

CMU Controller Registers

Offset	Register Name	Description
0x0000	X32K_CTL	32K XTAL clock control register
0x0004	X32M_CTL	32M XTAL clock control register
0x0008	ACT_3M_CTL	RC 3M clock control register
0x000C	CMU_SYSCLK	SYSCLK Control Register
0x0010	CMU_DEVRST	DEVRST Control Register
0x0014	CMU_DEVCLKEN	DEVCLKEN Control Register

0x0018	CMU_SPI0CLK	SPI0CLK Control Register
0x001C	CMU_SPI1CLK	SPI1CLK Control Register
0x0020	CMU_SPI2CLK	SPI2CLK Control Register
0x0024	CMU_PWM0CLK	PWM0 clock Control Register
0x0028	CMU_PWM1CLK	PWM1 clock Control Register
0x002C	CMU_PWM2CLK	PWM2 clock Control Register
0x0030	CMU_PWM34CLK	PWM3 clock Control Register
0x0038	CMU_AUDIOCLK	AUDIO clock control register
0x003c	CMU_TIMER0CLK	Timer0 clock Control Register
0x0040	CMU_TIMER1CLK	Timer1 clock Control Register
0x0044	CMU_TIMER2CLK	Timer2 clock Control Register
0x0048	CMU_TIMER3CLK	Timer3 clock Control Register
0x004C	CMU_EXTICLK	EXTICLK Control Register
0x0050	CMU_MEMCLKEN	RAMCLK Control Register
0x0058	CHIP_VERSION	Chip version
0x005c	RMU_RSTSTA	BLE reset signal state register
0x0060	XTAL_32M_REQ	32M clock requires control register
0x0100	COREPLL_CTL	COREPLL control register
0x0104	AUDPLL_CTL	AudioPLL control register
0x010c	COREPLL_SSC_CTL	COREPLL ssc register
0x2200	HCL32K_CTL	HCL32KHz control register
0x2240	HCL4Hz_CTL	HCL4Hz control register

7.2.4 CMU Register Description

7.2.4.1 X32K_CTL

X32K OSC control register.

Offset = 0x0000(VDD)

Bit(s)	Name	Description	R/W	Reset
31:3	-	Reserved	R	0x0
2	CKO32K_OEN	CKO32K clock output enable 0:disable 1:enable If disable, P_HCL32K would output signal ‘0’	R/W	0x0
1	XTAL32K_ON	When XTAL32K_REQ set to1, this flag bit read as 1 indicate select 32K crystal version.	R	x

0	XTAL32K_REQ	X32K crystal or RC version select: 0: RC version 1: crystal version	R/W	0x0

7.2.4.2 X32M_CTL

X32M OSC control register.

Offset = 0x0004(VDD)

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1	XTAL32M_ON	When XTAL32M_REQ set to 1, this flag bit read as 1 indicate select 32M crystal version.	R	x
0	XTAL32M_REQ	32M enable 0:disable 1:enable If BLE was in sleep states, 32M_EN would wake up the BLE. If BLE was in wake states, 32M_EN would require the crystal 32M only.	R/W	0x1

7.2.4.3 ACT_3M_CTL

3M OSC control register.

Offset = 0x0008(VDD)

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	0x0
5	RC3M_OK	RC3M OK ,indicate the RC3M clock is ok	R	x
4:1	RSEL	RSEL:	R/W	0x8
0	RC3MEN	RC_3M enable signal 0:Disable 1: Enable	R/W	0x1

7.2.4.4 CMU_SYSCLK

CMU_SYSCLK Control register

Offset = 0x000C

Bit(s)	Name	Description	R/W	Reset

31:18	-	reserved	R	0x0
17:16	BLE_HCLK_DIV	BLE HCLK divisor 00 : /1 01 : /2 10 : /4 11 : reserved	R/W	0x0
15	BLE_HCLK_SEL	HBridge bypass enable 0: bypass, BLE HCLK = H_CLK 1: not bypass, BLE HCLK = H_CLK/BLE_HCLK_DIV	R/W	0x0
14	-	Reserved	R	0x0
13	HOSC_A	Cpu high freq active 0:not active 1:active	R	x
12	LOSC_A	Cpu low freq active 0:not active 1:active	R	x
11:10	APB_DIV	APB_CLK divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
9	AHB_DIV	CPU_CLK divisor 0: /1 1: /2	R/W	0x0
8	CPU_COREPLL	CPU_COREPLL clock ACTIVE 0:not active 1:active	R	x
7	CPU_32M	CPU_32M clock ACTIVE 0:not active 1:active	R	x
6	CPU_32K	CPU_32K clock ACTIVE 0:not active 1:active	R	x
5	CPU_3M	CPU_3M clock ACTIVE 0:not active 1:active	R	x
4	SLEEP_HFCLK_SEL	SLEEP_HFCLK_SEL 0:32K 1:3M	R/W	0x0
3	-	Reserved	R	0x0
2	PCLKG	PCLK GATED select: 0: enable 1: disable	R/W	0x1

1:0	CPU_CLK_SEL	CPU_CLK_SEL select: 00:RC_3M 01:CK_32K_O 10:CLK_32M_O 11:CK_COREPLL	R/W	0x0

Note: When the CPU needs to reset the BLE module, first switch HFCLK to RC_3M

7.2.4.5 CMU_DEVRST

CMU_DEVRST Control register （VDD）

Offset = 0x0010

Bit(s)	Name	Description	R/W	Reset
31	IRC	IRC controller reset	R/W	0x0
30	BIST	Bist controller reset	R/W	0x0
29:27	-	Reserved	R	0x0
26	BLE_LLCC	BLE LLCC controller reset	R/W	0x1
25	BLE	BLE Soft IP control block reset.	R/W	0x1
24	HRESET	BLE HCLK reset control block reset.	R/W	0x1
23:17	-	Reserved	R	0x0
16	AUDIO	Including ADC_D and DMICIF and I2STX and I2SRX	R/W	0x0
15	KEY	KEY control block reset.	R/W	0x0
14:11	-	Reserved	R	0x0
10	PWM0	PWM0~4 control block reset.	R/W	0x0
9	TWI1	TWI1 control block reset.	R/W	0x0
8	TWI0	TWI0 control block reset.	R/W	0x0
7	UART2	UART2 control block reset.	R/W	0x0
6	UART1	UART1 control block reset.	R/W	0x0
5	UART0	UART0 control block reset.	R/W	0x0
4	SPI2	SPI2 control block reset.	R/W	0x0
3	SPI1	SPI1 control block reset.	R/W	0x0
2	SPI0	SPI0 control block reset.	R/W	0x0
1	SPICACHE	SPICACHE control block reset.	R/W	0x0
0	DMA	DMA control block reset.	R/W	0x0

Note: Write ‘0’ to reset the block.

7.2.4.6 CMU_DEVCLKEN

CMU_DEVCLKEN Control register

Offset = 0x0014

Bit(s)	Name	Description	R/W	Reset
31	IRC_CLK	IRC 200K clock enable bit: 0: disable 1: enable	R/W	0x0
30	IRC_RXCLK	IRC 16M clock enable bit: 0: disable 1: enable	RW	0x0
29	-	Reserved	RW	0x1
28	HCL32K	HCL32K clock enable bit 0: disable 1: enable	R/W	0x0
27	HCL4Hz	HCL4Hz clock enable bit 0: disable 1: enable	R/W	0x0
26	LLCC_CLK_REQ_o	BLE Soft IP HCLK clock request 0: de-asserted 1: asserted	R	x
25	BLE_HCLK_Gating	BLE Soft IP HCLK clock gating 0: disable 1: enable	R/W	0x1
24	BLE_HCLK_EN	BLE Soft IP HCLK clock enable bit 0: disable 1: enable	R/W	0x0
23	TIMER3CLKEN	Timer3 clock enable bit: 0: disable 1: enable	R/W	0x0
22	TIMER2CLKEN	Timer2 clock enable bit: 0: disable 1: enable	R/W	0x0
21	TIMER1CLKEN	Timer1 clock enable bit: 0: disable 1: enable	R/W	0x0
20	TIMER0CLKEN	Timer0 clock enable bit: 0: disable 1: enable	R/W	0x0
19	LRADC	LRADC controller clock enable bit: 0: disable 1: enable	R/W	0x0
18	I2SRX	I2SRX clock enable bit: 0: disable 1: enable	R/W	0x0
17	I2STX	I2STX clock enable bit:	R/W	0x0

		0: disable 1: enable		
16	ADC	ADC clock enable bit. Including ADC and DMIC 0: disable 1: enable	R/W	0x0
15	KEY	KEY clock enable bit: 0: disable 1: enable	R/W	0x0
14	PWM4CLKEN	PWM4 clock enable bit: 0: disable 1: enable	R/W	0x0
13	PWM3CLKEN	PWM3 clock enable bit: 0: disable 1: enable	R/W	0x0
12	PWM2CLKEN	PWM2 clock enable bit: 0: disable 1: enable	R/W	0x0
11	PWM1CLKEN	PWM1 clock enable bit: 0: disable 1: enable	R/W	0x0
10	PWM0CLKEN	PWM0 clock enable bit and the PWM controller clock enable bitnote2 0: disable 1: enable	R/W	0x0
9	TWI1CLKEN	TWI1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
8	TWI0CLKEN	TWI0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
7	UART2CLKEN	UART2 controller clock enable bit: 0: disable 1: enable	R/W	0x0
6	UART1CLKEN	UART1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
5	UART0CLKEN	UART0 Controller clock enable bit: 0: disable 1: enable	R/W	0x0
4	SPI2CLKEN	SPI2 controller clock enable bit: 0: disable 1: enable	R/W	0x0
3	SPI1CLKEN	SPI1 controller clock enable bit:	R/W	0x0

		0: disable 1: enable		
2	SPI0CLKEN	SPI0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
1	SPICACHECLKEN	SPICACHECLK controller clock enable bit: 0: disable 1: enable	R/W	0x0
0	DMACLKEN	DMA clock enable bit: 0: disable 1: enable	R/W	0x0

Note:

1. Some other clocks are always on, include: APB_En (APB bridge clock), CMU_En, RTC_En, INTC_En.
2. To use PWM1~PWM4,mut enable PWM controller clock enable(PWM0CLKEN)

7.2.4.7 CMU_SPI0CLK

CMU_SPI0CLK Control register

Offset = 0x0018

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	SEL	SPI clock select: 0 : CLK_32M_O 1 : CK_COREPLL	R/W	0x0
2:0	DIV	SPI0 controller clock divisor: 0x00: /1 … n:/(2^n) … 0x05/32 Others: reserved SPI_CLK=CLK_32M_O/DIV	R/W	0x0

7.2.4.8 CMU_SPI1CLK

CMU_SPI1CLK Control register

Offset = 0x001C

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	SEL	SPI clock select: 0 : CLK_32M_O 1 : CK_COREPLL	R/W	0x0
2:0	DIV	SPI1 controller clock divisor: 0x00: /1 … n:/(2^n) … 0x05/32 Others: reserved SPI_CLK=CLK_32M_O/DIV	R/W	0x0

7.2.4.9 CMU_SPI2CLK

CMU_SPI2CLK Control register

Offset = 0x0020

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	SEL	SPI clock select: 0 : CLK_32M_O 1 : CK_COREPLL	R/W	0x0
2:0	DIV	SPI1 controller clock divisor: 0x00: /1 … n:/(2^n) … 0x05/32 Others: reserved SPI_CLK=CLK_32M_O/DIV	R/W	0x0

7.2.4.10 CMU_PWM0CLK

CMU_PWM0CLK Control register

Offset = 0x0024

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0

3	CLKSEL	PWM controller clock select: 0: CLK_32M_O 1: CLK_32K_O	R/W	0x0
2:0	CLKDIV	PWM controller clock divisor: 0: /1 1: /2 2: /4 3: /8 4: /16 5: /32 6: /64 7: /128	R/W	0x0

7.2.4.11 CMU_PWM1CLK

CMU_PWM1CLK Control register

Offset = 0x0028

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CLKSEL	PWM controller clock select: 0: CLK_32M_O 1: CLK_32K_O	R/W	0x0
2:0	CLKDIV	PWM controller clock divisor: 0: /1 1: /2 2: /4 3: /8 4: /16 5: /32 6: /64 7: /128	R/W	0x0

7.2.4.12 CMU_PWM2CLK

CMU_PWM2CLK Control register

Offset = 0x002C

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0

3	CLKSEL	PWM controller clock select: 0: CLK_32M_O 1: CLK_32K_O	R/W	0x0
2:0	CLKDIV	PWM controller clock divisor: 0: /1 1: /2 2: /4 3: /8 4: /16 5: /32 6: /64 7: /128	R/W	0x0

7.2.4.13 CMU_PWM34CLK

CMU_PWM3_PWM4 CLK Control register

Offset = 0x0030

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CLKSEL	PWM controller clock select: 0: CLK_32M_O 1: CLK_32K_O	R/W	0x0
2:0	CLKDIV	PWM controller clock divisor: 0: /1 1: /2 2: /4 3: /8 4: /16 5: /32 6: /64 7: /128	R/W	0x0

7.2.4.14 CMU_AUDIOCLK

CMU_PWM0CLK Control register

Offset = 0x0038

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0

<table>
<tr><td>20:19</td><td>RX_SRC</td><td>RX clock source select
00:RXCLK
01:TXCLK
10:EXT_CLKIN
11:Reserved</td><td>R/W</td><td>0x0</td></tr>
<tr><td>18:16</td><td>RX_DIV</td><td>Audio_clk divisor from AUDIOPLL
<table>
<tr><td rowspan="2">CLKDIV</td><td colspan="2">PLL_CLK(MHz)</td></tr>
<tr><td>24.576</td><td>22.5792</td></tr>
<tr><td>000:/1</td><td>24.576</td><td>22.5792</td></tr>
<tr><td>001:/2</td><td>12.288</td><td>11.2896</td></tr>
<tr><td>002:/3</td><td>8.192</td><td>7.5264</td></tr>
<tr><td>003:/4</td><td>6.144</td><td>5.6448</td></tr>
<tr><td>004:/6</td><td>4.096</td><td>3.7632</td></tr>
<tr><td>005:/8</td><td>3.072</td><td>2.8224</td></tr>
<tr><td>006:/12</td><td>2.048</td><td>1.8816</td></tr>
<tr><td>007:reserved</td><td>-</td><td>-</td></tr>
</table>
In I2SRX master mode, there is 256FS for I2SRX module
In I2SRX slave mode while no extern mclk input,512*FS was need for I2SRX module
In TDM4 RX slave mode while no extern mclk input, a mclk unless than 1024*FS was need for I2SRX module.
PLL_CLK select in AUDIOPLL_CTL register</td><td>R/W</td><td>0x6</td></tr>
<tr><td>15:12</td><td>-</td><td>Reserved</td><td>R</td><td>0x0</td></tr>
<tr><td>11</td><td>TX_SRC</td><td>TX clock source select
0:TXCLK
1:EXT_CLKIN</td><td>R/W</td><td>0x0</td></tr>
<tr><td>10:8</td><td>TX_DIV</td><td>Audio_clk divisor from AUDIOPLL
<table>
<tr><td rowspan="2">CLKDIV</td><td colspan="2">PLL_CLK(MHz)</td></tr>
<tr><td>24.576</td><td>22.5792</td></tr>
<tr><td>000:/1</td><td>24.576</td><td>22.5792</td></tr>
<tr><td>001:/2</td><td>12.288</td><td>11.2896</td></tr>
<tr><td>002:/3</td><td>8.192</td><td>7.5264</td></tr>
<tr><td>003:/4</td><td>6.144</td><td>5.6448</td></tr>
<tr><td>004:/6</td><td>4.096</td><td>3.7632</td></tr>
<tr><td>005:/8</td><td>3.072</td><td>2.8224</td></tr>
<tr><td>006:/12</td><td>2.048</td><td>1.8816</td></tr>
<tr><td>007:reserved</td><td>-</td><td>-</td></tr>
</table>
In i2stx master mode, there is 256FS for I2STX module
In i2stx slave mode while no extern mclk input,512*FS was need for I2STX module
PLL_CLK select in AUDIOPLL_CTL register</td><td>R/W</td><td>0x6</td></tr>
<tr><td>7:3</td><td>-</td><td>Reserved</td><td>R</td><td>0x0</td></tr>
<tr><td>2:0</td><td>ADC_DIV</td><td>Audio_clk divisor from AUDIOPLL</td><td>R/W</td><td>0x0</td></tr>
</table>

		PLL_CLK=24.576MHz				
		Reg_Cfg	CLK_DIV	ADC_CLK		
		0x0	6	4.096M		
		0x1	8	3.072M		
		0x2	12	2.048M		
		0x3	24	1.024M		
		0x4	48	512K		
		others	reserved	-		

7.2.4.15 CMU_TIMER0CLK

CMU_TIMER0CLK Control register

Offset = 0x003C

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	0x0
4	TCSS	Timer clock source select 0:CLK_32M_O 1: CLK_32K_O	R/W	0x0
3:0	DIV	TIMER0 controller clock divisor: TIMER0_CLK =CLK_32M_O/(2^{DIV}) 0: /1 1: /2 2: /4 3: /8 … 15: /32768	R/W	0x0

7.2.4.16 CMU_TIMER1CLK

CMU_TIMER1CLK Control register

Offset = 0x0040

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	0x0
4	TCSS	Timer clock source select 0:CLK_32M_O	R/W	0x0

		1: CLK_32K_O		
3:0	DIV	TIMER1 controller clock divisor: TIMER1_CLK =CLK_32M_O/(2^{DIV}) 0: /1 1: /2 2: /4 3: /8 … 15: /32768	R/W	0x0

7.2.4.17 CMU_TIMER2CLK

CMU_TIMER2CLK Control register

Offset = 0x0044

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	0x0
4	TCSS	Timer clock source select 0:CLK_32M_O 1: CLK_32K_O	R/W	0x0
3:0	DIV	TIMER2 controller clock divisor: TIMER2_CLK =CLK_32M_O/(2^{DIV}) 0: /1 1: /2 2: /4 3: /8 … 15: /32768	R/W	0x0

7.2.4.18 CMU_TIMER3CLK

CMU_TIMER3CLK Control register

Offset = 0x0048

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	0x0
4	TCSS	Timer clock source select	R/W	0x0

		0:CLK_32M_O 1: CLK_32K_O		
3:0	DIV	TIMER3 controller clock divisor: TIMER3_CLK =CLK_32M_O/(2^{DIV}) 0: /1 1: /2 2: /4 3: /8 … 15: /32768	R/W	0x0

7.2.4.19 CMU_EXTICLK

CMU_EXTICLK Control register

Offset = 0x004C

Bit(s)	Name	Description	R/W	Reset
31:1	-	Reserved	R	0x0
0	CLKSEL	EXTI controller clock select: 0: CLK_32K_O 1: RC3M	R/W	0x0

7.2.4.20 CMU_MEMCLKEN

CMU_MEMCLKEN Control register

Offset = 0x0050

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	ROM0CLKEN	ROM0 clock enable bit : 0: disable 1: enable	R/W	0x1
7	RAM7CLKEN	RAM7clock enable bit : 0: disable 1: enable	R/W	0x1
6	RAM6CLKEN	RAM6clock enable bit : 0: disable 1: enable	R/W	0x1
5	RAM5CLKEN	RAM5 clock enable bit :	R/W	0x1

		0: disable 1: enable		
4	RAM4CLKEN	RAM4 clock enable bit : 0: disable 1: enable	R/W	0x1
3	RAM3CLKEN	RAM3 clock enable bit : 0: disable 1: enable	R/W	0x1
2	RAM2CLKEN	RAM2 clock enable bit : 0: disable 1: enable	R/W	0x1
1	RAM1CLKEN	RAM1 clock enable bit : 0: disable 1: enable	R/W	0x1
0	RAM0CLKEN	RAM0 clock enable bit : 0: disable 1: enable	R/W	0x1

7.2.4.21 COREPLL_CTL

Corepll control register.

Offset = 0x0100(VDD)

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R/W	0x0
12:8	LDIV	When APS[3] = 1,corepll output frequency control: Freq = 8M * LDIV, LDIV>=5; Debug used	R/W	0x0
7:6	-	Reserved	R/W	0x0
5	LOCK	COREPLL phase match detect: 0: COREPLL phase not match; 1: COREPLL phase match	R	x
4	EN	COREPLL enable 0: disable 1: enable	R/W	0x0
3:0	APS	COREPLL select: 0000 : 32M **** 0001 : 48M 0010 : 64M 0011 : 80M 0100 : 96M	R/W	0x0

		0101~0111 : reserved 1xxx: If ASP[3] = 1, COREPLL output freq control by LDIV , reference to COREPLL_CTL[12:8]		

7.2.4.22 AUDPLL_CTL

Audiopll control register.

Offset = 0x0104(VDD)

Bit(s)	Name	Description	R/W	Reset
31:7	-	Reserved	R	0x0
6	-	For analog future use	R/W	0x0
5	LOCK	AUDIOPLL phase match detect: 0: AUDIOPLL phase not match; 1: AUDIOPLL phase match	R	x
4	EN	AUDIOPLL enable 0: disable 1: enable	R/W	0x0
3:0	AUD_APS	AUDIO PLL Clock Select 0000:22.5185MHz 0001:22.5574MHz 0010:22.5882MHz 0011:22.6341MHz 0100:24.5106MHz 0101:24.5714MHz 0110:24.5797MHz 0111:24.6486MHz	R/W	0x0

7.2.4.23 COREPLL_SSC_CTL

COREPLL debug control register.

Offset = 0x010c (VDD)

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	R	0x0
14	SSC_EN	spread spectrum in PLL enable 0: disable 1: enable	R/W	0x0
13:0	SSC_config	Set ssc block clock config	R/W	0x0FC8

7.2.4.24 HCL32K_CTL

HCL control register

Offset = 0x2200(VDD)

Bit(s)	Name	Description	R/W	Reset
31:14	-	Reserved, be read as zero	R	0x0
12:4	HCL32K_CONFIG	HCL CONFIG	R/W	0x2A
3:1	-	Reserved	R	x
0	Hcl_32K_en	Hcl_32K Enable 0:disable 1: enable	R/W	0x0

7.2.4.25 HCL4Hz_CTL

HCL control register

Offset = 0x2240(VDD)

Bit(s)	Name	Description	R/W	Reset
31:16	HCL4Hz_ADJ	HOSC adjust data	R/W	0x0
15:12	-	Reserved	R	x
3:2	HCL4HZ_CONFIG	HCL CONFIG	R/W	0x128
1	-	Reserved	R	x
0	Hcl_4Hz_en	Hcl_4Hz Enable 0:disable 1: enable	R/W	0x0

7.3 Reset/Boot

7.3.1 Overview

Reset module manages the reset actions of the (SOC&BLE), include below:

- Reset signal of pin from P_Reset
- Reset signal from register
- Watch dog reset
- A Power-on reset

7.3.2 Function Description

Table 7-2 Scope of reset action

module	Power on reset	Chip_en	dev_rst	WD_rst	Preset	DEBUG_SYS_RST
CPU(M0)	Yes	Yes	-	Yes	Yes	Yes
CPU(debug module)	Yes	Yes	Yes	Yes	Yes	No
BLE	Yes	Yes	Yes	Yes	Yes	Yes
CMU	Yes	Yes	No	Yes	Yes	Yes
PMU	Yes	Yes	No	No	Yes	No
HCL	Yes	Yes	No	No	Yes	No
Other modules	Yes	Yes	Yes	Yes	Yes	Yes

7.4 RTC/WD/HCL

7.4.1 Overview

- A individual power supply pin: VDD and VDD12
- Internal oscillator or HCL optional
- Calendar with a alarm IRQ
- Two Timers with IRQS
- A watch dog which can be configured optional as IRQ or Reset
- With two HCL Circuit, one can calibrate 32.768KHz,another one can calibrate 4Hz
- HCL32K precious within 200ppm
- HCL4Hz precious within 20ppm

7.4.2 Function Description

7.4.2.1 Calendar with alarm IRQ

When cal_en enable, the calendar start to count, the minimum unit is second.

The alarm is a compare which alarm daily. When the alm_en is enable and “alarm time = calendar time”, an alm_irq is sent out.

7.4.2.2 Watch dog

Write 1 to WDEN will enable WD. when WD timer overflows, An internal reset or IRQ is generated. An internal reset is generated to force the system into reset status and then reboot.The WD timer overflows interval is set by CLKSEL.

Write 1 to CLR will clear the WD timer. The CLR will be cleared automatically after the WD timer cleared Write 1 to IRQP will clear the WD IRQ pending.

7.4.2.3 TIMER0/1

When EN=1, T0_VAL count down until equal to zero, If ZIEN=1, An IRQ will generate when T0_VAL=0. The IRQ can be cleared by writing 1 to ZIPD. When timer was working, reading register Tx_CNT could get the current timer counter.

When EN=0, T0_VAL can be written, but timer0 do not work.

There are 2 timers: timer0 and timer1, the two timers are the same logic.

7.4.2.4 TIMER2/3

Timer2/3 can work in three modes:

- Normal Timer
- Input counter
- Input Capture mode

7.4.3 RTC Register List

RTC base address

Name	Physical Base Address
RTC	0x40004000

RTC Controller Registers

Offset	Register Name	Description
0x0000	RTC_CTL	RTC Control Register
0x0004	RTC_DHMSALM	RTC Day Alarm Register
0x0008	RTC_DHMS	RTC Day Register
0x000c	RTC_YMD	RTC Year Register
0x0010	RTC_ACCESS	RTC freely access Register
0x001C	WD_CTL	Watch Dog Control register

7.4.4 RTC Register Description

7.4.4.1 RTC_CTL

Calendar Control Register
Offset=0x0000（VDD）

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7	Calendar4Hz_select	Calendar 4Hz clock select 0: divisor from CKO32K 1: HCL_4Hz	R/W	0x0
6	CKO32KHz_ss	CKO32KHz clock select 0: X32K 1: HCL_32K If use HCL_32K，Should be enable HCL_32K first.	R/W	0x0
5:4	-	Reserved	R	x

3	LEAP	RTC Leap Year bit 1: leap year 0: not leap year	R	0x1
2	CAL_EN	Calendar Enable 0: Disable 1: Enable	R/W	0x0
1	ALIE	Alarm IRQ Enable 0: Disable 1: Enable	R/W	0x0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	R/W	0x0

NOTE:

1. The CAL_EN bit must be disabled when The RTC_DHMS / RTC_YMD register being written. And RTC_DHMS / RTC_YMD register must be written before CAL_EN is enabled when set the time, or error will occur.

7.4.4.2 RTC_DHMSALM

Calendar DHMSALM Register

Offset=0x0004（VDD）

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20:16	HOUEAL	Alarm hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0
13:8	MINAL	Alarm minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0x0

7.4.4.3 RTC_DHMS

Calendar DHMS Register

Offset=0x0008（VDD）

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20:16	HOUR	Time hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0

13:8	MIN	Time minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SEC	Time second setting 00H – 3BH	R/W	0x0

7.4.4.4 RTC_YMD

Calendar YMD Register
Offset=0x000c（VDD）

Bit(s)	Name	Description	R/W	Reset
31:23	-	Reserved	R	0x0
22:16	YEAR	Time year setting 00H – 63H	R/W	0x0
15:12	-	Reserved	R	0x0
11:8	MON	Time month setting 01H – 0CH	R/W	0x1
7:5	-	Reserved	R	0x0
4:0	DATE	Time day setting 01H – 1FH	R/W	0x1

7.4.4.5 RTC_ACCESS

Calendar Access control Register
Offset=0x0010（VDD）

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7:0	ACCESS	These bits can be accessed by CPU freely.	R/W	0x0

7.4.4.6 WD_CTL

Watchdog control Register
Offset=0x001C（VDD）

Bit(s)	Name	Description	R/W	Reset
31..7	-	Reserved	R	x
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	R/W	0x0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Reset,1: irq-.	R/W	0x0

		0：Send Reset signal when watchdog overflow. 1：Send IRQ signal when watchdog overflow.		
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 1: Enable 0: Disable	R/W	0x0
3..1	CLKSEL	Watch Dog timer CUPDATA Select, WDCKS CUPDATA Selected Watch Dog Length The watch dog's overflow value is 180. 000:1khz 176 ms 001:512hz 352 ms 010:256hz 703ms 011:128hz 1.4 s 100:64hz 2.8s 101:32hz 5.6 s 110:16hz 11.2s 111:16khz 11.25ms	R/W	0x0
0	-	Reserved	R	x

7.4.5 TIMER Register List

TIMER base address

Name	Physical Base Address
TIMER	0x40004100

TIMER Controller Registers

Offset	Register Name	Description
0x0000	T0_CTL	Timer0 Control register
0x0004	T0_VAL	Timer0 Value
0x0008	T0_CNT	Timer0 count register
0x0040	T1_CTL	Timer1 Control register
0x0044	T1_VAL	Timer1 Value lower byte
0x0048	T1_CNT	Timer1 count register
0x0080	T2_CTL	Timer2 Control register
0x0084	T2_VAL	Timer2 Value register
0x0088	T2_CNT	Timer2 count register
0x008C	T2_CAP	Timer2 capture value register
0x00C0	T3_CTL	Timer3 Control register
0x00C4	T3_VAL	Timer3 Value register
0x00C8	T3_CNT	Timer3 count register

0x00CC	T3_CAP	Timer3 capture value register

7.4.6 TIMER Register Description

7.4.6.1 T0_CTL

Timer0 control register
Offset=0x0000（VDD）

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	x
5	EN	Timer Enable 0:Disable, 1:Enable	R/W	0x0
4:3	-	Reserved	R	x
2	RELO	Timer0 Reload 0:Not reload,1:Reload	R/W	0x0
1	ZIEN	Timer0 Zero IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the irq signal until the pending bit was cleared.	R/W	0x0
0	ZIPD	Timer IRQ Pending, Writing 0 to clear this bit.	R/W	0x0

Note: The timer only can count down.

7.4.6.2 T0_VAL

Timer0 value register
Offset=0x0004（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	VAL	Read or write Timer/Counter value register	W	0x0

7.4.6.3 T0_CNT

Timer0 current counter register
Offset=0x0008（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer value	R	0x0

7.4.6.4 T1_CTL

Timer1 control register
Offset=0x0040（VDD）

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	x
5	EN	Timer Enable 0:Disable, 1:Enable	R/W	0x0
4:3	-	Reserved	R	x
2	RELO	Timer Reload 0:Not reload,1:Reload	R/W	0x0
1	ZIEN	Timer0 Zero IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the irq signal until the pending bit was cleared.	R/W	0x0
0	ZIPD	Timer IRQ Pending, Writing 0 to clear this bit.	R/W	0x0

Note: The timer only can count down.

7.4.6.5 T1_VAL

Timer1 value register
Offset=0x0044（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	VAL	Read or write Timer/Counter value register	W	0x0

7.4.6.6 T1_CNT

Timer1 current counter register
Offset=0x0048（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer value	R	0x0

7.4.6.7 T2_CTL

Timer2 control register
Offset=0x80（VDD）

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
13	IN_SEL	Counter mode and capture mode signal input source select 0:from Timer_CAP 1:from IR_ANA_OUT	RW	0x0
12	LEVEL	Current input pulse level. Using for counter mode and capture mode The LEVEL value represents the level level corresponding to the previous trigger edge in the current state. That is, the rising edge of the previous trigger, the LEVEL value is read back to 0. The LEVEL value is read back to 1 when the previous trigger edge is on the falling edge	R	0x0
11	DIR	Timer timing /count mode: 0：down 1：up	R/W	0x0
10:9	MODE_SEL	Timer mode select: 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	R/W	0x0
8	CAPTURE_IP	Capture event irq pending Writing 1 to clear this bit. Irq pending include counter mode and capture mode	R/W	0x0
7:6	CAPTURE_SE	Capture signal edge select 00:falling edge 01:rising edge 1x:both falling edge and rising edge Edge select include counter mode and capture mode	R/W	0x0
5	En	Timer Enable 0:Disable 1:Enable	R/W	0x0
4:3	-	Reserved	R	x
2	RELO	Timer Reload enable 0:Not reload 1:Reload	R/W	0x0
1	ZIEN	Timer IRQ Enable In timer/counter mode: When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared. If DIR='0',T2_CNT compare with ZERO If DIR='1',T2_CNT compare with T2_VAL. For more detail reference to timer0/1 block diagram	R/W	0x0

		In input capture mode Every trigger edge would cause a capture irq, which pending reference to CAPTURE_IP		
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit. If occurred a timer overflow or zero, this pending would be set to '1'	R/W	0x0

7.4.6.8 T2_VAL

Timer2 value register
Offset=0x84（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	VAL	Set timer counter value. If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an irq. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero. If timer setting in countdown mode, timer would countdown form Tx_VAL to zero. When the current timer counter equal to zero. it would cause an irq. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL. When in counter mode,Tx_VAL[7:0] was used.	R/W	0x0

7.4.6.9 T2_CNT

Timer2 current counter register
Offset=0x88（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	CNT	Timer current value registers.	R	0x0

7.4.6.10 T2_CAP

Timer3 current counter register
Offset=0x8C（VDD）

Bit(s)	Name	Description	R/W	Reset

31:0	CAP	Capture value register Using in capture mode, when capture irq occurred, read this register to get counter of pulse width counter. If would be reload by every trigger edge set in Tx_CTL.	R	0x0

7.4.6.11 T3_CTL

Timer3 control register
Offset=0xC0（VDD）

Bit(s)	Name	Description	R/W	Reset
31:14	-	Reserved	R	0x0
13	IN_SEL	Counter mode and capture mode signal input source select 0:from Timer_CAP 1:from IR_ANA_OUT	RW	0x0
12	LEVEL	Current input pulse level. Using for counter mode and capture mode The LEVEL value represents the level level corresponding to the previous trigger edge in the current state. That is, the rising edge of the previous trigger, the LEVEL value is read back to 0. The LEVEL value is read back to 1 when the previous trigger edge is on the falling edge	R	0x0
11	DIR	Timer timing /count mode: 0：down 1：up	R/W	0x0
10:9	MODE_SEL	Timer mode select: 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	R/W	0x0
8	CAPTURE_IP	Input Capture mode event irq pending Writing 1 to clear this bit.	R/W	0x0
7:6	CAPTURE_SE	Input Capture mode signal edge select 00:falling edge 01:rising edge 1x:both falling edge and rising edge	R/W	0x0
5	En	Timer Enable 0:Disable 1:Enable	R/W	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable	R/W	0x0

		0:Not reload 1:Reload		
1	ZIEN	Timer IRQ Enable. Include timer mode and input capture mode. In timer mode, When this bit is enabled, Timer_IRQ sent out the irq signal until the pending bit was cleared. If DIR='0',T2_CNT compare with ZERO If DIR='1',T2_CNT compare with T2_VAL. For more detail reference to timer2/3 block diagram In input capture mode, this bit would set be '1'when every trigger edge was found, which was set in CAPTURE_SE	R/W	0x0
0	ZIPD	Timer mode IRQ Pending, Writing 1 to clear this bit.	R/W	0x0

7.4.6.12 T3_VAL

Timer3 value register
Offset=0xC4（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	VAL	Set timer counter value. If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an irq. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero. If timer setting in countdown mode, timer would countdown form Tx_VAL to zero. When the current timer counter equal to zero. it would cause an irq. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL. When in counter mode,Tx_VAL[7:0] was used.	R/W	0x0

7.4.6.13 T3_CNT

Timer3 current counter register
Offset=0xC8（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	CNT	Timer current value registers.	R	0x0

7.4.6.14 T3_CAP

Timer3 current counter register

Offset=0xCC（VDD）

Bit(s)	Name	Description	R/W	Reset
31:0	CAP	Capture value register Using in capture mode, when capture irq occurred, read this register to get counter of pulse width counter. If would be reload by every trigger edge set in Tx_CTL.	R	0x0

8 DMA

8.1 Overview

- DMA transmission is independent of the CPU.
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory.
- Support byte enable transmit
- Not support Non aligned data access
- 4-channel ordinary DMA, all device support single transmit mode. Only one of the 4 DMA channels can transfer data at the same time.
- The Priority DMA0>DMA1>DMA2>DMA3
- 4 channel only send one interrupts to the CPU on completion of certain operational events as following:
  - DMA0TCIP
  - DMA1TCIP
  - DMA2TCIP
  - DMA3TCIP
  - DMA3HFIP
  - DMA2HFIP
  - DMA1HFIP
  - DMA0HFIP

8.2 DMA DRQ source

Table 8-1 DMA drq source table

DRQ number	DRQ source
Drq_0	Memory
Drq_1	SPI0_RX FIFO
Drq_2	SPI0_TX FIFO
Drq_3	SPI1_RX FIFO
Drq_4	SPI1_TX FIFO
Drq_5	SPI2_RX FIFO
Drq_6	SPI2_TX FIFO
Drq_7	UART0_RX FIFO
Drq_8	UART0_TX FIFO
Drq_9	UART1_RX FIFO
Drq_10	UART1_TX FIFO
Drq_11	UART2_RX FIFO
Drq_12	UART2_TX FIFO
Drq_13	TWI0_RX FIFO
Drq_14	TWI0_TX FIFO
Drq_15	TWI1_RX FIFO

Drq_16	TWI1_TX FIFO
Drq_17	I2SADC_RX FIFO
Drq_18	I2S_TX FIFO
Drq_19	PWM_TX FIFO

8.3 Register list

DMA base address

Name	Physical Base Address	KSEG1 Base Address
DMACONTROLLER	0x4000a000	0x4000a000

DMA controller register list

Offset	Register Name	Description
0x0000	DMAIP	DMA Interrupt Pending Register
0x0004	DMAIE	DMA Interrupt Enable Register
0x0100	DMA0CTL	DMA0 control Register
0x0104	DMA0START	DMA0 Start Register
0x0108	DMA0SADDR	DMA0 Source Address Register
0x010c	DMA0DADDR	DMA0 Destination Address Register
0x0110	DMA0FrameLen	DMA0 Frame Length Register
0x0114	DMA0RemainCounter	DMA0 Remain Counter Register
0x0200	DMA1CTL	DMA1 control Register
0x0204	DMA1START	DMA1 Start Register
0x0208	DMA1SADDR	DMA1 Source Address Register
0x020c	DMA1DADDR	DMA1 Destination Address Register
0x0210	DMA1FrameLen	DMA1 Frame Length Register
0x0214	DMA1RemainCounter	DMA1 Remain Counter Register
0x0300	DMA2CTL	DMA2 control Register
0x0304	DMA2START	DMA2 Start Register
0x0308	DMA2SADDR	DMA2 Source Address Register
0x030c	DMA2DADDR	DMA2 Destination Address Register
0x0310	DMA2FrameLen	DMA2 Frame Length Register
0x0314	DMA2RemainCounter	DMA2 Remain Counter Register
0x0400	DMA3CTL	DMA3 control Register
0x0404	DMA3START	DMA3 Start Register
0x0408	DMA3SADDR	DMA3 Source Address Register
0x040c	DMA3DADDR	DMA3 Destination Address Register
0x0410	DMA3FrameLen	DMA3 Frame Length Register
0x0414	DMA3RemainCounter	DMA3 Remain Counter Register

8.4 Register Description

8.4.1 DMAIP

DMA Interrupt Pending Register

Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0x0
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear.	RW	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear.	RW	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear.	RW	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear.	RW	0x0
7:4	-	Reserved	R	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0

8.4.2 DMAIE

DMA Interrupt Enable Register

Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	-	0x0
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0

8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
7:4	-	Reserved	-	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	RW	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	RW	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	RW	0x0

8.4.3 DMA0CTL

DMA0 control Register

Offset = 0x0100

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	-	0x0
20:16	DRQW	DRQ signal wait cycle select 0: wait 1 cycle 1: wait 2 cycle … 31: wait 32 cycle	RW	0x0
15	reload	Reload the DMA0 controller registers and start DMA0 transmission after current DMA0 transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
14:13	TWS	Transmit data width select 0: 32bit 1:16bit 2:8bit 3: Reserved	RW	0x0
12	DAM0	Destination address mode 0: increment 1: constant	RW	0x0
11:8	DSTSL0	Destination select: 4'b0000: memory	RW	0x0

		4'b0001: SPI0 TX FIFO 4'b0010: SPI1 TX FIFO 4'b0011: SPI2 TX FIFO 4'b0100: UART0 TX FIFO 4'b0101: UART1 TX FIFO 4'b0110: UART2 TX FIFO 4'b0111: TWI0 TX FIFO 4'b1000: TWI1 TX FIFO 4'b1001: I2S TX FIFO 4'b1010: PWM TX FIFO 4'b1011~:others reserved		
7:5	-	Reserved	-	0x0
4	SAM0	Source address mode 0: increment 1: constant	RW	0x0
3:0	SRCSL0	Source Select: 4'b0000: memory 4'b0001: SPI0 RX FIFO 4'b0010: SPI1 RX FIFO 4'b0011: SPI2 RX FIFO 4'b0100: UART0 RX FIFO 4'b0101: UART1 RX FIFO 4'b0110: UART2 RX FIFO 4'b0111: TWI0 RX FIFO 4'b1000: TWI1 RX FIFO 4'b1001: I2S RX/ADCFIFO 4'b1010~: others reserved	RW	0x0

8.4.4 DMA0START

DMA0 Start Register

Offset = 0x0104

Bit(s)	Name	Description	R/W	Reset
31:1	-	Reserved	R	x
0	DMA0START	DMA0 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

8.4.5 DMA0SADDR

DMA0 Source Address Register

Offset = 0x0108

Bit(s)	Name	Description	R/W	Reset
31:0	DMA0SADDR	The source address [31:0] of DMA0 transmission.	RW	0x0

8.4.6 DMA0DADDR

DMA0 Destination Address Register

Offset = 0x010c

Bit(s)	Name	Description	R/W	Reset
31:0	DMA0DADDR	The destination address [31:0] of DMA0 transmission.	RW	0x0

8.4.7 DMA0FrameLen

DMA0 Frame Length Register

Offset = 0x0110

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA0FrameLen	The frame length of DMA0 transmission（Byte）.	RW	0x0

8.4.8 DMA0RemainCounter

DMA0 Remain Counter Register

Offset = 0x0114

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA0RemainCounterH	The Remain Counter of DMA0 transmission.	R	0x0

8.4.9 DMA1CTL

DMA1 control Register

Offset = 0x0200

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	-	0x0
20:16	DRQW	DRQ signal wait cycle select 0: wait 1 cycle 1: wait 2 cycle … 31: wait 32 cycle	RW	0x0
15	reload	Reload the DMA1 controller registers and start DMA0 transmission after current DMA1 transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
14:13	TWS	Transmit data width select 0: 32bit 1:16bit 2:8bit 3: Reserved	RW	0x0
12	DAM1	Destination address mode 0: increment 1: constant	RW	0x0
11:8	DSTSL1	Destination select: 4'b0000: memory 4'b0001: SPI0 TX FIFO 4'b0010: SPI1 TX FIFO 4'b0011: SPI2 TX FIFO 4'b0100: UART0 TX FIFO 4'b0101: UART1 TX FIFO 4'b0110: UART2 TX FIFO 4'b0111: TWI0 TX FIFO 4'b1000: TWI1 TX FIFO 4'b1001: I2S TX FIFO 4'b1010: PWM TX FIFO 4'b1011~:others reserved	RW	0x0
7:5	-	Reserved	-	0x0
4	SAM1	Source address mode 0: increment 1: constant	RW	0x0
3:0	SRCSL1	Source Select: 4'b0000: memory 4'b0001: SPI0 RX FIFO 4'b0010: SPI1 RX FIFO 4'b0011: SPI2 RX FIFO 4'b0100: UART0 RX FIFO	RW	0x0

		4'b0101: UART1 RX FIFO 4'b0110: UART2 RX FIFO 4'b0111: TWI0 RX FIFO 4'b1000: TWI1 RX FIFO 4'b1001: I2S RX/ADCFIFO 4'b1010~: others reserved		

8.4.10 DMA1START

DMA1 Start Register

Offset = 0x0204

Bit(s)	Name	Description	R/W	Reset
31:1	-	Reserved	R	x
0	DMA1START	DMA1 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMA1 controller if the DMA1 transmission is complete or DMA1 transmission error occurs. This bit can be written '0' to abort DMA1 transmission.	RW	0x0

8.4.11 DMA1SADDR

DMA1 Source Address Register

Offset = 0x0208

Bit(s)	Name	Description	R/W	Reset
31:0	DMA1SADDR	The source address [31:0] of DMA1 transmission.	RW	0x0

8.4.12 DMA1DADDR

DMA1 Destination Address Register

Offset = 0x020c

Bit(s)	Name	Description	R/W	Reset
31:0	DMA1DADDR	The destination address [31:0] of DMA1 transmission.	RW	0x0

8.4.13 DMA1FrameLen

DMA1 Frame Length Register

Offset = 0x0210

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA1FrameLen	The frame length of DMA1 transmission（Byte）.	RW	0x0

8.4.14 DMA1RemainCounter

DMA1 Remain Counter Register

Offset = 0x0214

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA1RemainCounter	The Remain Counter of DMA1 transmission.	R	0x0

8.4.15 DMA2CTL

DMA2 control Register

Offset = 0x0300

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	x
20:16	DRQW	DRQ signal wait cycle select 0: wait 1 cycle 1: wait 2 cycle … 31: wait 32 cycle	RW	0x0
15	reload	Reload the DMA2 controller registers and start DMA2 transmission after current DMA2 transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
14:13	TWS	Transmit data width select	RW	0x0

		0: 32bit 1: 16bit 2: 8bit 3: Reserved		
12	DAM2	Destination address mode 0: increment 1: constant	RW	0x0
11:8	DSTSL2	Destination select: 4'b0000: memory 4'b0001: SPI0 TX FIFO 4'b0010: SPI1 TX FIFO 4'b0011: SPI2 TX FIFO 4'b0100: UART0 TX FIFO 4'b0101: UART1 TX FIFO 4'b0110: UART2 TX FIFO 4'b0111: TWI0 TX FIFO 4'b1000: TWI1 TX FIFO 4'b1001: I2S TX FIFO 4'b1010: PWM TX FIFO 4'b1011~:others reserved	RW	0x0
7:5	-	Reserved	R	x
4	SAM2	Source address mode 0: increment 1: constant	RW	0x0
3:0	SRCSL2	Source Select: 4'b0000: memory 4'b0001: SPI0 RX FIFO 4'b0010: SPI1 RX FIFO 4'b0011: SPI2 RX FIFO 4'b0100: UART0 RX FIFO 4'b0101: UART1 RX FIFO 4'b0110: UART2 RX FIFO 4'b0111: TWI0 RX FIFO 4'b1000: TWI1 RX FIFO 4'b1001: I2S RX/ADCFIFO 4'b1010~: others reserved	RW	0x0

8.4.16 DMA2START

DMA2 Start Register

Offset = 0x0304

Bit(s)	Name	Description	R/W	Reset

31:1	-	Reserved	R	x
0	DMA2START	DMA2 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMA2 controller if the DMA2 transmission is complete or DMA2 transmission error occurs. This bit can be written '0' to abort DMA2 transmission.	RW	0x0

8.4.17 DMA2SADDR

DMA2 Source Address Register

Offset = 0x0308

Bit(s)	Name	Description	R/W	Reset
31:0	DMA2SADDR	The source address [31:0] of DMA2 transmission.	RW	0x0

8.4.18 DMA2DADDR

DMA2 Destination Address Register

Offset = 0x030c

Bit(s)	Name	Description	R/W	Reset
31:0	DMA2DADDR	The destination address [31:0] of DMA2 transmission.	RW	0x0

8.4.19 DMA2FrameLen

DMA2 Frame Length Register

Offset = 0x0310

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA2FrameLen	The frame length of DMA2 transmission（Byte）.	RW	0x0

8.4.20 DMA2RemainCounter

DMA2 Remain Counter Register

Offset = 0x0314

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA2RemainCounter	The Remain Counter of DMA2 transmission.	R	0x0

8.4.21 DMA3CTL

DMA3 control Register

Offset = 0x0400

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	x
20:16	DRQW	DRQ signal wait cycle select 0: wait 1 cycle 1: wait 2 cycle … 31: wait 32 cycle	RW	0x0
15	reload	Reload the DMA3 controller registers and start DMA3 transmission after current DMA3 transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
14:13	TWS	Transmit data width select 0: 32bit 1: 16bit 2: 8bit 3: Reserved	RW	0x0
12	DAM3	Destination address mode 0: increment 1: constant	RW	0x0
11:8	DSTSL3	Destination select: 4'b0000: memory 4'b0001: SPI0 TX FIFO 4'b0010: SPI1 TX FIFO 4'b0011: SPI2 TX FIFO 4'b0100: UART0 TX FIFO 4'b0101: UART1 TX FIFO	RW	0x0

		4'b0110: UART2 TX FIFO 4'b0111: TWI0 TX FIFO 4'b1000: TWI1 TX FIFO 4'b1001: I2S TX FIFO 4'b1010: PWM TX FIFO 4'b1011~:others reserved		
7:5	-	Reserved	R	x
4	SAM3	Source address mode 0: increment 1: constant	RW	0x0
3:0	SRCSL3	Source Select: 4'b0000: memory 4'b0001: SPI0 RX FIFO 4'b0010: SPI1 RX FIFO 4'b0011: SPI2 RX FIFO 4'b0100: UART0 RX FIFO 4'b0101: UART1 RX FIFO 4'b0110: UART2 RX FIFO 4'b0111: TWI0 RX FIFO 4'b1000: TWI1 RX FIFO 4'b1001: I2S RX/ADCFIFO 4'b1010~: others reserved	RW	0x0

8.4.22 DMA3START

DMA3 Start Register

Offset = 0x0404

Bit(s)	Name	Description	R/W	Reset
31:1	-	Reserved	R	x
0	DMA3START	DMA3 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMA3 controller if the DMA3 transmission is complete or DMA3 transmission error occurs. This bit can be written '0' to abort DMA3 transmission.	RW	0x0

8.4.23 DMA3SADDR

DMA3 Source Address Register

Offset = 0x0408

Bit(s)	Name	Description	R/W	Reset
31:0	DMA3SADDR	The source address [31:0] of DMA3 transmission.	RW	0x0

8.4.24 DMA3DADDR

DMA3 Destination Address Register

Offset = 0x040c

Bit(s)	Name	Description	R/W	Reset
31:0	DMA3DADDR	The destination address [31:0] of DMA3 transmission.	RW	0x0

8.4.25 DMA3FrameLen

DMA3 Frame Length Register

Offset = 0x0410

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA3FrameLen	The frame length of DMA3 transmission（Byte）.	RW	0x0

8.4.26 DMA3RemainCounter

DMA3 Remain Counter Register

Offset = 0x0414

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	DMA3RemainCounter	The Remain Counter of DMA3 transmission.	R	0x0

9 Transfer and Communication

9.1 UART

9.1.1 Overview

ATB110X Platform contains three UART interfaces: UART0, UART1 and UART2. ALL UART has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- Capable of speeds of 115200*nbps，1Mbps ,2Mbps,4Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ mode to transmit data
- RX BaudRate tolerance≤±2%
- Only UART0 support upgrade firmware

9.1.2 Function Description

UART（Universal Asynchronous Receiver/Transmitter）is usually an individual (or part of an)integrated circuit used for serial communications over a computer or peripheral device serial port. UART are now commonly included in microcontrollers.

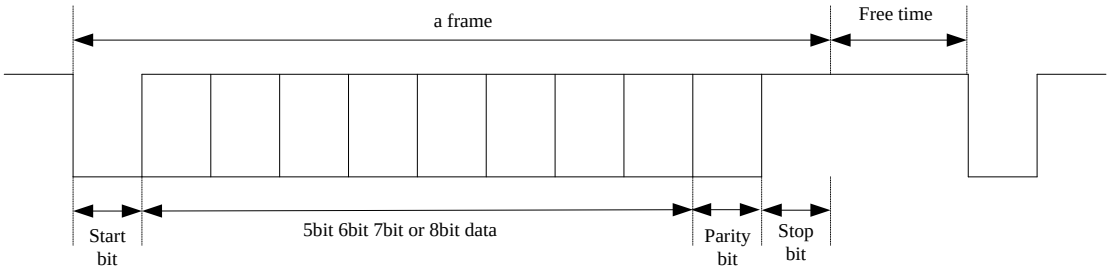


Figure 9-1 Uart timing

The UART0 Baud Rate must be selected by setting the UART0_CTL1.

UART0BauRate=8M/UART0x_BR。The default boudrate of UART0 is 115200 Bps。

Special Note:

When receive data by IRQ mode, if the FIFO number received not meets the trigger level, wait until the time is out of the trigger level data bytes.

9.1.3 Operation Manual

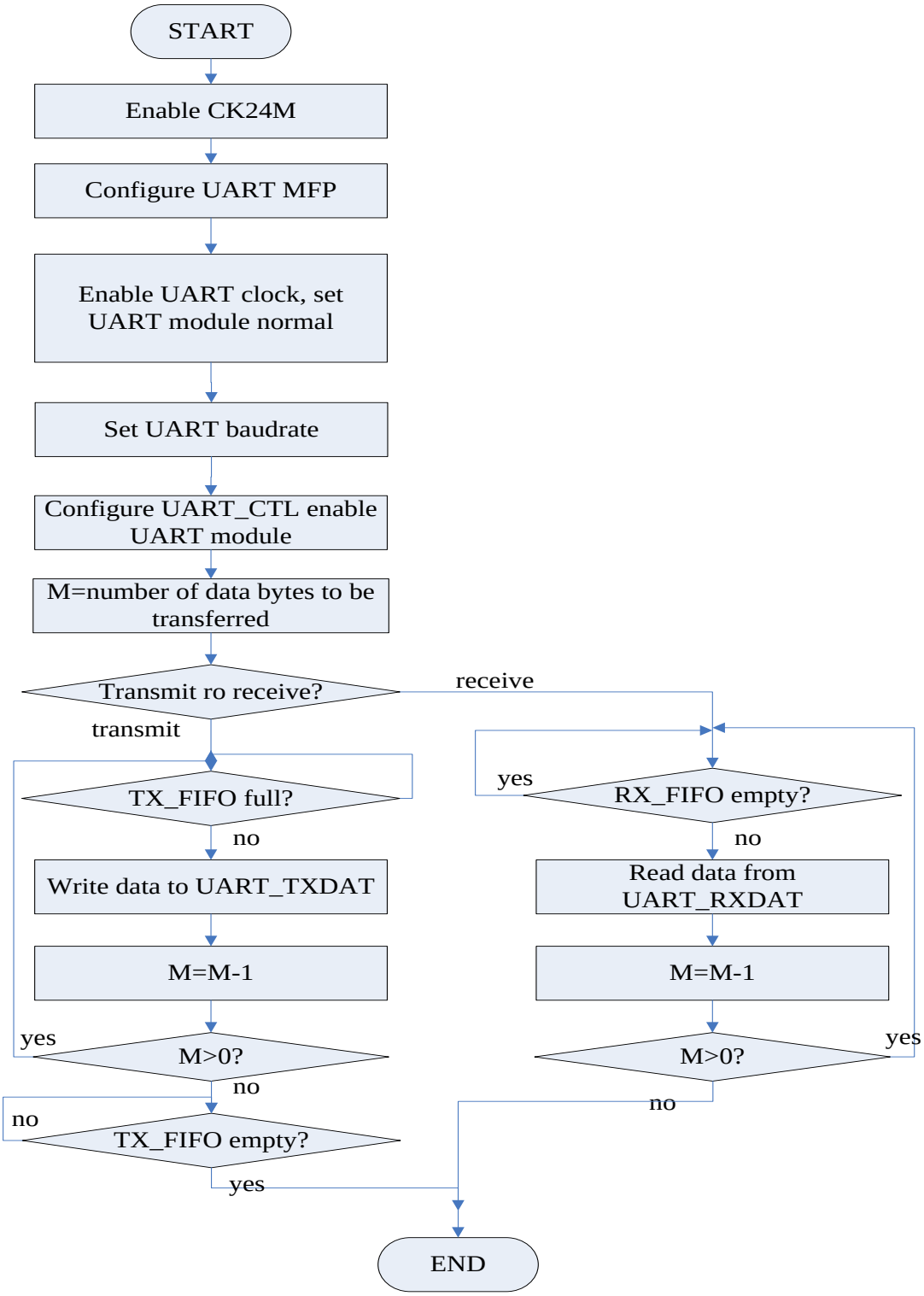


Figure 9-2 UART1 operation flow

9.1.4 Register List

UART Registers Block Base Address

Name	Physical Base Address
UART0	0x4000D000
UART1	0x4000E000
UART2	0x4000F000

UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register
0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register
0x000C	UARTx_STA	UART Status Register
0x0010	UARTx_BR	UART BAUDRATE divider Register

9.1.5 Register Description

9.1.5.1 UARTx_CTL

UARTx Control Register

Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31	RXENABLE	UART RX disable 1：normal 0：disable	R/W	0x0
30	TXENABLE	UART TX disable 1：normal 0：disable	R/W	0x0
29:24	-	-	-	0x0
23	TX_FIFO_EN	UART TX FIFO enable: 0: Disable 1: Enable	R/W	0x0
22	RX_FIFO_EN	UART RX FIFO enable: 0: Disable 1: Enable	R/W	0x0
21:10	-	Reserved	RW	0x0
19	TXIE	UART TX IRQ Enable. 0: Disable 1: Enable	R/W	0x0

18	RXIE	UART RX IRQ Enable. 0: Disable 1: Enable	R/W	0x0
17	TXDE	UART TX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
16	RXDE	UART RX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
15	EN	UART Enable. 0:disable 1: enable	R/W	0x0
14	-	Reserved	R/W	0x0
13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: request to send data 1: no request	R/W	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	R/W	0x0
11:10	RDIC	UART RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00,01 because at lease 8 bytes necessary.	R/W	0x0
9:8	TDIC	UART TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00,01 because at lease 8 bytes necessary.	R/W	0x0
7	CTSE	CTS Enable. If this bit is 1, the transmitter checks CTS- before sending the next data byte. Note: This bit has no effect if Autoflow enable bit is set. 0: do not checks CTS- before sending	R/W	0x0

		1: checks CTS- before sending		
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	R/W	0x0
3	WUEN	Wake up enable 0：disable 1：enable UART0 used only.	RW	0x0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0：1 stop bit 1：2 stop bit	R/W	0x0
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	R/W	0x0

9.1.5.2 UARTx_RXDAT

UART Receive FIFO Data Register

Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	x

9.1.5.3 UARTx_TXDAT

UART Transmit FIFO Data Register

Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TXDAT	Transmited Data. The depth of FIFO is 8 bit × 16 levels	W	0x0

9.1.5.4 UARTx_STA

UART Status Register

Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	x
24	WSTA	UART0 wake up status bit 0: sleep 1: wake up UART0 used only.	R	0x0
23	PAER	Parity Status. 0: Parity OK 1: Parity error. Writing 1 to the bit will clear the bit. When parity error.	R/W	0x0
22	STER	Stop Status. 0: Stop OK 1: Stop error. Writing 1 to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0x0
20:16	TXFL	TX FIFO Level. The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0x0
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	0x1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0x0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	0x0
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0x0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	0x1

4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit. When clock error.	R/W	0x0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	R/W	0x0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	R/W	0x0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	R/W	0x1
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	R/W	0x0

9.1.5.5 UARTx_BR

UART BAUDRATE divider register

Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:28	-	Reserved	R	0x0
27:16	TXBRDIV	UART TX BAUDRATE divider BaudRate= Colck_source/BaudRate diveder	RW	0x028
15:12	-	Reserved	R	0x0
11:0	RXBRDIV	UART RX BAUDRATE divider BaudRate= Colck_source/BaudRate diveder	RW	0x028

9.2 TWI

9.2.1 Overview

- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Both master and slave supports DMA mode
- Only 7-bit address mode support
- Internal Pull-Up Resistor (15k) optional
- Two TWI modules
- 8 Bit x8 TX FIFO and 8Bit x8 RX FIFO
- Pull-up resistors are required on both of the TWI signal lines as the TWI drivers are open drain typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal pull-Up resistor in standard and fast mode.

9.2.2 Function Description

An Inter-IC bus，used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI.

TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

9.2.2.1 Timing Parameter

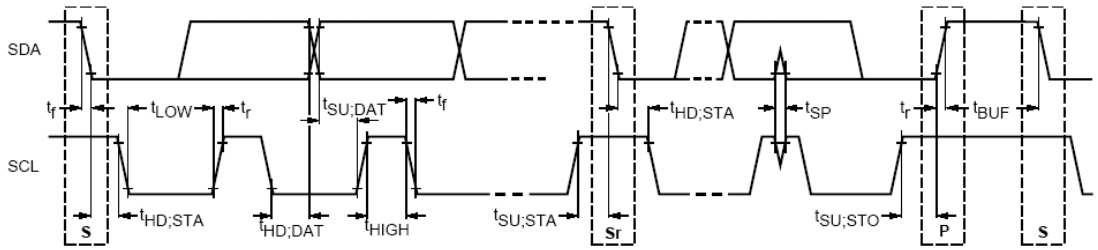


Figure 9-3 TWI Timing

Table 9-1 TWI Timing

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	

SCL clock frequency	fSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	4.0	–	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	–	1.3	–	us
HIGH period of the SCL clock	tHIGH	4.0	–	0.6	–	us
Set-up time for a repeated START condition	tSU;STA	4.7	–	0.6	–	us
Data set-up time	tSU;DAT	250	-	100	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20	300	ns
Set-up time for STOP condition	tSU;STO	4.0	–	0.6	–	us
Bus free time between a STOP and START condition	tBUF	4.7	–	1.3	–	us
Capacitive load for each bus line	Cb	–	400	–	400	pF

Reference TWI_Bus_Spec3 (THE TWI-BUS SPECIFICATION VERSION2.1 JANUARY 2000).

9.2.2.2 Software control process

Write 8Bytes data to the 0x10 address of AT24C02 EEPROM, and its data stream is as follows：

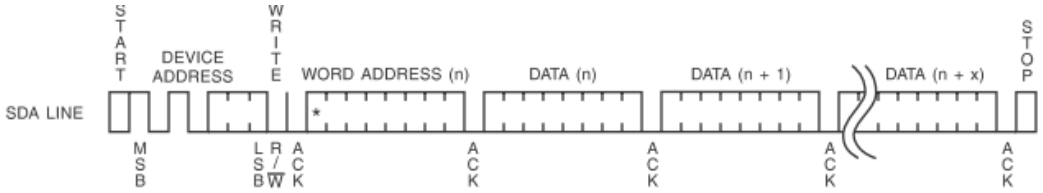


Figure 9- 4 TWI write data

The command process writes 8Bytes data for S+A+Reg1+D+P access time (refer to TWIx_CMD register instructions).

1, TWIx_DATCNT is configured to be 8.

2, write the address of the slave device to 1Byte from TWIx_TxDAT, and the internal Memory address of 1Byte from the device, so TWIx_CMD [3:1] chooses the address of 2Bytes.

3, continue to write to TWIx_TxDAT data sent to 8Bytes, TWIx_CMD[8] enable

4, the data value of the configuration of the CMD register is: 0x8D05

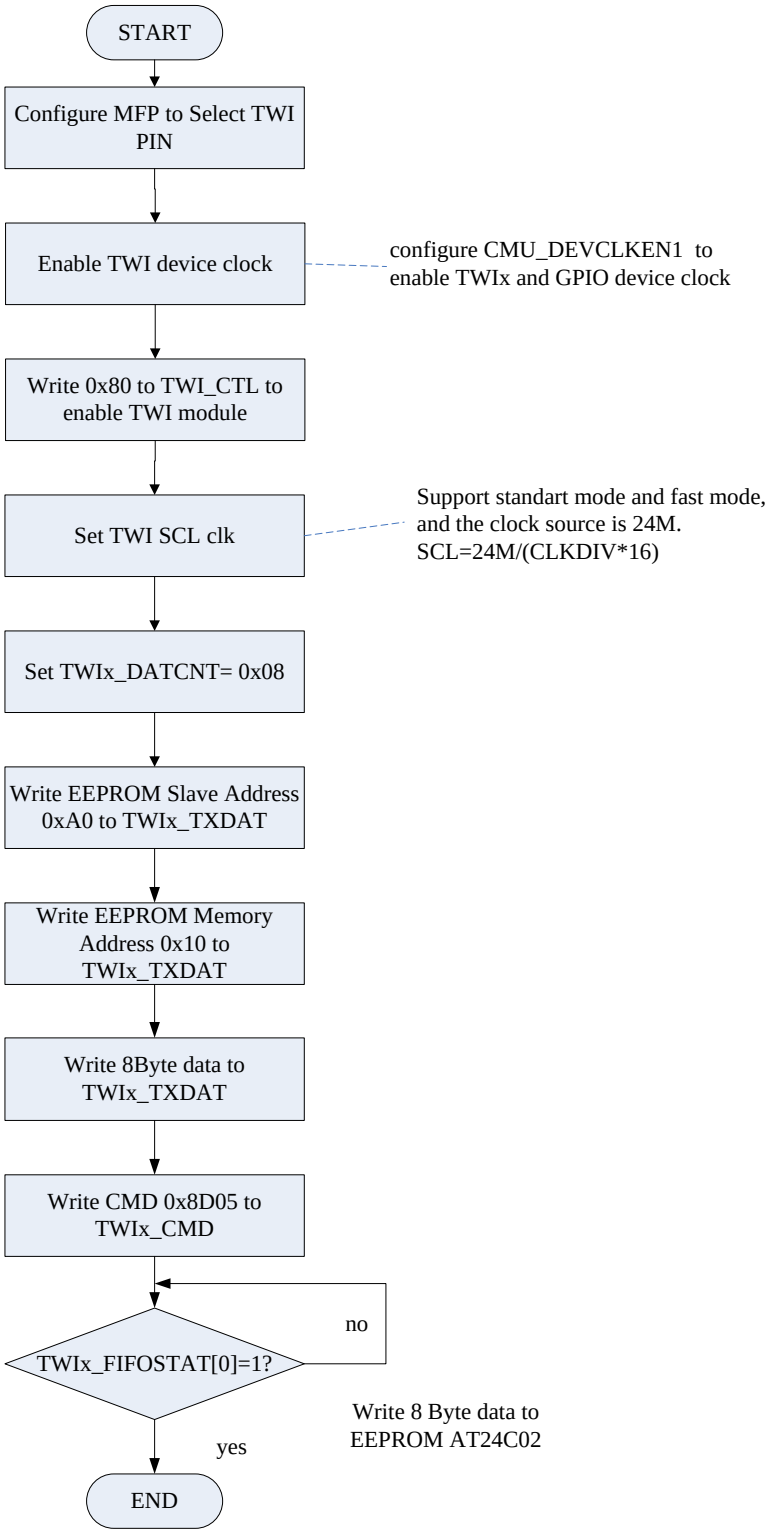


Figure 9-5 write 8Bytes data to EEPROM flow

Read 8Bytes data from the 0x10 address of AT24C02 EEPROM, and its data stream is as follows：

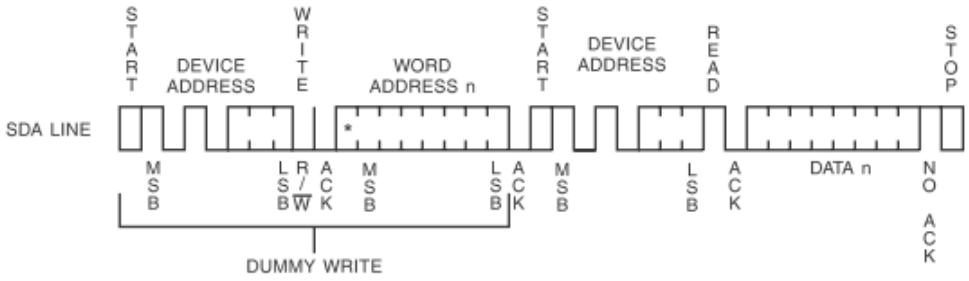


Figure 9-6 TWI read data

The command process reads 10Bytes data for S+A+ Reg1 +RS+Ar+D+P access sequence.

1, TWIx_CNT is configured to be 10.

2. Write the slave device address to TWIx_TxDAT, the internal Memory address of 1Byte from 1Byte.

3. Write the 1Byte from the device address.

4, the value of configuring the CMD register is: 0x8F35,

Then it is the data that reads back from the TWIx_RxDAT from the 10Bytes.

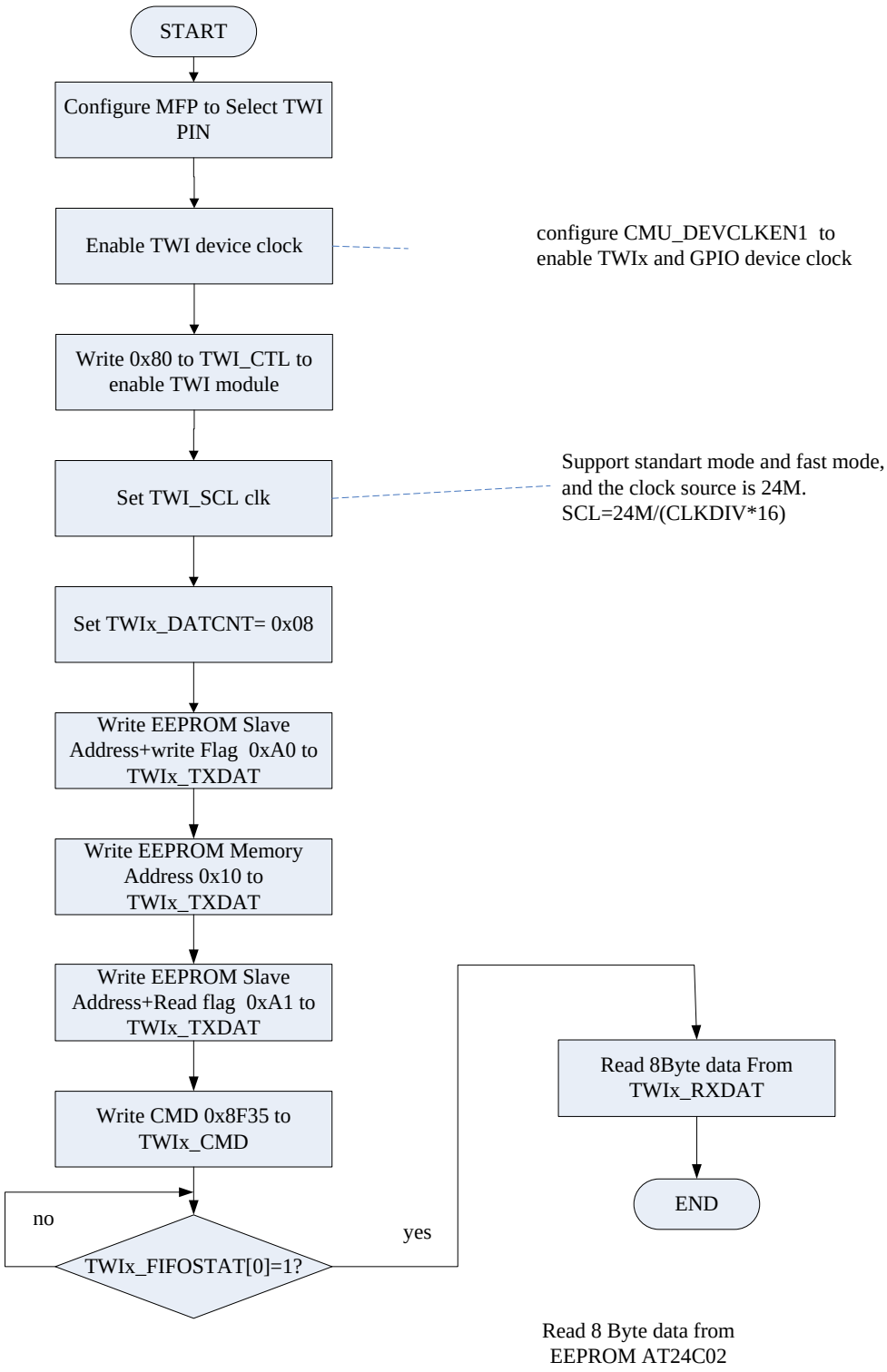


Figure 9-7 read 8Bytes data from EEPROM flow

9.2.3 Register List

TWI Controller Registers Address

Name	Physical Base Address
TWI0	0x4000B000
TWI1	0x4000C000

TWI module Controller Registers

Offset	Register Name	Description
0x0000	TWIx_CTL	TWI Control Register
0x0004	TWIx_CLKDIV	TWI Clock Divide Register
0x0008	TWIx_STAT	TWI Status Register
0x000c	TWIx_ADDR	TWI Address Register
0x0010	TWIx_TXDAT	TWI TX Data Register
0x0014	TWIx_RXDAT	TWI RX Data Register
0x0018	TWIx_CMD	TWI Command Register
0x001c	TWIx_FIFOCTL	TWI FIFO control Register
0x0020	TWIx_FIFOSTAT	TWI FIFO status Register
0x0024	TWIx_DATCNT	TWI Data transmit counter
0x0028	TWIx_RCNT	TWI Data transmit remain counter

9.2.4 Register Description

9.2.4.1 TWIx_CTL

TWI control register.

Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	IRQC	TWI IRQ Control 0: set when RX FIFO received 1 bytes data in IRQ mode 1: set when RX FIFO received 4 bytes data in IRQ mode	RW	0x0
9	DRQTE	TX DRQ enable 0：disable 1：enable	RW	0x0
8	DRQRE	RX DRQ enable 0：disable 1：enable	RW	0x0

7	-	Reserved	R	0x0
6	IRQE	IRQ Enable. 0: Disable 1: Enable	RW	0x0
5	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	RW	0x0
4	-	Reserved	R	0X0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus.	RW	0x0
1	RB	Release Bus. Write 1 to this bit will release the bus.	RW	0x0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0x0

9.2.4.2 TWIx_CLKDIV

TWI Clock Divide Control Register

Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	CLKDIV	Clock Divider Factor (only for master mode). TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=32M/(CLKDIV*16)	RW	0x0

9.2.4.3 TWIx_STAT

TWI Status Register

Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	SRGC	Slave receive general call 0: not receive a general call 1: receive a general call	R	0x0
9	SAMB	Slave address match bit 0: slave address not match 1: slave address match	R	0x0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0x0
7	TCB	Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing 1 to this bit will clear it.	RW	0x0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0x0
5	STAD	Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0x0
4	STPD	Stop detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	RW	0x0
3	-	Reserved	RW	0x0
2	IRQP	IRQ Pending Bit. 1: IRQ 0: No IRQ Set condition: 1. transfer complete 2. detect normal stop bit (no bus error) 3. arbit fail Clear condition: Writing 1 to this bit will clear it.	RW	0x0
1	BEB	Bus error bit 0: No error occur	RW	0x0

		1: Bus error occur Write “1” to clear this bit The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data.		
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived	R	0x0

9.2.4.4 TWIx_ADDR

TWI Address Register

Offset = 0x000C

Bit(s)	Name	Description	R/W	Reset
31：8	-	Reserved	R	0x0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. TWI_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master.	RW	0x0
0	-	Reserved.	R	0x0

9.2.4.5 TWIx_TXDAT

TWI Data Register

Offset = 0x0010

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	DA	The registers of Data or address to be transfer, or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB’s are the slave TWI device address while the LSB is the Read/Write bit. 8 levels FIFO，8 x 8bit	W	0x0

9.2.4.6 TWIx_RXDAT

TWI Data Register

Offset = 0x0014

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	DA	The Receive data Register 8 levels FIFO，8 x 8bit	R	0x0

9.2.4.7 TWIx_CMD

TWI Command Register

Offset = 0x0018

Bit(s)	Name	Description	R/W	Reset
31：16	-	Reserved	R	0x0
15	SECL	Start to execute the command list 0: not execute 1: execute command	RW	0x0
14:13	-	Reserved	R	0x0
12	WRS	Write or Read select 0: write 1: read This bit only used in Slave mode.	RW	0x0
11	MSS	Master or slave mode select 0: slave mode 1: Master mode	RW	0x0
10	SE	Stop enable 0: disable 1: enable	RW	0x0
9	NS	NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data	RW	0x0
8	DE	Data enable 0: disable 1: enable The counts of data transmitted depend on the TWIx_CNT	RW	0x0

		register.		
7:5	SAS	Second address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address	RW	0x0
4	RBE	Restart bit enable 0: not send restart bit 1: send restart bit	RW	0x0
3:1	AS	Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address include slave address and slave internal memory address.	RW	0x0
0	SBE	Start bit enable 0: not send start bit 1: send start bit	RW	0x0

The list of general commands for TWI access sequence is as follows:

Write data of master:

1、 S+A+Reg1+D+P

2、 S+A+ Reg1+ Reg2+D+P

3、 S+A+ Reg1+ D+P

Read data of master:

1、 S+A+ Reg1+RS+Ar+D+P

2、 S+A+ Reg1+ Reg2+RS+Ar+D+P

3、 S+A+ Reg1+P+S+Ar+ D+P

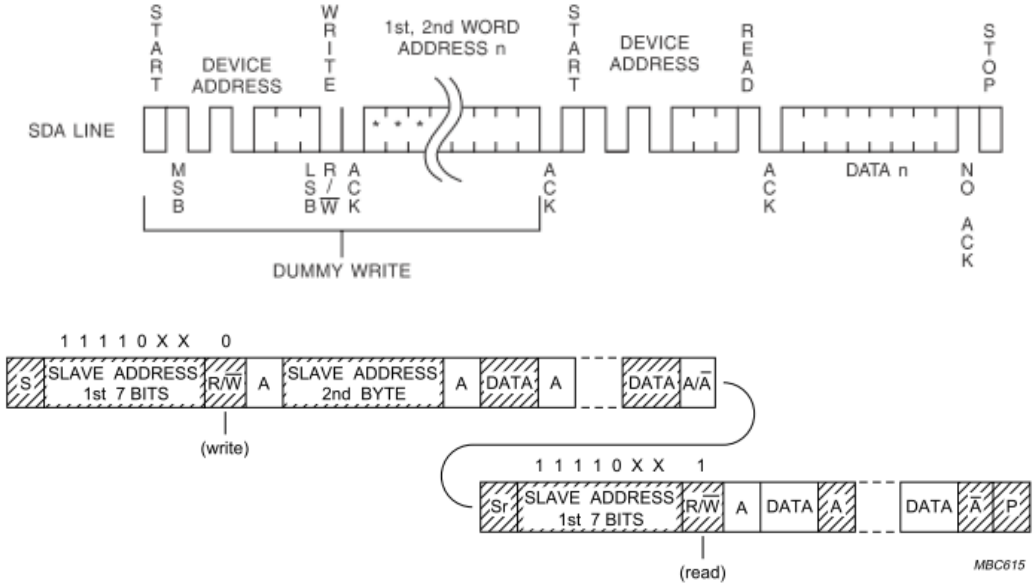
Write data of slave:

1、 D+RL

Read data of slave：

1、 RL+D

Note:S=Start; RS=ReStart; P=Stop; A=Slave address; Ar=Slave address+Read Flag; SAR= Reg; D=data (nByte); RL=Release Bus



9.2.4.8 TWIx_FIFOCTL

TWI FIFO control register

Offset = 0x001C

Bit(s)	Name	Description	R/W	Reset
31:3	-	Reserved	R	0x0
2	TFR	TX FIFO reset bit Write 1 to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	RW	0x0
1	RFR	RX FIFO reset bit Write 1 to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	RW	0x0
0	NIB	NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute，generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	RW	0x0

9.2.4.9 TWIx_FIFOSTAT

TWI FIFO status register

Offset = 0x0020

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:12	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0x0
11:8	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0x0
7	-	Reserved	R	0x0
6	WRS	Write or read status bit when acts as slave， used only in FIFO mode 0: master write to slave 1: master read from slave	R	0x0
5	TFF	TX FIFO full bit 0: not full 1: full	R	0x0
4	TFE	TX FIFO empty bit 0: empty 1: not empty	R	0x0
3	RFF	RX FIFO full bit 0: not full 1: full	R	0x0
2	RFE	RX FIFO empty bit 0: empty 1: not empty	R	0x0
1	RNB	Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data Write 1 to clear this bit	RW	0x0
0	CECB	Command Execute Complete bit 0: not complete 1: complete	R	0x1

9.2.4.10 TWIx_DATCNT

TWI Counter Register

Offset = 0x0024

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Data Transmit counter	RW	0x0

9.2.4.11 TWIx_RCNT

TWI Remain Counter Register

Offset = 0x0028

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Remain counter	R	0x0

9.3 SPI

9.3.1 Overview

SPI0:

- Only support master mode
- Support SPI normal mode: mode 0\3
- Support 3wire mode(1x IO)
- Support 1x IO/2x IO/4x IO/Dual read SNOR
- Support 16 level delay chain(1 ns step)
- Support 16bit CRC
- Support 32bit seed 8bit randomize
- Support IRQ and DMA mode to transmit data
- Support the highest SPI clock frequency up to 96MHz.

SPI1\2:

- Support SPI normal mode: mode 0\1\2\3
- Only support normal 4 wire mode(1x IO)
- Support IRQ and DMA mode to transmit data
- Support the highest SPI clock frequency up to 96MHz.

9.3.2 Function Description

The SPI module is designed according to Motorola serial peripheral interface protocols. It can be configured as either a master or slave device. It can generate a large range of SPI clock so as to communicate with different devices supporting SPI protocols. Especially, this module support three operation mode: write & read, write only, read only mode.

SPI write & read mode use the MOSI pin to serially write instructions, addresses or data to the device. It also uses the MISO pin to read data or status from the device synchronous. This mode is designed to meet normal SPI application.

9.3.2.1 SPI Mode Timing

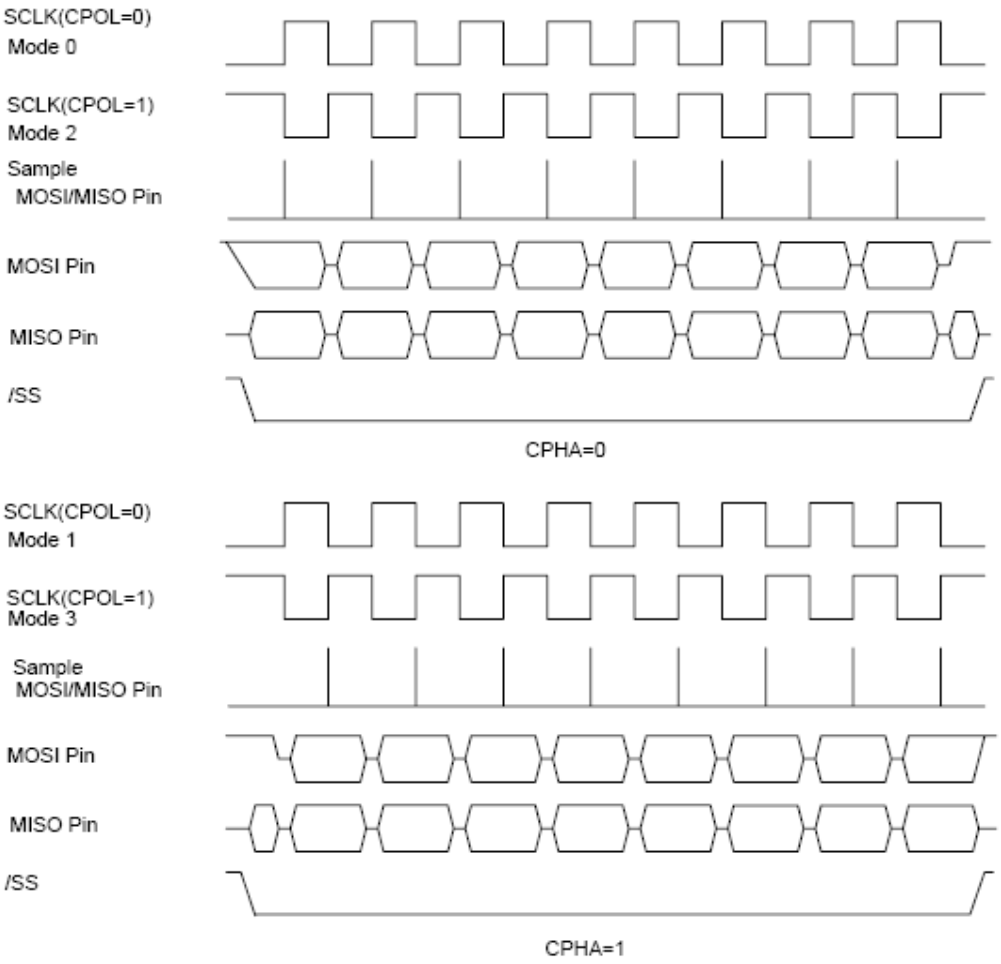


Figure 9-8 SPI mode timing

9.3.2.2 Page Program Timing

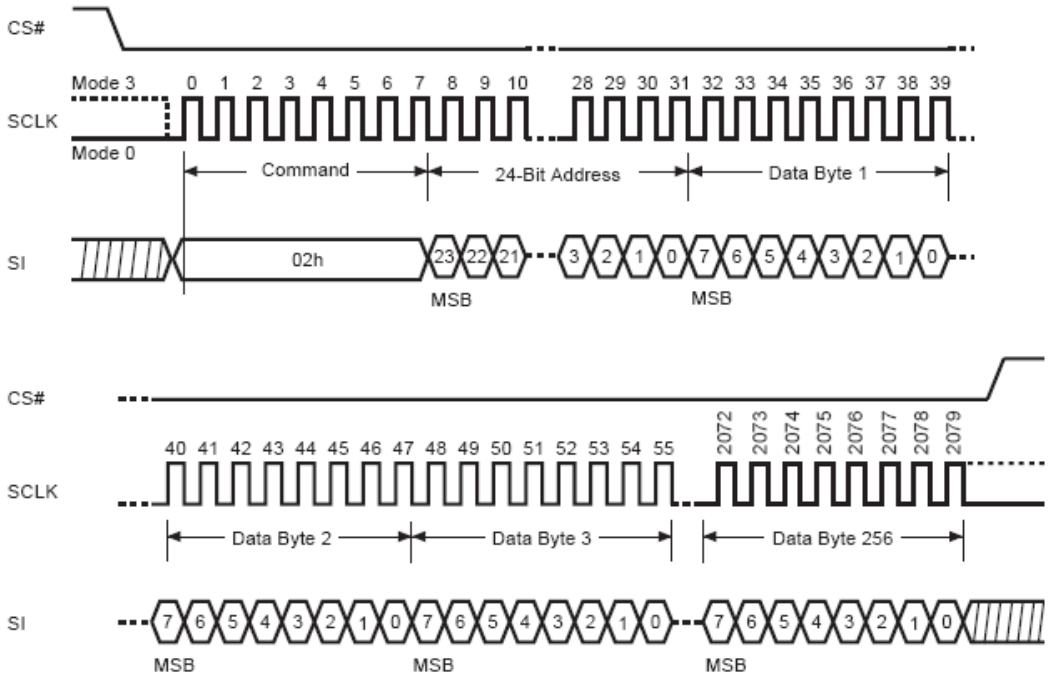


Figure 9-9 SPI page program timing

9.3.2.3 3 Wire Mode

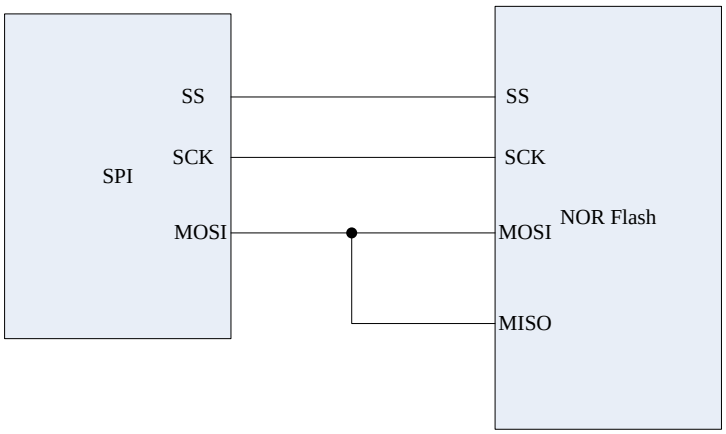


Figure 9-10 3-wires mode

9.3.2.4 Dual Read Timing

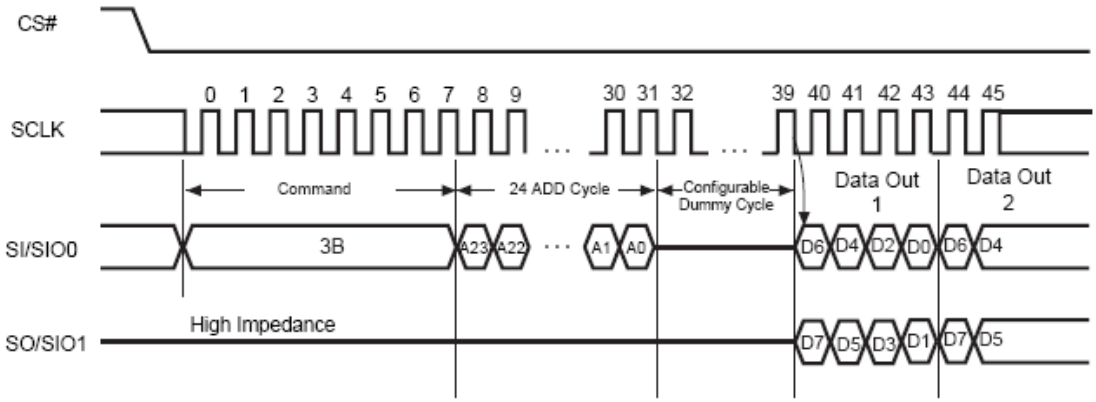


Figure 9-11 SPI dual read timing

9.3.2.5 2x Read Timing

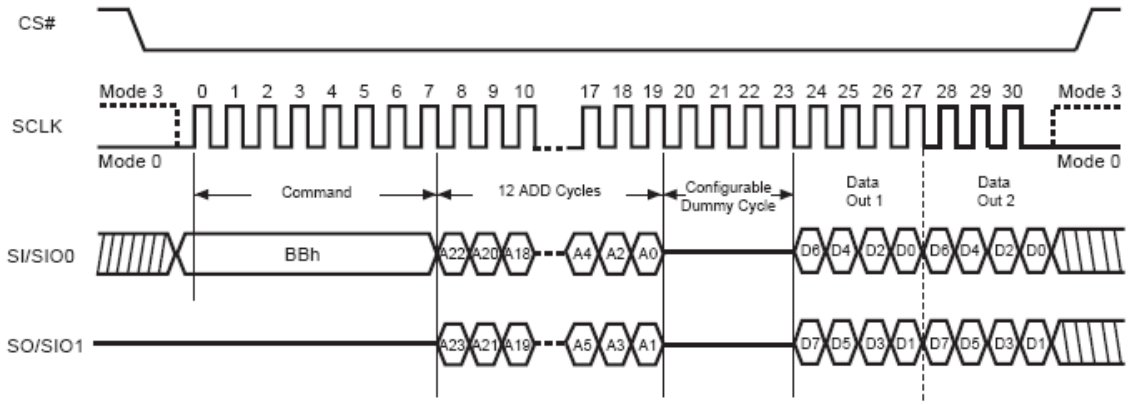


Figure 9-12 SPI 2x read timing

9.3.2.6 Quad Read Timing

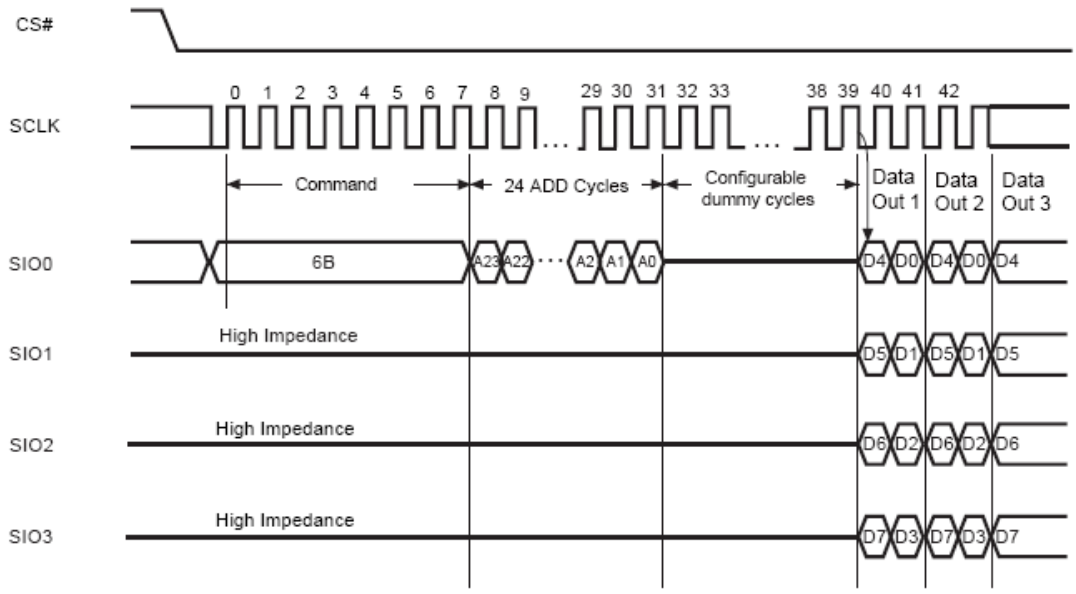


Figure 9-13 Quad Read Timing

9.3.2.7 4x Read Timing

When in 4x mode，spi_mosi is used as spi_io0，and spi_miso is used as spi_io1.
The 4x mode instruction is “EBh”, and there are eight “dummy” clocks after the 24-bit address。

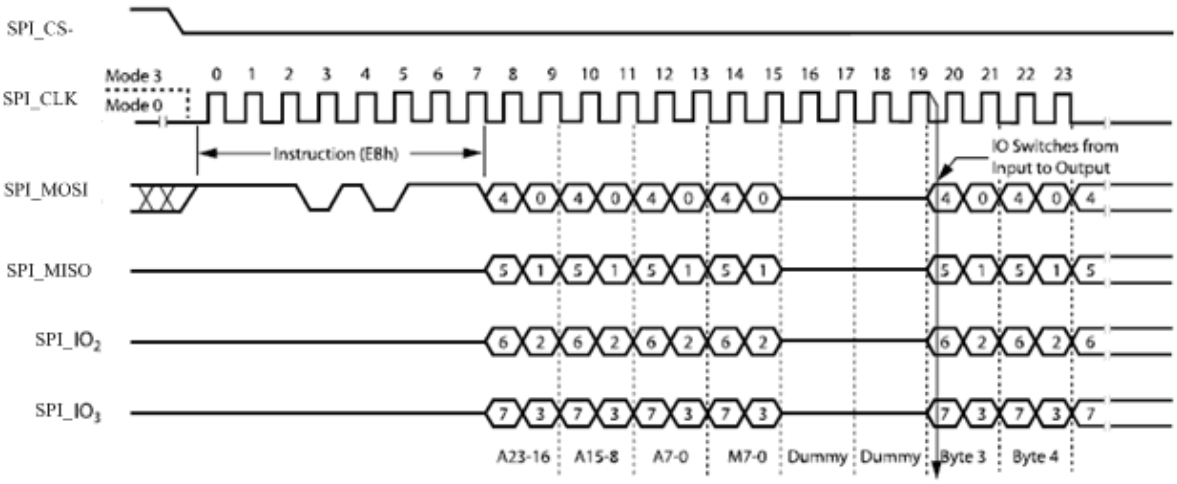


Figure 9-14 SPI 4x Read Timing(1)

The Mode bits (M7-0) equals “A5”hex, so the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown blow. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low.

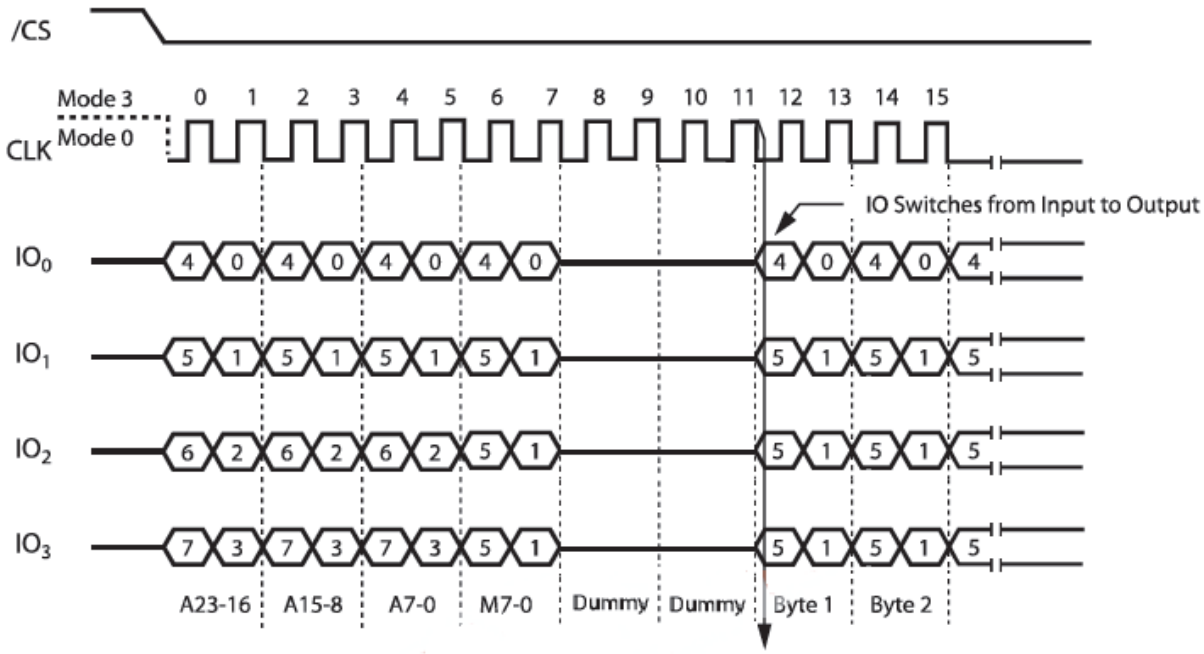


Figure 9-15 SPI 4x Read Timing(2)

9.3.3 Operation Manual

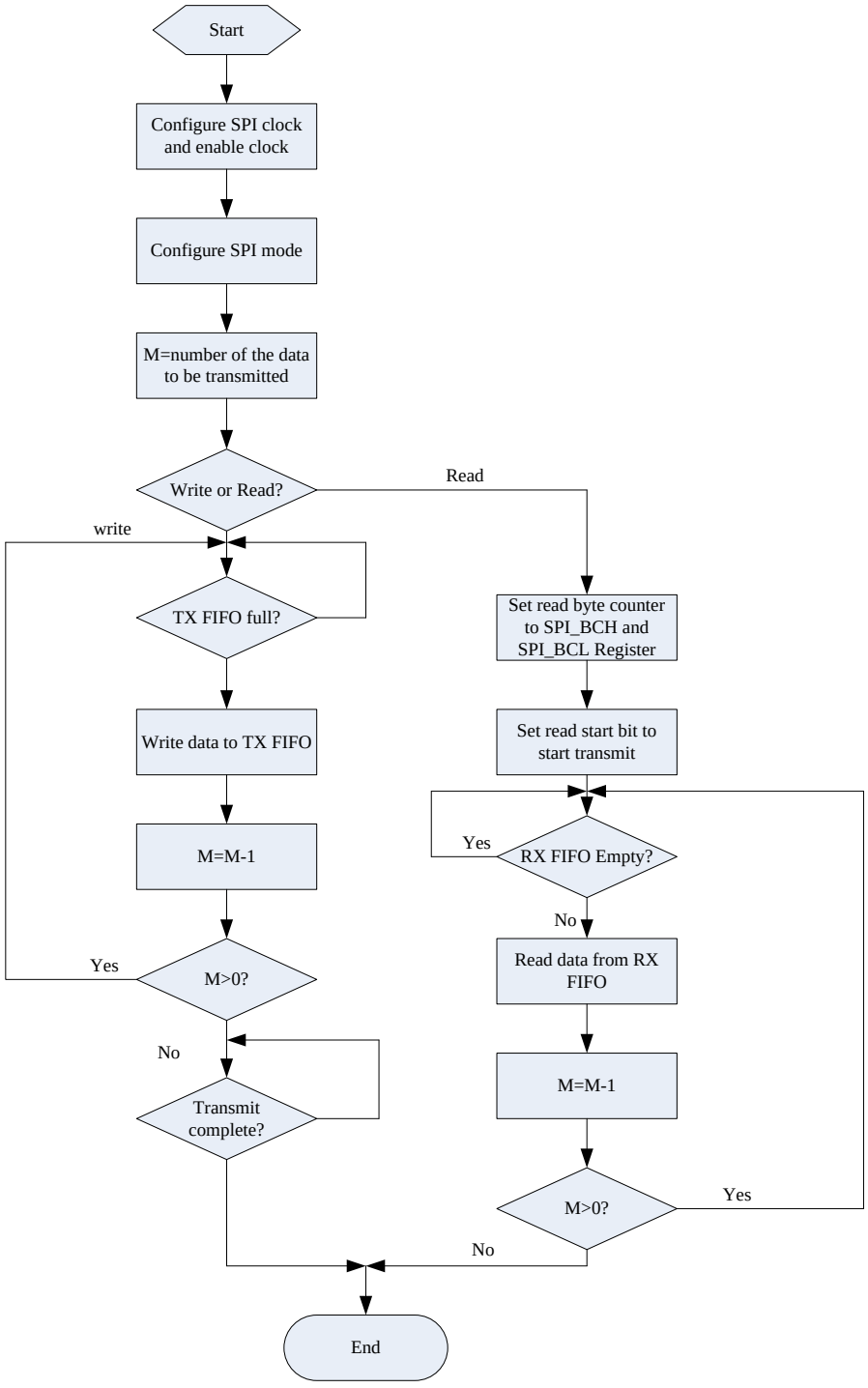


Figure 9-16 SPI operation flow

9.3.4 SPI0 Register List

SPI0 Registers Block Base Address

Name	Physical Base Address
SPI0	0x40011000

SPI0 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI0_CTL	SPI0 Control Register
0x0004	SPI0_STA	SPI0 Status Register
0x0008	SPI0_TXDAT	SPI0 Transmit FIFO Data Register
0x000C	SPI0_RXDAT	SPI0 Receive FIFO Data Register
0x0010	SPI0_BC	SPI0 Byte Counter Register
0x0018	CACHE_ERROR_ADDR	Cache Error address Register
0x001C	NO_CRC_ADDR	NO CRC Start Address

9.3.5 SPI0 Register Description

9.3.5.1 SPI0_CTL

SPI Control Register
Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	SPI_DELAY_HIGH	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) The high bit of DelayChain, configuring DelayChain configuration bits with 5Bit from Bit[19:16], and configuring Delay time to the maximum 31ns..	R/W	0x0
29	NO_CRC_RAND_RXEN	NO CRC Area Rx Randomizer Enable (Cache Interface Only) No CRC area will enable rx randomize function when enable SPI_CTL[12] and this bit simultaneously. 0: Disable 1: Enable	R/W	0x0
28	SPI_MODE_SELECT	SPI Mode Select	R/W	0x0

		0: Mode3 1: Mode0		
27	DUAL_QUAD_SELECT	SPI Dual/Quad Mode Select It works only when SPI_IO_MODE select 2x IO mode or 4x IO mode 0: 2x/4x mode 1: dual/quad mode	R/W	0x0
26	RX_WRITE_SEL	SPI Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0
25:24	TIME_OUT_CTRL	Time Out Control (Cache Interface Only) 00: wait 16 cycles 01: wait 32 cycles 10: wait 64 cycles 11: wait 128 cycles	R/W	0x0
23:22	CRC_ERROR_TIME	CRC Error Times (Cache Interface Only) 00: 2times 01: 4times 10: 8times 11: 16times	R/W	0x0
21	CRC_IRQ_EN	CRC Error IRQ Enable (Cache Interface Only) SPI will set CRC Error pending when CRC_Error_TIME times consecutive error occurs 0: Disable 1: Enable	R/W	0x0
20	CRC_EN	CRC Enable (Cache Interface Only) 0: Disable 1: Enable	R/W	0x0
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: delay 1 ns 0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns	R/W	0x0

		1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns 1110: delay 14 ns 1111: delay 15 ns		
15	RAND_PAUSE	Randomizer pause 0: normal 1:pause	R/W	0x0
14	RAND_SEL	Randomizer seed select 0: use effuse bits 1: use register SPI_SEED value	R/W	0x0
13	RAND_TXEN	SPI Master TX Randomizer enable 0: disable 1: enable	R/W	0x0
12	RAND_RXEN	SPI Master RX Randomizer enable 0:disable 1:enable	R/W	0x0
11:10	SPI_IO_MODE	SPI data I/O mode select 00: 1x I/O mode select 01: 1x I/O mode select 10: 2x I/O mode select 11: 4x I/O mode select	R/W	0x0
9	SPI_3WIRE	SPI Master 3-wire mode enable 0:disable 1:enable use 3-wire mode only in master read only or write only mode.	R/W	0x0
8	SPI_REQ	SPI Bus Request (AHB Interface Only, Please reference operation manual) 0:disable 1:enable	R/W	0x0
7	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 1 level empty; 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 1 level full.; 0: disable 1: enable	R/W	0x0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable (AHB Interface Only) 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable (AHB Interface Only) 0: Disable	R/W	0x0

		1: Enable		
3	SPI_SS	SPI NSS pin control output (AHB Interface Only) 0: output low 1: output high	R/W	0x0
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

9.3.5.2 SPI0_STA

SPI Status Register
Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	x
8	SPI_READY	SPI Ready (AHB Interface Only, please reference operation manual) 0: not ready 1: ready	R	0x0
7	CRC_PD	CRC Error Pending, Write 1 to this bit will clear it. (Cache Interface Only) 0: No CRC Error Pending 1: CRC Error Pending.	R/W	0x0
6	SPI_BUSY	SPI master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0
5	SPI_TXFU	SPI TX FIFO Full (AHB Interface Only) 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI TX FIFO Empty (AHB Interface Only) 0: not empty 1: empty	R	0x1
3	SPI_RXFU	SPI RX FIFO Full (AHB Interface Only) 0: not full 1: full	R	0x0
2	SPI_RXEM	SPI RX FIFO Empty (AHB Interface Only)	R	0x1

		0: not empty 1: empty		
1	CRC_ERROR	CRC Error Status, Write 1 to this bit will clear it. (Cache Interface Only) 0: No CRC Error 1: CRC Error.	R/W	0x0
0	-	Reserved	R	x

9.3.5.3 SPI0_TXDAT

SPI Transmit FIFO Data Register
Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7:0	SPI_TXDAT	SPI Tx Data[7:0] Writing this field will send 1 byte to 8bitx4 levels depth SPI TX FIFO	W	0x0

9.3.5.4 SPI0_RXDAT

SPI Transmit FIFO Data Register
Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	x
7:0	SPI_RXDAT	SPI Rx Data[7:0] Reading this field will fetch 1 byte from 8bitx4 levels depth SPI RX FIFO only when SPI_CTL. RAND_RXEN disable	R	0x0

9.3.5.5 SPI0_BC

SPI Bytes Count Register, this register is used for setting SPI bytes counter bits in SPI master read only mode.
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be received	R	0x0
15:0	SPI_BC	Bytes Counter [15: 0]	R/W	0x0

9.3.5.6 CACHE_ERROR_ADDR

Cache Error Addr Register

Offset=0x0018

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	x
23:5	CACHE_ERROR_ADDR	Cache read ERROR Address, only for cpu to inquire	R	0x7FFFF
4:0	-	Reserved	R	x

9.3.5.7 NO_CRC_ADDR

NO CRC ADDR Register

Offset=0x001c

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	x
23:5	START_ADDR	Start address of no crc area in spi norflash Note:This is high 16bit addr of LOGIC norflash addr, NOR_ADDR[23:5]	W/R	0x7FFFF
4:0	-	Reserved	R	x

9.3.6 SPI1 Register List

SPI1 Registers Block Base Address

Name	Physical Base Address
SPI1	0x40012000

SPI1 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI1_CTL	SPI1 Control Register
0x0004	SPI1_STA	SPI1 Status Register
0x0008	SPI1_TXDAT	SPI1 Transmit FIFO Data Register
0x000C	SPI1_RXDAT	SPI1 Receive FIFO Data Register
0x0010	SPI1_BC	SPI1 Byte Counter Register

9.3.7 SPI1 Register Description

9.3.7.1 SPI1_CTL

SPI1 Control Register,
Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0x0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27:23	-	Reserved	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0x0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0x0
20	RX_WRITE_SEL	SPI Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0
19:15	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 00000: no delay 00001: delay 1 ns 00010: delay 2 ns 00011: delay 3 ns 00100: delay 4 ns … … 01111: delay1 5 ns 10000: delay1 6 ns	R/W	0x0

		10001: delay 17 ns … … 11111: delay 31 ns		
14:12	-	Reserved	R/W	0x0
11	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 1 level empty; When DMA remain counter < 4, trigger DRQ until all data transfer completely; 0: disable 1: enable	R/W	0x0
10	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 1 level full.; When DMA remain counter < 4, trigger DRQ until all data received completely; 0: disable 1: enable	R/W	0x0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO is not full. 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, trigger SPI RX IRQ when SPI RX FIFO is not empty. 0: disable 1: enable	R/W	0x0
7:6	-	Reserved	R/W	0x0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	0x1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only	R/W	0x0

		11: Read and Write		

9.3.7.2 SPI1_STA

SPI1 Status Register

Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	x
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0x0
10	-	Reserved	R	x
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0x0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0x0
7	SPI_RXFU	SPI RX FIFO Full 0: not full 1: full	R	0x0
6	SPI_RXEM	SPI RX FIFO Empty 0: not empty 1: empty	R	0x1
5	SPI_TXFU	SPI TX FIFO Full 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI TX FIFO Empty 0: not empty 1: empty	R	0x1
3	SPI_TIRQ_PD	SPI TX IRQ Pending, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0x0
2	SPI_RIRQ_PD	SPI RX IRQ Pending, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0x0
1	-	Reserved	R	x

0	SPI_BUSY	SPI master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0

9.3.7.3 SPI1_TXDAT

SPI1 data register, this register is used for writing data to SPI TX FIFO.
Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:0	SPI_TXDAT	SPI TX FIFO,32bitx2 levels When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx8levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0x0

9.3.7.4 SPI1_RXDAT

SPI1 data register, this register is used for reading data from SPI RX FIFO
Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31:0	SPI_RXDAT	SPI RX FIFO, When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx8levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx2 levels	R	0x0

9.3.7.5 SPI1_BC

SPI1 Bytes Count Register, This register is used to setting SPI bytes counter bits
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	SPI_BC	Bytes Counter [12: 0]	R/W	0x0

9.3.8 SPI2 Register List

SPI1 Registers Block Base Address

Name	Physical Base Address
SPI2	0x40013000

SPI2 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI2_CTL	SPI2 Control Register
0x0004	SPI2_STA	SPI2 Status Register
0x0008	SPI2_TXDAT	SPI2 Transmit FIFO Data Register
0x000C	SPI2_RXDAT	SPI2 Receive FIFO Data Register
0x0010	SPI2_BC	SPI2 Byte Counter Register

9.3.9 SPI2 Register Description

9.3.9.1 SPI2_CTL

SPI1 Control Register

Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0x0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27:23	-	Reserved	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0x0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0x0

20	RX_WRITE_SEL	SPI Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0
19:15	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 00000: no delay 00001: delay 1 ns 00010: delay 2 ns 00011: delay 3 ns 00100: delay 4 ns … … 01111: delay1 5 ns 10000: delay1 6 ns 10001: delay 17 ns … … 11111: delay 31 ns	R/W	0x0
14:12	-	Reserved	R/W	0x0
11	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 1 level empty; When DMA remain counter < 4, trigger DRQ until all data transfer completely; 0: disable 1: enable	R/W	0x0
10	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 1 level full.; When DMA remain counter < 4, trigger DRQ until all data received completely; 0: disable 1: enable	R/W	0x0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO is not full.. 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, trigger SPI RX IRQ when SPI RX FIFO is not empty. 0: disable 1: enable	R/W	0x0
7:6	-	Reserved	R/W	0x0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable	R/W	0x0

		0: Disable 1: Enable		
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	0x1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

9.3.9.2 SPI2_STA

SPI1 Status Register

Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	x
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0x0
10	-	Reserved	R	x
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0x0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0x0
7	SPI_RXFU	SPI RX FIFO Full 0: not full 1: full	R	0x0
6	SPI_RXEM	SPI RX FIFO Empty	R	0x1

		0: not empty 1: empty		
5	SPI_TXFU	SPI TX FIFO Full 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI TX FIFO Empty 0: not empty 1: empty	R	0x1
3	SPI_TIRQ_PD	SPI TX IRQ Pending, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0x0
2	SPI_RIRQ_PD	SPI RX IRQ Pending, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0x0
1	-	Reserved	R	x
0	SPI_BUSY	SPI master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0

9.3.9.3 SPI2_TXDAT

SPI1 data register, this register is used for writing data to SPI TX FIFO
Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:0	SPI_TXDAT	SPI TX FIFO,32bitx2 levels When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx8levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0x0

9.3.9.4 SPI2_RXDAT

SPI1 data register, this register is used for reading data from SPI RX FIFO
Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31:0	SPI_RXDAT	SPI RX FIFO, When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx8levels	R	0x0

		When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx2 levels		

9.3.9.5 SPI2_BC

SPI1 Bytes Count Register, This register is used to setting SPI bytes counter bits
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	x
12:0	SPI_BC	Bytes Counter [12: 0]	R/W	0x0

10 Man-Machine Interface

10.1 I2S

10.1.1 Overview

- Support I2S Transmitter(TX) & Receiver(RX)
- Support I2S master mode & slave mode.
- I2S Support Sample Rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k.
- Support i2s model、left-justified、right-justified、TDM mode(TDM4、rx only)

10.1.2 Function Description

10.1.3 Operation Manual

10.1.3.1 I2S Operation

I2S is a serial audio transmission bus. ATB110X's I2S supports master slave mode, and the output has eight I/O: I2STX_MCLK， I2STX_BCLK， I2STX_LRCLK， I2STX_DAT， I2SRX_MCLK， I2SRX_BCLK，I2SRX_LRCLK，I2SRX_DAT.

1. LRCLK is equal to the sampling rate, for example, the output sampling rate is 48kHz, and the LRCLK is 48kHz.

2. BCLK is TXBCLKSET *2*Fs (TDM mode, TXBCLKSET *4*Fs).

3.The serial data output DAT is a binary complement audio data. One audio data of a single channel is sent in a serial way on the DAT, the high position is in the front, the low position is after, and the 16 BCLK is occupied.

4. MCLK is 256*Fs, and the master clock ensures that the signal can be transmitted synchronously. For example, the output sampling rate is 48kHz, then MCLK = 256*48kHz = 12.288MHz.

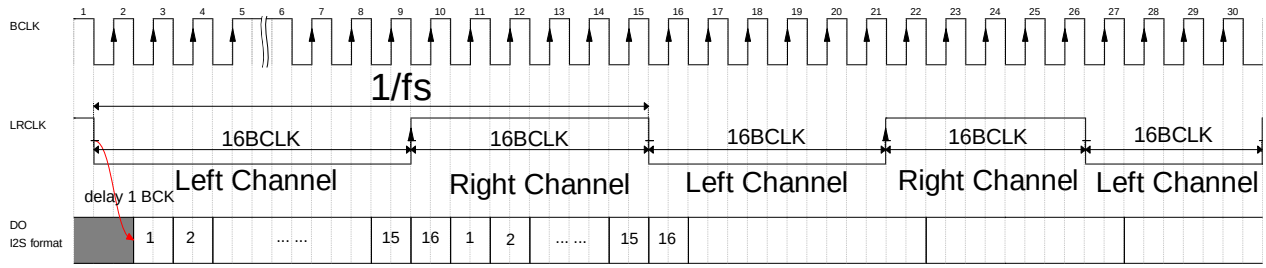


Figure 10-1 I2S 16bit standard Timing

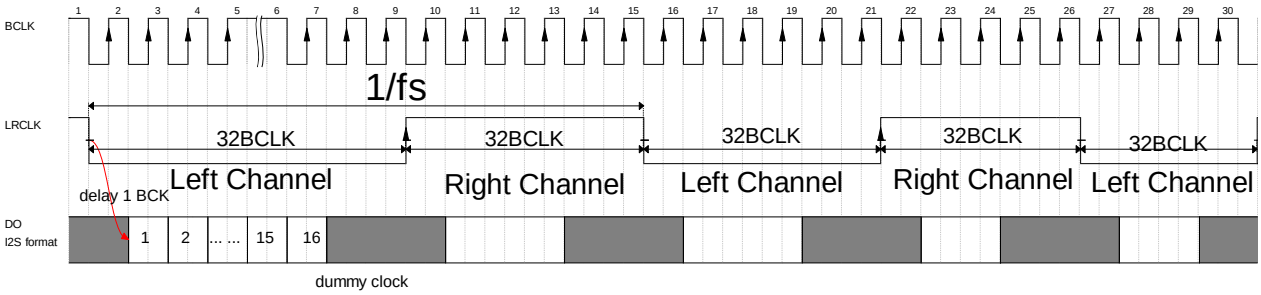


Figure 10-2 I2S 32bit standard Timing

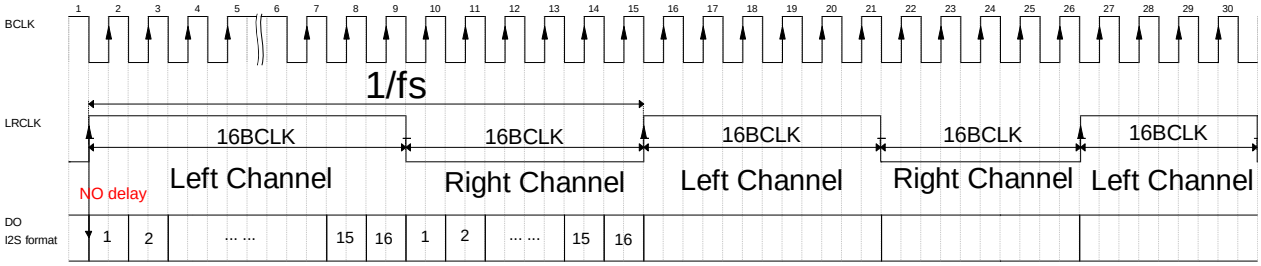


Figure 10-3 I2S 16bit left/right justified Timing

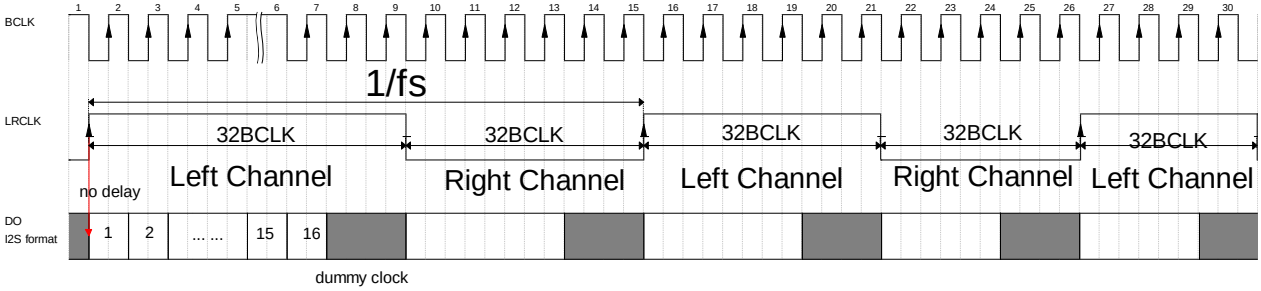


Figure 10-4 I2S 32bit left justified Timing

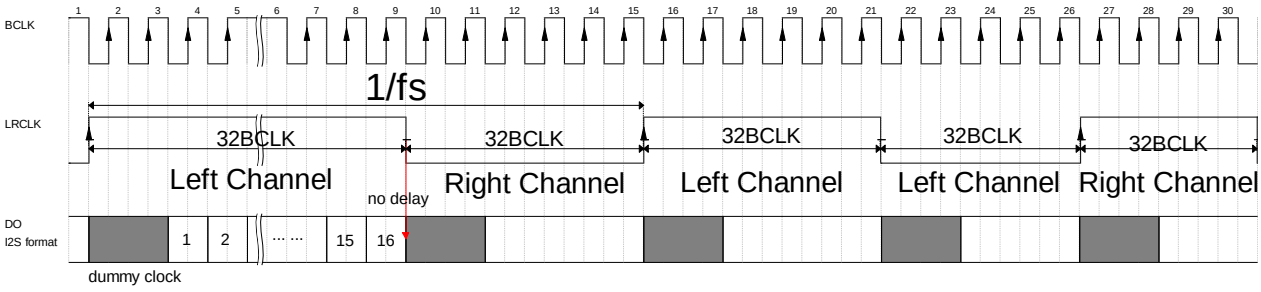


Figure 10-5 I2S 32bit right justified Timing

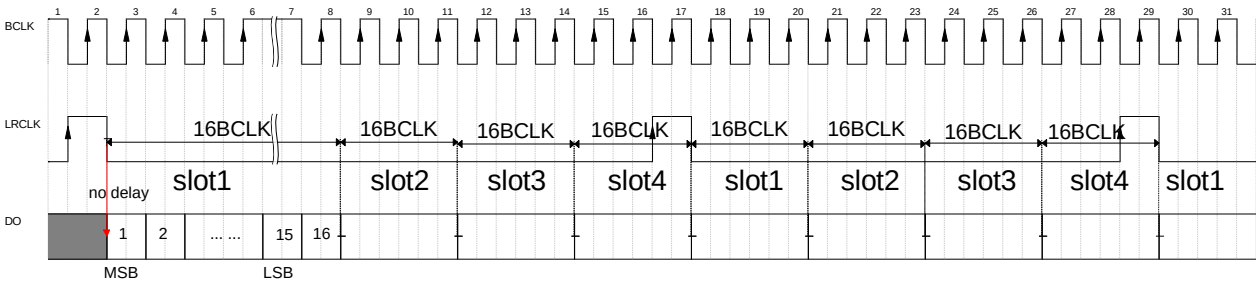


Figure 10-6 TDM-A-16bit Timing

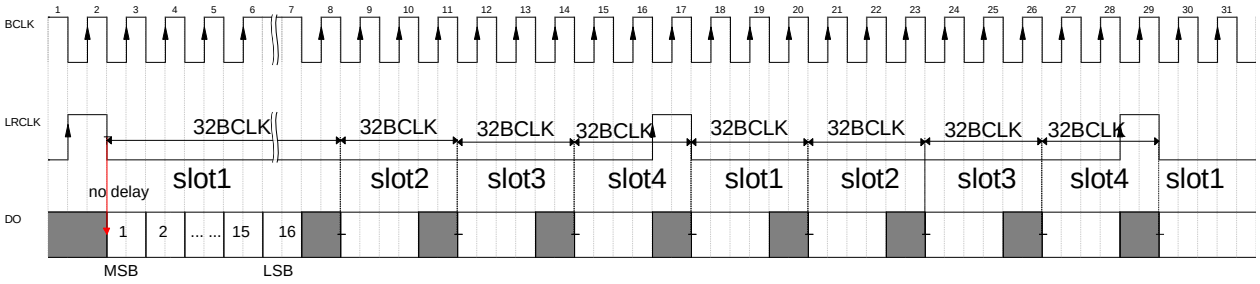


Figure 10-7 TDM-A-32bit Timing

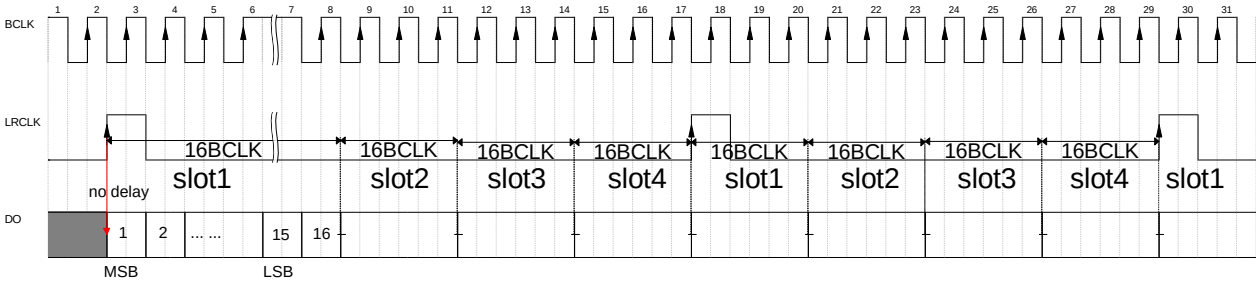


Figure 10-8 TDM-B-16bit Timing

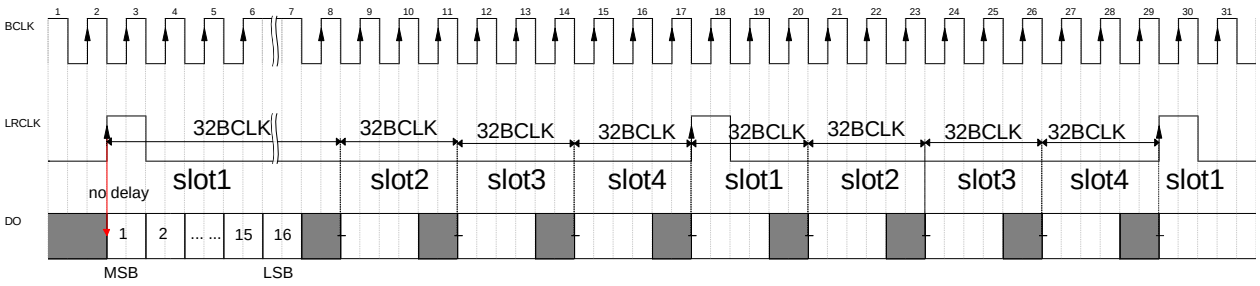


Figure 10-9 TDM-B-32bit Timing

10.1.4 Register List

I2S Controller Registers Address

Name	Physical Base Address
I2S_Control_Register	0x40015000

I2S Controller Registers

Offset	Register Name	Description
0x0000	I2S_TX_CTL	I2S TX control Register
0x0004	I2S_RX_CTL	I2S RX control Register
0x0008	I2S_TXFIFOCTL	I2S FIFO control Register
0x000c	I2S_TXFIFOSTAT	I2S FIFO state Register
0x0010	I2S_DAT_FIFO	I2S FIFO Data Register

10.1.5 Register Description

10.1.5.1 I2S_TX_CTL

I2S TX control Register
Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	TXMSMODE	I2S mode select: 0:I2S Master mode; 1:I2S Slave mode	RW	0x0
6	TX_SMCLK	MCLK(256FS) source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only.	RW	0x1
5:4	-	Reserved	R	0x0
3	TXBCLKSET	Set the number of bits per channel 0x0:32bit 0x1:16bit Note: The valid digits both are 16bit, and see the timing diagram above	RW	0x1
2:1	TXMODELSEL	I2S TX Mode selection for transmission data 00: i2s model 01: left-justified 10: right-justified 11: Reserved	RW	0x0
0	TXEN	I2S TX Enable. 0: Disable 1: Enable	R/W	0x0

10.1.5.2 I2S_RX_CTL

I2S RX control Register

Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
32:8	-	Reserved	R	0x0
10	TDM_MSEL	TDM mode select 0:TDMA 1:TDMB	RW	0x0
9	I2SRX_5W_EN	5wire enable: 0:disable 1:enable When set the bit, I2S0RX enable is controlled by I2STX0_CTL[0]. At this time, the interface is the mode of receiving and receiving at the same sampling rate TX and RX shareTXMCLK/TXBCLK/TXLRCLK	RW	0x0
8	-	Reserved	R	0x0
7	RXMSMODE	I2S mode select: 0:I2S Master mode; 1:I2S Slave mode	RW	0x0
6	RX_SMCLK	MCLK source when in slave mode 0:from internal module 1:from extern input by pad of Mclk	RW	0x1
5:4	-	Reserved	R	0x0
3	TXBCLKSET	Set the number of bits per channel 0x0:32bit 0x1:16bit Note: The valid digits both are 16bit, and see the timing diagram above	RW	0x1
2:1	RXMODELSEL	I2S RX Mode selection for transmission data 0 0:i2s model 01: left-justified 10: right-justified 11: TDM mode(4 channel)	RW	0x0
0	RXEN	I2S RX Enable. 0: Disable 1: Enable	R/W	0x0

10.1.5.3 I2S_TXFIFOCTL

I2S TX FIFO Digital Control Register
Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
31:3	-	Reserved	R	0x0
2	TXFFIE	TX FIFO empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	TXFFDE	TX FIFO empty DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	TXFRST	TX FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

10.1.5.4 I2S_TXFIFOSTAT

I2S TX FIFO State Register
Offset = 0x000C

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	0x0
5	TXFEIP	I2STX FIFO Empty IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
4:0	TXFS	I2STX FIFO Status This 4 bits shows how many sample fifo not filled. For example, when read as 4, means CPU/DMA can write 4 samples to fifo.	R	0x8

10.1.5.5 I2S_DAT

I2S FIFO Data Register
Offset = 0x0010

Bit(s)	Name	Description	R/W	Reset
31:16	I2SDAT	I2S FIFO Data FIFO is 16-bit * 16 levels.	W	x
15:0	-	Reserved	R	0x0

10.2 Voice ADC

10.2.1 Overview

- Build in mono 16-bit lower power sigma-delta ADC, SNR (A-weighted):83dB.
- ADC supports only sample rate 8k and 16k Hz.
- Support Digital MIC and Analog MIC
- A digital high-pass filter can be used to remove DC offsets when ADC use
- Supports mono single-ended input analog microphone.

10.2.2 Function Description

10.2.2.1 Voice ADC performance

Table 10-1 ADC Characteristics

AUDIOPLL=0x16,BTVCC=3.280V , VDIG=0.967V , VREF=0.568V , VDD=1.200V， ADC_GAIN=0db					
Parameter	**Test condition**	**Min**	**Typ**	**Max**	**Unit**
Input Common Mode Voltage			0.567		mV
Full Scale input Voltage	**(THD+N=-40dB)**		384		mVrms
Noise	➢ Fs=8KHz ➢ Fs=8KHz,A-weighted ➢ Fs=16KHz ➢ Fs=16KHz,A-weighted		-81.5 -84.4 -83.1 -84.5		dbFS
SNR	**Input = -dbV)** ➢ Fs=8KHz ➢ Fs=8KHz,A-weighted ➢ Fs=16KHz ➢ Fs=16KHz,A-weighted		 82.2 84.4 83.1 84.5		dB
Dynamic Range	**384uVrms input (-60db of max input level)** ➢ Fs=8KHz ➢ Fs=8KHz,A-weighted ➢ Fs=16KHz ➢ Fs=16KHz,A-weighted		 82.7 85.6 83.8 85.3		dB
THD+N	**Best at 324mVrms (-8.2dbV) input** ➢ Fs=8KHz ➢ Fs=8KHz,A-weighted ➢ Fs=16KHz ➢ Fs=16KHz,A-weighted		 81.3 83.4 81.3 81.9		dB

Passband Ripple	**Fs=16Khz(from 20 to 7.5Khz)** **Fs=8Khz(from 20 to 3.75Khz)**	-0.007 +0.001		+0.113 +0.188	db
Stopband Attenuation		-60			db

Figure 10-10 1.2V，0db ADC THD+N VS AMP curve

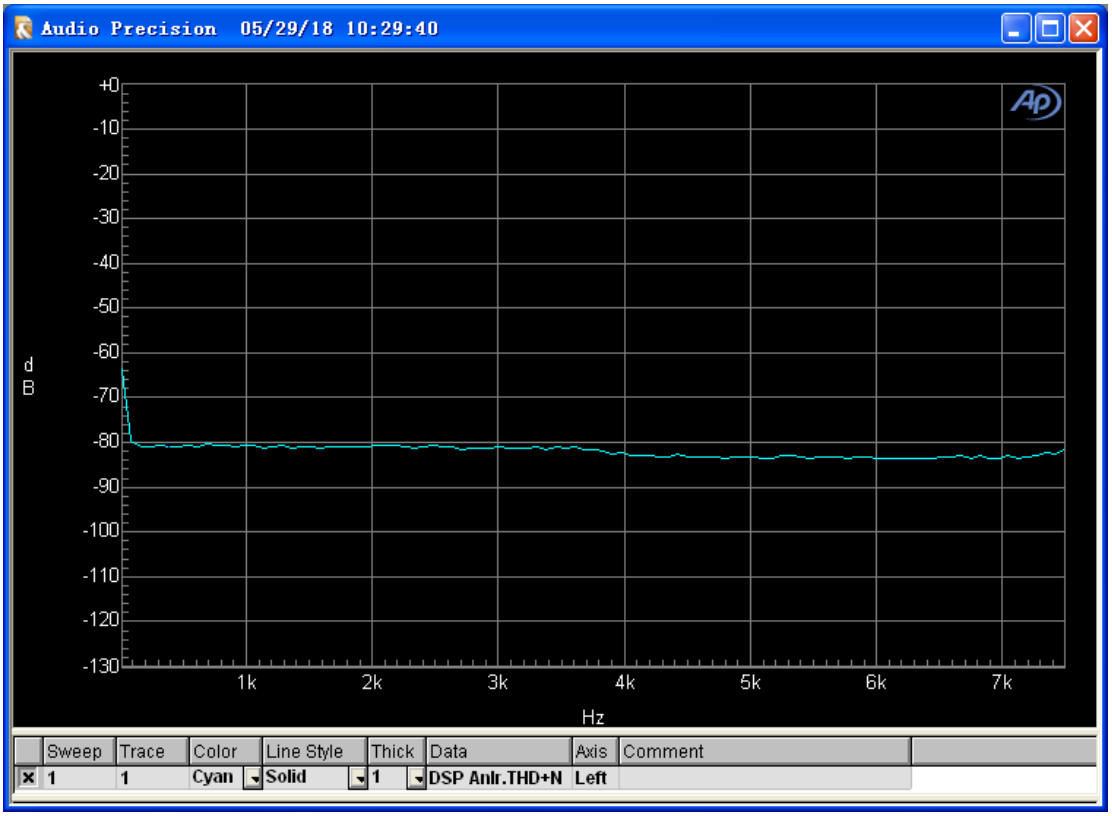


Figure 10-11 1.2V，0db，326mVrms input，BW=20~8KHz

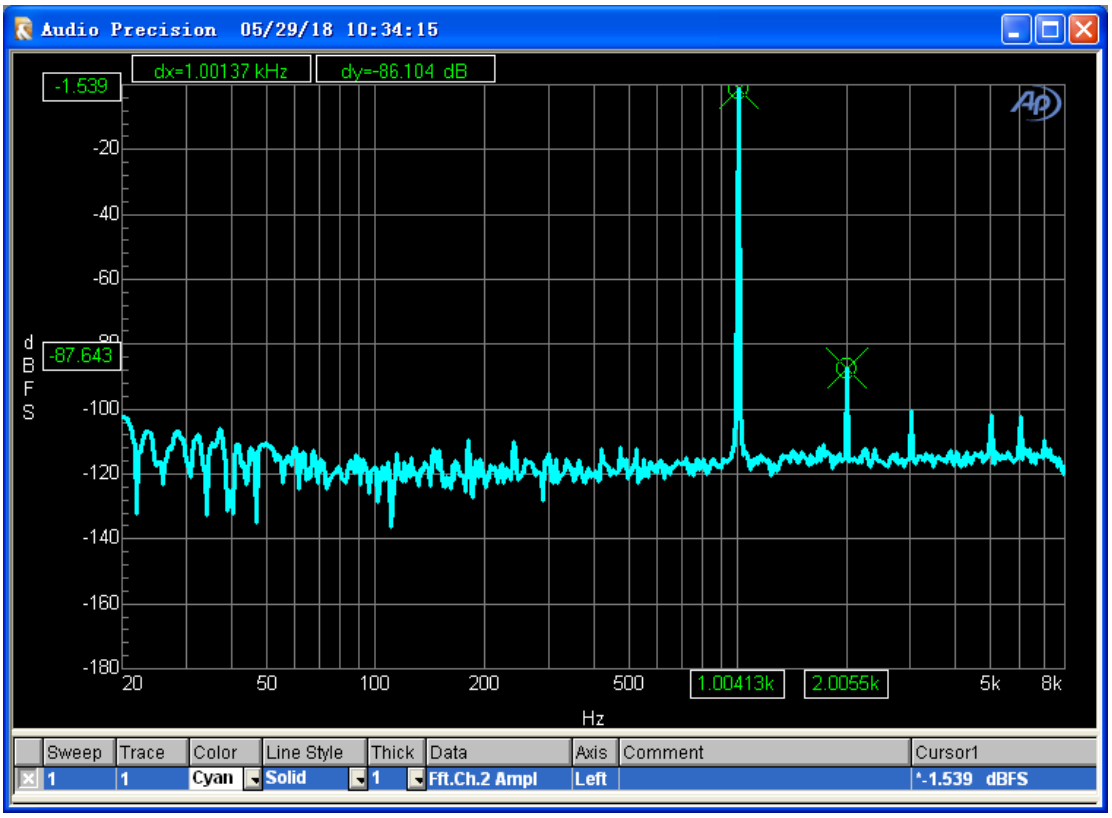


Figure 10-12 Spectrum diagram 1.2V，30db，beat at 326mVrms input

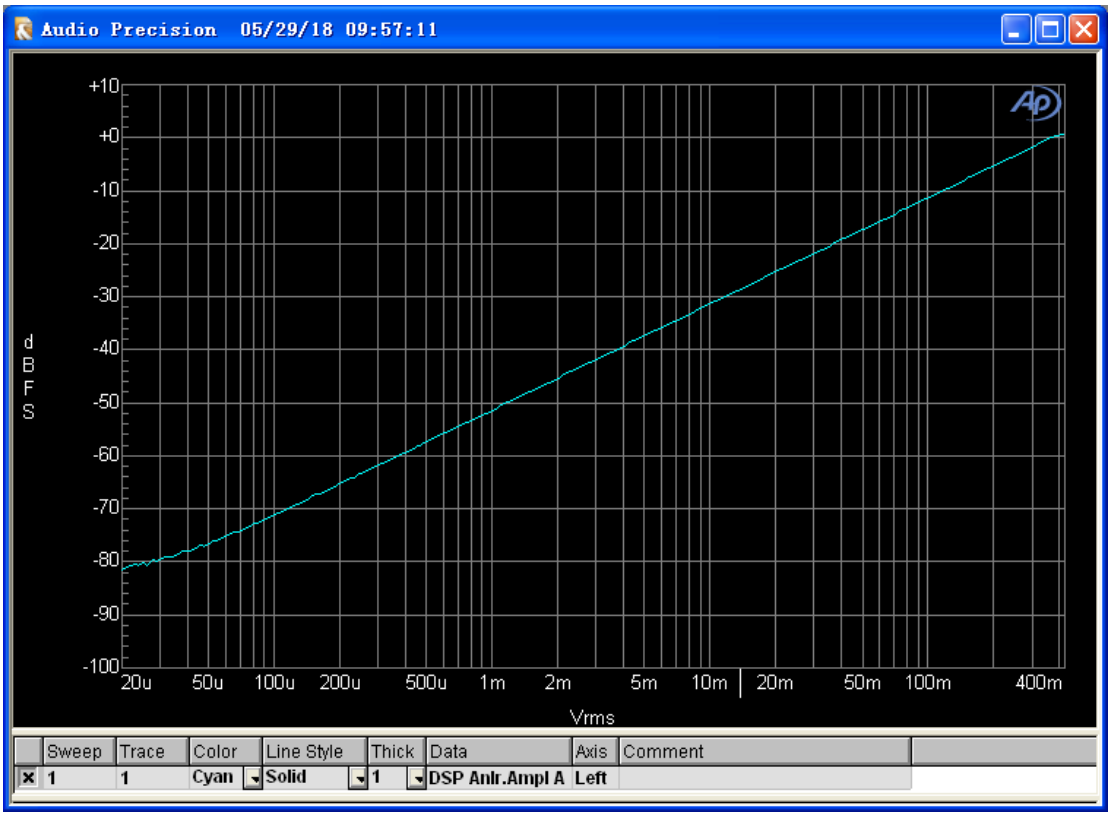


Figure 10-13 1.2V，0db 20uVrms ~ 424.3 mVrms (1.2Vpp))

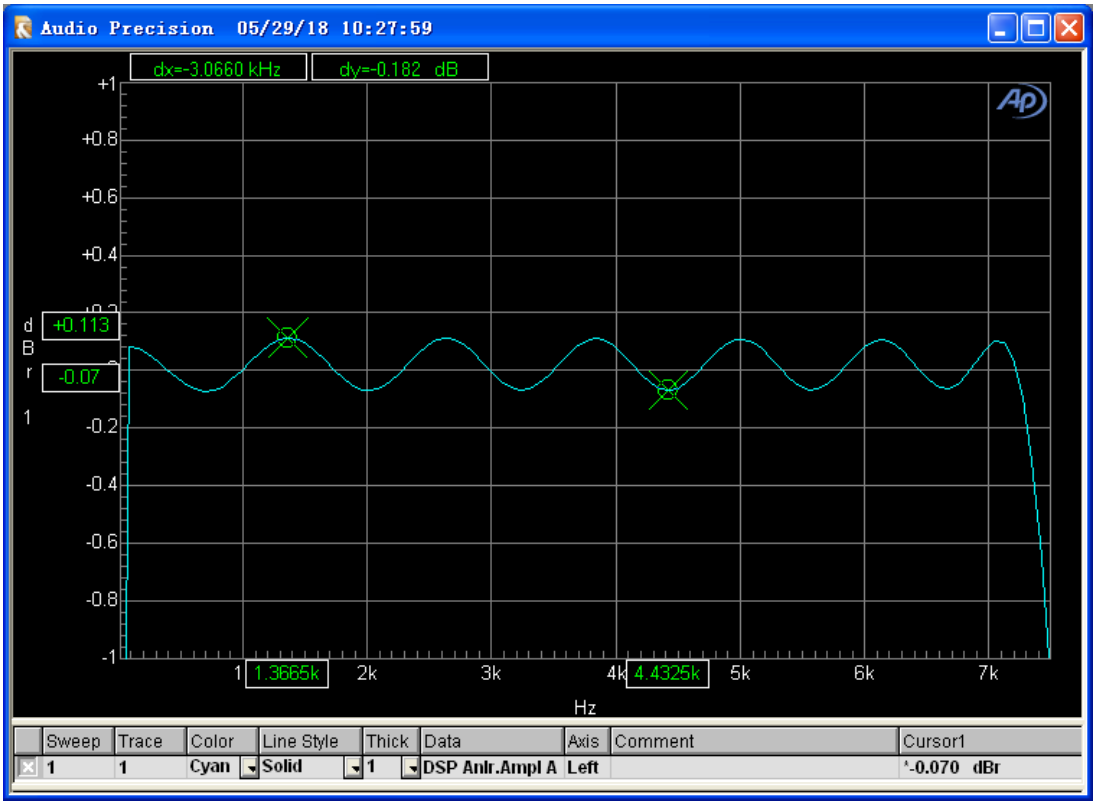


Figure 10-14 1.2V，0db，Ripple in band, and frequency response curve

10.2.2.2 DMIC

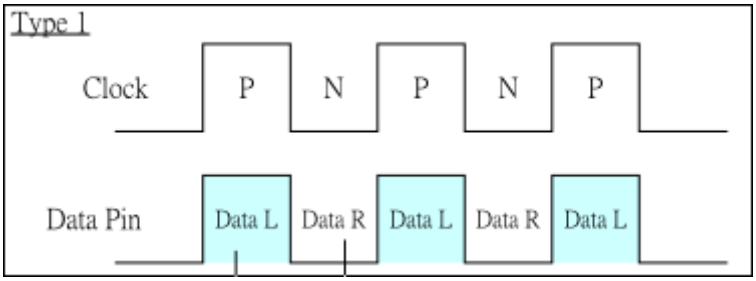


Figure 10-15 DMIC Interface

DMIC_CLK rising edge samples DMICx_DATA (x=0,1) as left channel data, and falling edge samples as right channel data.

10.2.2.3 High pass filter

Table 10-2 ADC HFP config table

HPF_CFG	-3db Cut-off frequency @8khz sampling	-3dbCut-off frequency @16khz	Delaying of the step forward DC estimation @8khz	Delaying of the step forward DC estimation @16khz

	rate	sampling rate	sampling rate	sampling rate
Level 0	0.6hz	1.2hz	1.54s	0.77s
Level 1	2.5hz	5hz	480ms	240ms
Level 2	10hz	20hz	120ms	60ms
Level 3	39hz	80hz	30ms	15ms

Note: ADC start up time (related to peripheral circuit) and HFP stable-time.

10.2.3 Register List

ADC Controller Registers Address

Name	Physical Base Address
ADC_Control_Register	0x40015400

ADC Controller Registers

Offset	Register Name	Description
0x0000	ADC_DIGCTL	ADC Digital Control Register
0x0004	ADC_FIFOCTL	ADC fifo Control Register
0x0008	ADC_STAT	ADC State Register
0x000c	ADC_DAT	ADC Data Register
0x0010	ADC_ANACTL	ADC Analog Control Register
0x0014	DMIC_CTL	Digital microphone Control Register

10.2.4 Register Description

10.2.4.1 ADC_DIGCTL

ADC Digital Control Register

Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:7	-	Reserved	R	0x0
6:5	HPF_CFG	High pass filter config 00: level 0 01: level 1 10: level 2 11: level 3 Note: Different levels can be set according to different usage scenarios. The higher the level, the higher the response frequency, the quicker the	RW	0x0

		response.		
4	HPFREN	High Pass Filter Enable 0x0：disable 0x1：enable	RW	0x0
3:2	ADCGC	ADC Digital Gain Control 00: 0dB(bypass) 01: 0dB(bypass) 10: 6dB(x2) 11: 12dB(x4)	RW	0x0
1	ADDEN	ADC Digital Debug Enable 0x0: Disable 0x1: Enable	RW	0x0
0	AADEN	ADC Analog Debug Enable 0x0: Disable 0x1: Enable	RW	0x0

10.2.4.2 ADC_FIFOCTL

ADC fifo control Register
Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	ADFIS	ADC FIFO Input Select: 0x0: ADC 0x1: I2SRX	RW	0x0
2	ADFFIE	ADC FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	ADFFDE	ADC FIFO Full DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	ADFRST	ADC FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

10.2.4.3 ADC_FIFOSTAT

ADC State Register
Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0

8	ADFIP	ADC FIFO Full IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
7:5	-	Reserved	R	0x0
4:0	ADFS	ADC FIFO Status. These 5 bits shows how many samples fifo filled. For example, when read as 6, means CPU can read 6 samples from fifo.	R	0x0

10.2.4.4 ADC_DAT

ADC Data Register
Offset = 0x000c

Bit(s)	Name	Description	R/W	Reset
31:16	ADDAT	ADC Data FIFO is 16bit * 16 levels.	R	x
15:0	-	Reserved	R	0x0

Note: ADC has only one channel (mono).

10.2.4.5 ADC_ANACTL

AnalogIN OP Control Register
Offset = 0x0010

Bit(s)	Name	Description	R/W	Reset
31:30	-	Reserved	R	x
29	VMIC_EN	AMIC&DMIC power en 0：disable 1：enable	RW	0x0
28:16	MICOPBC	Bias current of MIC OP control	RW	0x115A
15	INCCEN	MIC INPUT dc blocking cap charge enable 0:disable 1:enable	RW	0x0
14	REF_FILTER	ADC VREF FILTER ENABLE 1: Enable 0: Disable	RW	0x0
13	VREF_PD	ADC VREF PULLDOWM RES ENABLE 1: Enable 0: Disable	RW	0x1
12	VREF_EN	ADC VREF ENABLE 1: Enable	RW	0x0

<table>
<tr><td></td><td></td><td>0: Disable</td><td></td><td></td></tr>
<tr><td>11</td><td>BIASLESSEN</td><td>Total bias current descrease by 50%
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>10</td><td>BIASBOOSTEN</td><td>Total bias current increased by 50%
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>9</td><td>BIASEN</td><td>Bias current generator enable
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>8</td><td>VRDAEN</td><td>Sigma delta modulator’s voltage reference enable
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>7</td><td>SDMEN</td><td>SDM ENABLE
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>6</td><td>MICINPDH</td><td>MIC INPUT CHANNEL pull down
1: Enable
0: Disable</td><td>RW</td><td>0x1</td></tr>
<tr><td>5</td><td>MICOPENH</td><td>MIC op enable
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>4</td><td>AMICEN</td><td>AMIC INPUT CHANNEL ENABLE
1: Enable
0: Disable</td><td>RW</td><td>0x0</td></tr>
<tr><td>3:0</td><td>INGC</td><td>INPUT GAIN CONTROL
(INGC<3>=0 usually for adc 0db test, input res is 31k)
<table>
<tr><td>INGC<3>=0 usually for adc 0db test, input res is 31k</td><td>INGC<3>=1 usually for mic channel, input res is 5.5k</td></tr>
<tr><td>0000: 0dB</td><td>1000:15DB</td></tr>
<tr><td>0001: 3dB</td><td>1001:18DB</td></tr>
<tr><td>0010: 6dB</td><td>1010:21DB</td></tr>
<tr><td>0011: 9dB</td><td>1011:24DB</td></tr>
<tr><td>0100: 12dB</td><td>1100:27DB</td></tr>
<tr><td>0101: 15dB</td><td>1101:30DB</td></tr>
<tr><td>0110: 18dB</td><td>1110:33DB</td></tr>
<tr><td>0111: 21dB</td><td>1111:36DB</td></tr>
</table></td><td>RW</td><td>0xa</td></tr>
</table>

10.2.4.6 DMIC_CTL

Digital microphone Control Register

Offset = 0x0014

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	x
4	DMICEN	DMIC channel enable 0:disable 1:enable	RW	0x0
3	DRFS	DMIC Rising or falling edge sampling Select 0x0: latch data at dmic_clk rising edge(left channel data) 0x1: latch data at dmic_clk falling edge(right channel data)	RW	0x0
2	DMIC_OVFS_SEL	DMIC oversampling rate control: 0:128fs 1:64fs	RW	0x0
1:0	DMIC_PRE_GAIN	Gain control for Dmic 00:1x 01:2x 10:4x 11:8x for all dmic interface	RW	0x0

10.3 IRC

10.3.1 Overview

- Support de-bounce function
- Support IRC receive function, include hardware mode and software mode (self-learning), Support pulse mode (dedicated IRC receiver) and carrier mode (shared IRC transmitter).
- Support IRC transfer function, which support TC9012/NEC/RC5/RC6 protocol
- Support IRC(infrared remote control) Inputs
- Support RC5\RC6\9012\NEC (8bit) protocol, compatible 36 kHz, 38 kHz, 40 kHz carrier.

10.3.2 Function Description

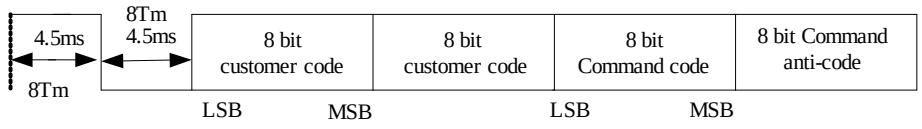
10.3.2.1 9012 protocol

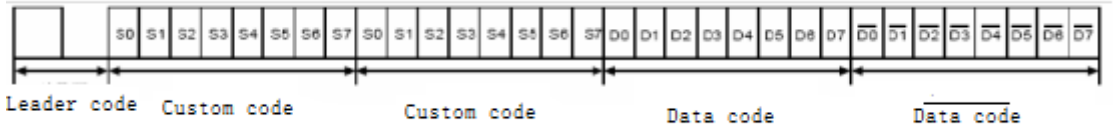
The 9012 protocol uses a pulse distance encoding of the bits. Each pulse is one Tm (560μs) long 38 kHz carrier burst. A logical "1" takes 4Tm (2.25ms) to transmit, while a logical "0" is only 2Tm (1.12ms). The recommended carrier duty-cycle is 1/4 or 1/3.

Tm=256/Fosc=0.56ms (Fosc=455 kHz)
Repetition time=192Tm=108ms
Carrier frequency = Fosc/12

- 8 bit customer code and 8 bit command code length
- customer and command are transmitted twice for reliability
- Pulse distance modulation
- Bit time of 2Tm(1.12ms) for logic “0” or 4Tm (2.25ms) for logic “1”

With this protocol the LSB is transmitted first. In this case Customer code and Command is transmitted. A message is started by 8Tm (4.5ms) AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by 8Tm (4.5ms) space, which is then followed by the Customer code and Command. Customer code and Command are transmitted twice. The second time the command bits are inverted and can be used for verification of the received message.





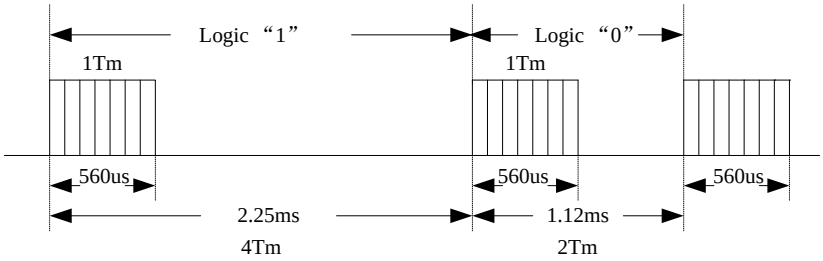


Figure 10-16 9012 protocol time(1)

A command is transmitted only once, even when the key on the remote control remains pressed. Every 192Tm a repeat code is transmitted for as long as the key remains down. This repeat code is simply one 8Tm (4.5ms) AGC pulse followed by one 8Tm (4.5ms) space and a logic “1”or”0” +1Tm (560μs) burst.

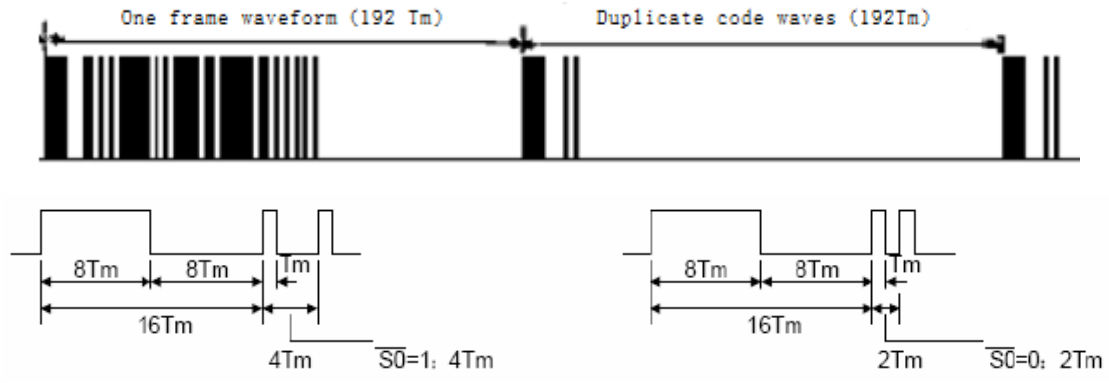


Figure 10-17 9012 protocol time(2)

10.3.2.2 NEC protocol (8bits)

The NEC protocol uses a pulse distance encoding of the bits. Each pulse is one Tm (560μs) long 38kHz carrier burst. A logical "1" takes 4Tm (2.25ms) to transmit, while a logical "0" is only 2Tm (1.12ms). The recommended carrier duty-cycle is 1/4 or 1/3.

Tm=256/Fosc=0.56ms (Fosc=455kHz)
Repetition time=192Tm=108ms
Carrier frequency = Fosc/12

- 8 bit customer and 8 bit command length
- customer and command are transmitted twice for reliability
- Pulse distance modulation
- Bit time of 2Tm(1.12ms) for logic “0” or 4Tm (2.25ms) for logic “1”

With this protocol the LSB is transmitted first. In this case Customer code and Command is transmitted. A message is started by 16Tm (9ms) AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by 8Tm (4.5ms) space, which is then followed by the Customer code and Command. Customer code and Command are transmitted twice. The second time all bits are inverted and can be used for

verification of the received message. The total transmission time is constant because every bit is repeated with its inverted length.

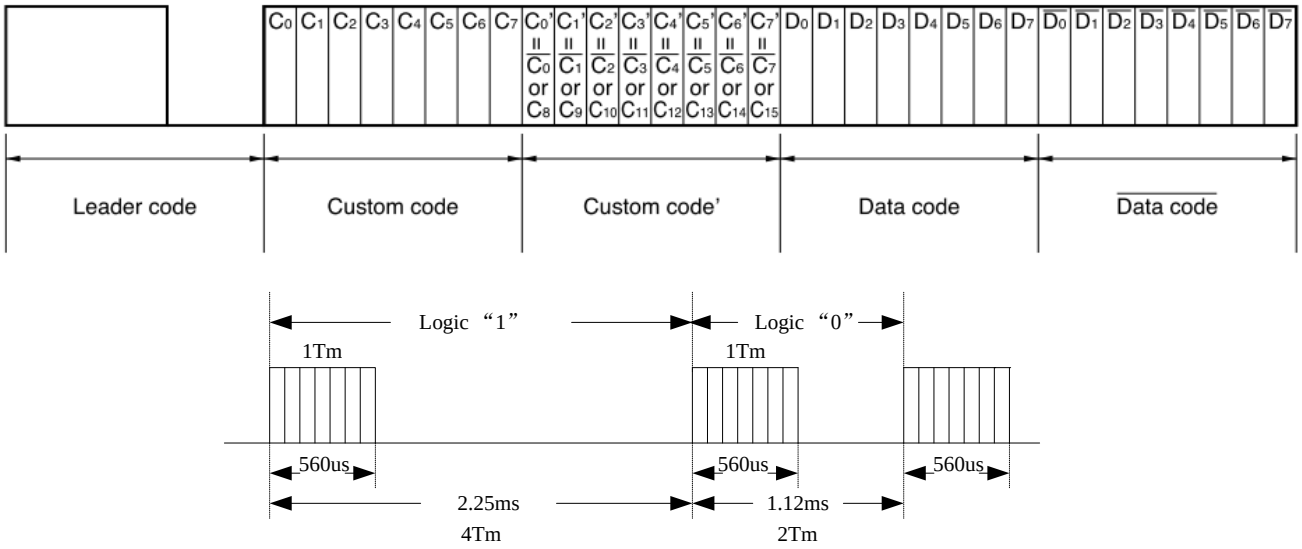
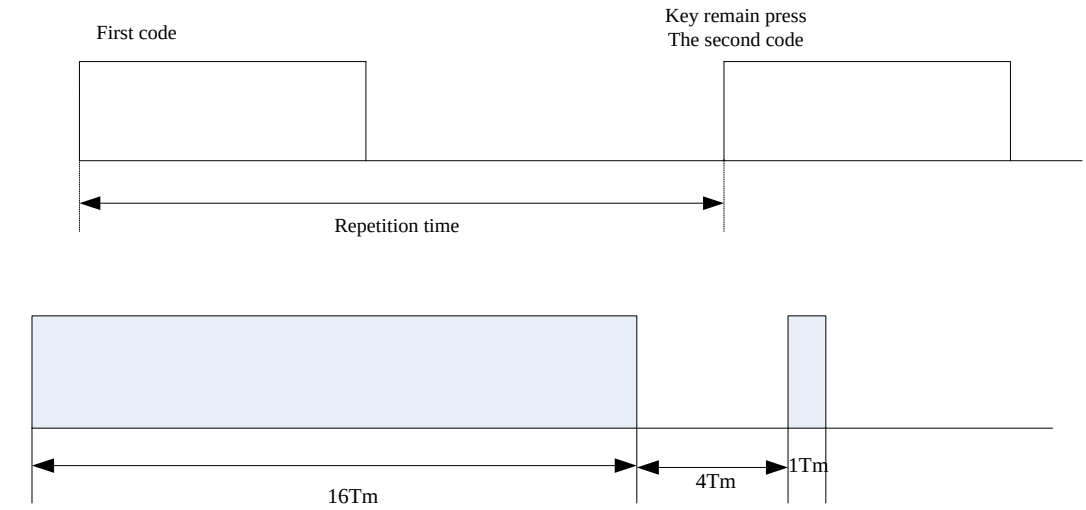


Figure 10-18 NEC protocol time(1)

A command is transmitted only once, even when the key on the remote control remains pressed. Every 192Tm a repeat code is transmitted for as long as the key remains down. This repeat code is simply a 16Tm (9ms) AGC pulse followed by a 4Tm (2.25ms) space and one Tm (560μs) burst.



Repeat code

Figure 10-19 NEC protocol time(2)

10.3.2.3 RC5 protocol

The protocol uses bi-phase modulation (or so-called Manchester coding) of a 38kHz IR carrier frequency. All bits are of equal length of 1.8ms in this protocol, with half of the bit time filled with a burst of the 38 kHz carrier and the other half being idle. A logical zero is represented by a burst in the first half of the bit time. A logical one is represented by a burst in the second half of the bit time. The pulse/pause ratio of the 38 kHz carrier frequency is 1/3 or 1/4, to reduce power consumption.

1 bit-time = 3 x 256 /Fosc= 1.688ms (Fosc=455 kHz)
Tm= 1 bit-time/2=0.844ms
Repetition time= 4 x 16 x 2Tm=108ms
Carrier frequency = Fosc/12

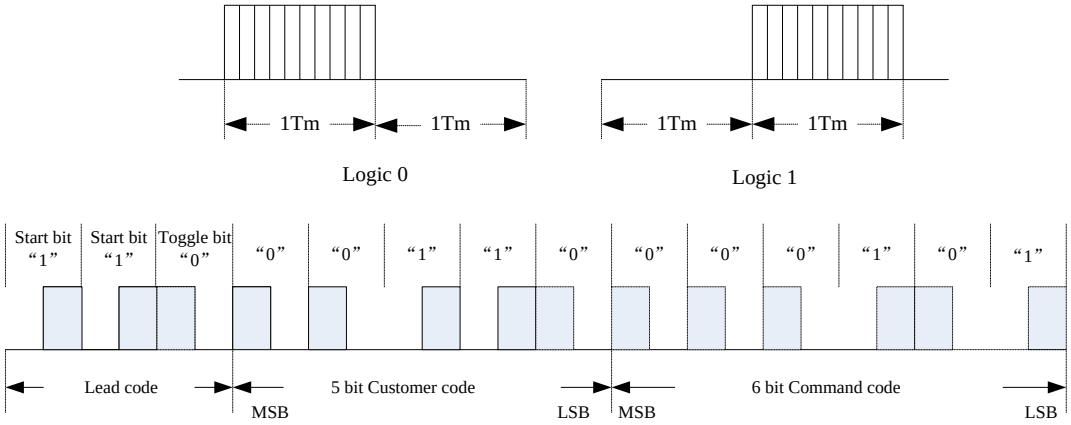


Figure 10-20 RC5 protocol time(1)

The first two pulses are the start pulses, and are both logical "1". Please note that half a bit time is elapsed before the receiver will notice the real start of the message.
The 3d bit is a toggle bit. This bit is inverted every time a key is released and pressed again. This way the receiver can distinguish between a key that remains down, or is pressed repeatedly.
The next 5 bits represent the IR device address, which is sent with MSB first. The address is followed by a 6 bit command, again sent with MSB first.
A message consists of a total of 14 bits, which adds up to a total duration of 28Tm. Sometimes a message may appear to be shorter because the first half of the start bit S1 remains idle. And if the last bit of the message is a logic "0" the last half bit of the message is idle too.
As long as a key remains down the message will be repeated every 128Tm(108ms). The toggle bit will retain the same logical level during all of these repeated messages. It is up to the receiver software to interpret this auto repeat feature.

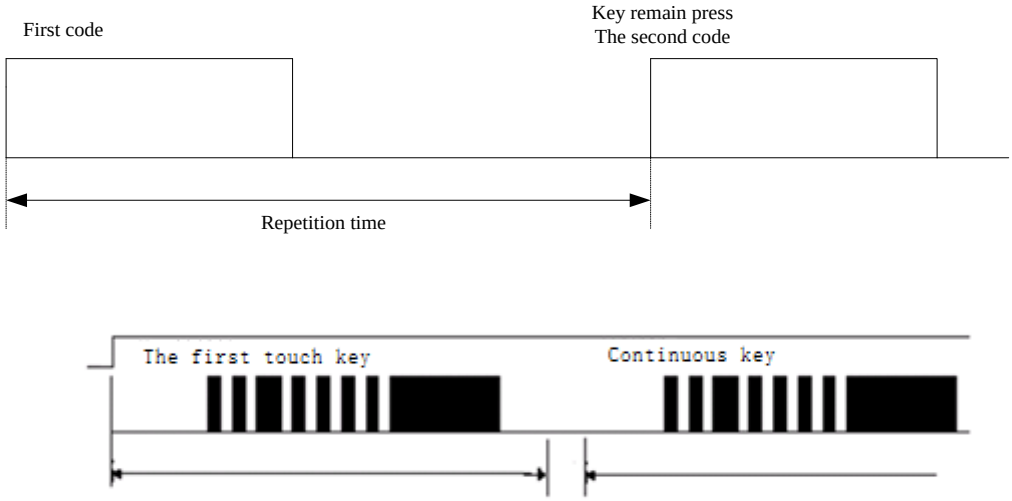


Figure 10-21 RC5 protocol time(2)

10.3.2.4 RC6 protocol

Only support RC6 mode 0.

RC-6 signals are modulated on a 36 kHz Infra Red carrier. The duty cycle of this carrier has to be between 25% and 50%.

Data is modulated using Manchester coding. This means that each bit (or symbol) will have both a mark and space in the output signal. If the symbol is a "1" the first half of the bit time is a mark and the second half is a space. If the symbol is a "0" the first half of the bit time is a space and the second half is a mark.

The main timing unit is 1t, which is 16 times the carrier period (1/36k * 16 = 444μs)

1 T = 1 x 16 /36K= 444us

1Bit= 2T=888us

Transmission time= Total 22 Bits= 23.1 ms (message) + 2.7 ms (no signal)

Repetition time=240T= 106.7ms

LS SB	mb2 mb0	TR	a7…a0	c7…c0	signal free	
Header			Control	information		

The signal frame as below:

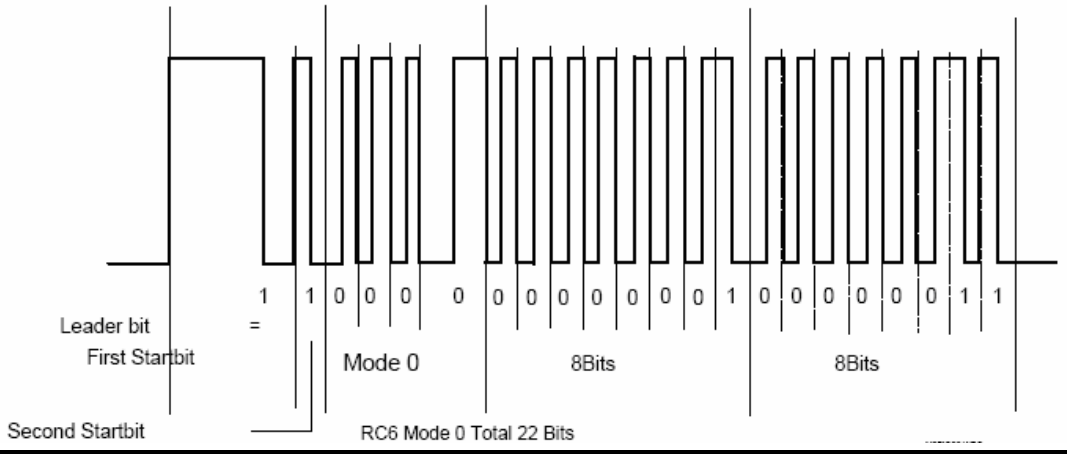


Figure 10-22 RC6 protocol time(1)

The leader pulse, which has a mark time of 6t (2.666ms) and a space time of 2t (0.889ms). This leader pulse is normally used to set the gain of the IR receiver unit.

Normal bits, which have a mark time of 1t (0.444ms) and space time of 1t (0.444ms). A "0" and "1" are encoded by the position of the mark and space in the bit time.

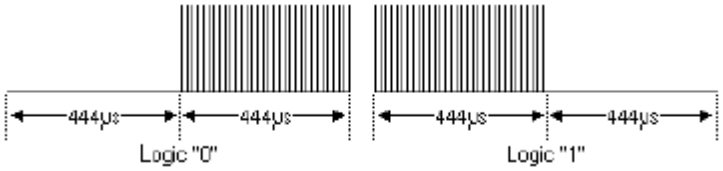


Figure 10-23 RC6 protocol time(2)

Trailer bits TR, which have a mark time of 2t (0.889ms) and a space time of 2t (0.889ms). Again a "0" and "1" are encoded by the position of the mark and space in the bit time. This bit serves as the traditional toggle bit, which will be inverted whenever a key is released. This allows the receiver to distinguish between a new key or a repeated key.

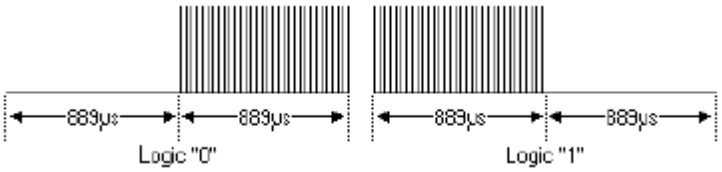


Figure 10-24 RC6 protocol time(3)

Control field:
This field holds 8 bits which are used as address byte. This means that a total of 256 different devices can be controlled using mode 0 of RC-6. The msb is transmitted first.
Information field:
The information field holds 8 bits which are used as command byte. This means that each device can have up to 256 different commands. The msb is transmitted first.

10.3.3 Register List

IRC Registers Block Base Address

Name	Physical Base Address
IRC	0x40010000

IRC Registers Offset Address

Offset	Register Name	Description
0x0000	IRC_RX_CTL	Infrared remote control(IRC) RX interface control register
0x0004	IRC_RX_STA	IRC RX status register
0x0008	IRC_RX_CC	IRC RX customer code register
0x000C	IRC_RX_KDC	IRC RX key data code register
0x0010	IRC_ANA_CTL	IRC RX analog block control register
0x0100	IRC_TX_CTL	IRC TX control register
0x0104	IRC_TX_STA	IRC TX status register
0x0108	IRC_TX_CC	IRC TX customer code register
0x010c	IRC_TX_KDC	IRC Tx key data code register

10.3.4 Register Description

10.3.4.1 IRC_RX_CTL

Infrared remote control register

Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20	CC_CMP	Custom code compare bypass 0: not bypass 1: bypass	RW	0x0
19	DATA_SRC	Data source 0 : IRC digital 1 : IRC analog	RW	0x0
18	DEMOD_EN	Demodulator enable 0: disable 1:enable	RW	0x0
17	MODE_SEL	IRC RX select 0 : software mode 1 : hardware mode(self-learning mode)	RW	0x0
16	DBB_EN	Debouncer enable 0:disable 1:enable	RW	0x0
15:4	DBC	Debouncer counter, 1 counter=1/16MHz Default counter=0xc80=200us	RW	0xc80
3	IRE	IRC RX enable	RW	0x0

		0: disable 1:enable		
2	IIE	IRC RX IRQ enable 0:disable 1:enable	RW	0x0
1:0	ICMS	IRC RX coding mode select 00:9012 code 01:8bits NEC code 10:RC5 code 11:RC6 code	RW	0x0

10.3.4.2 IRC_RX_STA

Infrared remote status register

Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	R	0x0
14:12	DEMOD_FREQ	RX Carrier frequency obtained by detection: 0: 30 KHz 1: 33 KHz 2: 36 KHz 3: 38 KHz 4: 40 KHz 5: 56 KHz	R	0x0
11	-	Reserved	R	0x0
10	DET_PRO_PD	Detect Protocol ok pending Write ‘1’ to clear this bit	R	0x0
9:8	PROTOCOL	Recognizes the input infrared protocol 00:9012 code 01:8bits NEC code 10:RC5 code 11: RC6 code	R	0x0
7	-	Reserved	R	0x0
6	UCMP	User code don’t match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:user code match 1:user code don’t match If RCC equal to ICC, this bit would be set to ‘1’. This bit was no used in self-learning mode.	RW	0x0
5	KDCM	Key data code don’t match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time	RW	0x0

		0:key data code match 1:key data code don't match If KDC was match to protocol, this bit would be set to '1'. This bit was no used in self-learning mode.		
4	RCD	Repeated code detected, Write 1 to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code	RW	0x0
3	Reserved		R	0x0
2	IIP	IRC IRQ pending bit. write 1 to this bit will clear it 0:no IRQ pending 1: IRQ pending	RW	0x0
1	-	Reserved	R	0x0
0	IREP	IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0x0

10.3.4.3 IRC_RX_CC

Infrared remote control customer code register.

Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:16	CCRCV	customer code received In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	RW	0x0

10.3.4.4 IRC_RX_KDC

Infrared remote control KEY data code register.

Offset=0x000c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data Note:If the key value is received, the register is updated. If repeat code is received, the register is not updated.	R	0x0

10.3.4.5 IRC_ANA_CTL

Infrared remote control analog control registers

Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:14	-	Reserved	RW	0x0
13:0	IRCAC	Infrared remote control analog control register	RW	0x0

10.3.4.6 IRC_TX_CTL

Infrared remote control register

Offset=0x0100

Bit(s)	Name	Description	R/W	Reset
31:17	-	Reserved	R	0x0
9	RELEASE	Tx release Write ‘1’ to release the KDC and CC code out Once transfer complete, hardware clear automatically.	RW	0x0
8	MOD_EN	Modulator enable 0: disable 1:enable	RW	0x0
7:5	MOD_FREQ	Carrier frequency 0: 30 KHz 1: 33 KHz 2: 36 KHz	RW	0x0

		3: 38 KHz 4: 40 KHz 5: 56 KHz		
4	RPC_TXEN	Repeat send tx enable 0 : disable 1 : enable	RW	0x0
3	IRE	IRC TX enable 0: disable 1:enable	RW	0x0
2	IIE	IRC TX IRQ enable 0:disable 1:enable	RW	0x0
1:0	ICMS	IRC TX coding mode select 00:9012 code 01:8bits NEC code 10:RC5 code 11: RC6 code	RW	0x0

10.3.4.7 IRC_TX_STA

Infrared remote status register

Offset=0x0104

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1	BUSY	IRC TX busy flag 0: IDEL 1:busy When CC and KDC was released out, busy would be 0. That means IRC_TX module can transmit.	RW	0x0
0	IP	IRQ pending 0:no IRQ pending 1: IRQ pending	RW	0x0

10.3.4.8 IRC_TX_CC

Infrared remote control customer code registers.

Offset=0x0108

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0

15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	RW	x

10.3.4.9 IRC_TX_KDC

Infrared remote control KEY data code register.

Offset=0x010C

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data	RW	0x0

10.4 KEY

10.4.1 Overview

- The debounce time can be configured
- Normal Row/Column scan mode:support up to 4*4+16=32 keys
- Matrix of IO Scan mode(lower power mode) support up to C_n^2+2n (n is number of IO): if n=7, 35 keys surported.

10.4.2 Function Description

10.4.2.1 Normal Row/Column Scan

Support up to 4*4+16=32 combine keys and the other 16 independent keys, the combine keys support multiple keys while pressing. it is recommended to switch to low-power the Matrix of IO Scan mode when entering standby mode in low-power multi-key pressing applications.

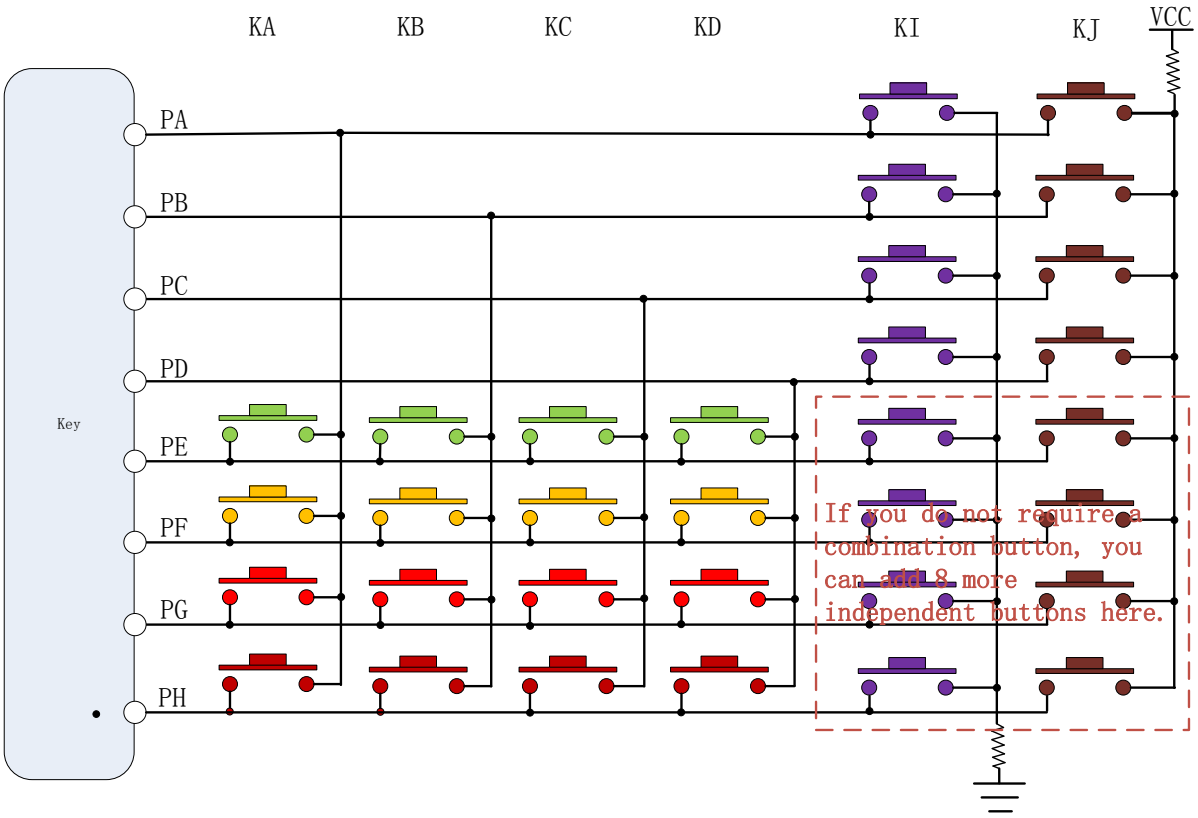


Figure 10-25 Row.Colum scan key

RAM List as the following table shows:

Table 10-2 ram list of key table in row/colum key mode

Register	bit	KEY ID							
KEY_INF00	7..0	KAPH	KAPG	KAPF	KAPE				
KEY_INF00	15..8	KBPH	KBPG	KBPF	KBPE				
KEY_INF00	23..16	KCPH	KCPG	KCPF	KCPE				
KEY_INF00	31..24	KDPH	KDPG	KDPF	KDPE				
KEY_INF02	15..8	KIPH	KIPG	KIPF	KIPE	KIPD	KIPC	KIPB	KIPA
KEY_INF02	7..0	KJPH	KJPG	KJPF	KJPE	KJPD	KJPC	KJPB	KJPA

10.4.2.2 Matrix of IO Scan

The lower power key mode, limited support 2 key pressed simultaneously in the mode. The maximum keys support in this mode： C_n^2 +2n(n=2,3,4,5,6,7,8)=44 keys, buy only up to C_n^2 +2n(n=7)=35 keys in deepsleep mode(only 35 keys can wakeup the system).

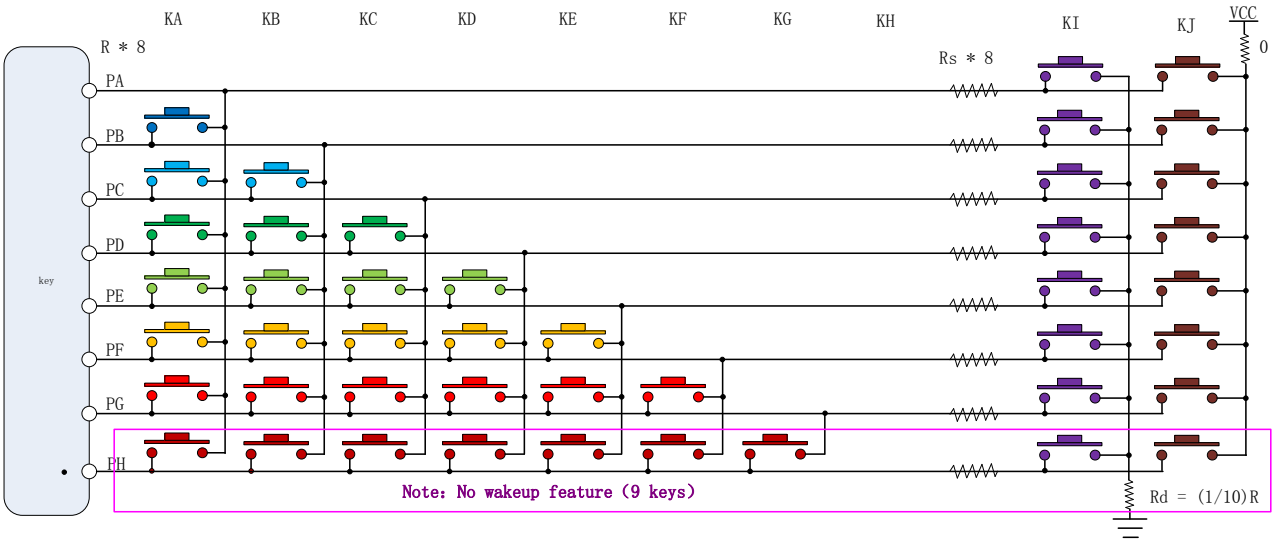


Figure 10-26 Maxtrix key

RAM List as the following table shows:

Table 10-3 ram list of key table in matrix mode

Regster	Bit	KEY ID							
KEY_INF00	7..0	KAPH	KAPG	KAPF	KAPE	KAPD	KAPC	KAPB	X
KEY_INF00	15..8	KBPH	KBPG	KBPF	KBPE	KBPD	KBPC	X	KBPA
KEY_INF00	23..16	KCPH	KCPG	KCPF	KCPE	KCPD	X	KCPB	KCPA
KEY_INF00	31..24	KDPH	KDPG	KDPF	KDPE	X	KDPC	KDPB	KDPA
KEY_INF01	7..0	KEPH	KEPG	KEPF	X	KEPD	KEPC	KEPB	KEPA
KEY_INF01	15..8	KFPH	KFPG	X	KFPE	KFPD	KFPC	KFPB	KFPA
KEY_INF01	23..16	KGPH	X	KGPF	KGPE	KGPD	KGPC	KGPB	KGPA
KEY_INF01	31..24	X	KHPG	KHPF	KHPE	KHPD	KHPC	KHPB	KHPA
KEY_INF02	15..8	KIPH	KIPG	KIPF	KIPE	KIPD	KIPC	KIPB	KIPA
KEY_INF02	7..0	KJPH	KJPG	KJPF	KJPE	KJPD	KJPC	KJPB	KJPA

Note：Refer to the key reference driver for the specific relationship

10.4.3 Register List

KEY Registers Address

Name	Physical Base Address
KEY	0x40018000

KEY Controller Registers

Offset	Register Name	Description
0x0000	Key_CTL	Key Control Register
0x0004	KEY_INFO0	Key Data Register0
0x0008	KEY_INFO1	Key Data Register1
0x000C	KEY_INFO2	Key Data Register2

10.4.4 Register Description

10.4.4.1 KEY_CTL

Key control Register

Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	x
23:21	WTS	Key Scan Wait Time Select. Key Scan Wait Time=WTS*32ms 000: 0ms 001: 32ms 010: 64ms 011: 96ms 100: 128ms 101: 160ms 110: 192ms 111: 224ms	RW	0x0
20	-	Reserved	R	x

19:17	DTS	Key Scan Debounce Time Select. 000: 10ms 001: 20ms 010: 40ms 011: 80ms 100: 160ms 101: 320ms 110: 640ms 111: other	RW	0x0
16	-	Reserved	R	x
15	IRP	Key Scan IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear the bit.	RW	0x0
14	IREN	Key Scan IRQ Enable. 0: Disable 1: Enable	RW	0x0
13	LFEN	Low frequency clock enable 0: Disable 1: Enable	RW	0x0
12	OTYP	Pull Up/Down Resistance show. 0: Pull Down Enable 1: Pull Up Enable	R	0x0
11:4	PENM	Pin [A:H] enable in all modes. 0: mask pin 1: enable pin	RW	0x0
3:2	-	Reserved	R	x
1	KMS	Key scan mode select: 0: Normal Row/Column Scan: 1: Matrix of IO Scan	RW	0x0
0	KEN	Key Scan Enable. 0: Disable 1: Enable	RW	0x0

10.4.4.2 KEY_INFO0

Key Data Register0

Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:24	KDPH~KDPA	PD output ‘L’be captured by PH~PA input Key value.	R	0x0

23:16	KCPH~KCPA	PC output ‘L’be captured by PH~PA input Key value.	R	0x0
15:8	KBPH~KBPA	PB output ‘L’be captured by PH~PA input Key value.	R	0x0
7:0	KAPH~KAPA	PA output ‘L’be captured by PH~PA input Key value.	R	0x0

10.4.4.3 KEY_INFO1

Key Data Register1
Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
31:24	KHPH~KHPA	PH output ‘L’be captured by PH~PA input Key value.	R	0x0
23:16	KGPH~KGPA	PG output ‘L’be captured by PH~PA input Key value.	R	0x0
15:8	KFPH~KFPA	PF output ‘L’be captured by PH~PA input Key value.	R	0x0
7:0	KEPH~KEPA	PE output ‘L’be captured by PH~PA input Key value.	R	0x0

10.4.4.4 KEY_INFO2

Key Data Register2
Offset = 0x000C

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	x
15:8	KIPH~KIPA	KI connected to the gnd，PH~PA input Key value.	R	0x0
7:0	KJPH~KJPA	KJ connected to the vdd，PH~PA input Key value.	R	0x0

10.5 PWM

10.5.1 Overview

- Support frequency and duty ratio adjustable
- Support 5 channel PWM channel, independent adjustable
- Support 3 modes: Fixed mode, Breath mode and programmable mode.
- The Fixed mode maximum supports 64K duty; duty can be configured arbitrarily by RAM, and can output PWM waveform with fixed frequency and duty cycle.
- The Breath mode supports the duty cycle gradient, enabling the breathing lamp to become brighter or darker.
- The programmable mode supports duty cycle in real time with RAM. Generate arbitrary waveform.

10.5.2 Function Description

10.5.2.1 Fixed Mode Timing

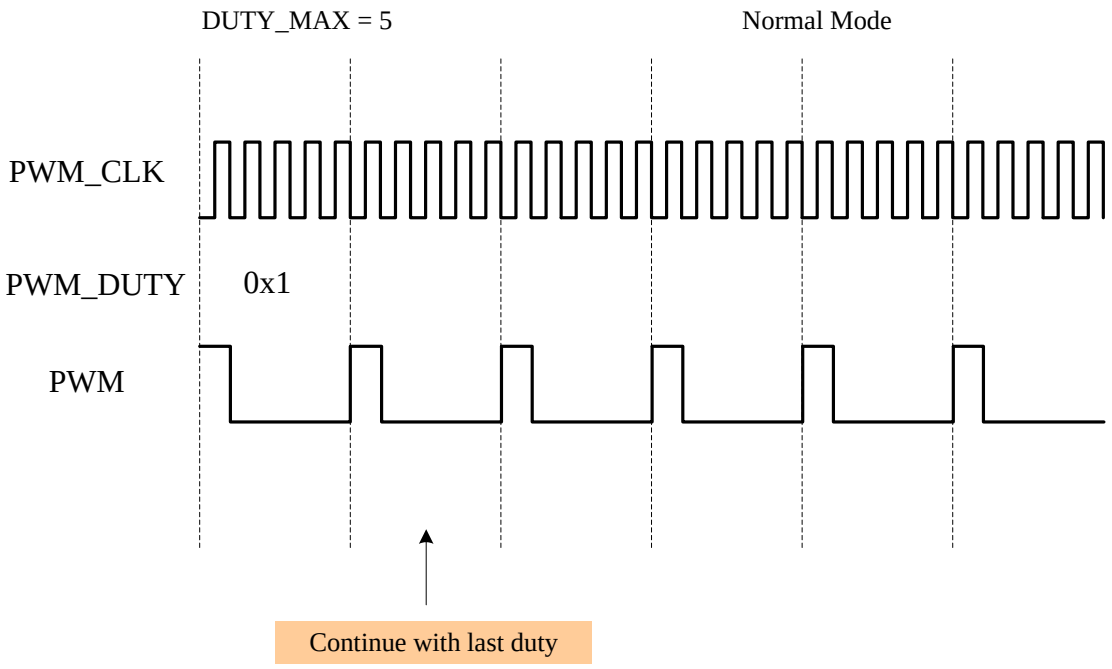


Figure 10-27 Fixed mode simple example

10.5.2.2 Breath Mode Timing

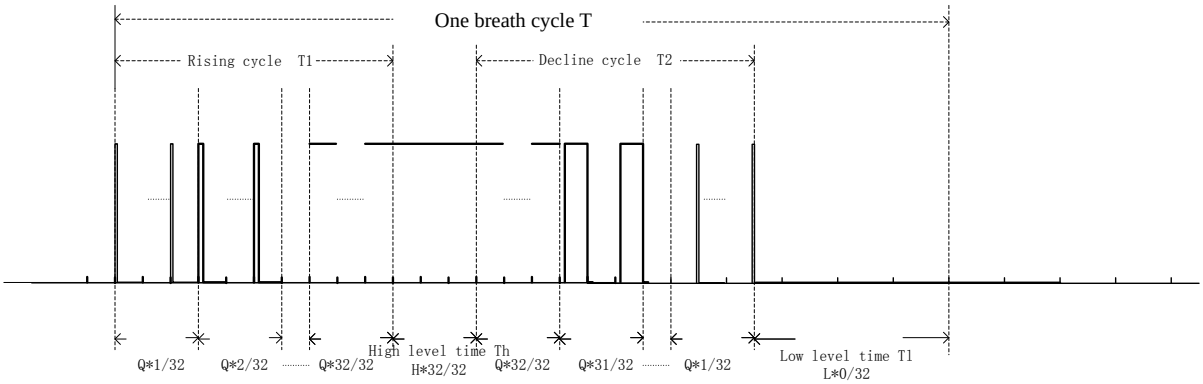


Figure 10-28 Breath mode simple example

10.5.2.3 Programmable Mode Timing

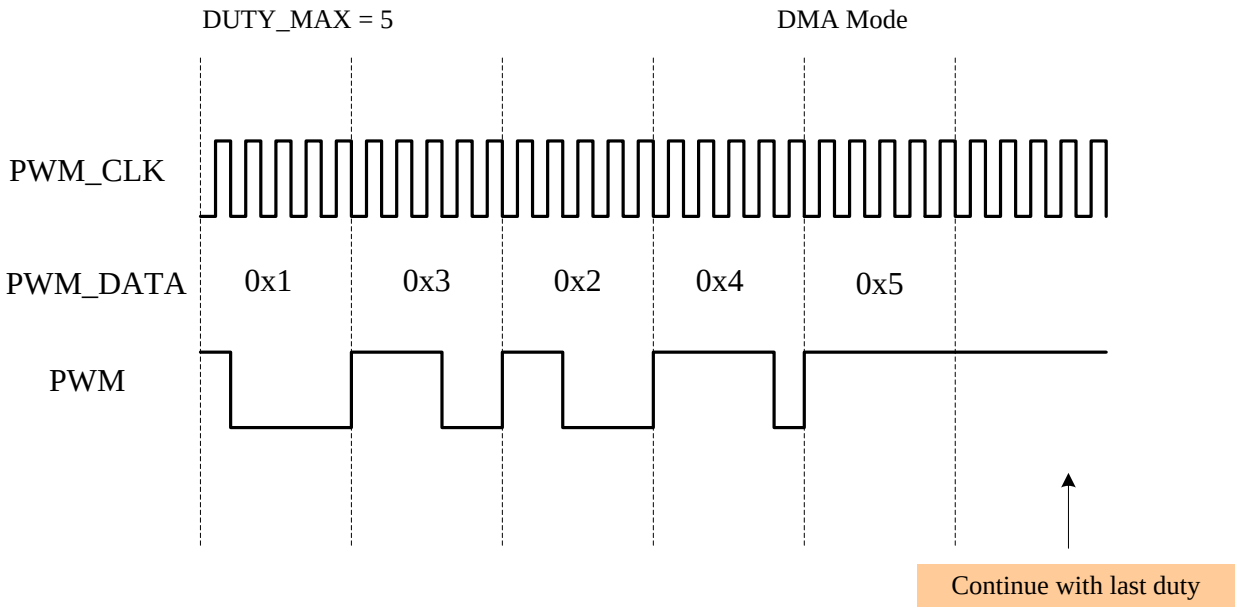


Figure 10-29 Programmable mode example used DMA transmission

PS：PWM_DUTY_MAX > (DMA_WAIT_CYCLE + 6) * (PWM_CLK / DMA_CLK)

10.5.3 Register List

PWM Controller Registers Address

Name	Physical Base Address
PWM	0x40017000

GPIO&MFP Controller Registers

Offset	Register Name	Description
0x0000	PWM0_CTL	PWM0 Output Control register
0x0004	PWM0_QHL	PWM0 breath mode Q/H/L register
0x0008	PWM0_DUTYMAX	PWM0 Duty Max register
0x000c	PWM0_DUTY	PWM0 Duty register
0x0010	PWM1_CTL	PWM1 Output Control register
0x0014	PWM1_QHL	PWM1 breath mode Q/H/L register
0x0018	PWM1_DUTYMAX	PWM1 Duty Max register
0x001c	PWM1_DUTY	PWM1 Duty register
0x0020	PWM2_CTL	PWM2 Output Control register
0x0024	PWM2_QHL	PWM2 breath mode Q/H/L register
0x0028	PWM2_DUTYMAX	PWM2 Duty Max register
0x002c	PWM2_DUTY	PWM2 Duty register
0x0030	PWM3_CTL	PWM3 Output Control register
0x0034	PWM3_QHL	PWM3 breath mode Q/H/L register
0x0038	PWM3_DUTYMAX	PWM3 Duty Max register
0x003c	PWM3_DUTY	PWM3 Duty register
0x0040	PWM4_CTL	PWM4 Output Control register
0x0044	PWM4_QHL	PWM4 breath mode Q/H/L register
0x0048	PWM4_DUTYMAX	PWM4 Duty Max register
0x004c	PWM4_DUTY	PWM4 Duty register
0x0050	PWM_DMACTL	PWM Enable Control register
0x0054	PWM_FIFODAT	PWM FIFO Data register
0x0058	PWM_FIFOSTA	PWM FIFO Status register

10.5.4 Register Description

10.5.4.1 PWM0_CTL

PWM0 Output Control Register
Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CH_EN	PWM0 Channel Enable 0: disable 1: enable	RW	0x0
2	POL_SEL	Polarity select: 0:PWM0 low voltage level active	RW	0x0

		1:PWM0 high voltage level active Only Active in fixed Mode		
1:0	MODE_SEL	PWM0 Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved	RW	0x0

10.5.4.2 PWM0_QHL

PWM0 Breath mode Q/H/L configuration Register
Offset = 0x0004

Bit(s)	Name	Description	R/W	Reset
31:18	-	Reserved	R	0x0
17:16	Q	Time of Every Duty =1/32 …32/32: Rising and DeclineTime:T2=(Q+1)*32*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0
15:8	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM\ Only Active in Breath Mode	RW	0x0
7:0	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0

Note: Rising and DeclineTime→High Level Time→Low Level Time, there will be a small time slot(t, one period of CMU_PWM ,not affect) in the gap between the 3 state transitions.

10.5.4.3 PWM0_DUTYMAX

PWM0 Duty Max Register
Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTYMAX	Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX DUTYMAX >= 0x1	RW	0x1

10.5.4.4 PWM0_DUTY

PWM0 Duty Register
Offset = 0x000c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTY	PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode	RW	0x0

10.5.4.5 PWM1_CTL

PWM1 Output Control Register
Offset = 0x0010

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CH_EN	PWM1 Channel Enable 0: disable 1: enable	RW	0x0
2	POL_SEL	Polarity select: 0:PWM1 low voltage level active 1:PWM1 high voltage level active Only Active in fixed Mode	RW	0x0
1:0	MODE_SEL	PWM1 Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved	RW	0x0

10.5.4.6 PWM1_QHL

PWM1 Breath mode Q/H/L configuration Register
Offset = 0x0014

Bit(s)	Name	Description	R/W	Reset
31:18	-	Reserved	R	0x0
17:16	Q	Time of Every Duty =1/32 …32/32: Rising and DeclineTime:T2=(Q+1)*32*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0

15:8	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM\ Only Active in Breath Mode	RW	0x0
7:0	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0

Note: Rising and DeclineTime→High Level Time→Low Level Time, there will be a small time slot(t, one period of CMU_PWM ,not affect) in the gap between the 3 state transitions.

10.5.4.7 PWM1_DUTYMAX

PWM1 Duty Max Register
Offset = 0x0018

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTYMAX	Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX DUTYMAX >= 0x1	RW	0x1

10.5.4.8 PWM1_DUTY

PWM1 Duty Register
Offset = 0x001c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTY	PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode	RW	0x0

10.5.4.9 PWM2_CTL

PWM2 Output Control Register
Offset = 0x0020

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CH_EN	PWM2 Channel Enable	RW	0x0

		0: disable 1: enable		
2	POL_SEL	Polarity select: 0:PWM2 low voltage level active 1:PWM2 high voltage level active Only Active in Normal Mode	RW	0x0
1:0	MODE_SEL	PWM2 Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved	RW	0x0

10.5.4.10 PWM2_QHL

PWM2 Breath mode Q/H/L configuration Register
Offset = 0x0024

Bit(s)	Name	Description	R/W	Reset
31:18	-	Reserved	R	0x0
17:16	Q	Time of Every Duty =1/32 …32/32: Rising and DeclineTime:T2=(Q+1)*32*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0
15:8	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM\ Only Active in Breath Mode	RW	0x0
7:0	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0

Note: Rising and DeclineTime→High Level Time→Low Level Time, there will be a small time slot(t, one period of CMU_PWM ,not affect) in the gap between the 3 state transitions.

10.5.4.11 PWM2_DUTYMAX

PWM2 Duty Max Register
Offset = 0x0028

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0

15:0	DUTYMAX	Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX DUTYMAX >= 0x1	RW	0x1

10.5.4.12 PWM2_DUTY

PWM2 Duty Register
Offset = 0x002c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTY	PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode	RW	0x0

10.5.4.13 PWM3_CTL

PWM3 Output Control Register
Offset = 0x0030

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CH_EN	PWM3 Channel Enable 0: disable 1: enable	RW	0x0
2	POL_SEL	Polarity select: 0:PWM3 low voltage level active 1:PWM3 high voltage level active Only Active in Normal Mode	RW	0x0
1:0	MODE_SEL	PWM3 Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved	RW	0x0

10.5.4.14 PWM3_QHL

PWM3 Breath mode Q/H/L configuration Register
Offset = 0x0034

Bit(s)	Name	Description	R/W	Reset

31:18	-	Reserved	R	0x0
17:16	Q	Time of Every Duty =1/32 …32/32: Rising and DeclineTime:T2=(Q+1)*32*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0
15:8	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM\ Only Active in Breath Mode	RW	0x0
7:0	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0

Note: Rising and DeclineTime→High Level Time→Low Level Time, there will be a small time slot(t, one period of CMU_PWM ,not affect) in the gap between the 3 state transitions.

10.5.4.15 PWM3_DUTYMAX

PWM3 Duty Max Register
Offset = 0x0038

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTYMAX	Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX DUTYMAX >= 0x1	RW	0x1

10.5.4.16 PWM3_DUTY

PWM3 Duty Register
Offset = 0x003c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTY	PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode	RW	0x0

10.5.4.17 PWM4_CTL

PWM4 Output Control Register

Offset = 0x0040

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CH_EN	PWM4 Channel Enable 0: disable 1: enable	RW	0x0
2	POL_SEL	Polarity select: 0:PWM4 low voltage level active 1:PWM4 high voltage level active Only Active in Normal Mode	RW	0x0
1:0	MODE_SEL	PWM4 Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved	RW	0x0

10.5.4.18 PWM4_QHL

PWM4 Breath mode Q/H/L configuration Register

Offset = 0x0044

Bit(s)	Name	Description	R/W	Reset
31:18	-	Reserved	R	0x0
17:16	Q	Time of Every Duty =1/32 …32/32: Rising and DeclineTime:T2=(Q+1)*32*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0
15:8	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM\ Only Active in Breath Mode	RW	0x0
7:0	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM Only Active in Breath Mode	RW	0x0

Note: Rising and DeclineTime→High Level Time→Low Level Time, there will be a small time slot(t, one period of CMU_PWM ,not affect) in the gap between the 3 state transitions.

10.5.4.19 PWM4_DUTYMAX

PWM4 Duty Max Register

Offset = 0x0048

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTYMAX	Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX DUTYMAX >= 0x1	RW	0x1

10.5.4.20 PWM4_DUTY

PWM4 Duty Register

Offset = 0x004c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	DUTY	PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode	RW	0x0

10.5.4.21 PWM_DMACTL

PWM Module Enable Register

Offset = 0x0050

Bit(s)	Name	Description	R/W	Reset
31:7	-	Reserved	R	0x0
6:4	DMA_SEL	000:PWM0 001:PWM1 010:PWM2 011:PWM3 100:PWM4 Other: Reserved	RW	0x0
3:1	-	Reserved	RW	0x0
0	START	PWM DMA START 0: disable 1: enable	RW	0x0

10.5.4.22 PWM_FIFODAT

PWM FIFO Data Register

Offset = 0x0054

Bit(s)	Name	Description	R/W	Reset

31:16	-	Reserved	R	0x0
15:0	DATA	DUTY DATA PWM DUDY = DUTY / DUTY_MAX Only Active in programmable Mode	R	0x0

Note: DUTY must be configured ≤ (DUTY_MUX), failing to do so may result in unpredictable behavior.

10.5.4.23 PWM_FIFOSTA

PWM FIFO Status Register

Offset = 0x0058

Bit(s)	Name	Description	R/W	Reset
31:5	-	Reserved	R	0x0
4:3	LEVEL	PWM FIFO level This field indicates pwm fifo empty level	R	0x2
2	EMPTY	PWM FIFO empty status: 0: not empty 1: empty	R	0x1
1	FULL	PWM FIFO full status: 0: not full 1: full	R	0x0
0	ERROR	PWM FIFO error status: 0: no error 1: error Writing 1 to the bit is clear	RW	0x0

11 GPIO/MFP

11.1 Overview

- Max support 30 IO, each IO can configure input and output port, which can output 0 or 1. It can also detect the level signal input by external circuit, and read 0 or 1 through internal registers.
- Every IO can configured wake up the system from standby mode
- Schmitt can be configured to open or close
- Built-in 15K upper pull resistance /1K pull resistance,could be selected
- The driving ability is adjustable. 4 levels

11.2 Function Description

A PAD can be configured muti-function by MFP_CTL, to pay attention to its priority relationship; the JTAG priority is the highest, and then the MFP function of each module.

11.2.1 IO Output

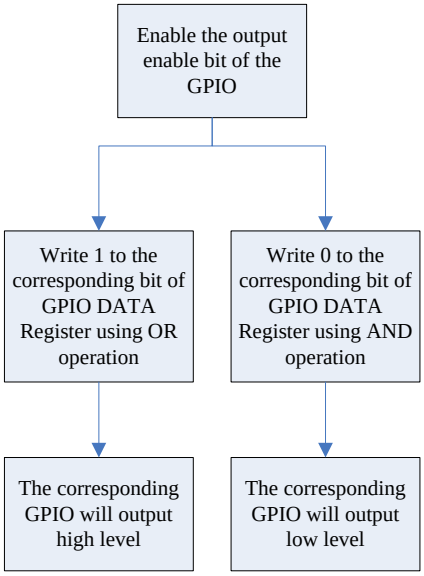


Figure 11-1 IO config output

11.2.2 IO Input

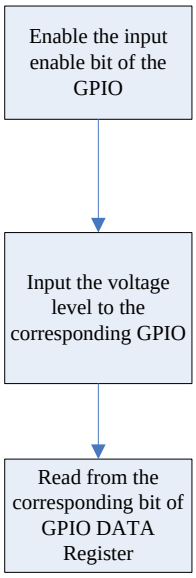


Figure 11-2 IO config input

11.3 Register List

IO_MFP Controller Registers Address

Name	Physical Base Address
IO_MFP	0x40016000

IO&MFP Controller Registers

Offset	Register Name	Description
0x0000	JTAG_EN	TJAG enable register
0x0004	IO0_CTL	IO0 Multiplexing Control Register
0x0008	IO1_CTL	IO1 Multiplexing Control Register
0x000C	IO2_CTL	IO2 Multiplexing Control Register
0x0010	IO3_CTL	IO3 Multiplexing Control Register
0x0014	IO4_CTL	IO4 Multiplexing Control Register
0x0018	IO5_CTL	IO5 Multiplexing Control Register
0x001C	IO6_CTL	IO6 Multiplexing Control Register
0x0020	IO7_CTL	IO7 Multiplexing Control Register
0x0024	IO8_CTL	IO8 Multiplexing Control Register
0x0028	IO9_CTL	IO9 Multiplexing Control Register
0x002C	IO10_CTL	IO10 Multiplexing Control Register
0x0030	IO11_CTL	IO11 Multiplexing Control Register
0x0034	IO12_CTL	IO12 Multiplexing Control Register
0x0038	IO13_CTL	IO13 Multiplexing Control Register

0x003C	IO14_CTL	IO14 Multiplexing Control Register
0x0040	IO15_CTL	IO15 Multiplexing Control Register
0x0044	IO16_CTL	IO16 Multiplexing Control Register
0x0048	IO17_CTL	IO17 Multiplexing Control Register
0x004C	IO18_CTL	IO18 Multiplexing Control Register
0x0050	IO19_CTL	IO19 Multiplexing Control Register
0x0054	IO20_CTL	IO20 Multiplexing Control Register
0x0058	IO21_CTL	IO21 Multiplexing Control Register
0x005C	IO22_CTL	IO22 Multiplexing Control Register
0x0060	IO23_CTL	IO23 Multiplexing Control Register
0x0064	IO24_CTL	IO24 Multiplexing Control Register
0x0068	IO25_CTL	IO25 Multiplexing Control Register
0x006C	IO26_CTL	IO26 Multiplexing Control Register
0x0070	IO27_CTL	IO27 Multiplexing Control Register
0x0074	IO28_CTL	IO28 Multiplexing Control Register
0x0078	IO29_CTL	IO29 Multiplexing Control Register
0x007C	MICIN_CTL	IO30 Multiplexing Control Register
0x0100	IO_ODAT	IO Output Data register
0x0108	IO_BSR	IO Output Data bit set register
0x0110	IO_BRR	IO Output Data bit reset register
0x0118	IO_IDAT	IO Input Data register
0x0120	IO_IRQ_PD	WAKE up source pending Register

11.4 Register Description

11.4.1 JTAG_EN

JTAG Enable Register

Offset=0x0000

Bit(s)	Name	Description	RW	Reset
31	JTAG_EN	JTAG function Enable. 0: disable 1: enable Control GPIO12(SWCLK) and GPIO13(SWDIO), and the JTAG function priority is the highest than other function.	RW	0x1
30:0	Reserved	Reserved	R	0x0

11.4.2 IO0_CTL

IO0 Multi-Function Control Register
Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0

8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO0 1：ADC0 2：PWM0 3：UART0_CTS 4：Reserved 5：Reserved 6：SPI1_MISO 7：TWI0_SCL 8：Reserved 9：Reserved 10：I2STX_MCLK 11：Reserved 12：Reserved 13：KEY0 14：IR_TX 15：IR_RX 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.3 IO1_CTL

IO1 Multi-Function Control Register

Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level	R/W	0x0

		001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved		
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO1 1：ADC1	R/W	0x0

		2：PWM1 3：UART0_RTS 4：Reserved 5：Reserved 6：SPI1_MOSI 7：TWI0_SDA 8：Reserved 9：Reserved 10：I2STX_BCLK 11：Reserved 12：Reserved 13：KEY1 14：IR_TX 15：IR_RX 16：Timer3_cap Others: Reserved		

11.4.4 IO2_CTL

IO2 Multi-Function Control Register
Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0

23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO2 1：ADC2 2：PWM2 3：UART0_RX 4：Reserved 5：Reserved 6：SPI1_SS 7：Reserved 8：Reserved 9：Reserved 10：I2STX_LRCLK 11：Reserved 12：Reserved 13：KEY2 14：Reserved 15：Reserved	R/W	0x0

		16：Timer2_cap Others: Reserved		

11.4.5 IO3_CTL

IO3 Multi-Function Control Register
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0

9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO3 1：ADC3 2：PWM3 3：UART0_TX 4：Reserved 5：Reserved 6：SPI1_CLK 7：Reserved 8：Reserved 9：Reserved 10：I2STX_DOUT 11：Reserved 12：Reserved 13：KEY3 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.6 IO4_CTL

IO4 Multi-Function Control Register

Offset=0x0014

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0

30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0

4:0	MFP	Multi-Function of IO 0：IO4 1：ADC4 2：PWM4 3：Reserved 4：UART1_TX 5：Reserved 6：Reserved 7：Reserved 8：TWI1_SCL 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY4 14：IR_TX 15：IR_RX 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.7 IO5_CTL

IO5 Multi-Function Control Register
Offset=0x0018

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable;	R/W	0x0

		Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.		
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO5 1：ADC5 2：PWM0 3：Reserved 4：UART1_RX 5：Reserved 6：Reserved 7：Reserved 8：TWI1_SDA 9：Reserved 10：Reserved 11：Reserved	R/W	0x0

		12：Reserved 13：KEY5 14：IR_TX 15：IR_RX 16：Timer3_cap 17：IR_RX_ANA Others: Reserved		

11.4.8 IO6_CTL

IO6 Multi-Function Control Register

Offset=0x001C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO:	RW	0x0

		0：disable 1：enable		
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO6 1：Reserved 2：PWM1 3：Reserved 4：Reserved 5：Reserved 6：SPI2_SS 7：TWI0_SCL 8：Reserved 9：IO_BT[0] 10：Reserved 11：I2SRX_MCLK 12：DMIC_CLK 13：Reserved 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.9 IO7_CTL

IO7 Multi-Function Control Register

Offset=0x0020

Bit(s)	Name	Description	R/W	Reset

31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable	R/W	0x0

		1: Enable		
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO7 1：Reserved 2：PWM2 3：Reserved 4：Reserved 5：Reserved 6：SPI2_CLK 7：TWI0_SDA 8：Reserved 9：IO_BT[1] 10：Reserved 11：I2SRX_BCLK 12：DMIC_DAT 13：KEY0 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.10 IO8_CTL

IO8 Multi-Function Control Register
Offset=0x0024

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0

24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO8 1：Reserved 2：PWM3 3：Reserved 4：UART1_CTS 5：Reserved 6：SPI2_SS	R/W	0x0

		7：TWI0_SCL 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY6 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved		

11.4.11 IO9_CTL

IO9 Multi-Function Control Register
Offset=0x0028

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3	R/W	0x1

		011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.		
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO9 1：Reserved 2：PWM4 3：Reserved 4：UART1_RTS 5：Reserved 6：SPI2_CLK 7：TWI0_SDA 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：Reserved 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.12 IO10_CTL

IO10 Multi-Function Control Register
Offset=0x002C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0

8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO10 1：Reserved 2：PWM0 3：UART0_TX 4：Reserved 5：UART2_TX 6：Reserved 7：Reserved 8：TWI1_SCL 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY1 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.13 IO11_CTL

IO11 Multi-Function Control Register

Offset=0x0030

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level	R/W	0x0

		001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved		
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO11 1：Reserved	R/W	0x0

		2：PWM1 3：UART0_RX 4：Reserved 5：UART2_RX 6：Reserved 7：Reserved 8：TWI1_SDA 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY2 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved		

11.4.14 IO12_CTL

IO12 Multi-Function Control Register
Offset=0x0034

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0

23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x1
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO12 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：Reserved 7：Reserved 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY5 14：IR_TX 15：IR_RX	R/W	0x0

		16：Timer2_cap Others: Reserved		

11.4.15 IO13_CTL

IO13 Multi-Function Control Register
Offset=0x0038

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0

9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x1
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO13 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：Reserved 7：Reserved 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY4 14：IR_TX 15：IR_RX 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.16 IO14_CTL

IO14 Multi-Function Control Register

Offset=0x003C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0

30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0

4:0	MFP	Multi-Function of IO 0：IO14 1：Reserved 2：PWM2 3：Reserved 4：Reserved 5：Reserved 6：SPI0_MISO 7：Reserved 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：KEY5 Others: Reserved	R/W	0x0

11.4.17 IO15_CTL

IO15 Multi-Function Control Register
Offset=0x0040

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0

23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO15 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：SPI0_SS Others: Reserved	R/W	0x0

11.4.18 IO16_CTL

IO16 Multi-Function Control Register

Offset=0x0044

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask.	R/W	0x0

		0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect		
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0

6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO16 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：SPI0_CLK Others: Reserved	R/W	0x0

11.4.19 IO17_CTL

IO17 Multi-Function Control Register
Offset=0x0048

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control	R/W	0x1

		000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.		
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO17 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：SPI0_MOSI Others: Reserved	R/W	0x0

11.4.20 IO18_CTL

IO18 Multi-Function Control Register

Offset=0x004C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module;	R/W	0x0

		1: Send interrupt to the INTC，when the IO trigger event is detect		
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable	R/W	0x0

		1: Enable		
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO18 1：Reserved 2：PWM3 3：Reserved 4：Reserved 5：UART2_RTS 6：SPI2_MOSI 7：TWI0_SCL 8：Reserved 9：Reserved 10：Reserved 11：I2SRX_LRCLK 12：DMIC_CLK 13：KEY6 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.21 IO19_CTL

IO19 Multi-Function Control Register

Offset=0x0050

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send	R/W	0x0

		IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.		
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO19 1：Reserved 2：PWM4 3：Reserved 4：Reserved 5：UART2_CTS 6：SPI2_MISO 7：TWI0_SDA 8：Reserved 9：Reserved	R/W	0x0

		10：Reserved 11：I2SRX_DIN 12：VMIC 13：Reserved 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved		

11.4.22 IO20_CTL

IO20 Multi-Function Control Register

Offset=0x0054

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1

11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO20 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved S 6：SPI0_IO2 7：Reserved 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：Reserved 14：IR_TX 15：IR_RX 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.23 IO21_CTL

IO21 Multi-Function Control Register
Offset=0x0058

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable.	R/W	0x0

		0: Disable 1: Enable		
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO21 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved S 6：SPI0_IO3 7：Reserved 8：Reserved 9：Reserved 10：Reserved 11：Reserved 12：Reserved 13：Reserved 14：IR_TX 15：IR_RX 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.24 IO22_CTL

IO22 Multi-Function Control Register
Offset=0x005C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge	R/W	0x0

		Others: Reserved		
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO22 1：Reserved 2：PWM0 3：Reserved 4：UART1_TX 5：Reserved	R/W	0x0

		6：SPI1_MISO 7：Reserved 8：Reserved 9：Reserved 10：I2STX_MCLK 11：Reserved 12：Reserved 13：KEY0 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved		

11.4.25 IO23_CTL

IO23 Multi-Function Control Register

Offset=0x0060

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2	R/W	0x1

		010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.		
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO23 1：Reserved 2：PWM1 3：Reserved 4：UART1_RX 5：Reserved 6：SPI1_MOSI 7：Reserved 8：Reserved 9：Reserved 10：I2STX_BCLK 11：Reserved 12：Reserved 13：KEY1 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.26 IO24_CTL

IO24 Multi-Function Control Register
Offset=0x0064

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0

8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO24 1：Reserved 2：PWM2 3：Reserved 4：Reserved 5：UART2_TX 6：SPI1_SS 7：Reserved 8：Reserved 9：Reserved 10：I2STX_LRCLK 11：Reserved 12：Reserved 13：KEY2 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.27 IO25_CTL

IO25 Multi-Function Control Register

Offset=0x0068

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level	R/W	0x0

		001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved		
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO25 1：Reserved	R/W	0x0

		2：PWM3 3：Reserved 4：Reserved 5：UART2_RX 6：SPI1_CLK 7：Reserved 8：Reserved 9：Reserved 10：I2STX_DOUT 11：Reserved 12：Reserved 13：KEY3 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved		

11.4.28 IO26_CTL

IO26 Multi-Function Control Register
Offset=0x006C

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC， when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0

23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO26 1：Reserved 2：PWM4 3：Reserved 4：Reserved 5：Reserved 6：SPI2_MISO 7：TWI0_SCL 8：Reserved 9：Reserved 10：Reserved 11：I2SRX_MCLK 12：Reserved 13：KEY4 14：Reserved 15：Reserved	R/W	0x0

		16：Timer2_cap Others: Reserved		

11.4.29 IO27_CTL

IO27 Multi-Function Control Register
Offset=0x0070

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC， when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is ‘1’.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0

9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO27 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：SPI2_MOSI 7：TWI0_SDA 8：Reserved 9：Reserved 10：Reserved 11：I2SRX_BCLK 12：Reserved 13：KEY5 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved	R/W	0x0

11.4.30 IO28_CTL

IO28 Multi-Function Control Register

Offset=0x0074

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC， when the IO trigger event is detect	R/W	0x0

30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.	R/W	0x0
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0

4:0	MFP	Multi-Function of IO 0：IO28 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：SPI2_SS 7：TWI1_SCL 8：Reserved 9：Reserved 10：Reserved 11：I2SRX_LRCLK 12：Reserved 13：KEY6 14：Reserved 15：Reserved 16：Timer2_cap Others: Reserved	R/W	0x0

11.4.31 IO29_CTL

IO29 Multi-Function Control Register
Offset=0x0078

Bit(s)	Name	Description	R/W	Reset
31	INT_MSK	IO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the IO trigger event is detect	R/W	0x0
30:28	-	Reserved	R	0x0
27:25	INT_TRIG_CTL	IO trigger mode 000: hight level 001: low level 010: rising edge 011: falling edge 100: dual edge Others: Reserved	R/W	0x0
24	IO_INTEN	IO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable;	R/W	0x0

		Generate IRQ pending when the IO trigger event is detect, and send IRQ to INTC when IO_INTC_MSK is '1'.		
23:14	-	Reserved	R	0x0
13:12	PADDRV	IO PAD Drive Control 000:Level 1 001:Level 2 010:Level 3 011:Level 4 Equivalent driving current: level 1:2.4mA, leve 2:4.8mA, level 3:7.2mA, level 4:9.5mA.	R/W	0x1
11	SMIT	PAD Schmitt enable bit of IO: 0：disable 1：enable	RW	0x0
10	IO1KPUEN	IO 1K PU Enable. 0: Disable 1: Enable	R/W	0x0
9	IO15KPDEN	IO 15K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	IO15KPUEN	IO 15K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	IOINEN	IO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	IOOUTEN	IO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4:0	MFP	Multi-Function of IO 0：IO29 1：Reserved 2：Reserved 3：Reserved 4：Reserved 5：Reserved 6：SPI2_CLK 7：TWI1_SDA 8：Reserved 9：Reserved 10：Reserved 11：I2SRX_DIN	R/W	0x0

		12：Reserved 13：Reserved 14：Reserved 15：Reserved 16：Timer3_cap Others: Reserved		

11.4.32 MICIN_CTL

MICIN Control Register
Offset=0x007C

Bit(s)	Name	Description	R/W	Reset
31:6	-	Reserved	R	0x0
5	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: MICIN	R/W	0x1
4:0	MFP	Multi-Function of IO 0：Reserved 1：DMIC_DAT Others: Reserved	R/W	0x0

11.4.33 IO_ODAT

IO Output Data register;
Offset = 0x0100

Bit(s)	Name	Description	RW	Reset
31:30	-	Reserved	R	0x0
29:0	IO_ODAT	IO[29:0] Output Data.	RW	0x0

11.4.34 IO_BSR

IO Output Data bit set register ;
Offset = 0x0108

Bit(s)	Name	Description	RW	Reset
31:30	-	Reserved	R	0x0
29:0	IO_BSR	IO[29:0] Output Data bit set register 0: there is no effect on the corresponding IO_ODAT position. 1: the corresponding IO_ODAT bit was set to 1.	RW	0x0

		And the position of the register itself is automatically cleared 0 after writing 1.		

11.4.35 IO_BRR

IO Output Data bit reset register;
Offset = 0x0110

Bit(s)	Name	Description	RW	Reset
31:30	-	Reserved	R	0x0
29:0	IO_BRR	IO[29:0] Output Data bit reset register 0: there is no effect on the corresponding IO_ODAT position. 1: the corresponding IO_ODAT bit was set to 0. And the position of the register itself is automatically cleared 0 after writing 1.	RW	0x0

11.4.36 IO_IDAT

IO Input Data register;
Offset = 0x0118

Bit(s)	Name	Description	RW	Reset
31:30	-	Reserved	R	0x0
29:0	IO_IDAT	IO[29:0] Input Data.	R	0x0

11.4.37 IO_IRQ_PD

IO WAKE up source pending Register
Offset=0x0120

Bit(s)	Name	Description	R/W	Reset
31:30	-	Reserved	R	0x0
29	IO29	IO29 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
28	IO28	IO28 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x

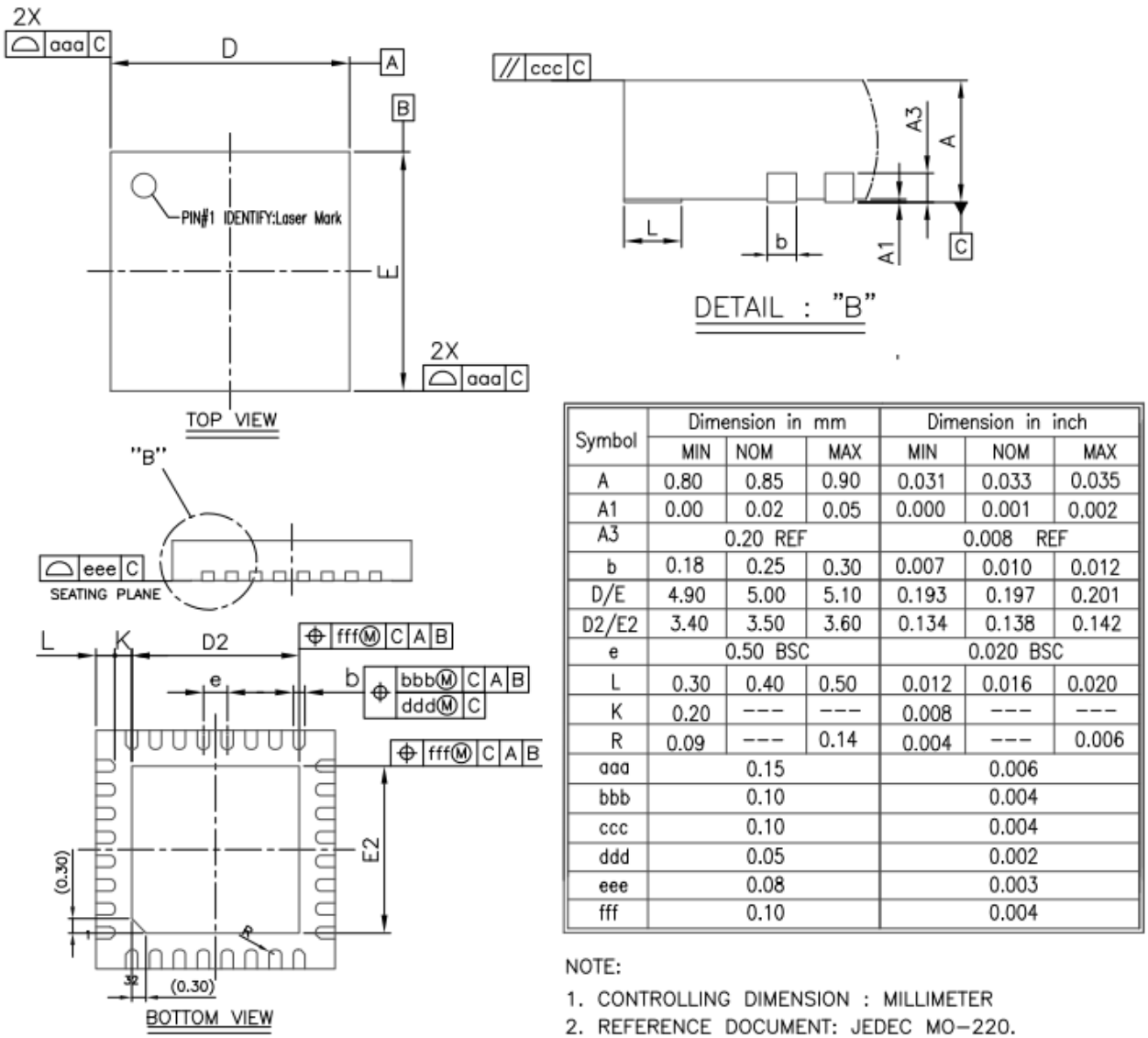
27	IO27	IO27 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
26	IO26	IO26IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
25	IO25	IO25IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
24	IO24	IO24IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
23	IO23	IO23 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
22	IO22	IO22 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
21	IO21	IO21 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
20	IO20	IO20 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
19	IO19	IO19 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
18	IO18	IO18 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
17	IO17	IO17 IRQ pending 0：No IRQ 1：IRQ	R/W	x

		Write 1 clear 0		
16	IO16	IO16IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
15	IO15	IO15IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
14	IO14	IO14IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
13	IO13	IO13 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
12	IO12	IO12 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
11	IO11	IO11 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
10	IO10	IO10 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
9	IO9	IO9 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
8	IO8	IO8 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
7	IO7	IO7 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
6	IO6	IO6 IRQ pending 0：No IRQ	R/W	x

		1：IRQ Write 1 clear 0		
5	IO5	IO5 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
4	IO4	IO4 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
3	IO3	IO3 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
2	IO2	IO2 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
1	IO1	IO1 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x
0	IO0	IO0 IRQ pending 0：No IRQ 1：IRQ Write 1 clear 0	R/W	x

12 Mechanical specifications

12.1 ATB1103 Package Drawing

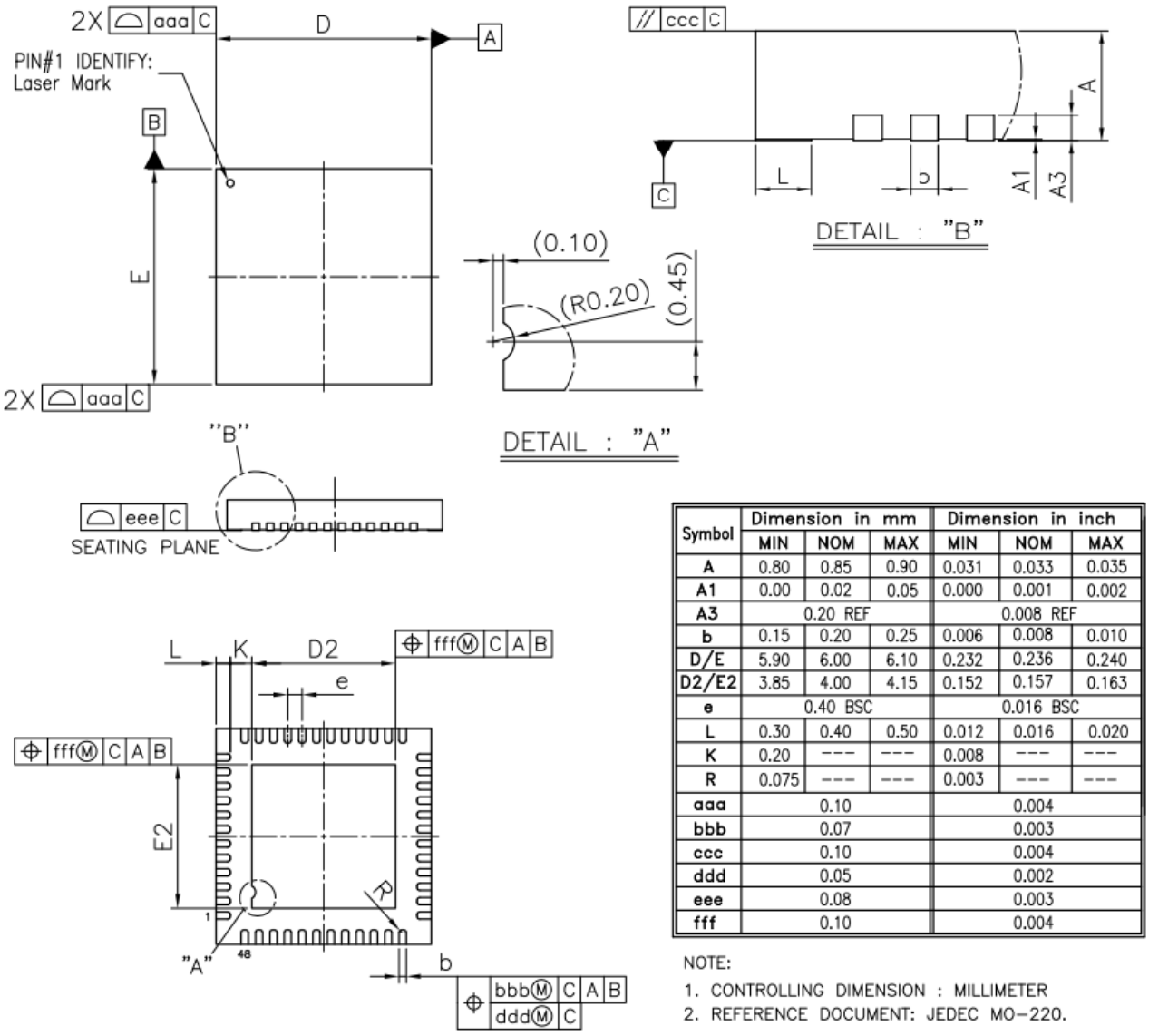


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.90	5.00	5.10	0.193	0.197	0.201
D2/E2	3.40	3.50	3.60	0.134	0.138	0.142
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.09	---	0.14	0.004	---	0.006
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 12-1 ATB1103 package drawing

12.2 ATB1109 Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	3.85	4.00	4.15	0.152	0.157	0.163
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 12-2 ATB1109 package drawing

13 Ordering information

Part Number	Package	Package Size	MOQ
ATB1103 (MCP 4Mbit wide-voltage Nor)	QFN32	5mm x 5mm x 0.75mm	4900
ATB1109	QFN48	6mm x 6mm x 0.75mm	4900

14 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Actions.Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from http://www.actions-semi.com

14.1 Reference design schematics of ATB1109 to 3Vmod

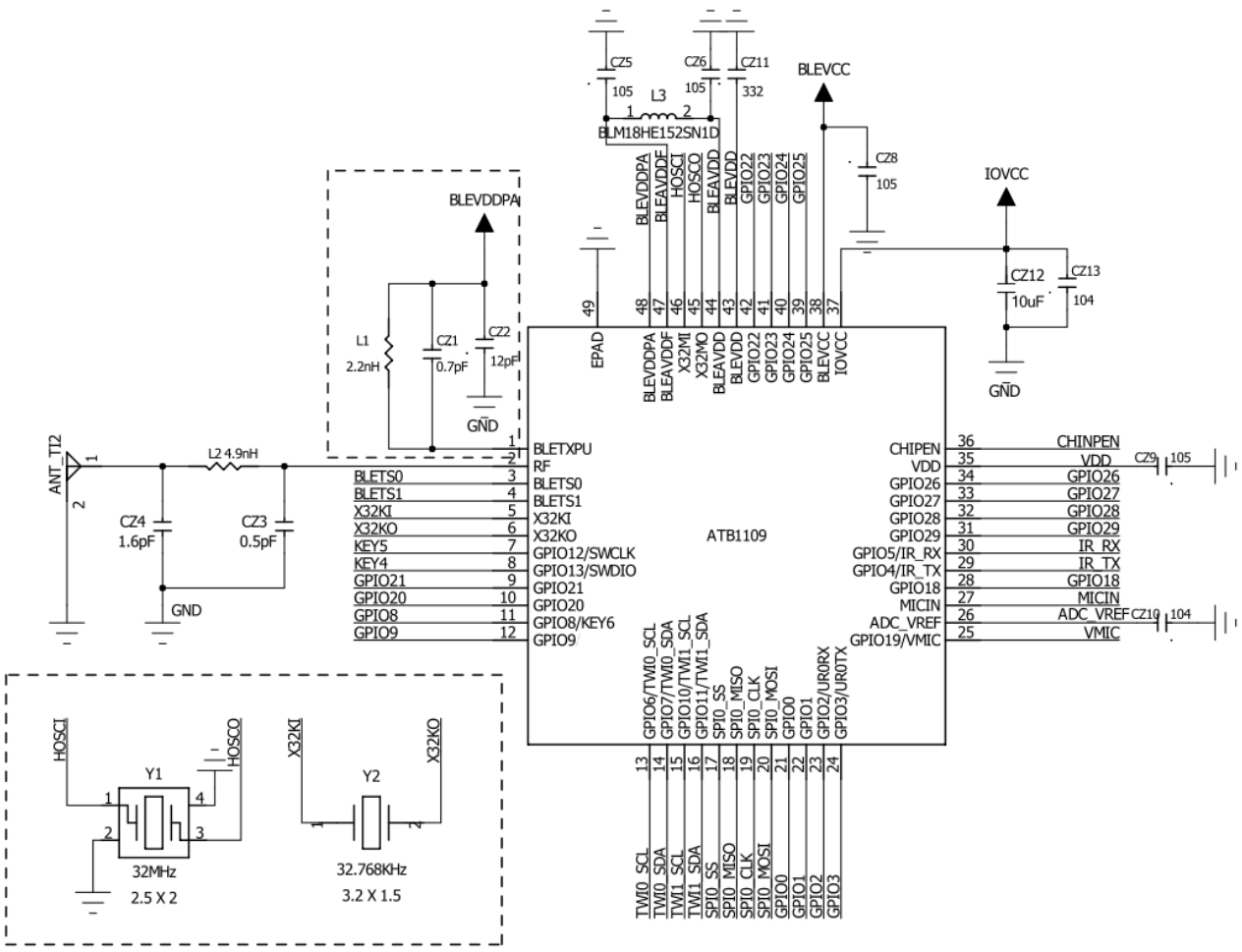


Figure 14-1 3 volt Schematic of ATB1109

Table 14-1 3 Volt External BOM of ATB1109

Designator	Quantity	Description
L1	1	2.2nH, 2.53A 22 MOHM, 0402
L2	1	4.9nH, 1.2A 71 MOHM SMD 0402
L3	1	FERRITE CHIP 1500 OHM 500MA 0603
CZ4	1	1.6pF CER 25V NP0 0402
CZ3	1	0.5pF CER 25V NP0 0402
CZ2	1	12pF CER 50V 2% NP0 0402

CZ1	1	0.7pF CER 25V NP0 0402
CZ11	1	3300Pf CER 25V NP0 0402
CZ10 CZ13	1	104 CER 25V 10% X5R 0402
CZ5 CZ6 CZ8 CZ9	4	1uF CER 25V 10% X5R 0603
CZ12	1	10uF CER 25V 10% X5R 0603
XTAL1	1	32 MHz +/-25ppm
XTAL2	1	32.768 KHz +/-100ppm

14.2 Reference design schematics of ATB1109 to 1Vmod

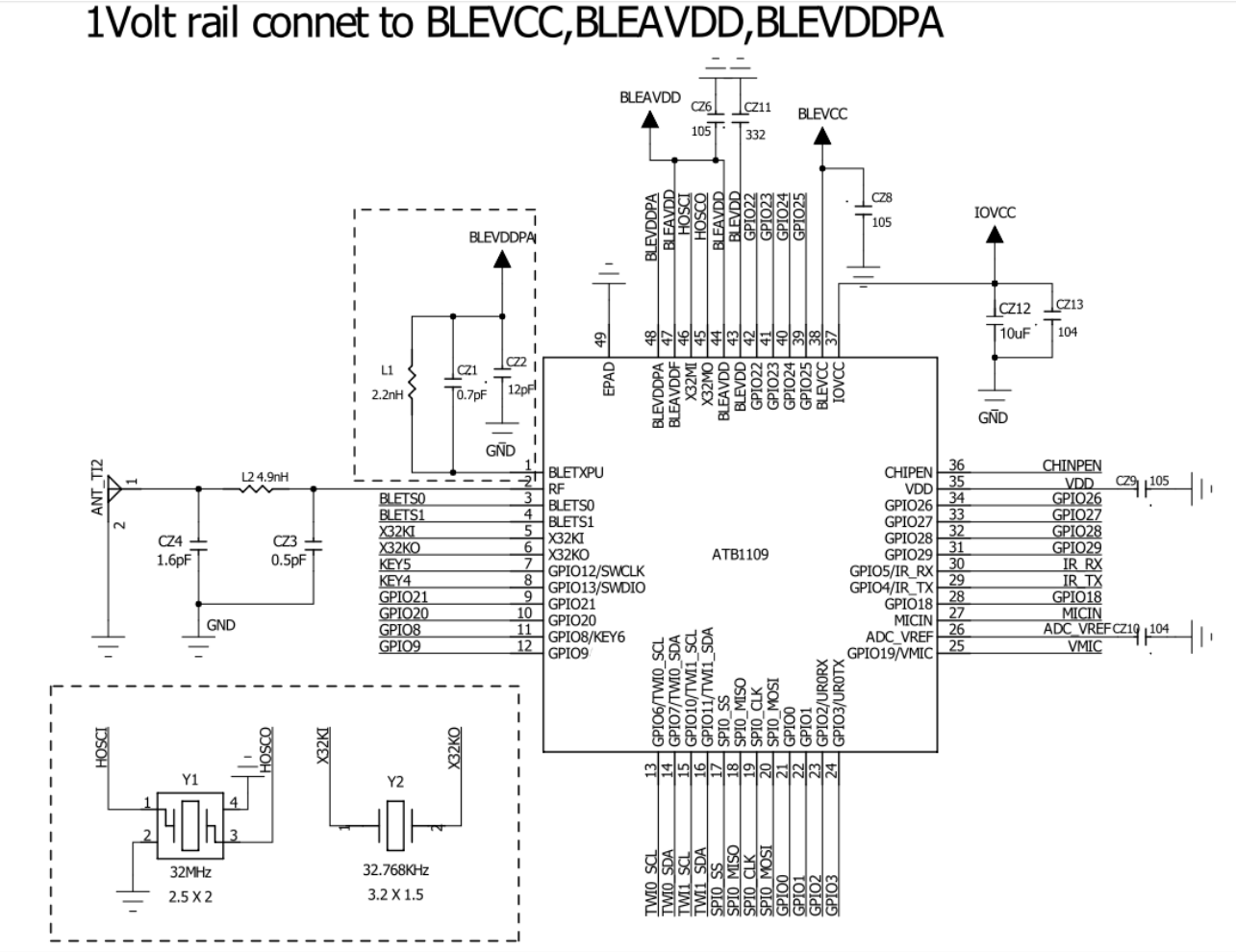


Figure 14-2 1 volt Schematic of ATB1109

Table 14-2 1 Volt External BOM of ATB1109

Designator	Quantity	Description
L1	1	2.2nH, 2.53A 22 MOHM, 0402
L2	1	4.9nH, 1.2A 71 MOHM SMD 0402
CZ4	1	1.6pF CER 25V NP0 0402
CZ3	1	0.5pF CER 25V NP0 0402
CZ2	1	12pF CER 50V 2% NP0 0402

CZ1	1	0.7pF CER 25V NP0 0402
CZ11	1	3300Pf CER 25V NP0 0402
CZ10 CZ13	1	104 CER 25V 10% X5R 0402
CZ6 CZ8 CZ9	3	1uF CER 25V 10% X5R 0603
CZ12	1	10uF CER 25V 10% X5R 0603
XTAL1	1	32 MHz +/-25ppm
XTAL2	1	32.768KHz +/-100ppm

14.3 Reference design schematics of ATB1103 to 3Vmod

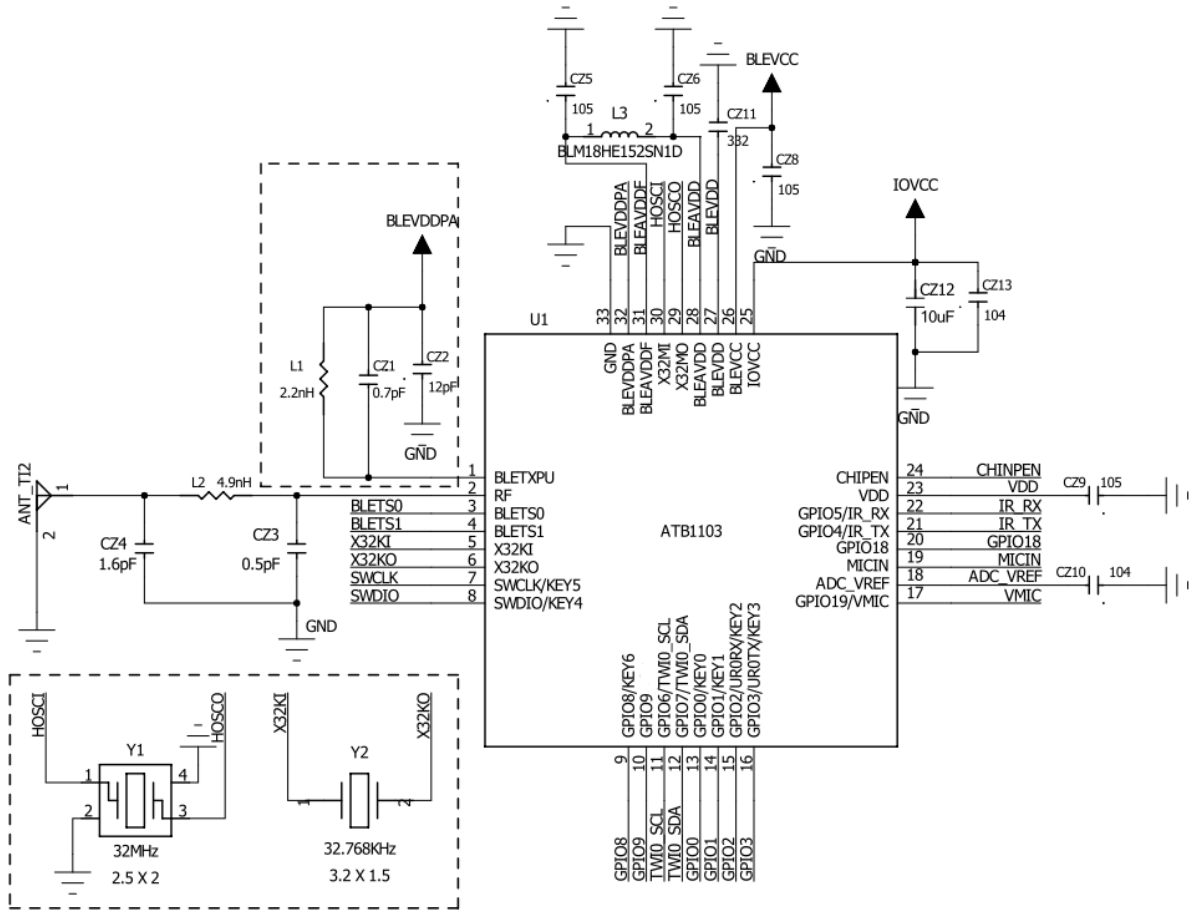


Figure 14-3 3 volt Schematic of ATB1103

Table 14-3 3 Volt External BOM of ATB1103

Designator	Quantity	Description
L1	1	2.2nH, 2.53A 22 MOHM, 0402
L2	1	4.9nH, 1.2A 71 MOHM SMD 0402
L3	1	FERRITE CHIP 1500 OHM 500MA 0603
CZ4	1	1.6pF CER 25V NP0 0402
CZ3	1	0.5pF CER 25V NP0 0402

CZ2	1	12pF CER 50V 2% NP0 0402
CZ1	1	0.7pF CER 25V NP0 0402
CZ11	1	3300Pf CER 25V NP0 0402
CZ10 CZ13	1	104 CER 25V 10% X5R 0402
CZ5 CZ6 CZ8 CZ9	4	1uF CER 25V 10% X5R 0603
CZ12	1	10uF CER 25V 10% X5R 0603
XTAL1	1	32 MHz +/-25ppm
XTAL2	1	32.768 KHz +/-100ppm

14.4 Reference design schematics of ATB1103 to 1Vmod

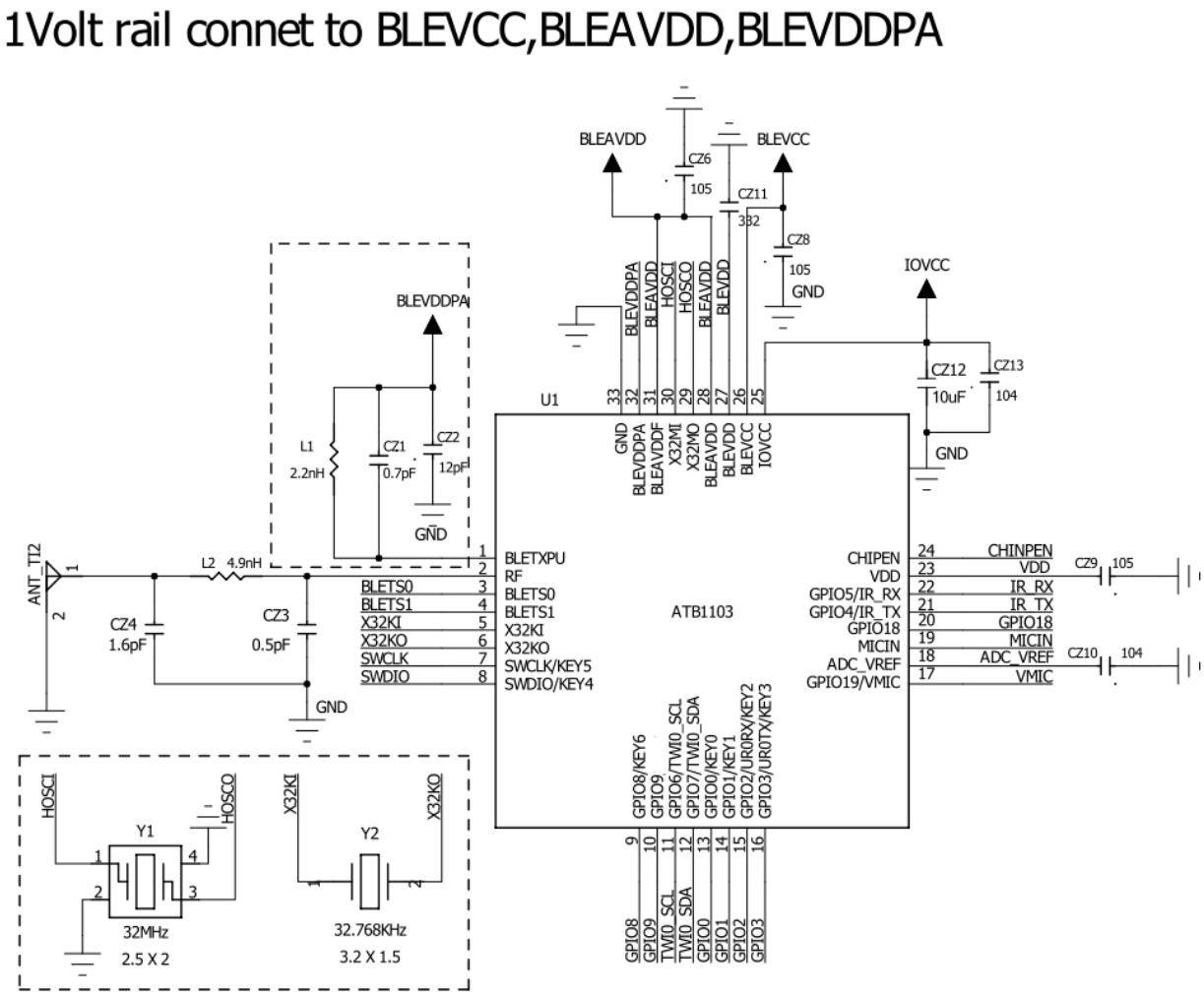


Figure 14-4 1 volt Schematic of ATB1103

Table 14-4 1 Volt External BOM of ATB1103

Designator	Quantity	Description
L1	1	2.2nH, 2.53A 22 MOHM, 0402
L2	1	4.9nH, 1.2A 71 MOHM SMD 0402
CZ4	1	1.6pF CER 25V NP0 0402

CZ3	1	0.5pF CER 25V NP0 0402
CZ2	1	12pF CER 50V 2% NP0 0402
CZ1	1	0.7pF CER 25V NP0 0402
CZ11	1	3300Pf CER 25V NP0 0402
CZ10 CZ13	1	104 CER 25V 10% X5R 0402
CZ6 CZ8 CZ9	3	1uF CER 25V 10% X5R 0603
CZ12	1	10uF CER 25V 10% X5R 0603
XTAL1	1	32 MHz +/-25ppm
XTAL2	1	32.769KHz +/-100ppm

14.5 Sensitive External RF Networks

14.5.1 BLETXPU Network

The BLETXPU network is the most sensitive external RF network in the BLE radio and is vital to the BLE transmitter passing FCC & ETSI emissions regulations. Therefore, this network is given preferential treatment in the reference design with all PCB design work starting with this network. The purpose of this network is to provide the DC feed point to the BLE PA power stage (i.e. into the BLETXPU pin) while filtering the transmitter harmonics. The key external components of the network are L1 and CZ1, and CZ2. The component's first-order function is for L1 and CZ1 to form a parallel resonator at the BLE TX operating frequency and for CZ1 and the BLETXPU pin's internal wirebond to form a series resonator at the TX 2 nd -harmonic. CZ2 acts as a RF-bypass at the TX operating frequency to provide a local AC-ground at the BLEVDDPA pin.

14.5.2 RF Network

The RF network is shared by the BLE radio's receiver and transmitter. This network serves two functions:
(1) to match the receiver and transmitter RF pin to 50Ohm , and
(2) to provide harmonic filtering of the transmitter output signal.
Because this matching network must match the TX PA to 50- Ohm while providing harmonic filtering, this circumstance becomes the limiting condition for the network. Matching a PA is much different than matching a receiver. The goal of the match is to provide specific impedance terminations at the fundamental, 2nd -harmonic, 3 rd -harmonic, etc. as seen by the PA's output device, and therefore, looking into the RF-pin with a VNA in receive mode usually isn't sufficient to meet all the criteria for the PA match. Hence, the RF network is the second most sensitive external network of the reference design and following the layout requirements of this network is very important.

14.5.3 BLEAVDD Network

The BLEAVDD network provides a SMPS ripple filter function. The ripple from the SMPS can degrade BLE

RF performance and is therefore filtered with CZ5, L3, and CZ6 components to reduce the ripple level. Component L3 is an inductive ferrite bead used for the broadband impedance frequency response provided by ferrite beads. All three components are 0603 geometry to keep their ESR's as low as possible.

14.6 PCB layout example and PCB guidelines

1. The key componentplace and route starts with the BLETXPU network with the goal to place the L1 and CZ1 components as close to the BLETXPU QFN pin as possible and minimize the PCB parasitic loop inductance of these components' routes. Thisgoal is achieved by minimizing the loop area A1 (shown in Figure "RF PCB layout example").

2. BLETXPU network is a harmonically rich network with a lot of the harmonic currents circulating to ground through CZ2 and this network can act like an "aggressor" to the RF network which is trying to reduce TX harmonic content.Particularly, the ground returns of the BLETXPU network (CZ2) and the RF network (CZ3 and CZ4) must be isolated as much as possible.

3. The CZ3 and CZ4 placement are on both sides of L2 to reduce EM coupling from BLETXPU/RF component terminals (i.e. A3 keep-out area) and are terminated with V2 and V3 structures. The V2 and V3 structuresare critical to lowering the effective via inductance and forcing the RFground currents down through the vias and into the dedicated ground plane. The V1 structure on CZ2 of the TXPU network and the CZ4-V3 structure must be isolated to prevent harmonically rich CZ2 currents from "bouncing" on the CZ4 ground terminal; hence, the A2 fill cut is made such that the RF-currents are forced through their respective via structures.

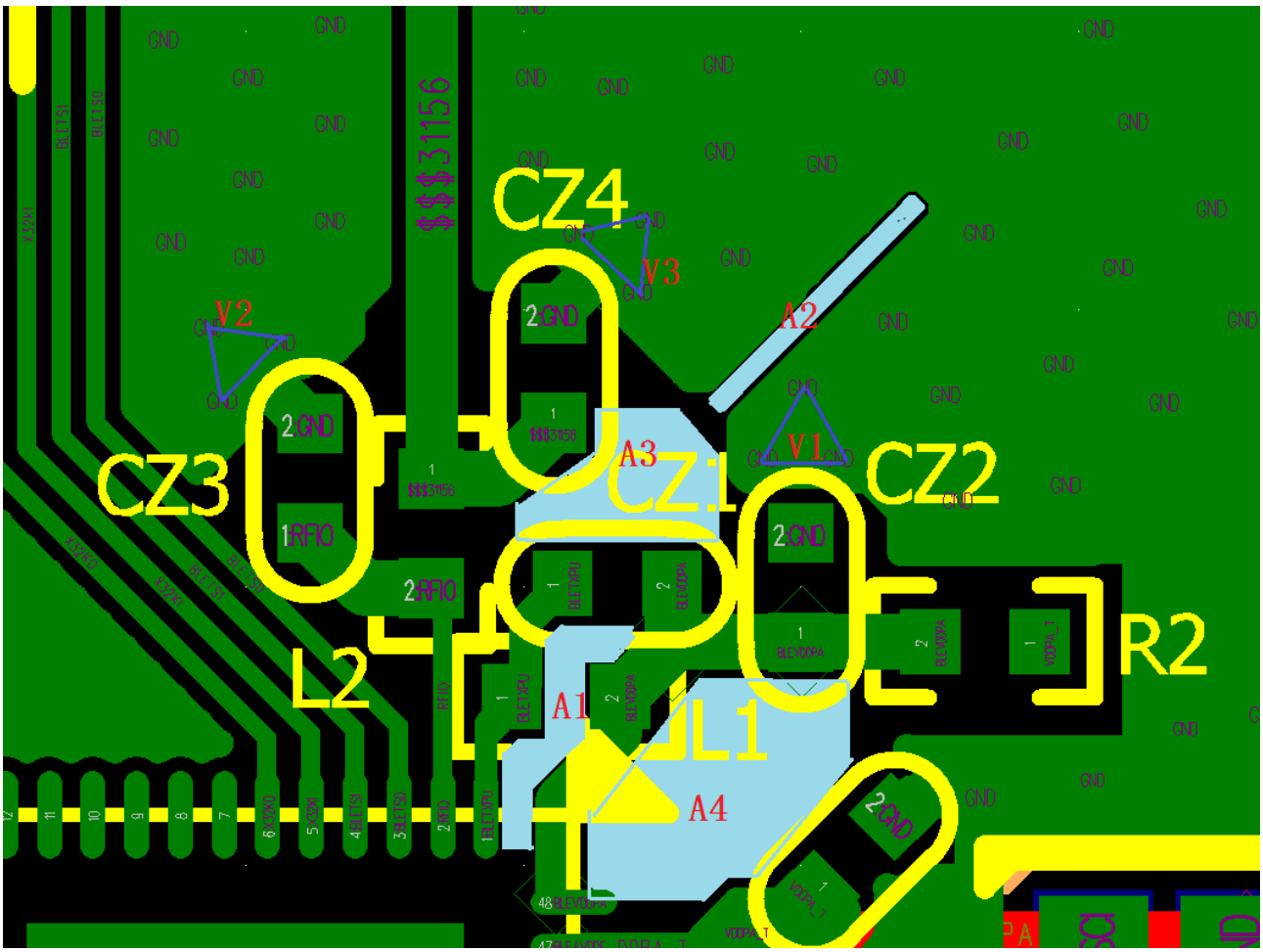


Figure 14-5 RF PCB layout example

15 Appendix

15.1 Acronym and Abbreviations

BLE: Bluetooth Low Energy
HCI: Host Controller Interface
ADC: Analog-to-Digital Converter
AMIC: Analog Micphone
DMIC: Digital Micphone
RF: Radio Frequency
GPIO: General Purpose Input Output
RoHS: Restriction of Hazardous Substances
SPI: Serial Peripheral Interface
TWI: Two-Wire Interface
UART: Universal Asynchronous Receiver Transmitter
dB: Decibel
DC: Direct Current
FIR: Fast Infrared
I2S: Inter-IC Sound
IR: Infrared
IRQ: Interrupt Request
LRADC: Low Resolution ADC
PA: Power Amplifier
PLL: Phase-Locked Loop
PMU: Power Management Unit
PWM: Pulse Width Modulation
RISC: Reduced Instruction Set Computing
RTC: Real-Time Clock
SOC: System on a Chip
SPEC: Specification
THD: Total Harmonic Distortion

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