



先进科技电子有限公司  
Advanced Technology Electronics CO., LTD.

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**ATE 7520**

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**PC POWER SUPPLY PWM SUPERVISOR**

**Data Sheet**

**REV: 1.0**

**April 19, 2007**



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# ATE7520

*Data Sheet Rev.1.0*

## GENERAL DESCRIPTION

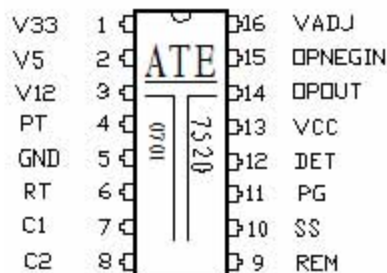
The ATE7520 is a pulse-width modulation (PWM) control circuit with complete protection circuits for used in the SMPS (Switched Mode Power Supply). It contains various functions, which are Over Voltage Protection, Under Voltage Protection, Power Good Output (PGO), Remote On/Off control and etc. It can minimize external components of switching power supply systems in personal computer.

Over Voltage Protection (OVP) monitors 3.3V, 5V, 12V and PT input voltage level. Under Voltage Protection (UVP) monitors 3.3V, 5V and 12V input voltage level. Power Good Output monitors the voltage level of power supply.

## FEATURES

- Complete PWM Control and Protection Circuitry
- Over Voltage Protection for 3.3V / 5V / 12V / PT
- Under Voltage Protection for 3.3V / 5V / 12V
- 280ms PG Time Delay
- Power Good Output is Open Drain Output
- PWM Control Output are Open Drain Output
- 280 mS Time Delay for UVP
- Remote ON/OFF function De-bounce Time
- Soft-Start function built-in
- 16-Pin Dual In-line Package

## PIN CONFIGURATION



Ordering Number	Package Type
ATE7520	DIP 16





## PIN DESCRIPTION

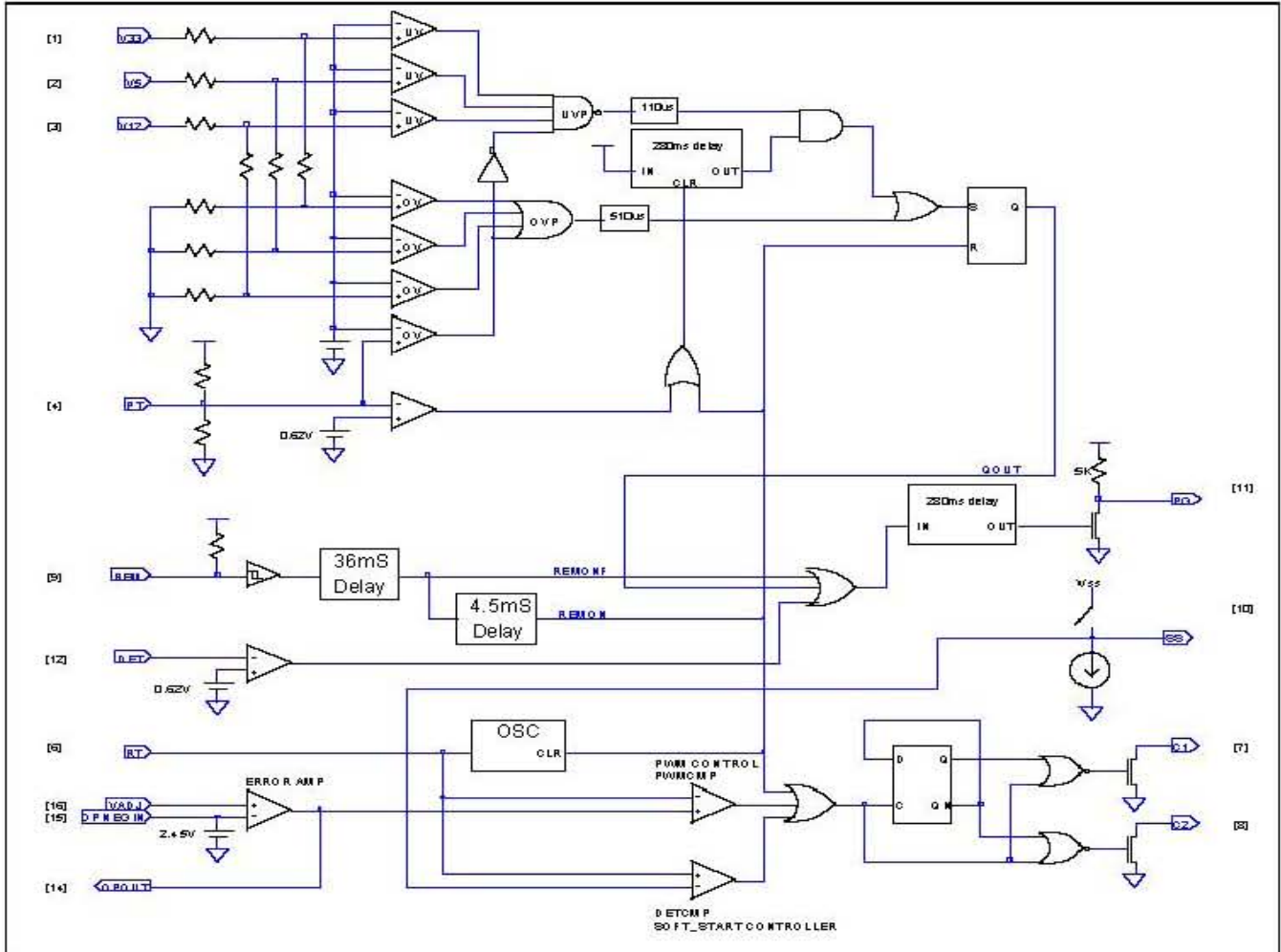
Pin No.	Pin Name	TYPE	FUNCTION
1	V33	I	OVP/UVP input FOR 3.3V.
2	V5	I	OVP/UVP input for 5V.
3	V12	I	OVP/UVP input for 12V.
4	PT	I	Extra OVP protection input.
5	GND	P	Ground.
6	RT	O	Oscillation frequency set by external resistor.
7	C1	O	PWM open drain output 1.
8	C2	O	PWM open drain output 2.
9	REM	I	Remote on/off input. REM="low" that means the main SMPS is turned-on. REM="high", the main SMPS is turned-off.
10	SS	O	Soft start function set by external capacitor.
11	PG	O	Power good signal. PG= "high" means "power good". PG= "low" means "power fail".
12	DET	I	Extra protection input.
13	VCC	P	Supply voltage.
14	OPOUT	O	OP compensation output.
15	OPNEGIN	I	OP compensation negative input.
16	VADJ	I	OP compensation positive input , feedback voltage sense input.

\*The difference between AT2005 (B) and ATE7520

ITEM	AT2005 (B)	ATE7520
Pin-6 (PWM frequency)	CT; external capacitor	RT; external resistor (ex. 120k $\Omega$ )
Pin-10	TPG; external capacitor (PG delay-time function)	SS; external capacitor (Soft-start function)
Soft-Start function	Set by internal circuit	Set by external capacitor (Pin-10:SS)



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS, VCC=5.5V

CHARACTERISTICS	SYMBOL	VALUE	Unit
Supply voltage	VCC	5.5	V
Drain output voltage	Vcc1, Vcc2	5.5	V
Drain output current	Icc1, Icc2	200	mA
Power dissipation	Pd	200	mW
Operating temperature	ToPr	-10 ~ +70	°C
Storage temperature	Tstg	-65 ~ +150	°C



# ATE 7520

## ELECTRICAL CHARACTERISTICS, $T_A=25^{\circ}\text{C}$ , $V_{CC}=5\text{V}$ ,

CHARACTERISTICS	SYMBOL	TEST CONDITION	Min.	Typ.	Max.	Unit
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### DEAD TIME CONTROL SECTION

INPUT THRESHOLD VOLTAGE	$V_{thdt}$	ZERO DUTY CYCLE	3.0	3.3	V
		MAX. DUTY CYCLE	0.1		

### ERROR AMP SECTION

CLOSE LOOP VOLTAGE GAIN		0.5V ~ 3.5V	65		dB	
CROSS OVER POINT		0dB	320		KHZ	
OPNEG BIAS VOLTAGE		OPNEG OPEN	2.38	2.45	2.52	V

### OUTPUT SECTION

OUTPUT SATURATION VOLTAGE	$V_{dssat}$	$I_d=200\text{mA}$	1.1	1.3	V
DRAIN OFF-STATE CURRENT	$I_{doff}$	$V_{cc}=V_d=V_s=0\text{V}$	2	10	$\mu\text{A}$
RISING TIME	$T_r$		100	200	ns
FALLING TIME	$T_f$		50	200	ns

### PROTECTION SECTION

OVER VOLTAGE PROTECTION (OVP)	$V_{33}$		3.8	4.1	4.3	V
	$V_5$		5.8	6.2	6.6	V
	$V_{12}$		4.41	4.64	4.90	V
	PT		1.2	1.25	1.3	V
UNDER VOLTAGE PROTECTION (UVP)	$V_{33}$		1.78	1.98	2.18	V
	$V_5$		2.70	3.00	3.30	V
	$V_{12}$		2.11	2.37	2.63	V
UVP DISABLE VOLTAGE	PT		0.55	0.62	0.68	V
UVP DELAY TIME	$T_{d.uvp}$		100	280	500	ms

### REMOTE ON/OFF SECTION

REM HIGH INPUT VOLTAGE	$V_{remh}$		2.0			V
REM LOW INPUT VOLTAGE	$V_{reml}$				0.8	V
REM PULL HIGH VOLTAGE	$V_{remo}$		2.0		5.25	V
REM DELAY TIME	$T_{rem}$		30	36	42	ms
REM OFF DELAY TIME	$T_{off}$		3.5	4.5	5.5	ms

### POWER GOOD SECTION

DETECTING INPUT VOLTAGE	$V_{det}$		0.55	0.62	0.68	V
PG OUTPUT PULL-UP RESISTOR	$R_{pup, pg}$			5		K $\Omega$



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PG OUTPUT LOAD RESISTOR	R <sub>pg</sub>		0.5	1	2	KΩ
PG DELAY TIME			150	280	350	ms
OUTPUT SATURATION VOLTAGE	V <sub>sat.pg</sub>	I <sub>pg</sub> =10mA		0.2	0.4	V

## SOFT START SECTION

SINK CURRENT OF SS	I <sub>ss.sink</sub>			13		uA
SOURCE CURRENT OF SS	I <sub>ss.source</sub>			700		uA

## TOTAL DEVICE

STANDBY SUPPLY CURRENT	I <sub>cc</sub>			10	20	mA
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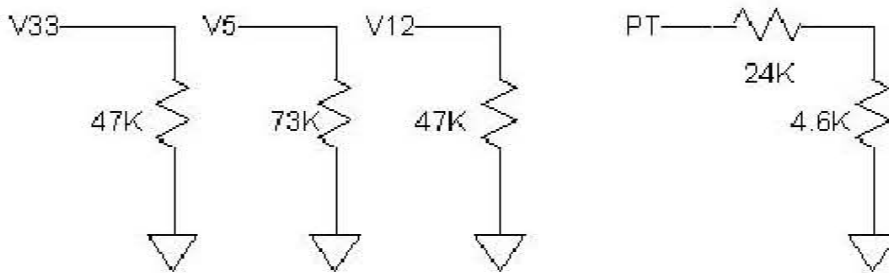
## OSCILLATION SECTION

OSCILLATION FREQUENCY	F <sub>osc</sub>	RT=120KΩ	50		70	KHZ
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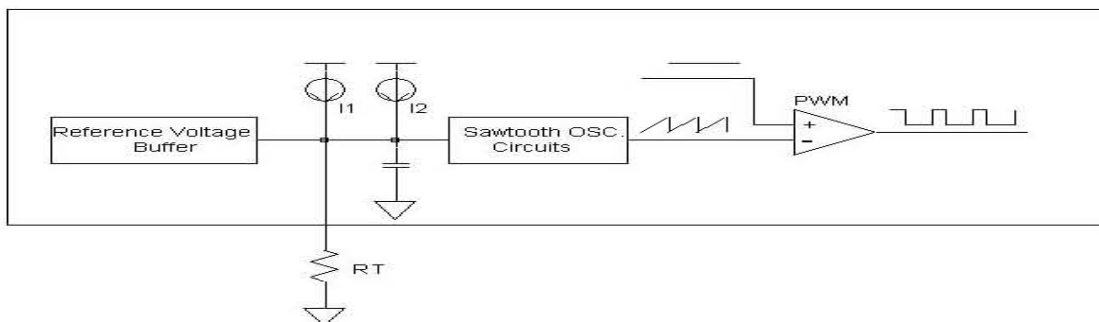
## APPLICATION NOTE

### 1. Input impedance:

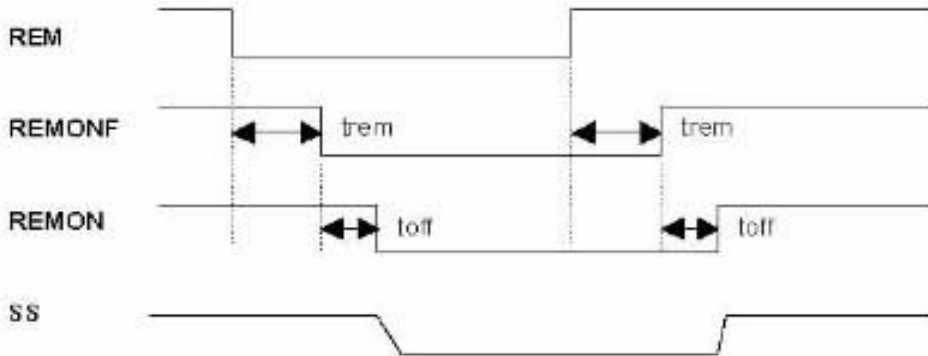
Pin No.	Pin Name	Input impedance
1	V33	47K Ω
2	V5	73K Ω
3	V12	47K Ω
4	PT	24 K Ω + 4.6 K Ω



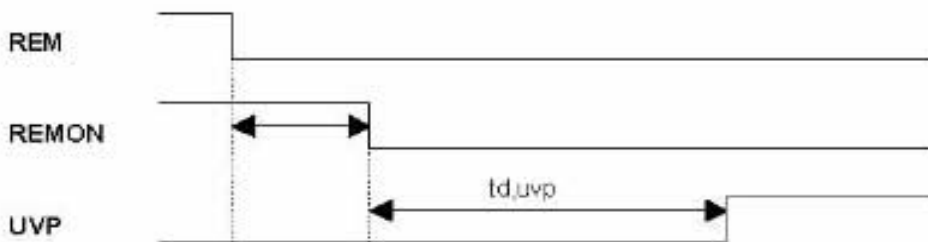
### 2. Sawtooth OSC. Function:



### 3. REMOTE ON/OFF :



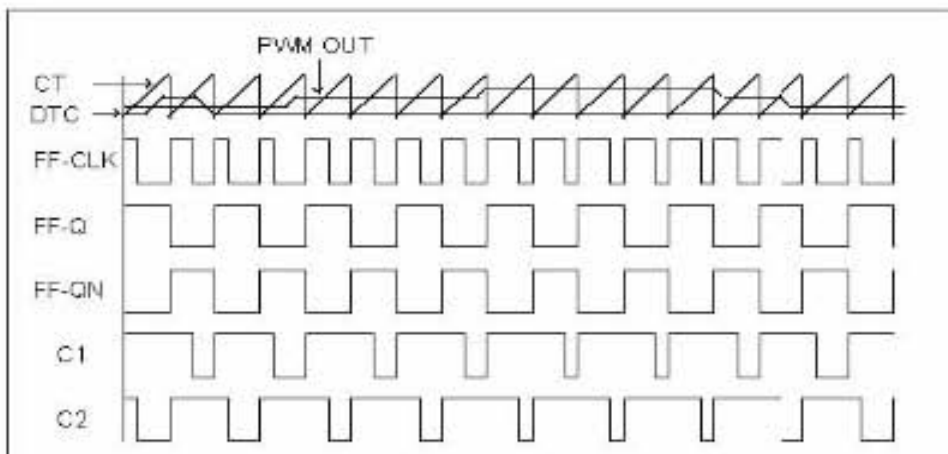
### 4. Under Voltage Protection Delay Time :



### 5. Pulse Width Modulation Block :

The output pulse width modulation is generated by comparison of the saw-tooth waveform from the capacitor  $C_T$  to the feedback of the voltage.

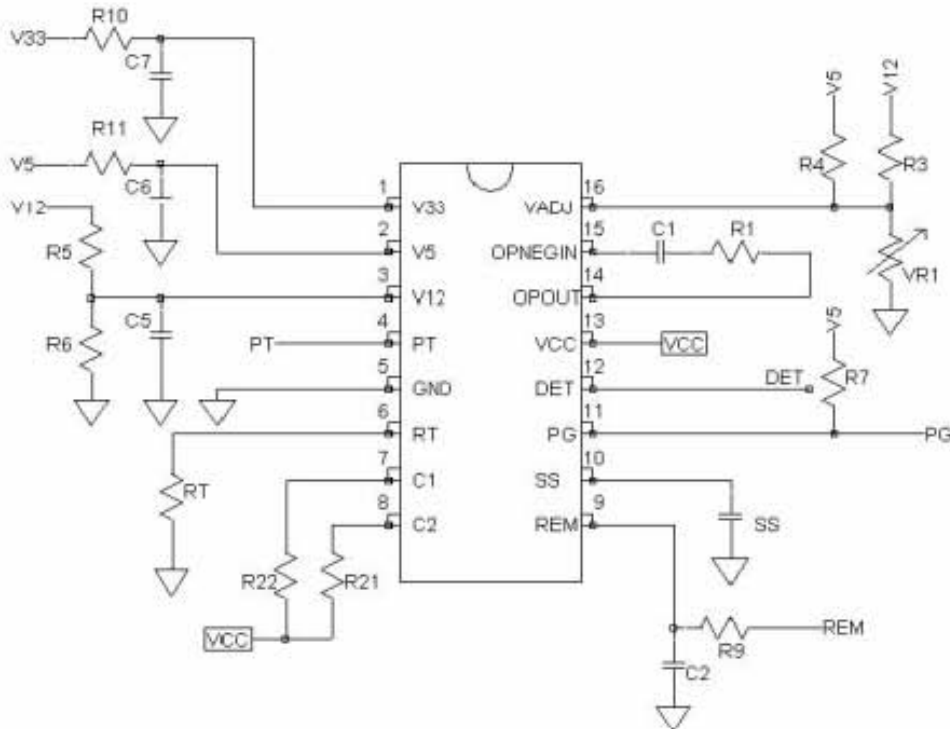
Therefore, an increase in feedback control signal amplitude cause a linear decrease of the output pulse width. Also, the SS(DTC and Soft-Start) limits the output pulse width. The timing diagram is shown as below:



### 6. The function of "PT":

This signal is prepared for extra OVP/OPP ( $V_{PT} > 1.25V$ ) or another Disable Under Voltage Protection function ( $V_{PT} < 0.62V$ )

### 7. Reference Application Circuit:

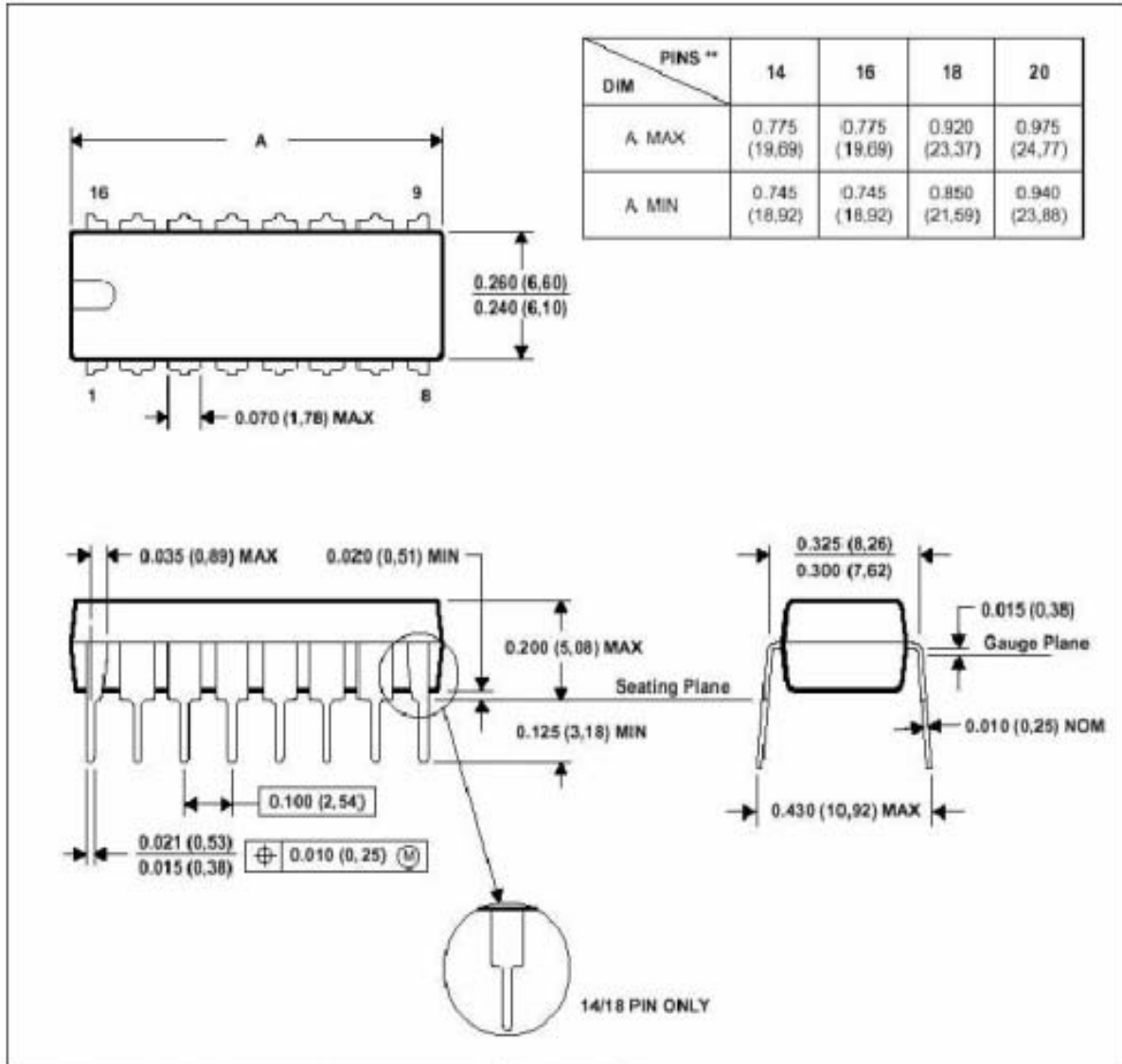


8. In some application power system, adding an external resistor (R9) could reduce the peak value spike from the environments to pin 9 (REM) and avoid pin 9 (REM) damaged by the external noise.



## MECHANICAL INFORMATION

### PLASTIC DUAL-IN-LINE PACKAGE



NOTE 1 : All linear dimensions are in inches ( millimeters ) .  
 NOTE 2 : This drawing is subject to change without notice.  
 NOTE 3 : Falls within JEDEC MS-001