Features

- SRAM based FPGA designed for Space use
  - 280K equivalent ASIC gates
  - Unlimited reprogrammability
  - SEE hardened cells (Configuration RAM, FreeRAM™, DFF, JTAG, I/O buffers)
  - No need for Triple Modular Redundancy (TMR)
- FreeRAM™:
  - 115200 Bits of Distributed RAM
  - 32x4 RAM blocks organization
  - Independent of Logic Cells
  - Single/Dual Port capability
  - Synchronous/Asynchronous capability
- Global Reset Option
- 8 Global Clocks and 4 Fast Clocks
- 8 LVDS transceivers and 8 LVDS receivers
- Cold sparing and PCI Compliant I/Os
  - 308 for 472pins MCGA package
  - 150 for 256pins MQFPF package
- Flexible Configuration modes
  - Master/Slave Capability
  - Serial/Parallel Capability
  - Check of the data during FPGA configuration
- Self Integrity Check (SIC) of the configuration during FPGA operation
- Performance
  - 100 MHz Internal Performance
  - 50MHz System Performance
  - 10ns 32X4 FreeRAM™ access time
- Operating range
  - Voltages
    - 1.65V to 1.95V (Core)
    - 3V to 3.6V (Clustered I/Os)
  - Temperature
    - - 55°C to +125°C
- Radiation Performance
  - Total Dose tested up to 300 krads (Si)
  - No single event latch-up below a LET of 80 MeV/mg/cm2
- ESD better than 2000V
- Quality Grades
  - QML-Q or V
  - ESCC
- Ceramic packages
  - 256pins MQFPF (150 I/Os, 8 LVDS Tx and 8 LVDS Rx)
  - 472pins MCGA (308 I/Os, 8 LVDS Tx and 8 LVDS Rx)
- Design Kit including
  - ATF280E and Configurator Samples
  - Evaluation Board
  - Software Design Tools
  - ISP Cable/Dongle

Rad Hard Reprogrammable FPGA

ATF280E

Advance Information

7750A–AERO–07/07

1. Description

The ATF280E is a radiation hardened SRAM-based reprogrammable FPGA. It has been especially designed for space application by implementing hardened cells and permanent self-integrity check mechanism.

The ATF280E is manufactured using the ATMEL 0.18µ rad-hard AT58KRHA CMOS technology.

The Atmel architecture is developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The ATF280E FPGA offers a patented distributed 10 ns SEU hardened SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool. They are organized by blocks of 32x4 bits. The ATF280E also embeds 8 global clocks, 4 high speed clocks, 8 LVDS Transmit channels, 8 LVDS Receive channels and a complete set of cold sparing programmable I/Os. The ATF280E I/Os are fully PCI-compliant.

The ATF280E is available in two space qualified packages. The MCGA472 package offers up to 324 I/Os for user application. The MQFP256 package is also proposed for application requiring less than 166 I/Os.

2. Pin Configuration

Table 2-1. ATF280E MCGA472 pin assignment

LEAD	Signal	Cluster	LEAD	Signal	Cluster	LEAD	Signal	Cluster
A3	VDD	1	**C7**	IO/D2	12	**E7**	IO/FCK4	12
A4	VSS	1	**C8**	IO/CHECKN	12	**E8**	IO	12
A5	IO	12	**C9**	IO	12	**E9**	IO	12
A6	VCC	12	**C10**	OLVDS6N	11	**E10**	VCC	12
A7	IO	12	**C11**	OLVDS6	11	**E11**	IO	12
A8	VCC	12	**C12**	ILVDS5N	11	**E12**	REFEast	11
A9	IO	12	**C13**	ILVDS5	11	**E13**	IO	10
A10	IO/D3	12	**C14**	IO	10	**E14**	IO	10
A11	VCCB	11	**C15**	VCC	10	**E15**	VCC	10
A12	IO	10	**C16**	IO	10	**E16**	IO/FCK3	10
A13	IO	10	**C17**	VCC	10	**E17**	IO/D5	10
A14	VCC	10	**C18**	IO	10	**E18**	IO/D6	10
A15	IO	10	**C19**	IO	10	**E19**	IO	9
A16	IO	10	**C20**	VSS	4	**E20**	IO	9
A17	IO	10	**C21**	VDD	5	**E21**	IO	9
A18	VCC	10	**C22**	VDD	6	**E22**	IO	9
A19	VSS	1	**D1**	VSS	6	**F1**	VCC	1
A20	VDD	3	**D2**	IO/A2/CS1N	1	**F2**	IO	1
B2	VSS	3	**D3**	IO	1	**F3**	IO	1
B3	VDD	3	**D4**	VCC	12	**F4**	IO/A0	1
B4	VCC	12	**D5**	IO	12	**F5**	IO	1
B5	IO	12	**D6**	CCLK	12	**F6**	IO	12
B6	IO	12	**D7**	IO	12	**F7**	IO/GCK6/CSOUTN	12
B7	IO	12	**D8**	IO	12	**F8**	IO/D0	12
B8	IO	12	**D9**	VCC	12	**F9**	IO	12
B9	IO	12	**D10**	IO	12	**F10**	IO	12
B10	OLVDS5N	11	**D11**	IO	12	**F11**	IO	12
B11	OLVDS5	11	**D12**	IO/D4	10	**F12**	VCC	10
B12	ILVDS6N	11	**D13**	VCC	10	**F13**	IO	10
B13	ILVDS6	11	**D14**	IO	10	**F14**	IO	10
B14	IO	10	**D15**	IO	10	**F15**	IO/D7	10
B15	IO/CS0	10	**D16**	IO	10	**F16**	DIODE	10
B16	VCC	10	**D17**	IO	10	**F17**	IO	9
B17	IO	10	**D18**	IO	10	**F18**	VCC	9
B18	IO	10	**D19**	VCC	9	**F19**	CON	9
B19	IO	10	**D20**	IO/D8	9	**F20**	VCC	9

LEAD	Signal	Cluster	LEAD	Signal	Cluster	LEAD	Signal	Cluster
B20	VDD	4	**D21**	VCC	9	**F21**	IO/D9	9
B21	VSS	3	**D22**	VSS	6	**F22**	IO	9
C1	VDD	4	**E1**	VCC	1	**G1**	IO	1
C2	VDD	4	**E2**	IO	1	**G2**	VCC	1
C3	VSS	4	**E3**	IO	1	**G3**	IO	1
C4	IO	12	**E4**	IO	1	**G4**	IO/A3	1
C5	IO	12	**E5**	IO	1	**G5**	IO	1
C6	IO	12	**E6**	VCC	12	**G6**	IO/GCK7/A1	1

Table 2-2. ATF280E MCGA472 pin assignment

LEAD	Signal	Cluster	LEAD	Signal	Cluster	LEAD	Signal	Cluster
G7	IO	12	**J8**	VCC	1	**L9**	IO	3
G8	VCC	12	**J9**	IO	1	**L10**	IO/A6	1
G9	IO/D1	12	**J10**	IO	12	**L11**	IO	1
G10	IO	12	**J11**	IO	12	**L12**	IO	10
G11	VCC	12	**J12**	IO	12	**L13**	IO	9
G12	IO	10	**J13**	IO	10	**L14**	IO	9
G13	IO	10	**J14**	IO/GCK5	10	**L15**	VCC	9
G14	IO	10	**J15**	VCC	9	**L16**	IO	9
G15	IO	10	**J16**	IO	9	**L17**	IO	9
G16	IO	9	**J17**	IO	9	**L18**	IO	9
G17	IO/GCK4	9	**J18**	IO	9	**L19**	IO	9
G18	IO/D10	9	**J19**	VCC	9	**L20**	OLVDS4	8
G19	IO	9	**J20**	IO/D11	9	**L21**	OLVDS3	8
G20	IO	9	**J21**	IO	9	**L22**	IO	7
G21	IO	9	**J22**	IO	9	**M1**	IO	1
G22	IO	9	**K1**	IO	1	**M2**	OLVDS7	2
H1	IO/A4	1	**K2**	ILVDS8	2	**M3**	OLVDS8	2
H2	IO	1	**K3**	ILVDS7	2	**M4**	VCCB	2
H3	IO	1	**K4**	VCC	1	**M5**	IO	3
H4	IO	1	**K5**	IO	1	**M6**	IO	3
H5	VCC	1	**K6**	VCC	1	**M7**	IO	3
H6	IO	1	**K7**	IO	1	**M8**	IO	3
H7	IO	1	**K8**	IO	1	**M9**	IO	3
H8	VCC	1	**K9**	IO	1	**M10**	IO	3
H9	VCC	12	**K10**	TCK	1	**M11**	IO	4
H10	IO	12	**K11**	IO	12	**M12**	IO/D14	7
H11	IO	12	**K12**	IO	10	**M13**	IO	7
H12	IO	12	**K13**	RESETN	10	**M14**	IO/D12	9
H13	IO	10	**K14**	IO	9	**M15**	VCCB	8
H14	VCC	10	**K15**	IO	9	**M16**	IO/D13	7
H15	VCC	10	**K16**	VCC	9	**M17**	IO	7
H16	VCC	9	**K17**	IO	9	**M18**	REFSouth	8
H17	IO	9	**K18**	VCC	9	**M19**	VCC	7
H18	IO	9	**K19**	IO	9	**M20**	ILVDS3N	8
H19	IO	9	**K20**	OLVDS4N	8	**M21**	ILVDS4N	8
H20	IO	9	**K21**	OLVDS3N	8	**M22**	IO	7
H21	IO	9	**K22**	IO	9	**N1**	IO	3
H22	IO	9	**L1**	IO/A7	1	**N2**	OLVDS7N	2

LEAD	Signal	Cluster	LEAD	Signal	Cluster	LEAD	Signal	Cluster
J1	IO	1	**L2**	ILVDS8N	2	**N3**	OLVDS8N	2
J2	IO	1	**L3**	ILVDS7N	2	**N4**	IO	3
J3	IO	1	**L4**	VCC	1	**N5**	IO/A9	3
J4	IO/A5	1	**L5**	REFNorth	2	**N6**	IO	3
J5	IO	1	**L6**	IO	1	**N7**	VCC	3
J6	VCC	1	**L7**	IO	1	**N8**	IO/A12	3
J7	IO	1	**L8**	IO/A8	3	**N9**	IO	3

Table 2-3. ATF280E MCGA472 pin assignment

LEAD	Signal	Cluster	LEAD	Signal	Cluster	LEAD	Signal	Cluster
N10	TMS	4	**R10**	IO	4	**U10**	VCC	4
N11	IO	4	**R11**	VCCB	5	**U11**	IO	4
N12	IO	6	**R12**	VCC	6	**U12**	IO	6
N13	M1	7	**R13**	IO	6	**U13**	IO	6
N14	IO	7	**R14**	VCC	6	**U14**	IO	6
N15	IO	7	**R15**	VCC	7	**U15**	IO	6
N16	IO	7	**R16**	IO	7	**U16**	IO/GCK2	6
N17	VCC	7	**R17**	IO	7	**U17**	IO	6
N18	IO	7	**R18**	VCC	7	**U18**	IO	7
N19	VCC	7	**R19**	IO	7	**U19**	IO	7
N20	ILVDS3	8	**R20**	IO	7	**U20**	IO	7
N21	ILVDS4	8	**R21**	IO	7	**U21**	IO/D15	7
N22	IO	7	**R22**	IO	7	**U22**	VCC	7
P1	VCC	3	**T1**	IO/A11	3	**V1**	IO	3
P2	IO	3	**T2**	IO	3	**V2**	IO	3
P3	IO	3	**T3**	IO	3	**V3**	IO	3
P4	VCC	3	**T4**	IO	3	**V4**	IO	3
P5	VCC	3	**T5**	IO	3	**V5**	IO	4
P6	IO	3	**T6**	TDO	3	**V6**	IO	4
P7	IO/A13	3	**T7**	IO/A14	3	**V7**	IO/A19	4
P8	VCC	3	**T8**	IO	4	**V8**	VCC	4
P9	IO/GCK1/A16	4	**T9**	IO	4	**V9**	VCC	4
P10	IO	4	**T10**	IO	4	**V10**	IO	4
P11	IO	6	**T11**	IO/A20	4	**V11**	REFWest	5
P12	IO	6	**T12**	IO	6	**V12**	IO	6
P13	IO	6	**T13**	VCC	6	**V13**	IO	6
P14	IO/GCK3	7	**T14**	IO	6	**V14**	VCC	6
P15	VCC	7	**T15**	VCC	6	**V15**	IO	6
P16	IO	7	**T16**	IO	6	**V16**	IO/A22	6
P17	VCC	7	**T17**	M2	7	**V17**	VCC	6
P18	IO	7	**T18**	IO/INIT	7	**V18**	IO	7
P19	IO	7	**T19**	IO	7	**V19**	IO	7
P20	IO	7	**T20**	IO	7	**V20**	IO	7
P21	IO	7	**T21**	VCC	7	**V21**	IO	7
P22	IO	7	**T22**	IO	7	**V22**	VCC	7
R1	IO	3	**U1**	IO	3	**W1**	VSS	7
R2	IO	3	**U2**	IO	3	**W2**	VCC	3
R3	IO	3	**U3**	VCC	3	**W3**	IO	3

LEAD	Signal	Cluster	LEAD	Signal	Cluster	LEAD	Signal	Cluster
R4	IO	3	**U4**	TDI	3	**W4**	VCC	3
R5	IO/A10	3	**U5**	VCC	3	**W5**	IO	4
R6	IO	3	**U6**	IO/GCK8/A15	3	**W6**	IO	4
R7	VCC	3	**U7**	TRST	4	**W7**	IO	4
R8	VCC	4	**U8**	IO	4	**W8**	IO	4
R9	VCC	4	**U9**	VCC	4	**W9**	IO	4

Table 2-4. ATF280E MCGA472 pin assignment

LEAD	Signal	Cluster	LEAD	Signal	Cluster
W10	IO	4	**AA4**	IO/A17	4
W11	VCC	4	**AA5**	IO	4
W12	IO	6	**AA6**	IO/A18	4
W13	IO	6	**AA7**	VCC	4
W14	VCC	6	**AA8**	IO	4
W15	IO	6	**AA9**	IO	4
W16	IO	6	**AA10**	ILVDS2	5
W17	M0	6	**AA11**	ILVDS2N	5
W18	IO	6	**AA12**	OLVDS1	5
W19	VCC	6	**AA13**	OLVDS1N	5
W20	IO	7	**AA14**	IO	6
W21	IO/LDC	7	**AA15**	IO	6
W22	VSS	7	**AA16**	IO	6
Y1	VDD	7	**AA17**	IO/A23	6
Y2	VDD	7	**AA18**	IO	6
Y3	VSS	9	**AA19**	VCC	6
Y4	IO	4	**AA20**	VDD	10
Y5	IO	4	**AA21**	VSS	10
Y6	IO	4	**AB3**	VDD	12
Y7	IO	4	**AB4**	VSS	12
Y8	IO	4	**AB5**	VCC	4
Y9	IO	4	**AB6**	VCC	4
Y10	ILVDS1	5	**AB7**	IO	4
Y11	ILVDS1N	5	**AB8**	IO/FCK1	4
Y12	OLVDS2	5	**AB9**	IO	4
Y13	OLVDS2N	5	**AB10**	IO	4
Y14	IO	6	**AB11**	IO	4
Y15	IO	6	**AB12**	IO/A21	6
Y16	IO	6	**AB13**	IO	6
Y17	VCC	6	**AB14**	IO	6
Y18	IO	6	**AB15**	IO	6
Y19	IO/OTSN	6	**AB16**	IO/FCK2	6
Y20	VSS	9	**AB17**	IO	6
Y21	VDD	7	**AB18**	IO	6
Y22	VDD	9	**AB19**	VSS	12
AA2	VSS	10	**AB20**	VDD	12
AA3	VDD	9			

3. Pin Description

Clock

GCK1:GCK8 - Global Clock (Input)

FCK1:FCK4 - Fast Clock (Input)

I/O

I/Oy_x - Programmable I/O (Input/Output)

The programmable I/Os are dedicated to user's application. Each programmable I/O can independently be configured as input, output or bidirectional I/O. Each I/O is part of an I/O cluster.

This leads to the following naming: I/Oy_x where 'y' is the cluster number (1 < y < 8) and 'x' is the I/O number in the cluster.

OLVDSx - LVDS Driver (Output)

OLVDSx where 'x' is the LVDS channel number (1 < x < 8).

OLVDSxN - Complimentary LVDS Driver (Output)

OLVDSxN where 'x' is the LVDS channel number (1 < x < 8).

ILVDSx - LVDS Receiver (Input)

ILVDSx where 'x' is the LVDS channel number (1 < x < 8).

ILVDSxN - Complimentary LVDS Receiver(Input)

ILVDSxN where 'x' is the LVDS channel number (1 < x < 8).

FPGA Configuration

M0, M1, M2 (Input)

The mode pins are dedicated TTL threshold inputs that determine the configuration mode to be used. Table 1 lists the states for each configuration mode. The mode pins should not be changed during power-on-reset, manual reset, or configuration download. The user may change the mode pins during configuration idle. These pins have no pull-up resistors to VCC, so they need to be driven by the user or tied off.

CCLK (Input/Output)

CCLK is the configuration clock pin. It is an input or output depending on the mode of operation. During power-on-reset or manual reset, it is a tri-stated output. During configuration download and in Mode 0, it is an output with a typical frequency of 1 MHz. During configuration download and in all other modes, it is a Schmitt trigger input with approximately 1V of hysteresis for noise immunity. It is an input during configuration idle, but is ignored. It is pulled to VCC with a nominal 50K internal resistor.

RESETn - Reset (Input)

RESETn is the FPGA configuration manual reset pin. It is available during all configuration states. It initiates a configuration clear cycle and, if operating in Mode 0, an auto configuration. It is a dedicated Schmitt trigger input with approximately 1V of hysteresis for noise immunity. It is pulled to VCC with a nominal 50K internal resistor.

INIT - (Input/Output)

INIT is a multi-function pin. During power-on-reset and manual reset, the pin functions as an open drain bi-directional I/O which releases High when the configuration clear cycle is complete, but can be held Low to hold the configuration in a reset state. Once released, the FPGA will proceed to either configuration download or idle, as appropriate. During configuration download, the INIT pin is again an open drain bi-directional pin which signals if an error is encountered during the download of a configuration bitstream. In addition, during the Check Function, the INIT pin drives Low for any configuration SRAM mismatch (see the description of the Check Function on page 16 for more details). While in open drain mode, the pin is pulled to VDD with a nominal 20K internal resistor. When not configuring, the INIT pin becomes a fully functional user I/O.

CON - Configuration Status (Input/Output)

CON is the FPGA configuration start and status pin. It is a dedicated open drain bi-directional pin. During power-on-reset or manual reset, CON is driven Low by the FPGA. In Modes 2, 6, or 7, when the FPGA has finished the configuration clear cycle, CON is released to indicate the device is ready for the user to initiate configuration download. The user may then drive CON Low to initiate a configuration download. After three clock cycles, CON is then driven Low by the FPGA until it finishes the download, and it is then released. In Mode 0, CON is not released by the FPGA at the end of power-on-reset or manual reset. Instead, CON is controlled by the FPGA until the end of the auto-configuration process. CON is released at the end of configuration download in Mode 0, and the user may then initiate a manual configuration download by driving CON Low. While in open drain mode, the pin is pulled to VDD with a nominal 10K internal resistor.

HDC - High During Configuration (output)

HDC(1) is driven High by the FPGA during power-on-reset, manual reset, and configuration download. During normal operation, the pin is a fully functional user I/O.

Note: 1. All user I/O default to inputs with pull-ups “on”. The HDC pin transitions from driving a strong “1” to a pull-up “1” after reset. The HDC pin will transition from driving a strong “1” to the user programmed state at the end of configuration download. If not programmed, the default state is input with pull-up.

LDC - Low During Configuration (output)

HDC(1) is driven Low by the FPGA during power-on-reset, manual reset, and configuration download. During normal operation, the pin is a fully functional user I/O.

Note: 1. All user I/O default to inputs with pull-ups “on”. The HDC pin transitions from driving a strong “1” to a pull-up “1” after reset. The HDC pin will transition from driving a strong “1” to the user programmed state at the end of configuration download. If not programmed, the default state is input with pull-up.

D0 - Configuration Data Bus - LSB (Input/Output)

D0 is the lsb of the FPGA configuration data bus used to download configuration data to the device. During power-on-reset or manual reset, D0 is controlled by the configuration SRAM. The D0 pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pull-up resistor as the SRAM at that location is cleared by the configuration clear cycle. D0 becomes an input during configuration download.

D1:D15 - Configuration Data Bus - Upper bits (Input/Output)

D1:D15 are the upper bits of the 8/16-bit parallel data bus used to download configuration data to the device. During power-on-reset or manual reset, D1:D15 are controlled by the configura-

tion SRAM. The D1:D15 pins will transition from the user programmed state to CMOS inputs with nominal 20K internal pull-up resistors as the SRAM at those locations is cleared by the configuration clear cycle.

When in Modes 2 or 6, D1:D7 become inputs during configuration download. D1:D7 are not used in the serial Modes 0, 1 and 7.

When in Modes 2 or 6, D8:D15 become optional inputs during configuration download. They become available as soon as the appropriate bit in the configuration control register is set. D8:D15 are not used in the serial Modes 0, 1 and 7.

A0:A19 - Configuration Address Bus (Input/Output)

A0:A19(1) are used to control external addressing of memories during downloads. During power-on-reset or manual reset, A0:A19 are controlled by the configuration SRAM. The A0:A19 pins will transition from the user programmed state to CMOS inputs with nominal 20K internal pull-up resistors as the SRAM at those locations is cleared by the configuration clear cycle. When in Mode 6, A0:A19 become outputs during configuration download. A0:A19 are used only in Mode 6.

Note: 1. Pin A2 is also pin CS1, which is available only for Mode 2. See the description for CS1 on page 5 for more details.

CS0/CS1 - Configuration Chip Select (Input/Output)

CS0 is an FPGA configuration chip select. It is active Low. During power-on-reset or manual reset, CS0 is controlled by the configuration SRAM. The CS0 pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pull-up resistor as the SRAM at that location is cleared by the configuration clear cycle. In Mode 1, it is used as a chip select to enable configuration to begin. It is most often used as the chip select of the downstream device in a cascade chain, and is usually driven by CSOUT of the upstream device. Releasing CS0 during configuration causes the Mode 1 FPGA to abort the download and release CON.

CS0 is used only in Mode 1. CS1 is used only in Mode 2

Note: 1. Pin CS1 is also pin A2, which is active only for Mode 6. See the description for A0:A19, on page 5 for more details.

CSOUT - Configuration Cascade Output (Output)

CSOUT is the configuration pin used to enable the downstream device in a cascade chain. During power-on-reset or manual reset, CSOUT is controlled by the configuration SRAM. The CSOUT pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pull-up resistor as the SRAM at that location is cleared by the configuration clear cycle. During configuration download, CSOUT becomes an optional output. It is enabled by default after reset, and may be enabled or disabled via the configuration control register. If the user has disabled the cascade function, the pin remains a user I/O. If the cascade function is enabled, the CSOUT pin is driven High at the start of configuration download. At the end of the device's portion of the cascade bitstream, the CSOUT pin is driven Low (and into the CS0 or CS1 of the downstream device) to enable the downstream device. CSOUT is released by the device at the end of the cascade bitstream and becomes a fully functional user I/O.

CHECK - Configuration Check (Input/Output)

CHECK is a configuration control pin used to control the Check Function. The Check Function takes a bitstream and compares it to the contents of a previously loaded bitstream and notifies the user of any differences. Any differences causes the INIT pin to go Low. During power-on-

reset or manual reset, CHECK is controlled by the configuration SRAM. The CHECK pin will transition from the user programmed state to a CMOS input with a nominal 20K internal pull-up resistor as the SRAM at that location is cleared by the configuration clear cycle. During configuration download, CHECK becomes an optional input. It is enabled by default after reset, and may be enabled or disabled via the configuration control register. If the user has disabled the Check Function, the pin remains a user I/O.

OTS - Dual Use Tri State (Input)

OTS is an input pin used to immediately tri-state all user I/O. It is enabled by a bit in the configuration control register. Once activated, it is always an input. The OTS tri-state control of Dual-use pins is superseded by the configuration logic's claim on those pins. If the user has disabled the OTS function, the pin remains as User I/O.

JTAG

TCK - Test Clock (input)

Used to clock serial data into boundary scan latches and control sequence of the test

state machine. TCK can be asynchronous with CLK.

TMS - Test Mode select (input)

Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.

TDI - Test data input (input)

Serial input data to the boundary scan latches. Synchronous with TCK

TDO - Test data output (output)

Serial output data from the boundary scan latches. Synchronous with TCK

TRST - Test Reset (input)

Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application.

Power Supply

VDD - Core Power Supply

VDD is the power supply input for the ATF280E core. VDD = 1.8V ± 0.2V

VCCy - I/O Power Supply

VCC is the power supply input for the programmable I/Os. Each I/O cluster has dedicated VCCy sources where 'y' is the cluster number ($1 < y < 8$). VCC can be independently configured to either 1.8V ± 0.2V or 3.3V ± 0.3V for each cluster.

VCCB - LVDS I/O Power Supply

VCCB is the power supply input for the LVDS I/Os. Each pair of LVDS channels has a dedicated VCCB sources. VCCB = 3.3V ± 0.3V

VREF - LVDS reference voltage

VREF is the reference voltage for LVDS buffer operations. Each LVDS cluster has dedicated VREF source. VREF = 1.25V ± 0.1V

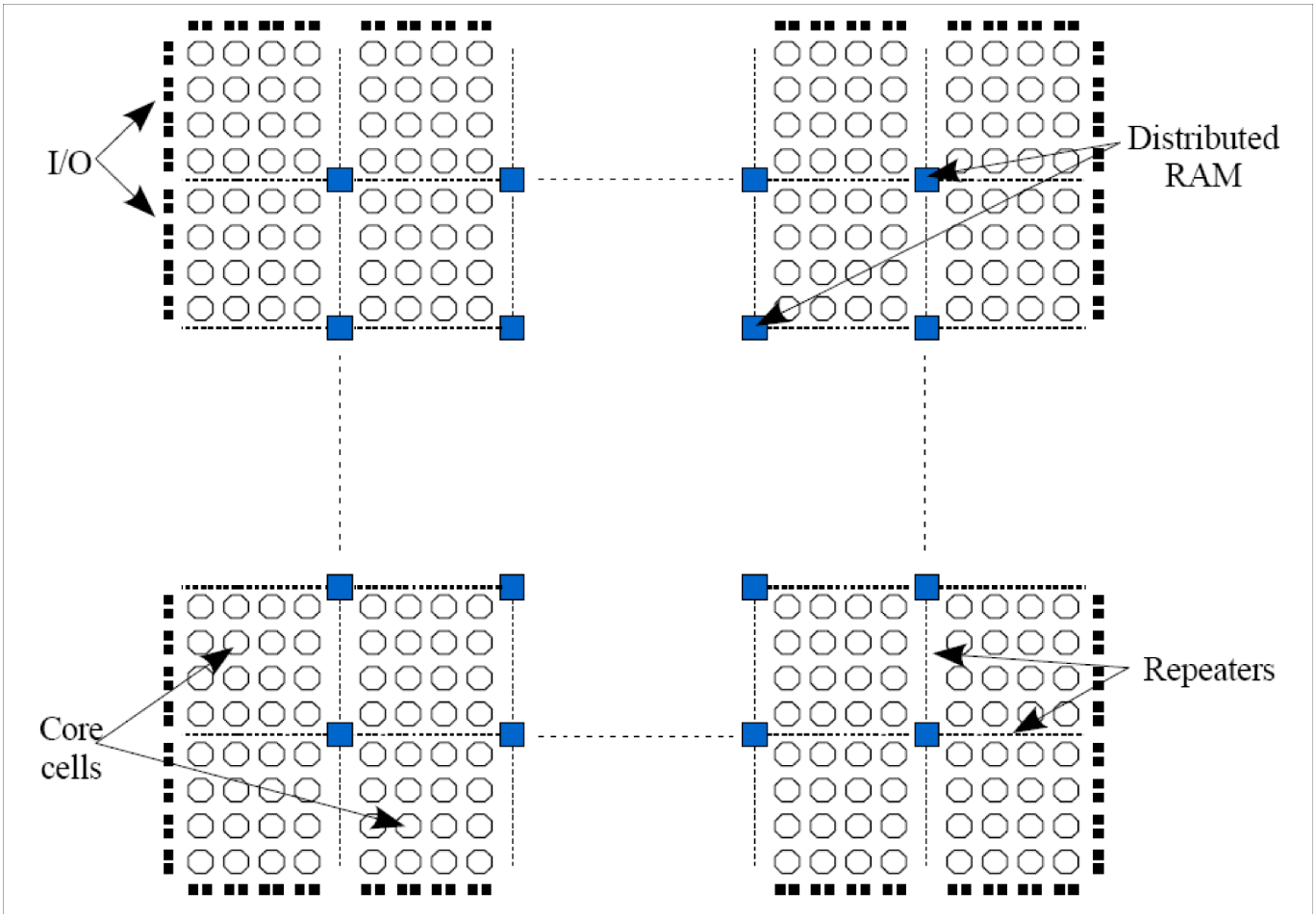
VSS - Ground

4. ATF280E FPGA Architecture

4.1 The Symmetrical Array

At the heart of the Atmel ATF280E architecture is a symmetrical array of identical cells. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells. At the intersection of each repeater row and column is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM (1), with either synchronous or asynchronous operation

Figure 4-1. Core device overview



Note: 1. the right-most column can only be used as single-port RAM.

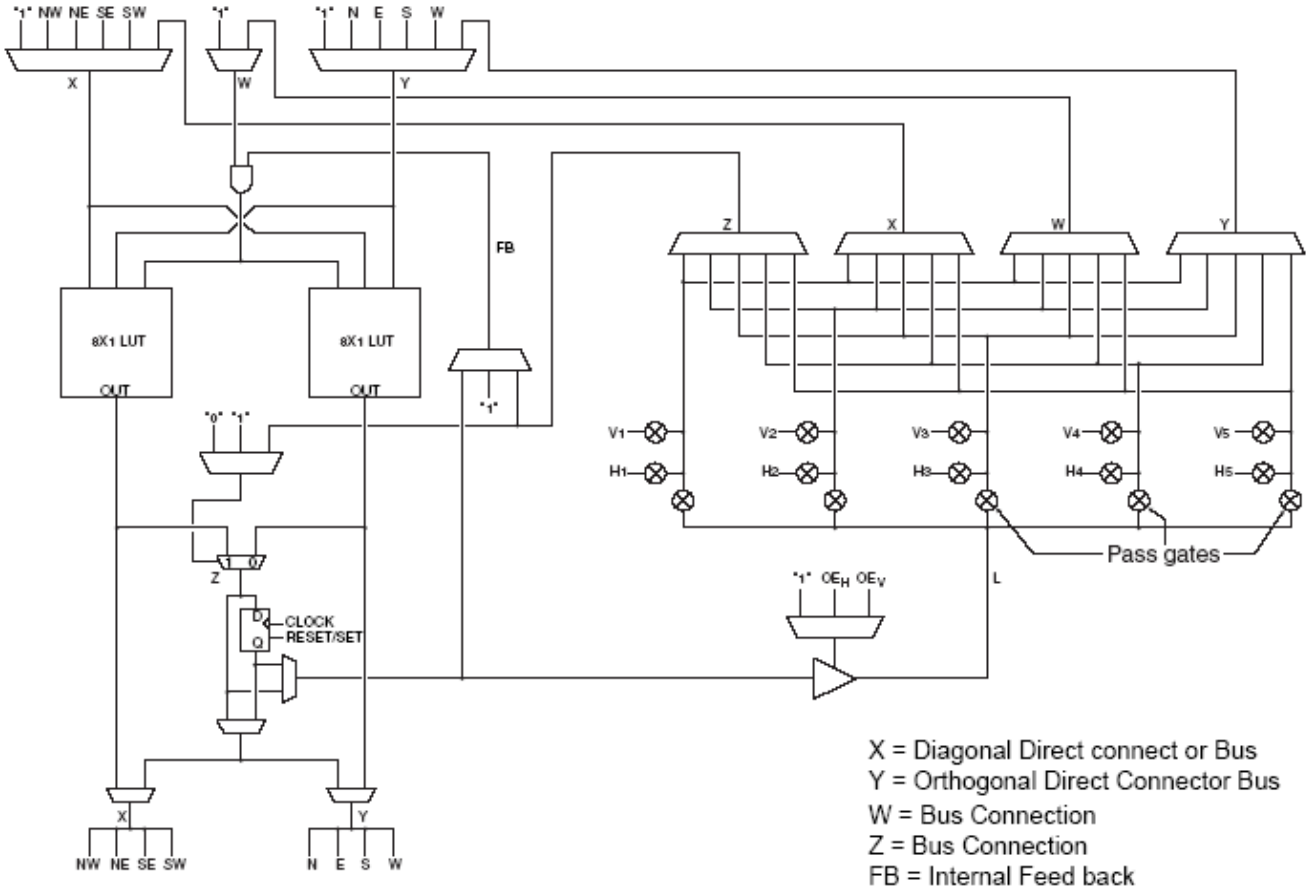
Figure 4-2. Floor-plan for a 12x12 cells array[1].

Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

4.2 The Core Cell

The following figure depicts the ATF280E cell which is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), and which can be combined to produce one 4-input LUT. This means that any cell can implement two functions of 3 inputs or one function of 4 inputs.

Figure 4-3. ATF280E Core Cell



Every cell includes a register element, a D-type flip-flop, with programmable clock and reset polarities. The initialization of the register is also programmable. It can be either SET or RESET. The flip-flop can be used to register the output of one of the LUT. It can also be exploited in conjunction with the feedback path element to implement a complete ripple counter stage in a single cell. The registered or unregistered output of each LUT can be feedback within the cell and treated as another input (Feedback signal in Figure 3). This allows, for example, a single counter stage to be implemented within one cell without using external routing resources for the feedback connection.

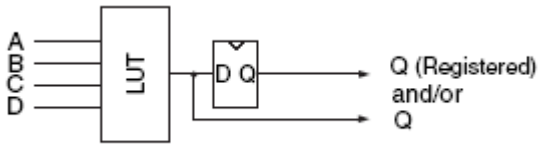
There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers as the product and carry terms can both be generated within a single logic cell.

The cell flexibility makes the ATF280E architecture well suited for most of the digital design application areas.

4.2.1 Synthesis Mode

This mode is particularly important for the use of VHDL design. VHDL Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

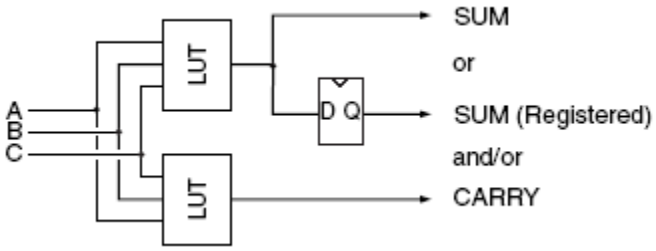
Figure 4-4. Synthesis Modes



4.2.2 Arithmetic Mode

This mode is frequently used in many designs. As can be seen in the figure, the ATF280E core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

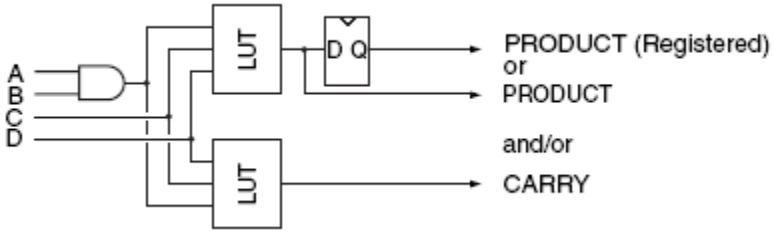
Figure 4-5. Arithmetic Mode



4.2.3 DSP/Multiplier Mode

This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the ATF280E architecture.

Figure 4-6. DSP/Multiplier Mode

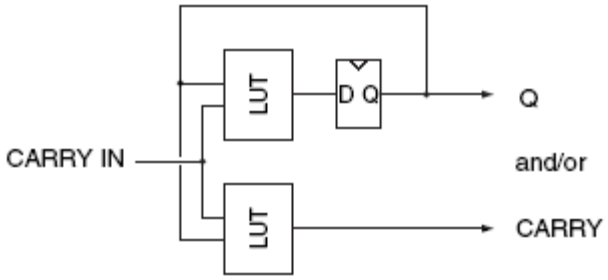


4.2.4 Counter Mode

Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit

counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

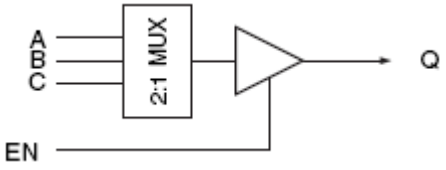
Figure 4-7. Counter Mode



4.2.5 Tri-state/Mux Mode

This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

Figure 4-8. Tri-state/Mux Mode

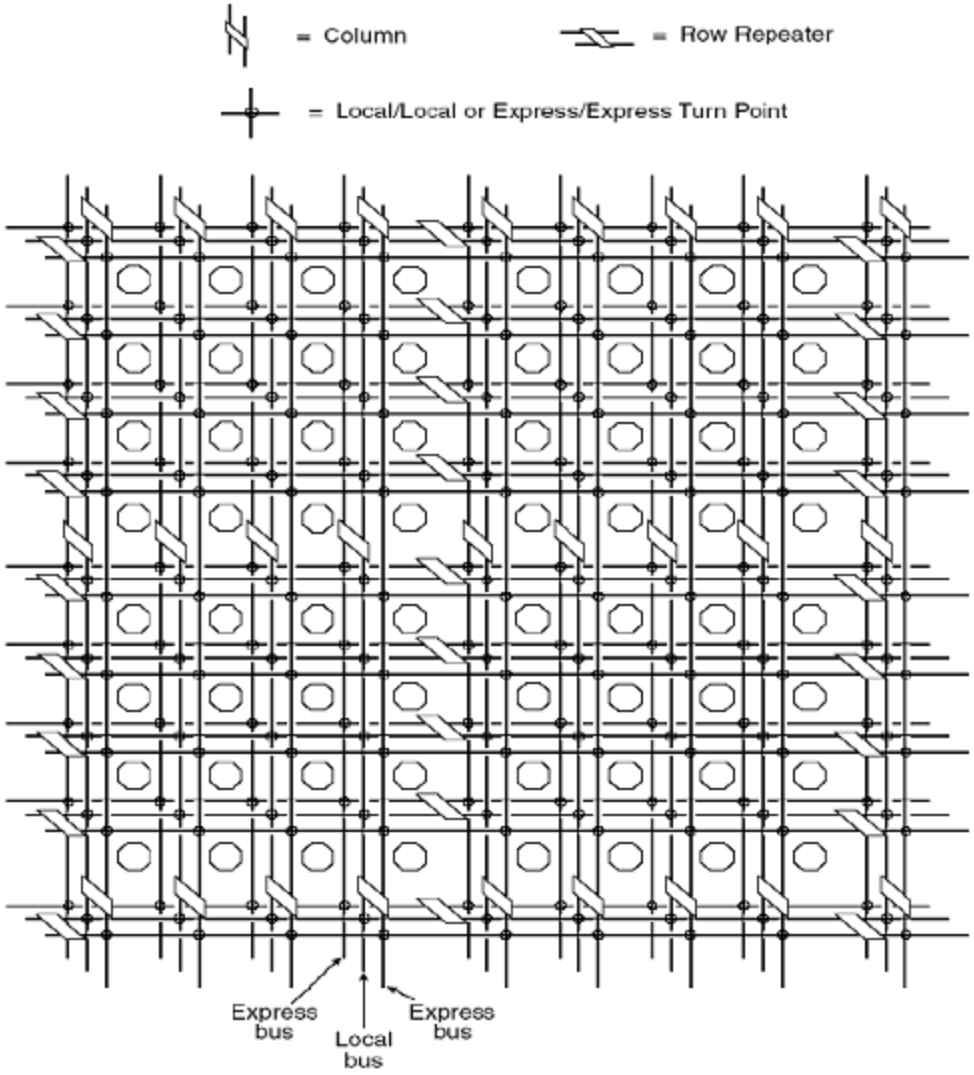


4.3 The Busing Network

The following figure depicts one of five identical busing planes. Each plane has three bus resources:

- a local-bus resource (the middle bus)
- two express-bus (both sides) resources

Figure 4-9. Busing Plane



The bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments.

Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane.

Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface (see following page).

Express/Express turns are implemented through separate pass gates distributed throughout the array.

4.3.1 Dual Function Bus Resource

Some of the bus resource on the ATF280E are used as a dual-function resource. The table hereafter shows which buses are used in a dual-function mode and which bus plane is used.

Table 4-1. Dual-function Buses

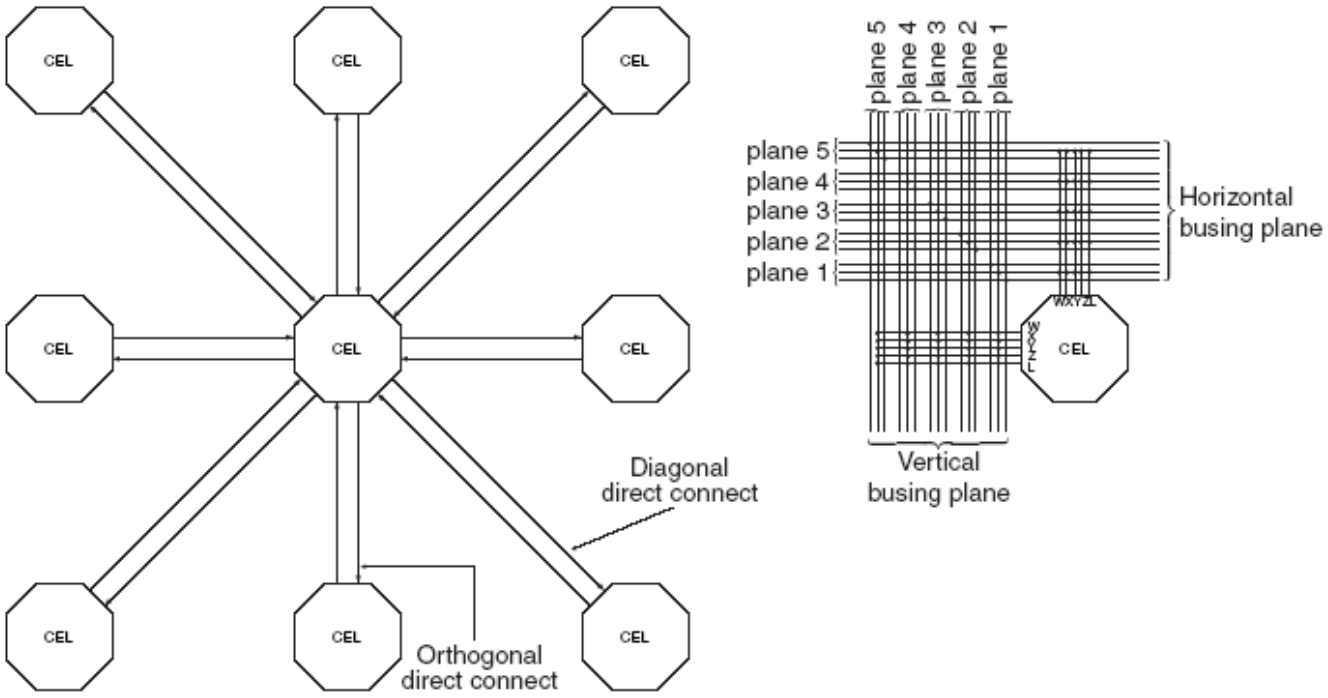
Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	
RAM Data Out	Local	2	Horizontal	
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

The ATF280E software tools are designed to accommodate dual-function buses in an efficient manner

4.4 Cell Connections

The following figure presents the direct connections between a cell and its eight nearest neighbors. It also summarizes the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4-10. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

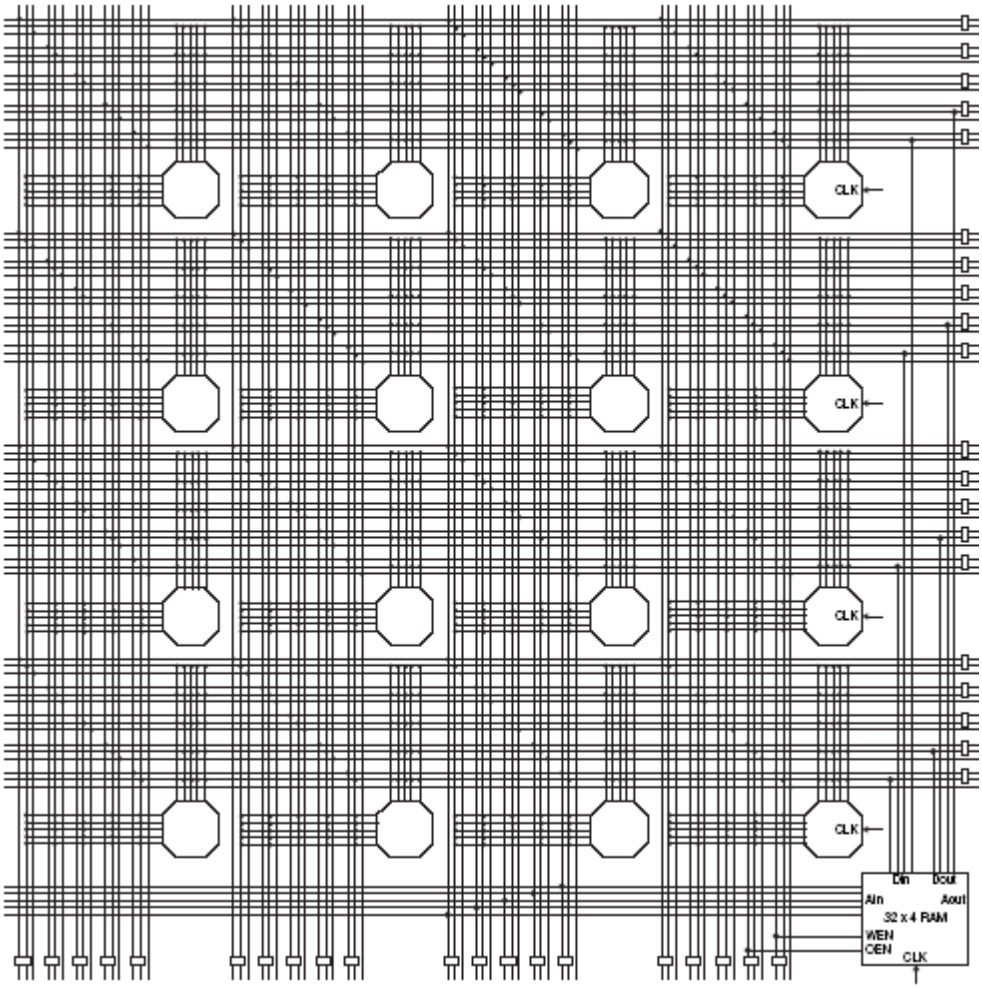
5. FreeRAM™

The ATF280E offers 115Kbits of dual-port RAM called FreeRAM™. The FreeRAM™ is made of 32 x 4 dual-ported RAM blocks and dispersed throughout the array as shown in the figure hereafter. This FreeRAM™ is SEU hardened.

A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A 5-bit Input Address Bus connects to five vertical express buses in same column. A 5-bit Output Address Bus connects to five vertical express buses in same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port.

Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 5-1. RAM Connections (One RAM Block)



Reading and writing of the 10ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous.

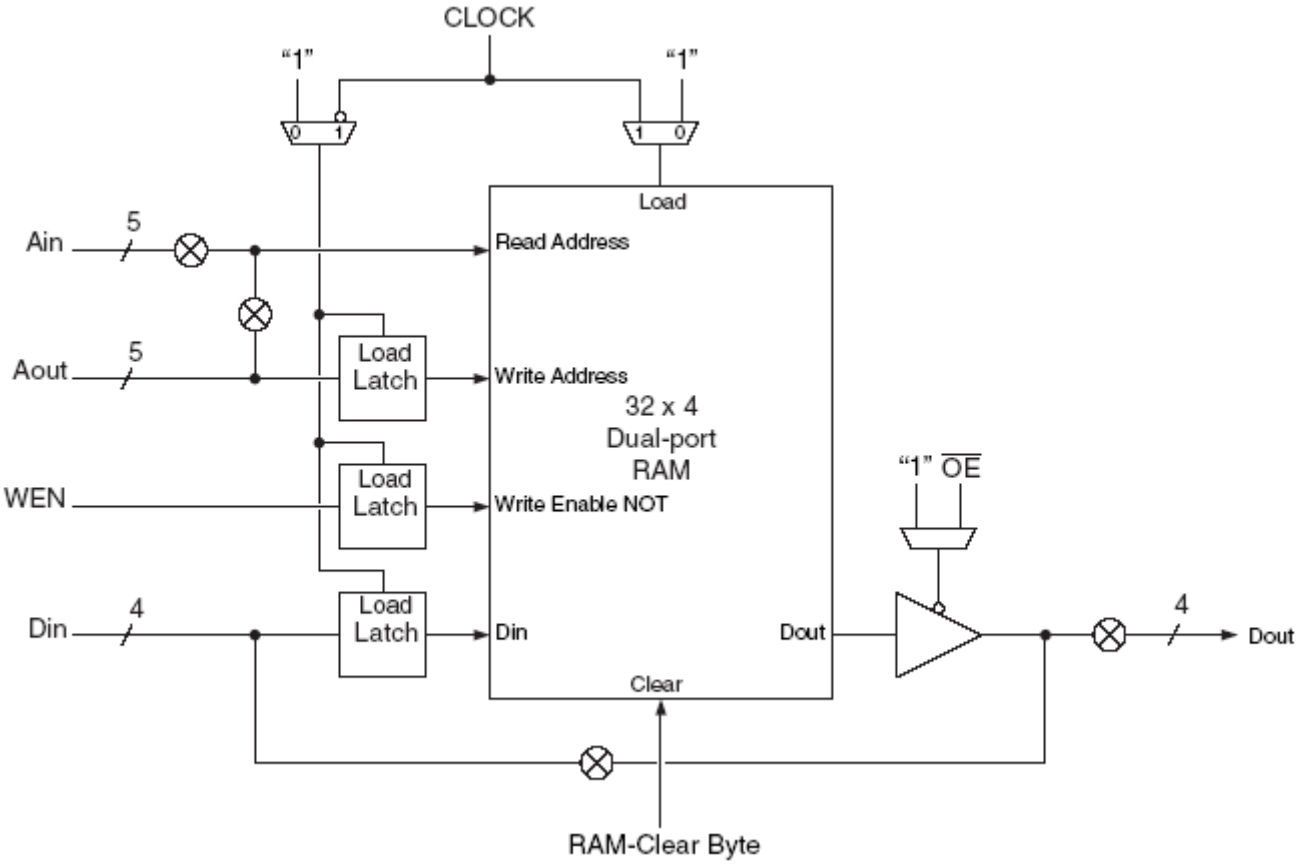
Latches on Write Address, Write Enable and Data In are transparent: when Load is logic 1, data flows through, when Load is logic 0, data is latched. These latches are used to synchronize Write Address, Write Enable Not, and Din signals for a synchronous RAM.

Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble is (Write) addressed and LOAD is logic 1 and WE is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or WE is logic 1, data is latched in the nibble.

The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select "1" (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block.

Writing any value to the RAM clear byte during configuration clears the RAM (see the "*AT40K/40KAL Configuration Series"* application note at www.atmel.com).

Figure 5-2. RAM Logic

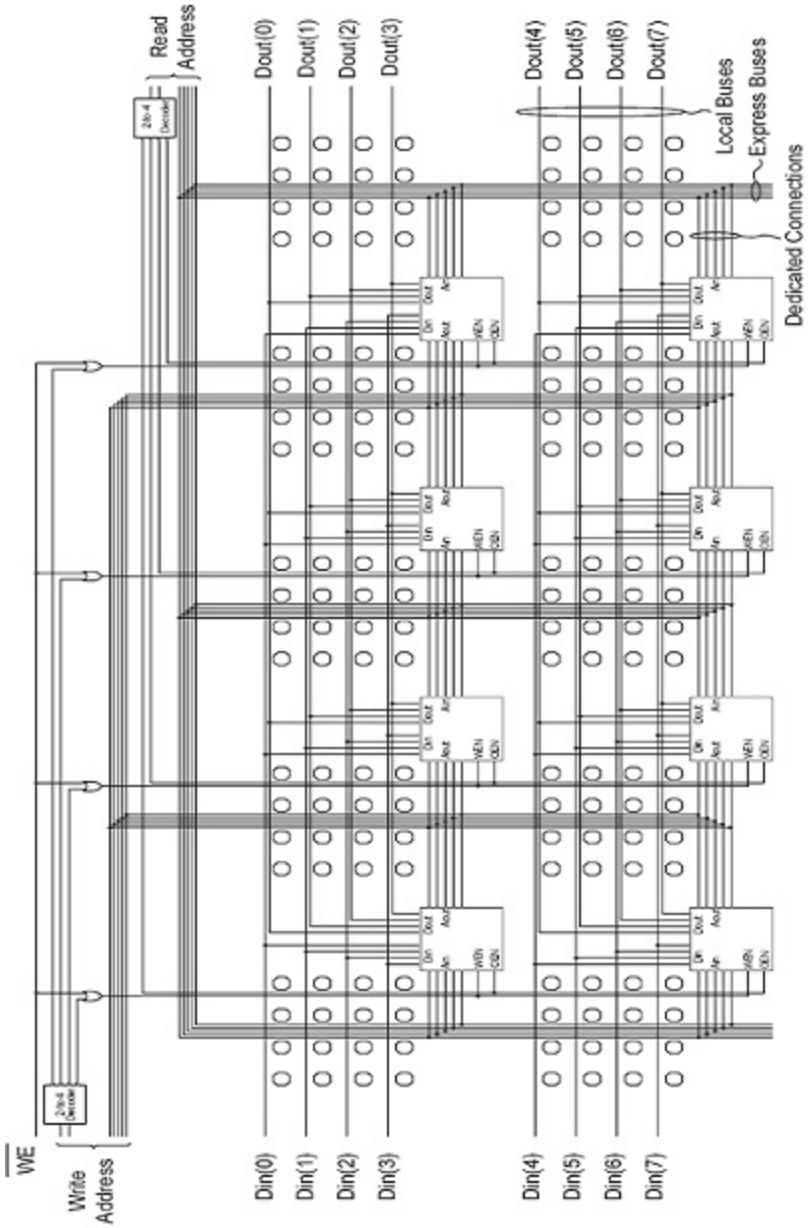


Note: Ain and Aout are 5 bits wide, and the memory block is 32x4.

Here is an example of a RAM macro constructed using ATF280E's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells in the sectors

occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 5-3. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



6. Clocking Scheme

The entire ATF280E clocking scheme (including clock trees and muxes) is SET hardened.

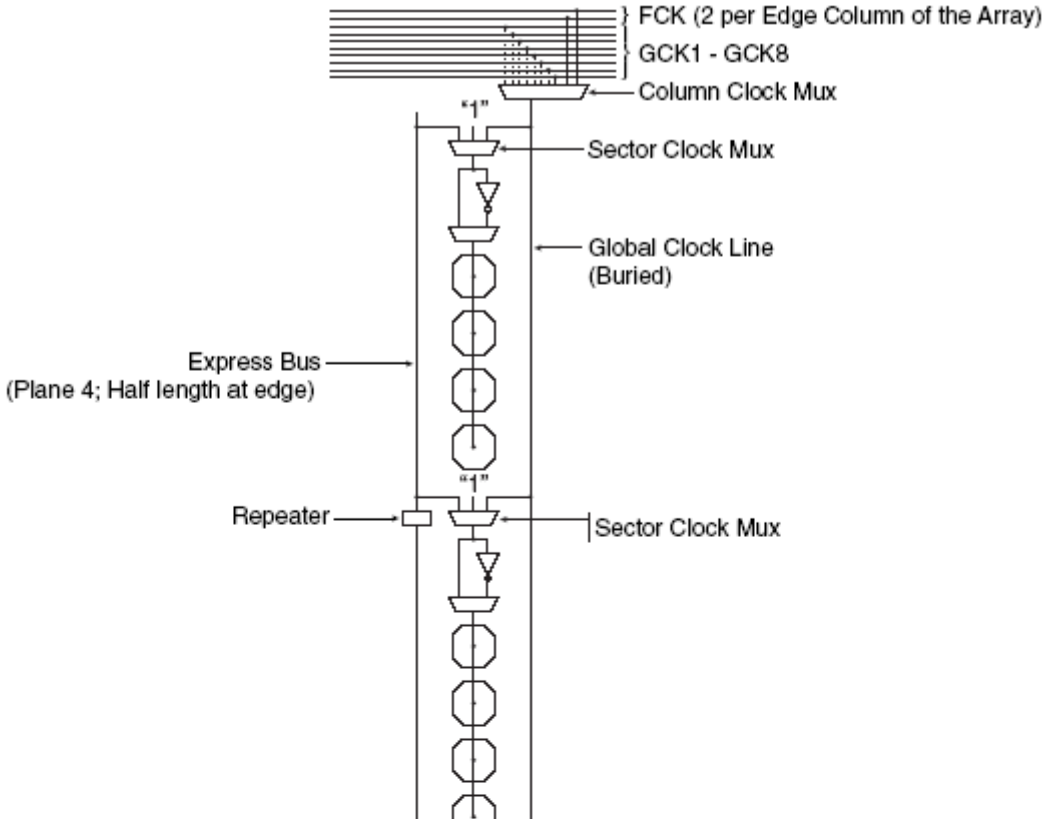
There are eight differential Global Clock buses (GCK1 - GCK8) on the ATF280E FPGA. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4).

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks.

The clock can either come from the Column Clock or from the Plane 4 express bus. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration at power-up, constant “0” is provided to each register’s clock pins. After configuration at power-up, the registers either set or reset, depending on the user’s choice. The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 6-1. Clocking (for One Column of Cells)



6.1 Global Clocks

Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible. These signals are distributed across the top edge of the FPGA along special high-speed buses. Global Clock signals can be distributed throughout the FPGA with less than 1 ns skew.

This can be done by using Assign Pin Locks command in the IDS software to lock the clocks to the Global Clock locations.

6.2 Fast Clocks

There are four Fast Clocks (FCK1 - FCK4) on the ATF280E, two per edge column of the array for PCI specification. Even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network.

The IDS software tools handle derived clocks to global clock connections automatically if used.

7. Set/Reset Scheme

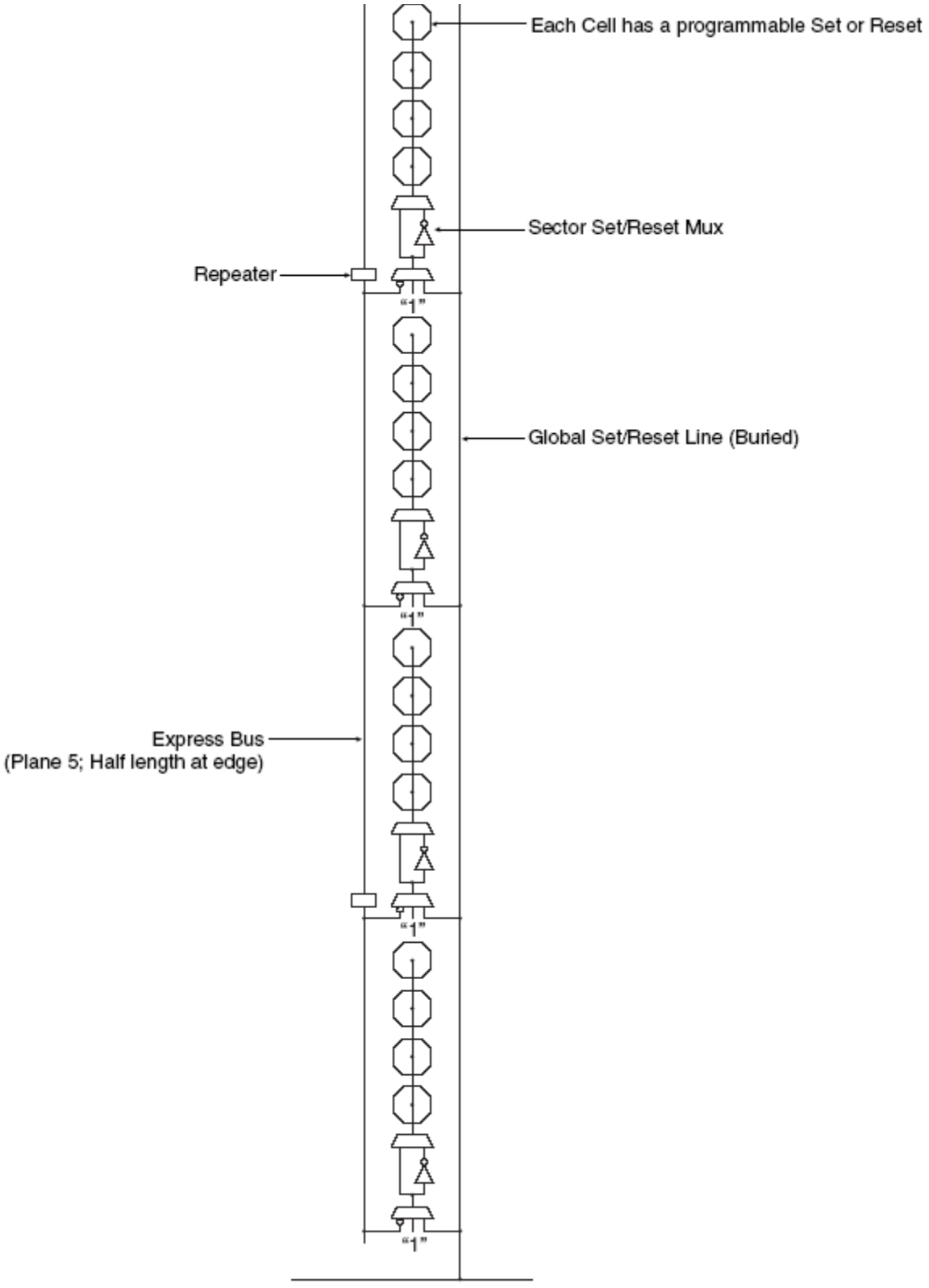
The ATF280E reset scheme is essentially the same as the clock scheme except that there is only one differential Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). Like the clocking scheme, set/reset scheme is SET hardened.

The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux (Figure 10). The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 7-1. Set/Reset (for One Column of Cells)



8. I/O Specifications

The ATF280E provides 2 types of I/O which are all cold sparing:

- programmable I/Os (PCI compatible)
- LVDS I/Os

The ATF280E periphery is divided into 12 clusters. Height clusters are dedicated to programmable I/Os and four clusters are dedicated to LVDS. Each cluster consists in a set of I/O together with its dedicated power supply source.

8.1 Programmable I/Os

Each Programmable I/O cluster has its dedicated power supply source. Programmable I/Os are powered through VCC pads. VDD and VSS power lines are common to all clusters.

Programmable I/O clusters accept 2 different voltages. This feature provides the possibility to use some programmable I/O clusters at either 1.8V or 3.3V.

Each programmable I/O can be configured as input, output or bi-directional. When configured as input an optional Schmitt trigger can be enabled on the I/O. When configured as output optional PCI compatibility can be enabled. In addition it is possible to select the buffer drive to optimize speed of the application.

In addition, the ATF280E provides pull-up and pull-down capability on each I/O. The following section presents all the configuration available on the programmable I/Os

8.1.1 Pull-up/Pull-down

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak “1” or “0” level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

8.1.2 JTAG

All programmable I/Os (including LVDS buffers) are 1149.1 compliant. Each I/O may be included or excluded from boundary scan chain during the configuration of the FPGA.

8.1.3 CMOS

The threshold level of the I/O is CMOS-compatible.

8.1.4 Schmitt

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 0.8V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

8.1.5 Delays

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

8.1.6 Drive

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW. The FAST setting has the highest drive capability (PCI compatible) buffer and the fastest slew rate. MEDIUM produces a medium drive buffer, while SLOW yields a standard buffer.

Drive capability is dependent upon setting FAST, MEDIUM and SLOW performance and supplies voltage.

Table 8-1. Drive Capability for VCC = 3.3V

VCC = 3.3V	IOh(mA)		IOl(mA)	
config.	**Worst case**	**typical**	**Worst case**	**typical**
Slow	13	20	17	30
Medium	5	8	5	10
Fast	18.5	29	23	40

Table 8-2. Drive Capability for VCC = 1.8V

VCC =1.8V	IOh(mA)		IOl(mA)	
config.	**Worst case**	**typical**	**Worst case**	**typical**
Slow	6	10	7	15
Medium	2	4	2	5
Fast	8	15	10	21

When no modification is performed by the user on the IDS software, the default configuration of the drive for the I/Os is SLOW.

8.1.7 Tri-State

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O's Source Selection mux. Of course, the output can be normal (0 or 1), as well.

8.1.8 Dual-use I/O

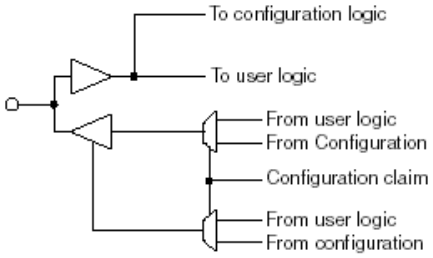
Any pin which functions as user I/O and configuration I/O is a dual-use I/O pin. INIT, HDC, LDC, D_0:D_{15}, A_0:A_{19}, CS_0, CS_1, CSOUT, CHECK, and OTS are all dual-use I/O pins.

It must be noted that while the configuration logic controls dual-use I/O pins during a particular mode of operation, the configuration logic does not control the pull-up, pull-down, CMOS/TTL threshold select, or Schmitt trigger selects.

The user must be cautioned to avoid possible system problems with the use of dual-use I/O pins. For example, turning off the internal pull-up resistor for the open drain INIT pin would not apply the weak High required of an open drain driver. Conversely, disabling the pull-up and enabling the pull-down of the HDC pin might be a good idea, since the user may then actually see the pin go Low at the end of configuration.

Dual-use pins share input buffers. It should be noted that even when the configuration has claimed a pin for its own purposes, the user input buffer is still fully functional. This implies that any user logic tied to the input buffers of the pins in question will remain operational.

Figure 8-1. Dual Use I/O principle



8.2 LVDS I/Os

Each LVDS cluster has its dedicated power supply source. LVDS I/Os are powered through VCCB pads. VDD and VSS power lines are common to all clusters.

The LVDS I/Os are composed of 8 LVDS transceiver (Tx) pairs, 8 receivers (Rx) pairs together with 4 reference voltages (Vref). The reference voltage must be connected to an accurate 1.25V voltage to give references to the transceivers and to the receivers.

The LVDS specification complies with the EIA-644 standard requirements.

8.2.1 JTAG

All LVDS I/Os are 1149.1 compliant. Each I/O may be included or excluded from boundary scan chain during the configuration of the FPGA.

9. ATF280E Configuration

Configuration is the process by which a design is loaded into an ATF280E FPGA. The ATF280E device is a SRAM based FPGA. this lead to an unlimited reprogrammability capability.

It is possible to configure either the entire device or only a portions of the device. Sections can be configured while others continue to operate undisturbed. The architecture of the ATF280E leads to a maximum bitstream size of 3M bits. It is possible to store configuration bit-streams of the ATF280E in one single 4Mbit EEPROM.

Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration data is transferred to the device in one of the six modes supported by the ATF280E. Three dedicated input pins, M0, M1, and M2 are used to determine the configuration mode.

9.1 Entering Configuration Modes

9.2 Configuration Modes

The ATF280E supports an auto-configuring Master mode, four Slave modes, and a Synchronous RAM Mode for accessing the SRAM-based configuration memory directly from a parallel microprocessor port.

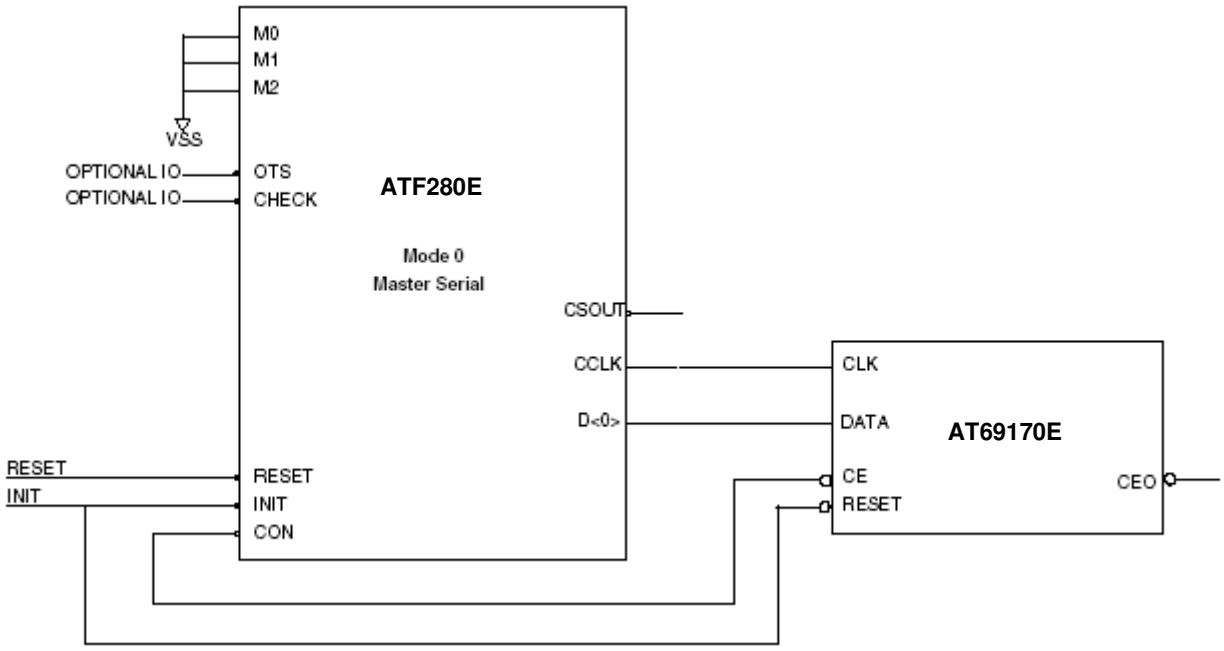
The following table summarizes the ATF280E configuration modes.

Table 9-1. Configuration Modes

Mode	Description	M2	M1	M0	CCLK	Data	Notes
0	Master Serial	0	0	0	Output	Serial	Auto-Configuration Serial EEPROM
1	Slave Serial	0	0	1	Input	Serial	Microprocessor or Serial EEPROM
7	Slave Serial		1	1	Input	Serial	Microprocessor or Serial EEPROM
2	Slave Parallel	0	1	0	Input	8 or 16 bit word	Microprocessor or parallel EEPROM
6	Slave Parallel	1	1	0	Input	8 or 16 bit word	20-bit address out, Parallel EPROM
4	Synchronous RAM	1	0	0	Input	8 or 16 bit word	24-bit Address In, Parallel Port of Microprocessor

In order to keep the maximum number of pins assigned to signals, it is recommended to use a serial configuration interface. Here is an example of ATF280E serial configuration architecture.

Figure 9-1. Mode 0 Configuration Architecture



For complete description of all the ATF280E configuration modes please refer to the “AT40K Series Configuration” application note on the ATMEL web site www.atmel.com.

9.3 Configuration Check

The download of the bit-stream from the EEPROM to the FPGA is checked (CRC). Once configured the FPGA will also self check the integrity of the configuration and generate a warning as soon as a difference is detected.

10. Development Software

The ATF280E is designed to quickly implement high performance, large gate count designs through the use of combined Atmel and industry standard tools used on Windows/Linux platform.

11. Power-On Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to ensure proper initialization. The power supply ramp-up time affects the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Moreover, the supply voltage must respect a sequence as described below:

The peripheral power up must be done before the core power up. No ramp up is required on VCC power supply.

Table 11-1. Power-on Supply Requirements

Description	Maximum Current(1)(2)
Maximum Current Supply	**3 A**

Notes: 1. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initialization current.

2. 2. Ramp-up time is measured from 0V DC to 1.8V DC. Peak current required lasts less than 2 ms, and occurs near the internal power on reset threshold voltage.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings[1]

Supply Voltage 1.8V I/Os (VCC buffers).....-0.3V to +2V Supply Voltage 3.3V I/Os (VCC buffers)..... -0.3V to +4V Supply Voltage Core (VDD array).....…….....-0.3V to +2V Storage Temperature.....-65°C to +150°C All Output Voltages with respect to Ground..... -0.3V to 4V ESD.....…..3000V	*NOTICE: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12.2 Operating Range

Table 12-1. Operating Range

Operating Temperature	-55°C to +125°C
VCC - I/O Power Supply	3.3V ± 0.3V 1.8V ± 0.15V
VCCB - LVDS I/O Power Supply	3.3V ± 0.3V
VREF - LVDS Reference Voltage	1.25 ± 0.1V
VDD - Core Power Supply	1.8V ± 0.15V

12.3 DC Characteristics

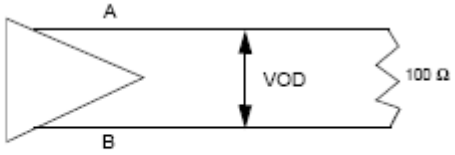
 Table 12-2. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{cc}			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{cc}	V
V_{OH}	High-level Input Voltage	I_{OH} = -4 mA V_{CC} = 3.0V	2.4			V
		I_{OH} = -12 mA V_{CC} = 3.0V	2.4			V
		I_{OH} = -16 mA V_{CC} = 3.0V	2.4			V
V_{OL}	Low-level Input Voltage	I_{OL} = +4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = +12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = +16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} max	-5		5	µA
		With pull-down, V_{IN} = V_{CC}	20	75	300	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-5		5	µA
		With pull-up, V_{IN} = V_{SS}	-300	-50	-20	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{OUT} =V_{CC} max	-5		5	µA
		With pull-down, V_{OUT} = V_{CC} max	20		300	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{OUT} = V_{SS}	-5			µA
		With pull-up, V_{OUT} = V_{SS} for CON	-500	-150	-110	µA
I_{CC}	Standby Current Consumption	Standby, un-programmed		1	5	mA
C_{IN}	Input Capacitance	All pins			10	pF
I_{ICS}	Cold sparing leakage Input current	Vdd = Vss = 0V Vin = 0 to VDD Max	-2		2	µA
I_{OCS}	Cold sparing leakage output current	Vdd = Vss = 0V Vin = 0 to VDD Max	-2		2	µA
V_{CSTH}	Supply threshold of cold sparing buffers	Iocs = 100 µA		0.5		V

Table 12-3. LVDS Driver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
|VOD|	Output differential voltage	Rload = 100Ω	251.4	452.2	mV	see Figure below
Vol	Output voltage low	Rload = 100Ω	1071	1731	mV	see Figure below
Voh	Output voltage high	Rload = 100Ω	804	1323	mV	see Figure below
VOS	Output offset voltage	Rload = 100Ω	937	1527	mV	see Figure below
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delta VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	200	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.2	mA	–
ISAB	Output current	Drivers shorted together	2.6	4.8	mA	–
Rbias	Bias resistor	–	16.3	16.7	**K**Ω	
Ibias	Bias static current	–	7	14.6	mA	–
F Max.	Maximum operating frequency	VDD = 3.3V ± 0.3V	–	200	MHz	Consumption 20.9 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	445	838	ps	see Figure below
Trise	Rise time 20-80%	Rload = 100Ω	445	841	ps	see Figure below
Tp	Propagation delay	Rload = 100Ω	1120	2120	ps	see Figure below
Tsk1	Duty cycle skew	Rload = 100Ω	0	80	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Figure 12-1. Test Termination Measurements



$$VOS = \frac{(VA + VB)}{2}$$

Figure 12-2. Rise and Fall times Measurements

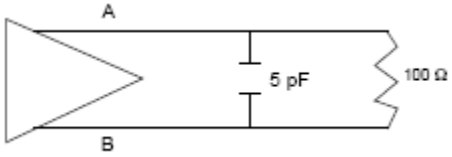


Table 12-4. LVDS Receiver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
Vi	Input voltage range	–	0	2400	mV	–
Vidth	Input differential voltage	–	-100	+100	mV	–
Tp	Propagation delay	Cout = 50 pF, VDD = 3.3V ± 0.3V	0.7	2.4	ns	–
Tskew	Duty cycle distortion	Cout = 50 pF	-	500	ps	–

12.4 AC Timing Characteristics - TBD

All input I/O characteristics measured from V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}.

All output I/O characteristics are measured as the average of T_{PDLH} and T_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.

Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Table 12-5. AC Characteristics

Cell Function	Parameter	Path	Value	Units	Notes
IO					
Input	t_{PD} (max)	pad -> x/y		ns	no extra delay
Input	t_{PD} (max)	pad -> x/y		ns	1 extra delay
Input	t_{PD} (max)	pad -> x/y		ns	2 extra delays
Input	t_{PD} (max)	pad -> x/y		ns	3 extra delays
Output, slow	t_{PD} (max)	Output, fast		ns	40 pF load
Output, medium	t_{PD} (max)	Output, fast		ns	40 pF load
Output, fast	t_{PD} (max)	Output, fast		ns	40 pF load
Output, slow	t_{PD} (max)	oe -> pad		ns	40 pF load
Output, slow	t_{PD} (max)	oe -> pad		ns	40 pF load
Output, medium	t_{PD} (max)	oe -> pad		ns	40 pF load
Output, medium	t_{PD} (max)	oe -> pad		ns	40 pF load
Output, fast	t_{PD} (max)	oe -> pad		ns	40 pF load
Output, fast	t_{PD} (max)	oe -> pad		ns	40 pF load
Cell Function	**Parameter**	**Path**	**Value**	**Units**	**Notes**
Global Clocks and Set/Reset					
GCK Input buffer	t_{PD} (max)	pad -> clock		ns	rising edge clock
FCK Input buffer	t_{PD} (max)	pad -> clock		ns	rising edge clock
Clock column driver	t_{PD} (max)	clock -> colclk		ns	rising edge clock
Clock sector driver	t_{PD} (max)	colclk -> secclk		ns	rising edge clock
GSRN Input buffer	t_{PD} (max)	colclk -> secclk		ns	from any pad to Global Set/Reset network

Cell Function	Parameter	Path	Value	Units	Notes
Global clock to output	t_{PD} (max)	clock pad -> out		ns	rising edge clock fully loaded clock tree rising edge DFF 20 mA output buffer 40 pF pin load
Fast clock to output	t_{PD} (max)	clock pad -> out		ns	rising edge clock fully loaded clock tree rising edge DFF 20 mA output buffer 40 pF pin load

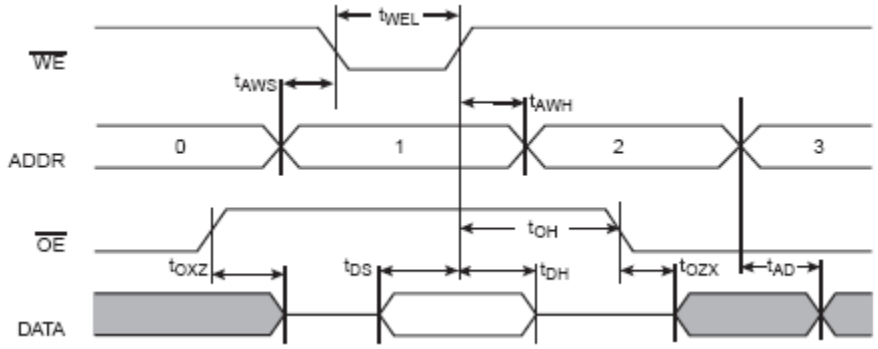
Table 12-6. FreeRAM AC Characteristics

Async RAM					
Write	t_{WECYC} (Minimum)	cycle time		ns	
Write	T_{WEL} (Minimum)	We		ns	Pulse width low
Write	T_{WEH} (Minimum)	We		ns	Pulse width high
Write	T_{AWS} (Minimum)	wr addr setup -> we		ns	
Write	T_{AWH} (Minimum)	wr addr hold -> we		ns	
Write	T_{DS} (Minimum)	din setup -> we		ns	
Write	T_{DH} (Minimum)	din hold -> we		ns	
Write /Read	T_{DD} (Maximum)	din -> dout		ns	rd addr = wr addr
Read	T_{AD} (Maximum)	rd addr -> dout		ns	
Read	T_{OZX} (Maximum)	oe -> dout		ns	
Read	T_{OXZ} (Maximum)	oe -> dout		ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time		ns	
Write	t_{CLKL} (Minimum)	Clk		ns	
Write	t_{CLKH} (Minimum)	Clk		ns	
Write	t_{WCS} (Minimum)	we setup -> clk		ns	
Write	t_{WCH} (Minimum)	we hold -> clk		ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk		ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk		ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk		ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk		ns	
Write/Read	t_{CD} (Maximum)	clk -> dout		ns	
Read	t_{AD} (Maximum)	rd addr -> dout		ns	
Read	t_{OZX} (Maximum)	oe -> dout		ns	
Read	t_{OXZ} (Maximum)	oe -> dout		ns	

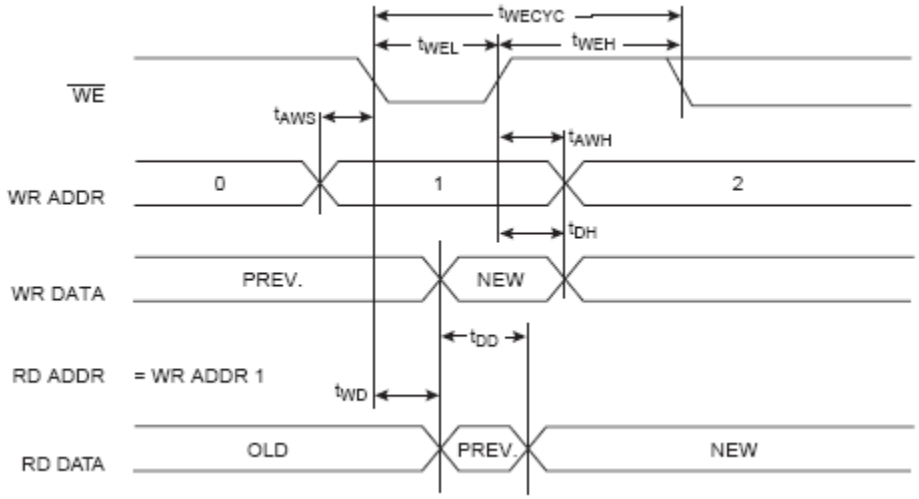
Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

12.4.1 FreeRAM Asynchronous Timing Characteristics

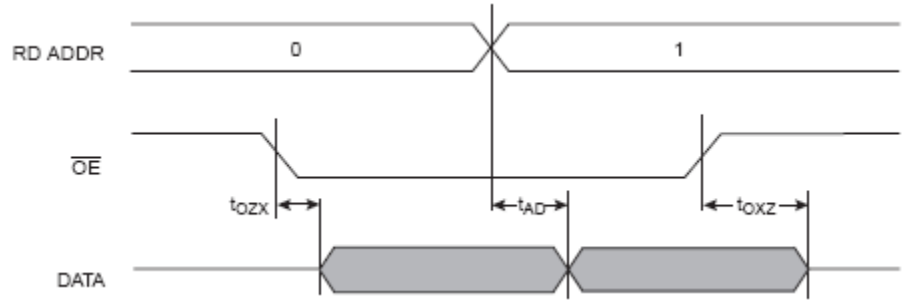
12.4.1.1 *Single-port Write/Read*



12.4.1.2 *Dual-port Write with Read*

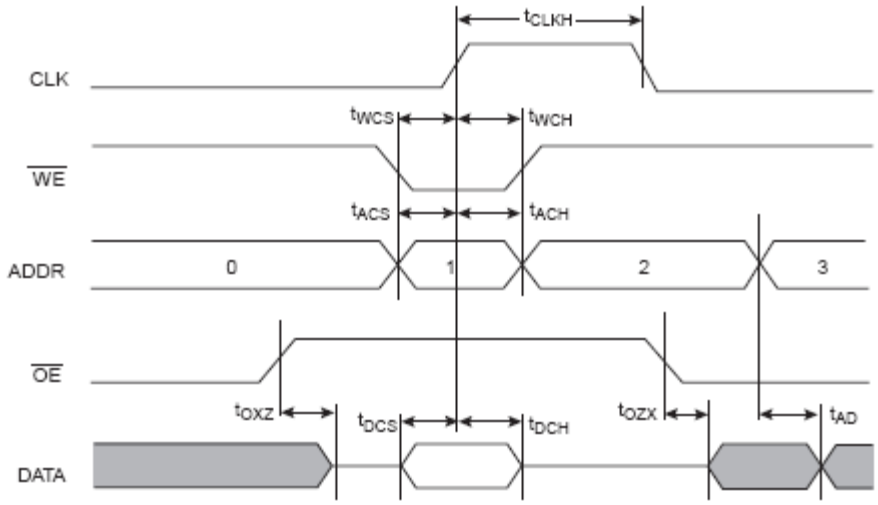


12.4.1.3 *Dual-port Read*

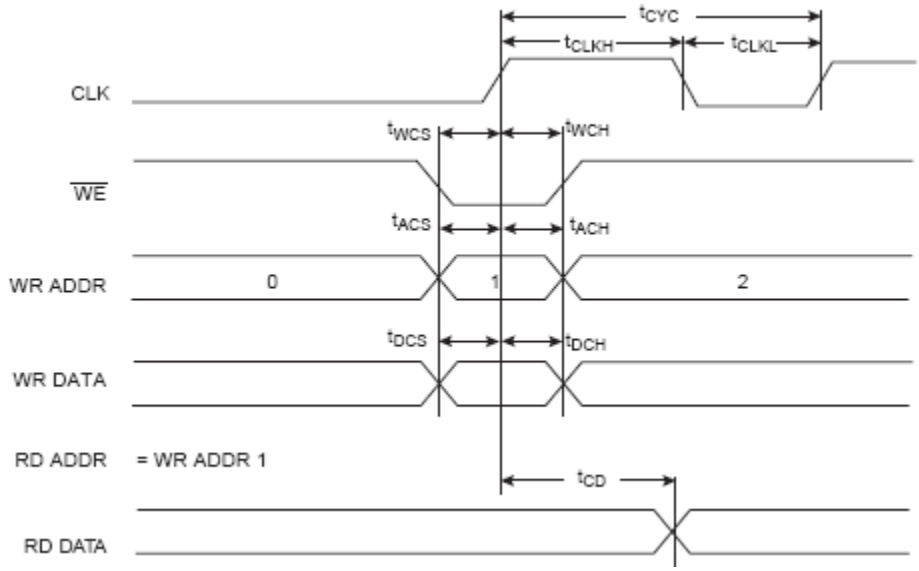


12.4.2 FreeRAM Synchronous Timing Characteristics

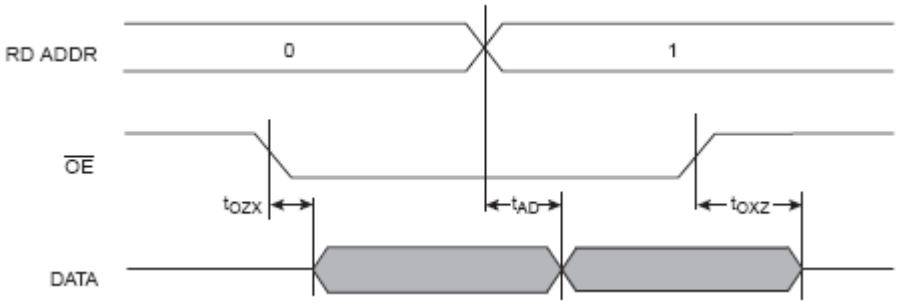
12.4.2.1 Single-port Write/Read



12.4.2.2 Dual-port Write with Read



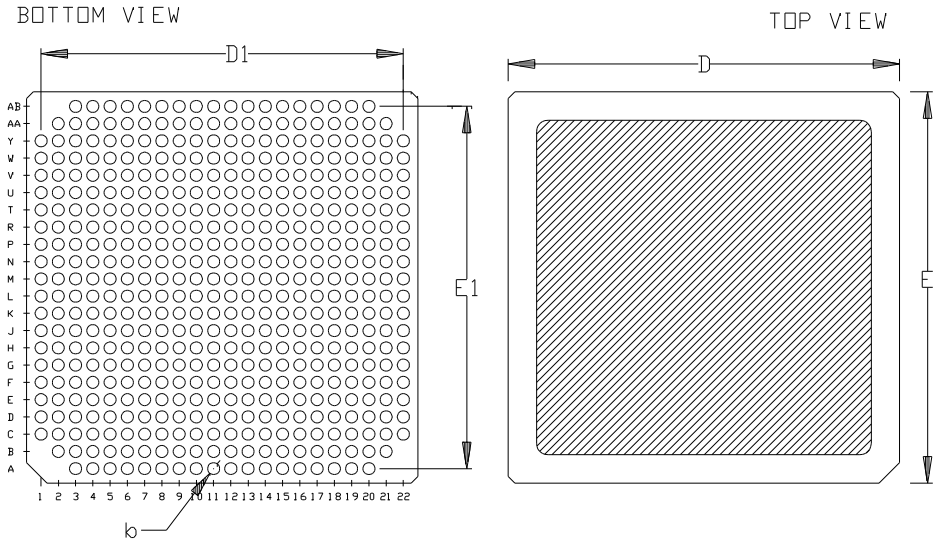
12.4.2.3 Dual-port Read

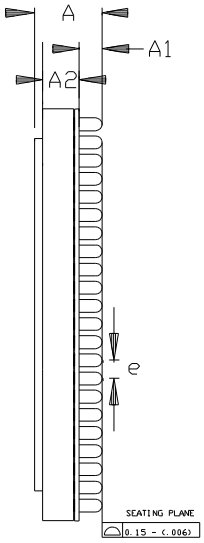


13. Packaging Information

MCGA 472

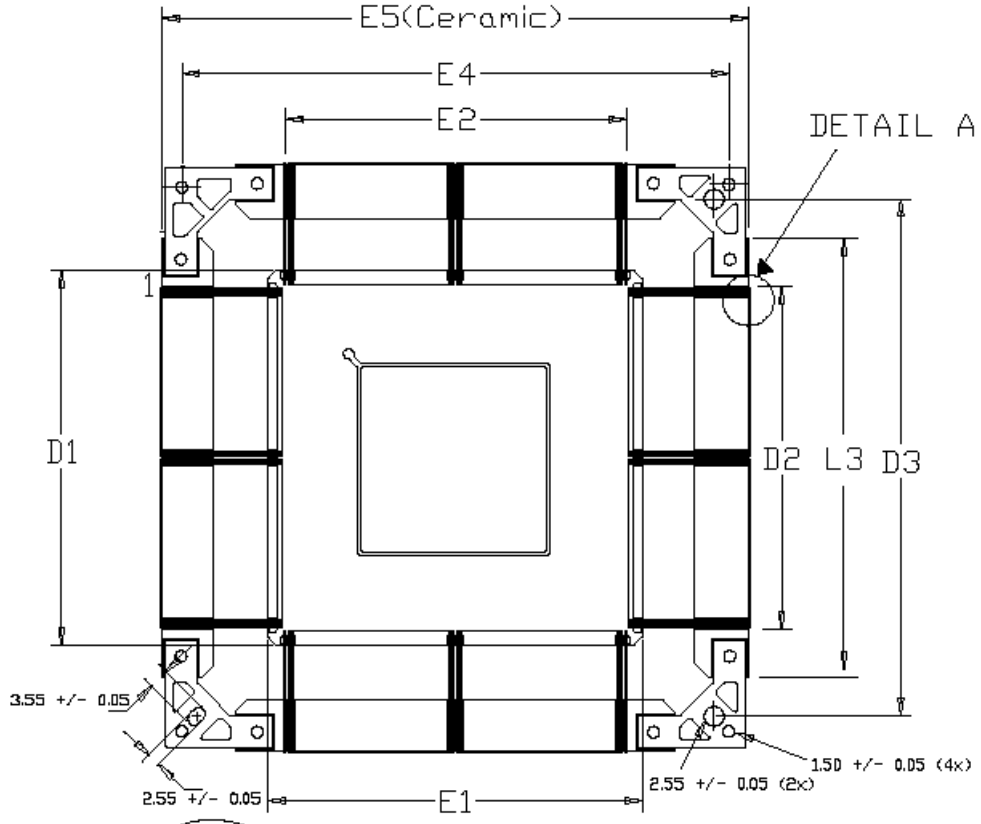
MCGA 472 (22 x 22 Pitch : 1,27mm)

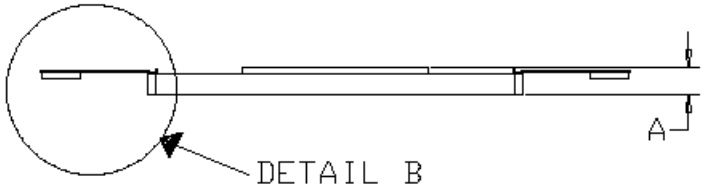


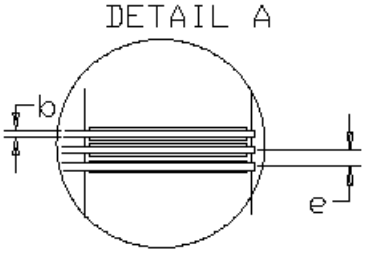


	MM		INCH	
	Min	Max	Min	Max
D/E	28,77	29,23	1.133	1.151
D1/E1	26,67(1.27x21)		1.05(.05x21)	
A1	1,40	1,85	.055	.073
A2	2,60	3.45	.102	.136
A	4.30	5.90	.169	.232
b	0,79	0,99	.031	.040
e	1,27 REF		.050	

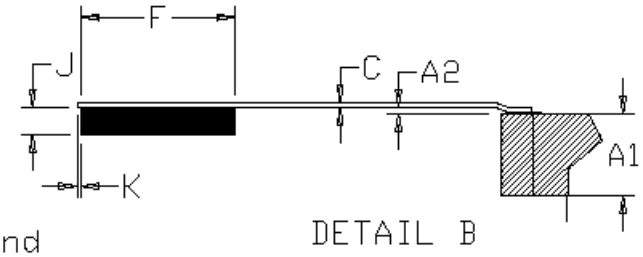
256-pin MQFPT







	mm (Ref)		inch	
	min	max	min	max
E1/D1	35.64	36.36	1.403	1.431
E2/D2	31.50 BSC		1.240 BSC	
D3	65.90 BSC		2.594 BSC	
E4	70.00 BSC		2.756 BSC	
E5	74.60	75.40	2.937	2.968
L3	56.30 BSC		2.217 BSC	
J	0.77	1.03	.030	.040
K	/	0.25	/	.010
F	7.05	8.45	.277	.332
C	0.10	0.20	.004	.008
A	2.50	3.22	.098	.127
A1	2.06	2.56	.081	.101
A2	0.20 BSC		.008 BSC	
e	0.50 BSC		.020 BSC	
b	0.20 TYP		.008 TYP	



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