炬力集成

ATJ 2051

PRODUCT DATA SHEET

(Version 1.1 08/2004)

Actions Semiconductor Co., Ltd

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1. Description

ATJ2051 is a single-chip for flash-based digital music player. It includes an audio decoder with a high performance DSP, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. ATJ2051 also provides an interface to flash memory, button and switch inputs, headphone, and microphone. ATJ2051's programmable architecture supports the MP3, WMA and other digital audio standards. For devices like USB-Disk, ATJ2051 can act as a USB mass storage slave device to personal computer system. Its low power consumption allows a long battery life, and an efficient flexible on-chip DC-DC converter allows many different battery configurations, including 1xAA, 1xAAA, 2xAA, 2xAAA and Li-Ion. Built-in Sigma-Delta DAC & a headphone driver to directly drive low impedance headphones. The ADC includes inputs for both Microphone and Analog Audio in to support voice recording features. Thus, the ATJ2051 provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio players with mass storage function.

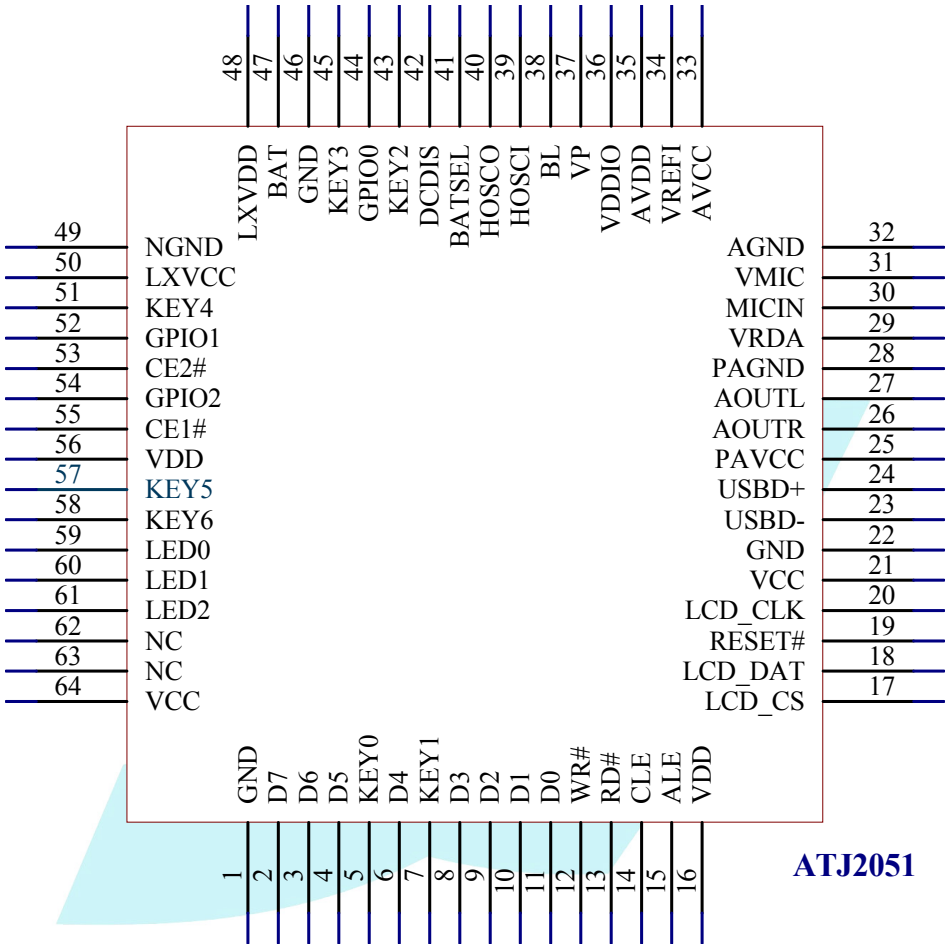
2. Features

- MPEG1/2/2.5 Audio Layer 1, 2, 3 decoder
- Support WMA Decoder
- Support MMC/SD card
- Digital Voice Recording with Actions Speech Algorithm
- 24 bits DSP Core with memory and on-chip Debug Support Unit (DSU)
- Integrated 8-bit MCU with DSU
- External up to 2(cs) x 64M/128M/256M/512M/1G/2G bytes Nand type Flash accessed by MCU or DMA
- Built-in DMA, CTC (Counter/Timer Controller) and interrupt controller for MCU
- Energy saving dynamic power management (PMU)
- Support USB2.0, Write speed(Max): 955k byte/s; Read speed(Max): 1033k byte/s
- Build in Stereo 18-bit Sigma-Delta DAC
- Build in Key Scan Circuit (5*2) and GPIO
- Support external serial Interface LCD driver
- Support 32 levels volume control
- Support Stereo 16-bit Sigma-Delta ADC for Microphone, sample rate at

8/12/16/22/24/32/48KHz

- MCU run at 24.576MHz(TYP), up to 60MHz
- SNR: 90dB (DAC TYP)
- Headphone driver output 2x11mW @16 Ohm(TYP)
- Operating Voltage: IO: 3.0V(TYP), Core: 2.0V(TYP)
- Standby Leakage Current: VCC: 35uA@3.0V(TYP) , VDD: 110uA@2.0V(TYP)
- Low Power Consumption, designed for greater than 15 (TYP) hours of operation on a single battery life. <65mW at typical MP3 decoder solution; <90mW at typical WMA decoder solution.
- 64-pin (10x10mm) LQFP package

3. Pin Description



Pin Sort by Number

Pin No.	Pin Name	I/O Type	Driver	Reset Default	Short Description
1	GND	PWR	/	/	Ground
2	D7	BI	/	L	Bit7 of ext. memory data bus
3	D6	BI	/	L	Bit6 of ext. memory data bus
4	D5	BI	/	L	Bit5 of ext. memory data bus
5	KEY0	I	1.9mA Driver	/	key scan circuit input

6	D4	BI	/	L	Bit4 of ext. memory data bus
7	KEY1	I	1.9mA Driver	/	key scan circuit input
8	D3	BI	/	L	Bit3 of ext. memory data bus
9	D2	BI	/	L	Bit2 of ext. memory data bus
10	D1	BI	/	L	Bit1 of ext. memory data bus
11	D0	BI	/	L	Bit0 of ext. memory data bus
12	WR-	O	/	H	Ext. memory write strobe
13	RD-	O	/	H	Ext. memory read strobe
14	CLE	O	/	L	Command latch enable for NAND type flash
	MMC_CMD	BI		/	Command/response for MMC/SD card
15	ALE	O	/	L	Address latch enable for NAND type flash
	MMC_DAT	BI		/	Serial data for MMC/SD card
16	VDD	PWR	/	/	Digital power
17	LCD_CS	BI	1.9mA Driver	Z	LCD CS PIN
18	LCD_DAT	BI	1.9mA Driver	Z	LCD DATA PIN
19	RESET-	I	SCU	H	System reset input (active low)
20	LCD_CLK	BI	1.9mA Driver	Z	LCD CLOCK PIN
21	VCC	PWR	/	/	Digital power
22	GND	PWR	/	/	Digital ground
23	USBD-	A	/	H	USB data minus
24	USBD+	A	/	H	USB data plus
25	PAVCC	PWR	/	/	Power supply for power amplifier(two bypass capacitors are 47uF and 0.1uF)
26	AOUTR	AO	/	/	Int. DAC right channel analog output
27	AOUTL	AO	/	/	Int. DAC left channel analog output
28	PAGND	PWR	/	/	Power amplifier ground
29	VRDA	AO	/	/	Bypass capacitor (typ. 0.47uF)

30	MICIN	AI	/	/	Microphone pre-amplifier input (0.8V-2.2V)
31	VMIC	AO	/	/	Power supply for microphone, 2.2V output
32	AGND	PWR	/	/	Analog ground
33	AVCC	PWR	/	/	Analog power
34	VREFI	AI	/	/	Voltage reference input (1.5V)
35	AVDD	PWR	/	/	Analog power
36	VDDIO	PWR	/	/	Power output (connect to VDD through a 4.7 Ohm (typ.) resistance)
37	VP	PWR	/	/	Power pin (When 2 Batteries mode, connect to BAT. Others mode Connect to VCC)
38	BL	PWR	/	/	Power output
39	HOSCI	AI	/	/	High frequency crystal OSC input
40	HOSCO	AO	/	/	High frequency crystal OSC output
41	BATSEL	I	/	/	Battery select. L: One Battery H: Two Batteries
42	DCDIS	I	/	L	Int. DC-DC control pin. H: Disable DC-DC. L: Enable DC-DC.
43	KEY2	I	1.9mA Driver	/	key scan circuit input
44	GPIO0	BI	1.9mA Driver	L	General purpose I/O port
	MMC_CLK	O		/	Clock output for MMC/SD card
45	KEY3	I	1.9mA Driver	/	key scan circuit input
46	GND	PWR	/	/	Ground
47	BAT	AI	/	/	Battery monitor pin
48	LXVDD	AO	/	/	VDD DC-DC pin
49	NGND	PWR	/	/	NMOS ground
50	LXVCC	AO	/	/	VCC DC-DC pin
51	KEY4	I	1.9mA Driver	/	key scan circuit input
52	GPIO1	BI	1.9mA Driver	Z	General purpose I/O port

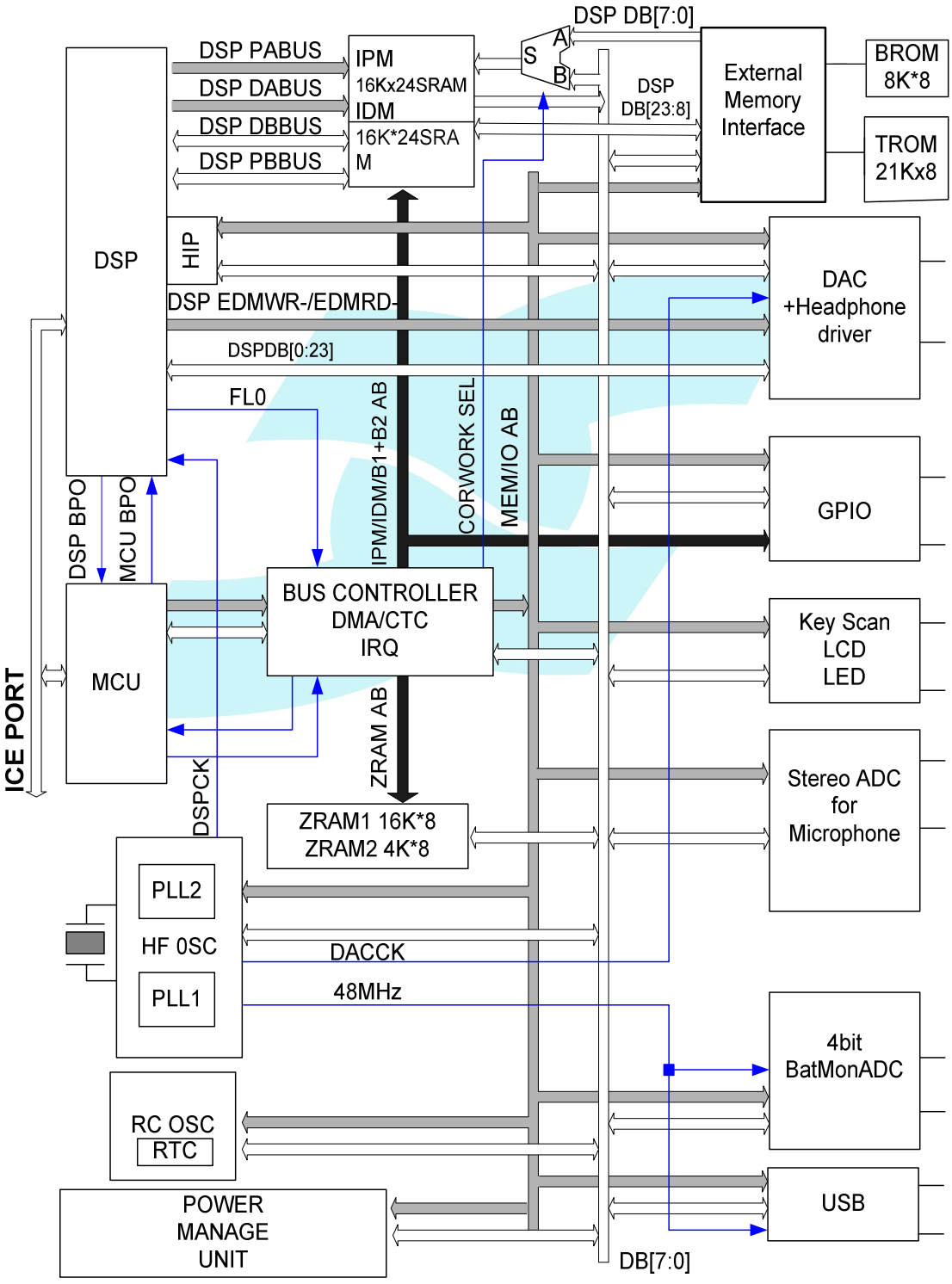
53	CE2-	O	/	H	Nand Flash chip enable (optional)
	MMC_CS-	O		/	Chip select for MMC/SD card
54	GPIO2	BI	1.9mA Driver	Z	General purpose I/O port
55	CE1-	O	/	H	Boot up Nand Flash chip enable (must be connected to Nand Flash)
56	VDD	PWR	/	/	Digital power
57	KEY5	O	1.9mA Driver	/	key scan circuit output
58	KEY6	O	1.9mA Driver	/	key scan circuit output
59	LED0	O	3.5mA Driver	L	LED 0 controller
60	LED1	O	3.5mA Driver	Z	LED 1 controller
61	LED2	O	3.5mA Driver	H	LED 2 controller
62	NC	/	/	/	Must not connect to high or low
63	NC	/	/	/	Must not connect to high or low
64	VCC	PWR	/	/	Digital power

Notes:

1. PWR----Power Supply 2. AI----Analog Input 3. AO----Analog Output 4. O----Output
5. I----Input 6. BI----Bi-direction 7. SCU----SCHIMITCU

4. Function Description

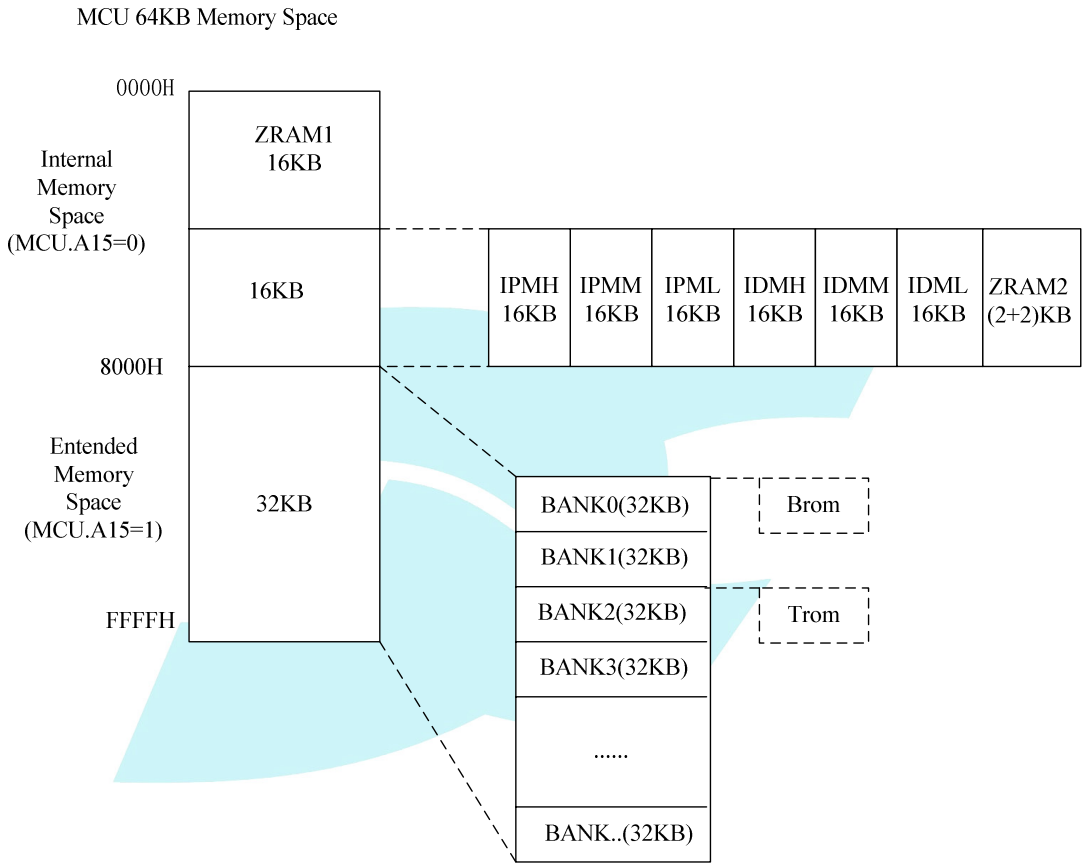
4.1 Functional Block Diagram



4.2 MCU Core

ATJ2051 integrates 8-bit MCU with on-chip ICE support. Instruction set is compatible with Z80. Process capability is controlled by software Up to 60 MHz.

ATJ2051includes 116 Kbytes of on-chip SRAM and 29Kbytes on-chip ROM. See the following flag for on chip memory mapping.



4.3 DSP Core

24-bit Harvard architecture DSP with on-chip ICE support is built in. It works with a memory word length of 24 bits. ATJ2051 has 16KB*24bit Program Memory (PM) and (16KB-256)*24bit Data Memory (DM). Memory-Mapped Register includes DAC interface. Process capability is controlled by software Up to 72 MIPS.

4.4 DMA Controller

ATJ2051 supports 3 kinds of DMA channels. DMA1/2 support Data exchange in Memory or IO. The last DMA is USB DMA.

4.5 General Purpose IO Ports

ATJ2051 has GPIO0, GPIO1, GPIO2. They are all general purpose IO ports.

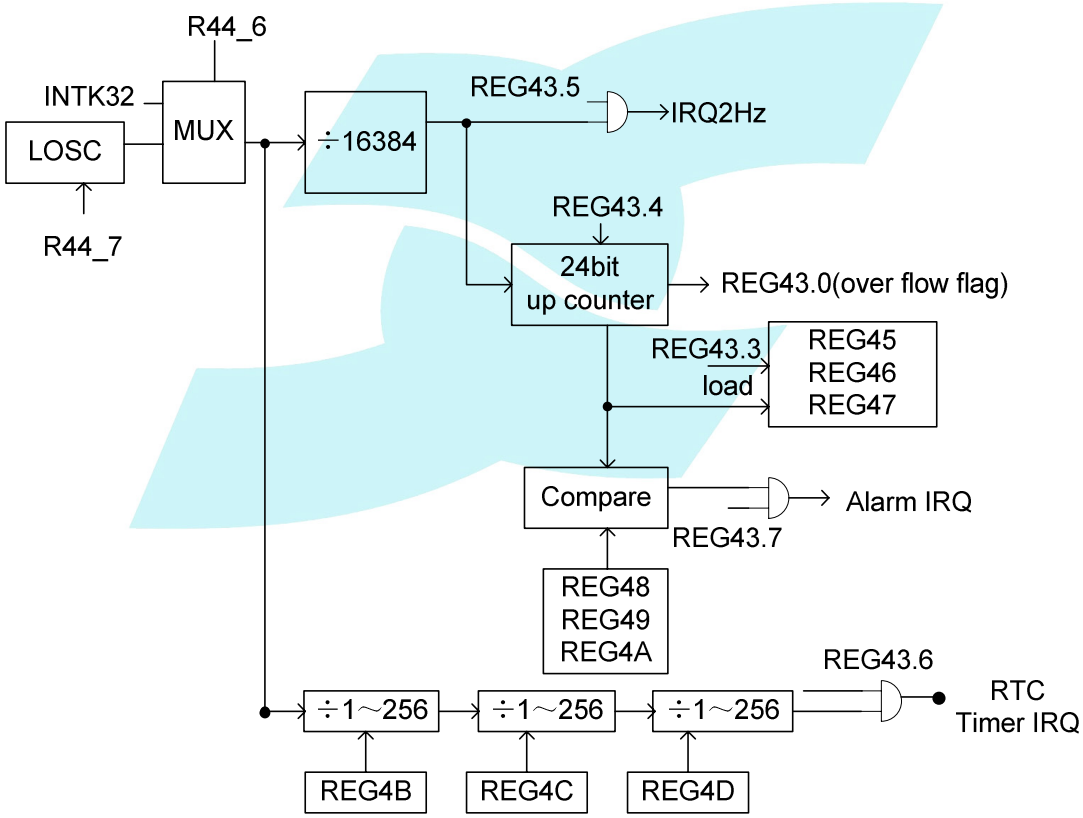
4.6 RTC/CTC/Watch Dog Timer

RTC is a 24-bit counter with the following function:

- Time
- Alarm
- Timer

CTC is a counter whose clock source is different with RTC's.

Watchdog can be set from 176-milisecond to 180-second with different step.



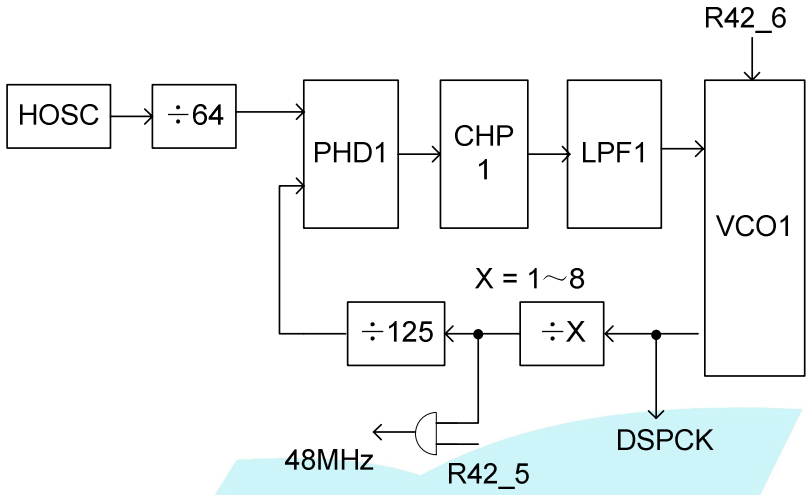
4.7 Oscillator/PLL

ATJ2051 supports 24.576MHz crystal, which is the system clock source.

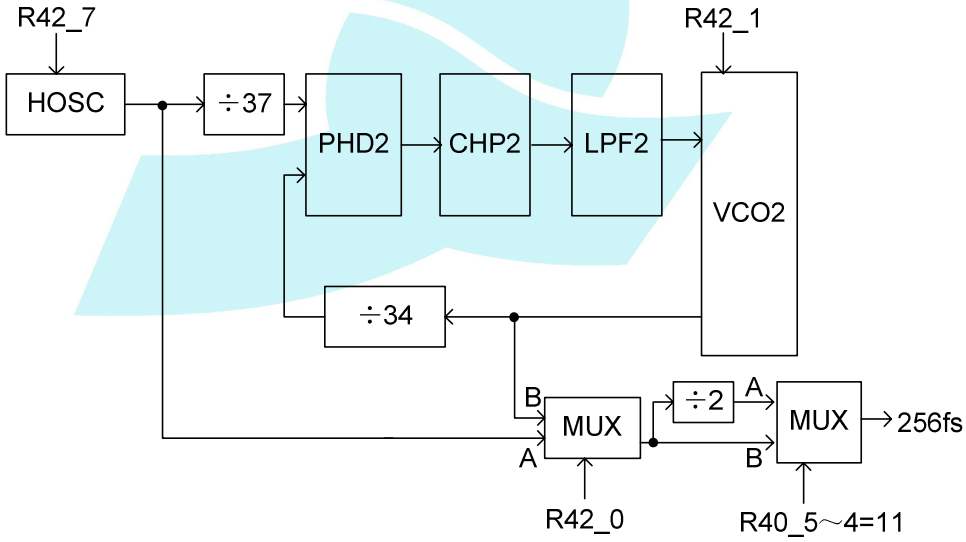
A low jitter PLL referenced to 24.576MHz is used to generate clock for DSP and for serial communication protocols such as USB, UART, etc. The clock used in serial communications is 48MHz so the PLL generates frequency at multiple of 48MHz to support DSP and serial

communication simultaneously. Another PLL referenced to 24.576MHz is used to generate 22.5792MHz for sample rate 44.1K/22.05KHz/11.025KHz.

PLL1 DIAGRAM



PLL2 DIAGRAM



4.8 Power Management Unit (PMU)

PMU consists of DC-DC converter, regulator and battery monitor.

In ATJ2051, there are two DC/DC converters and one liner regulator. One DC/DC converter is for VCC power supply and another is for VDD. The liner regulator is for VDD power supply when two battery mode or other conditions where need less external components.

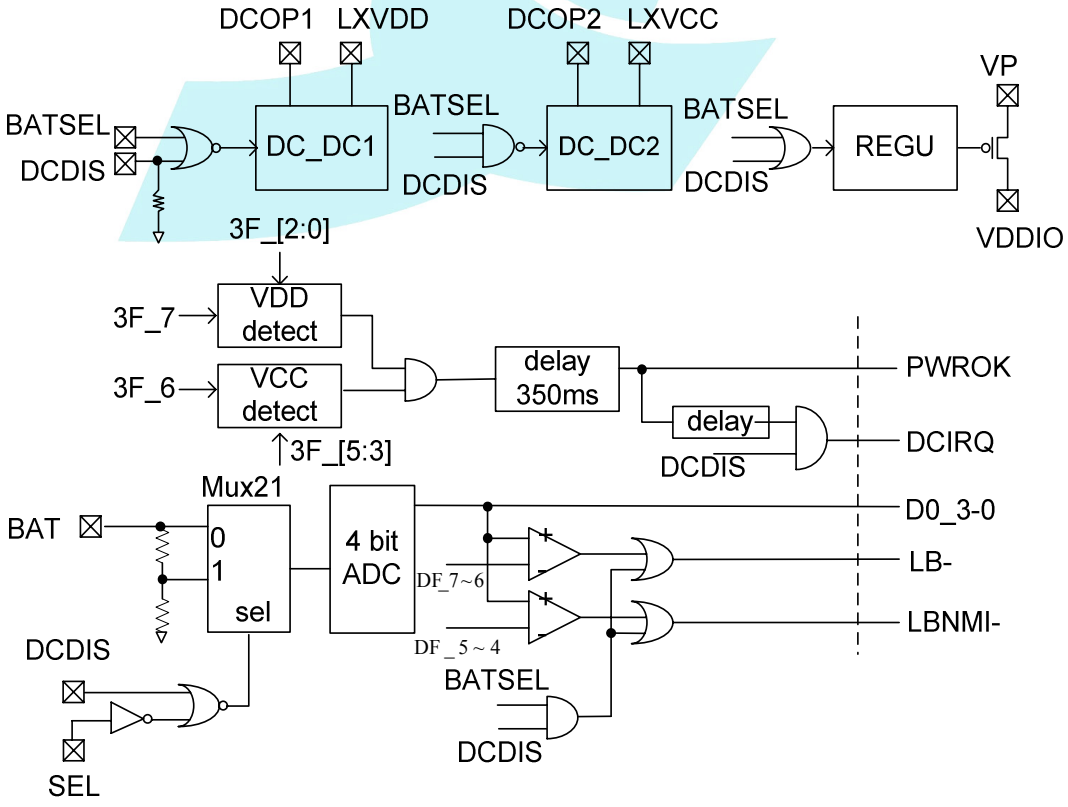
In ATJ2051, the default value of VCC is 3.0V and VDD is 2.0V. The regulator's default output is 2.0V;

all three values can be controlled by Registers. The VCC is from 2.8V to 3.3V; VDD is from 1.6V to 2.3V; the regulator is the same as VDD.

ATJ2051supports one-battery mode, two-battery mode, USB power supply or DC power line-in. There are two pins for mode configurations. One is “DCDIS”; the other is “BATSEL”, the truth table as follow:

DCDIS	BATSEL	DC/DC1(VDD)	DC/DC2(VCC)	Regulator	Mode descriptions
0	0	Yes	Yes	No	One battery with more external components, but more efficiency
0	1	No	Yes	Yes	Two battery
1	0	No	Yes	Yes	One battery with less external components, but less efficiency
1	1	No	No	Yes	USB power or DC power line-in

The pin of “DCDIS” has an on-chip pull down resistor. There is a built-in super low speed and low resolution ADC for battery monitor in ATJ2051. The level of minimum battery voltage warning can be configured by registers; the range is from 0.98V to 1.22V. The voltage level of resetting system can be controlled by register; the range is from 0.9V to 1.14V.

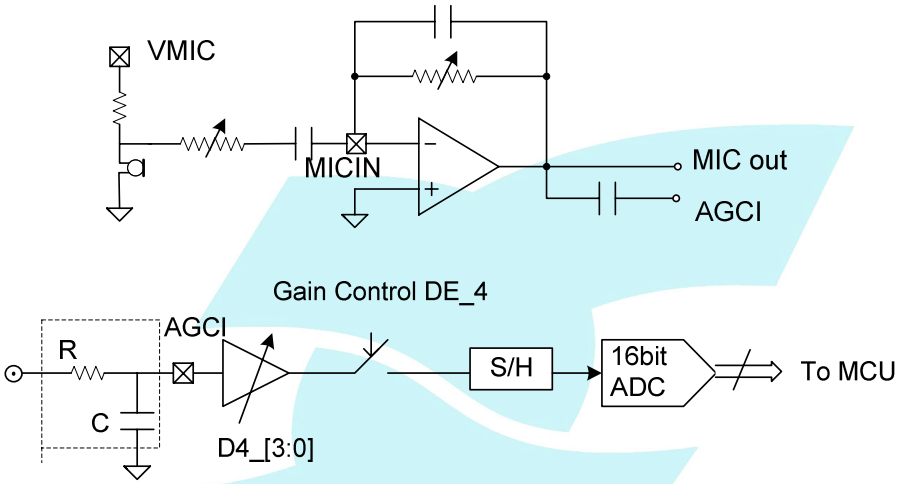


4.9 ADC

There are 2 Analog-to-Digital Converters integrated in ATJ2051:16-bit Σ-Δ ADC is for MIC Input and 4-bit ADC for Battery Monitor. The internal microphone amplifier has gain for recording. The VMIC pin is the power supply (2.2V) for microphone.

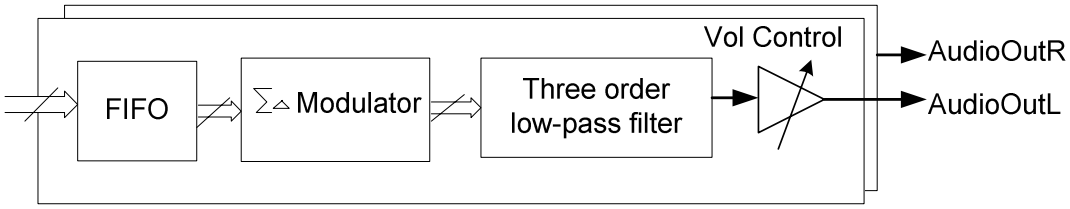
The audio ADC is an 18 bits sigma delta Analog-to-Digital Converter. Its input source can be selected from MIC amplifier, and it has two FIFO.

MIC & ADC Parts



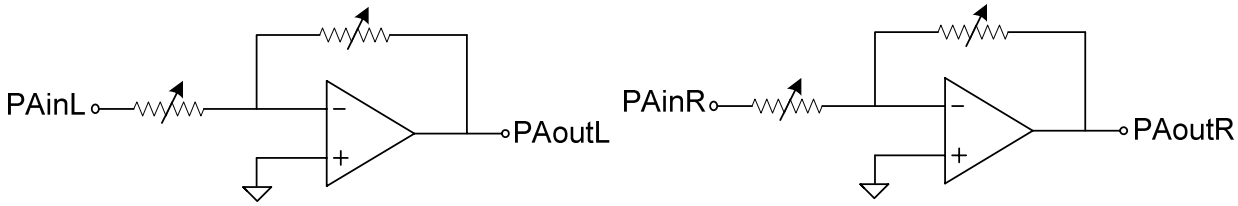
4.10 DAC

ATJ2051's DAC3 is an on-chip Sigma-Delta Modulator, composed by a high performance DAC. And the DAC analog block refers to the following diagram. The DAC interface supports 4-level play back FIFO (8 x 20-bit PCM data for L/R channel) and variable sample rates, such as 48K/ 44.1K / 32K/ 24K/ 22.05K/ 16K/ 12K/ 11.025K/ 8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24.576MHz to support 44.1K/2 2.05 K/ 11.025KHz with 256xFS clock for over-sampling, while 24.576MHz supports 48K/ 32K/ 24K/ 16K/ 12K/ 8KHz with 256XFS for over-sampling.

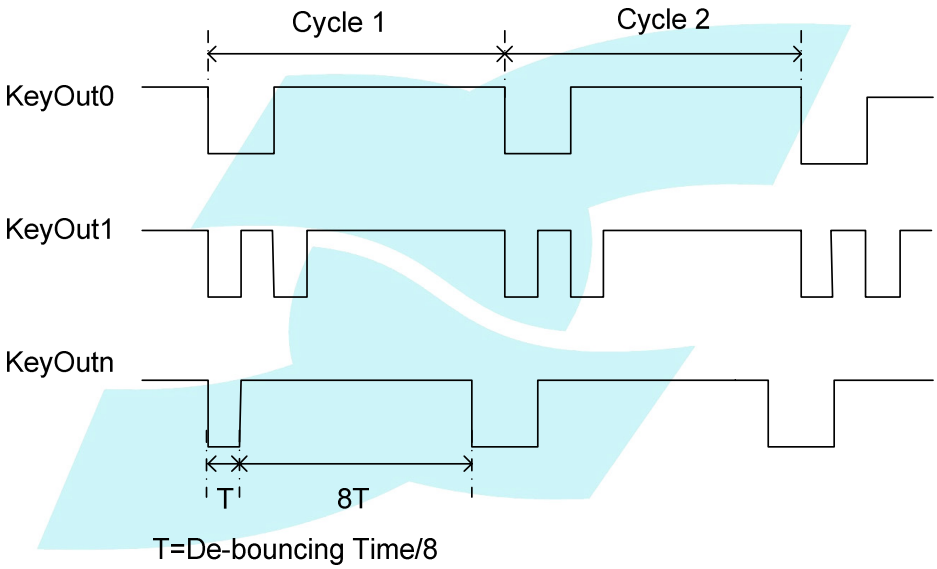


4.11 Headphone Driver

The output power of ATJ2051's amplifier is 13mW.(each channel)



4.12 Key Scan Interface



Key Scan Timing

When key scan circuit is enabled, ATJ2051 will scan the keyboard periodically. It drives pin Key out N scan pulse in turn. When any key is pressed, the corresponding Key out N will send out the scan pulse. When a key is pressed, pin Key in N connecting the key will be found low level.

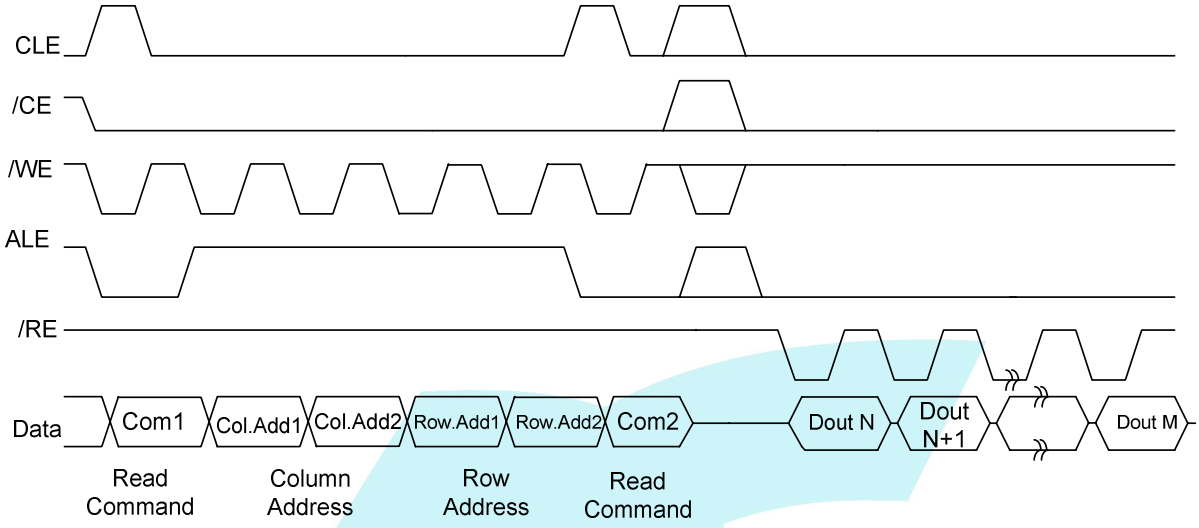
There are 12 internal 8-bit registers for key value latch per scan. But only another one register (Key Scan Data Register) for MCU may access key value. Those 12 internal registers are mapped into this register, and an internal pointer is used to point to the current register to return scan data when read. Any IO write to this register will clear the internal register, and the pointer will increase by 1 and point to the next register after read is performed.

4.13 External Memory Interface

ATJ2051 can support NAND type flash from 32M to 1G bytes.

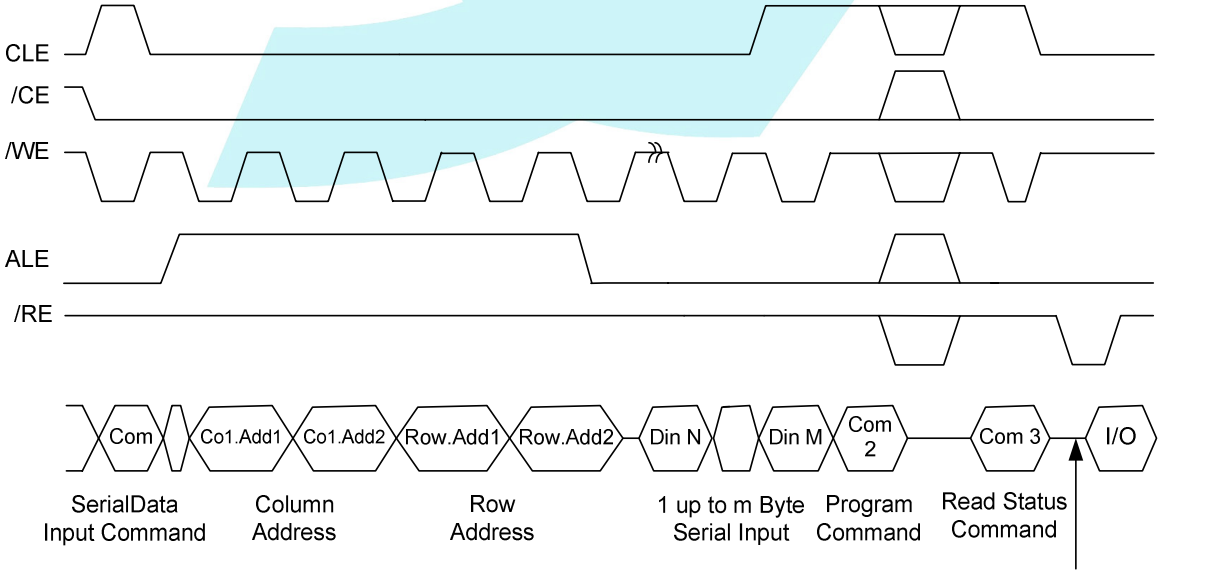
See the following for NAND flash Read/Write timing.

Read:



Nand Flash Read timing

Write:



Nand Flash Program timing

4.14 USB 2.0(FULL SPEED) SIE

Communications with the host can be made via speed-programmable USB interface (compliant with USB SPEC 2.0).

4.15 LCD Interface

ATJ2051 supports serial interface. Serial interface:

- Use LCD_CS to select LCD.
- Use LCD_CLK to generate WR clock
- Use LCD_DAT to WR data

4.16 LED Interface

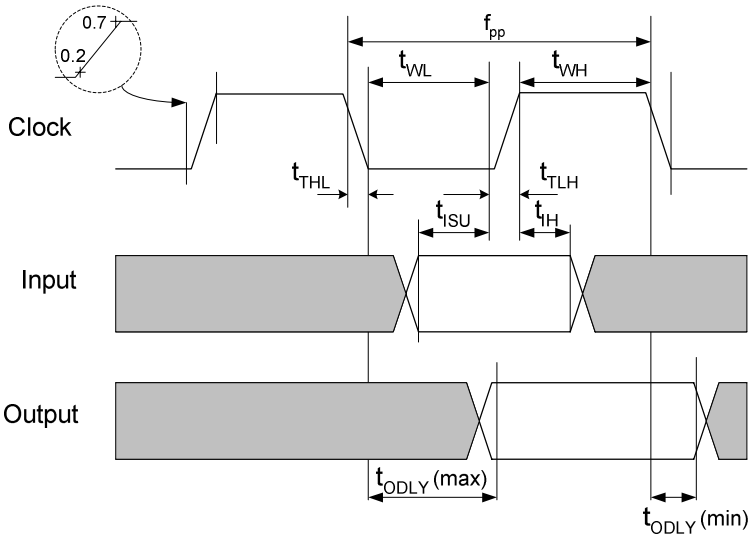
ATJ2051 supports most three LED display

- Use LED0 to drive first LED
- Use LED1 to drive second LED
- Use LED2 to drive third LED.

4.17 MMC/SD Card Interface

Multimedia Card/SD Card needs serial input/output interface to send command and receive data. The timing is indicated by the following figure:

MMC Interface Timing



Shaded areas are not valid.

Parameter	Symbol	Typical	Unit
Clock Frequency Data Transfer Mode	f_{PP}	12	MHZ
Clock low time	t_{WL}	30	ns
Clock high time	t_{WH}	25	ns
Clock rise time	t_{TLH}	15	ns
Clock fall time	t_{THL}	15	ns
Input setup time	t_{ISU}	10	ns
Input hold time	t_{IH}	10	ns
Output delay time	t_{ODLY}	20	ns

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	2.0 V	-0.5 to +2.7	V
	VCC	3.0V	-0.5 to +3.6	V
Input voltage	V_I	VCC >= 3.3	-0.5 to +3.9	V
		VCC < 3.3	-0.5 to VCC+0.6	V
Storage temperature	T_{stg}	/	-65 to +150	℃

Note:

1. T_O = 25℃ (Operating Temperature)
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

5.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz	/	15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	/	15	pF

Note: T_O = 25℃, VCC = 0 V.

5.3 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX	Unit
High-level output voltage	V_{OH}	I_{OH} = -2mA	2.4	/	/	V
Low-level output voltage	V_{OL}	I_{OL} = 2mA	/	/	0.4	V
High-level input voltage	V_{IH}	/	0.7*VCC	/	VCC + 0.6	V
Low-level input voltage	V_{IL}	/	-0.3	/	0.4VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, V_I = VCC, 0 V	/	/	±10	uA
Output leakage current	I_{LO}	VCC = 3.6 V, V_I = VCC, 0 V	/	/	±5	uA
GPIO Drive	$I_{DRIVER1}$	GPOA0,GPOA1,GPOA2	/	2.60	/	mA
	$I_{DRIVER2}$	Other GPIO	/	1.25	/	mA
Supply Current (Two battery mode)	I_{VDD}	In Full speed mode (MCU run 24.576MHz in internal SRAM, DSP run 36MIPS)	/	40	60	mA
		In Standby mode	50	110	350	uA
	I_{VCC}	In Full speed mode (MCU run 24.576MHz in internal SRAM, DSP run 36MIPS)	9	16	40	mA
		In Standby mode	25	35	70	uA

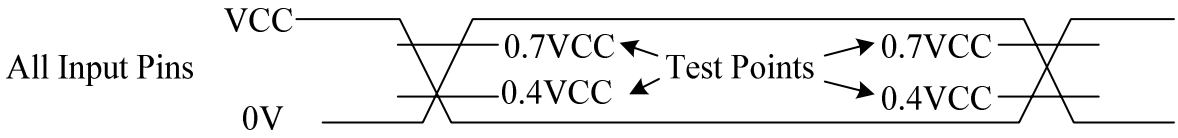
Notes:

1. TA = -10℃ to +70℃, VDD = 2.0 V, VCC = 3.0 V
2. I_{VDD} is the total power supply current for 2.0 V power supply. I_{VDD} is applied to the LOGIC, PLL and OSC blocks.

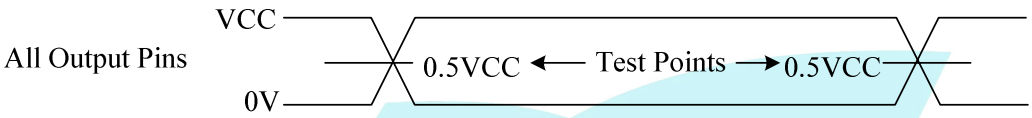
3. I_{VCC} is the total power supply current for 3.0 V power supply. I_{VCC} is applied to the USB, IO, TP and AD blocks.

5.4 AC Characteristics(TA = -10℃to +70℃, VDD = 1.8 to 2.7 V, VCC = 2.7 to 3.6 V)

5.4.1 AC test input waveform



5.4.2 AC test output measuring points

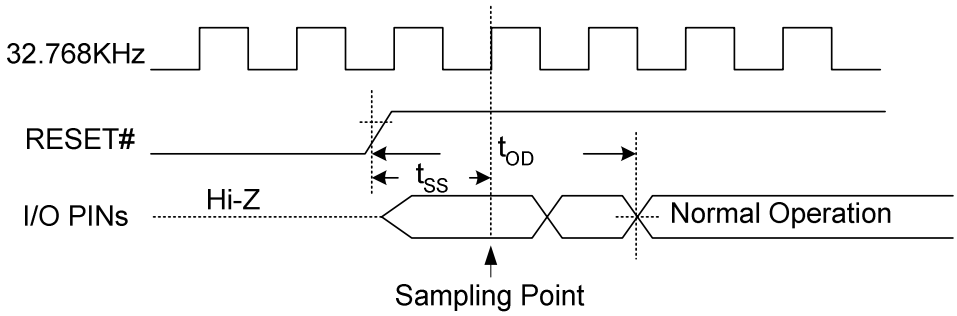


5.4.3 Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	160		us

5.4.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}			61.04	us
Output delay time (from RESET#)	t_{OD}		61.04		us

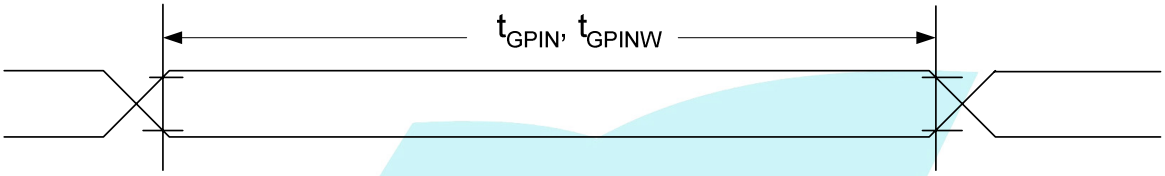


5.4.5 GPIO Interface Parameter

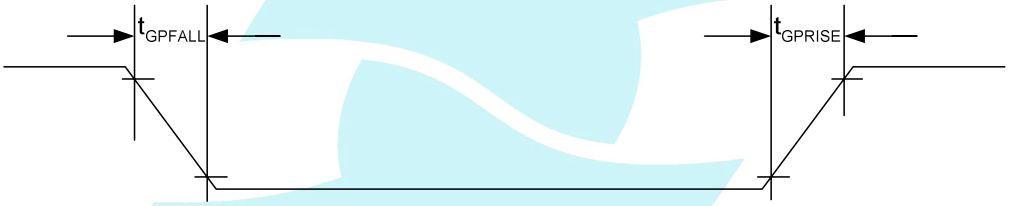
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	11/ f_{MCUCLK}		s
GPIO input rise time	t_{GPRISE}			200	ns
GPIO input fall time	t_{GPFALL}			200	ns
Output level width	t_{GPOUT}		11/ f_{MCUCLK}		s

Notes: f_{MCUclk} is the frequency that MCU is running upon.

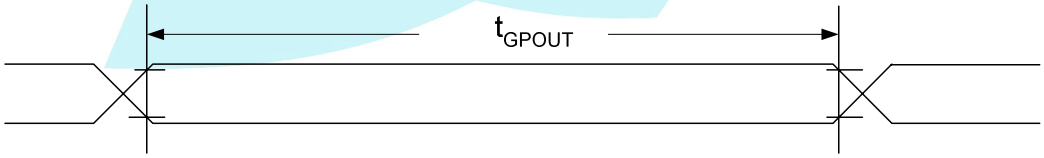
Input level width



Input rise/fall time

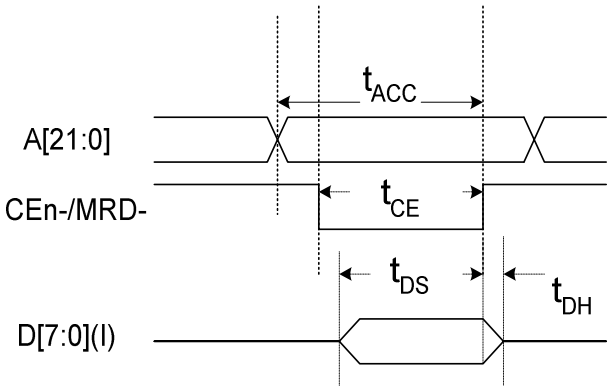


Output level width

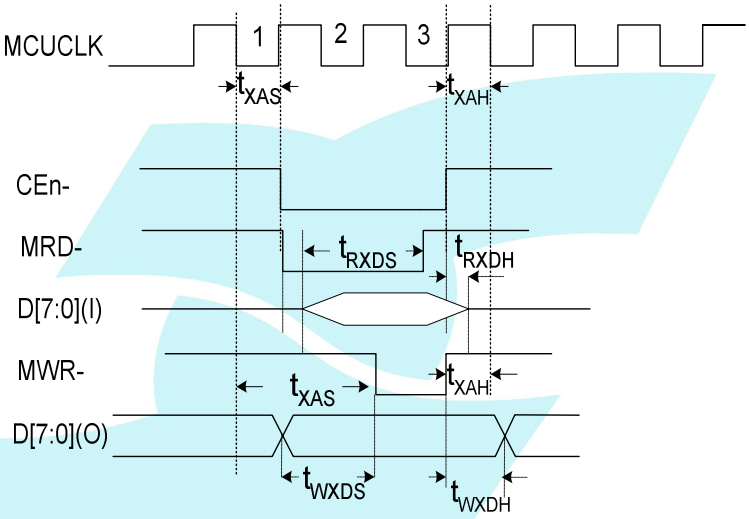


5.4.6 Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC}	HOSC=24.576MHz	102		ns
Data access time (from CEx#)[Note]	t_{CE}	HOSC=24.576MHz	82		ns
Data input setup time	t_{DS}	HOSC=24.576MHz	0		ns
Data input hold time	t_{DH}	HOSC=24.576MHz	0		ns



5.4.7 External System Bus Parameter



Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	0.5T		ns
	t_{XAS}	Memory Write	1.5T		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		0.5T		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		0	T	ns
Data output hold time(from command signal)Note 1	t_{WXDH}		3	0.5T	ns
Data input setup time (to command signal)Note 1	t_{RXDS}		0	2T	ns
Data input hold time(from command signal)**Note 1**	t_{RXDH}		0		ns

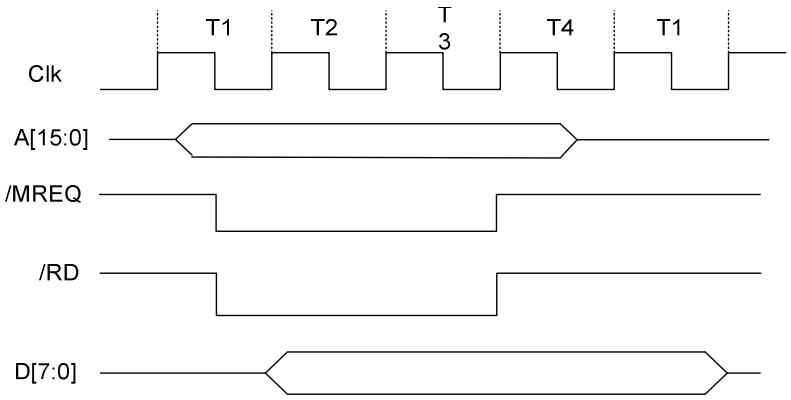
Notes:

1. RD#, WR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1 / f_{MCUCLK}.

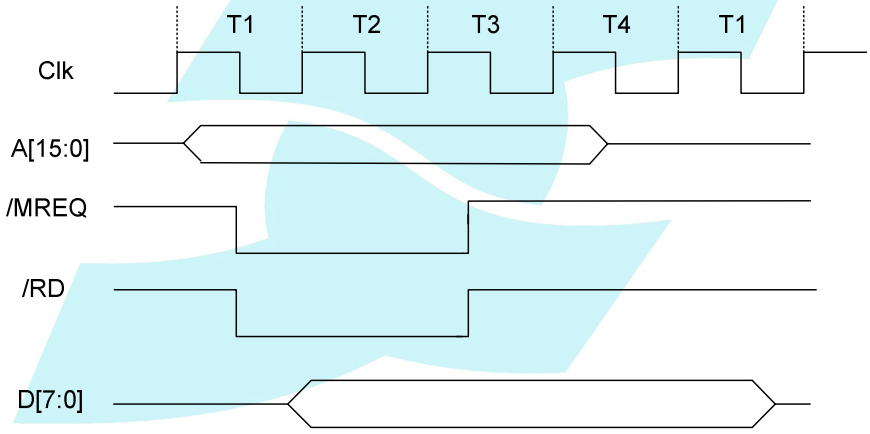
5.4.8 Bus Operation

Instruction Fetch Timing



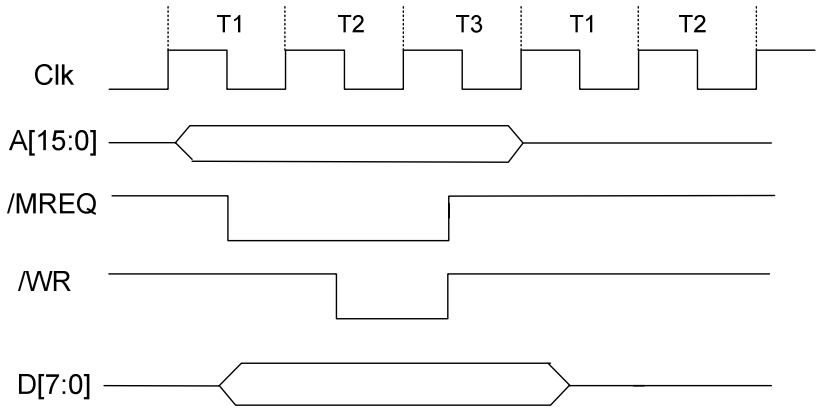
Instruction Fetch Timing

Memory Read Timing



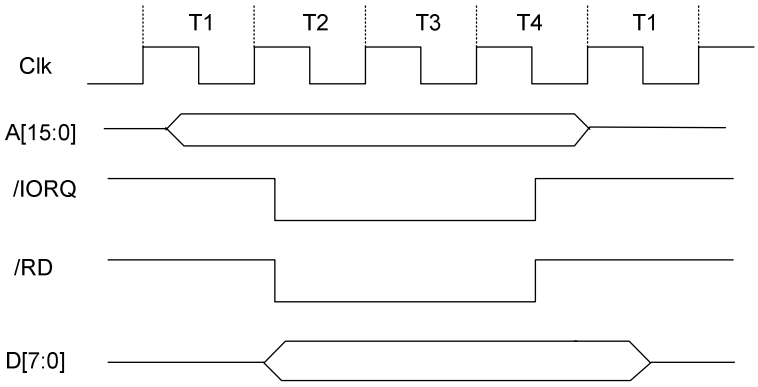
Memory Read Timing

Memory Write Timing



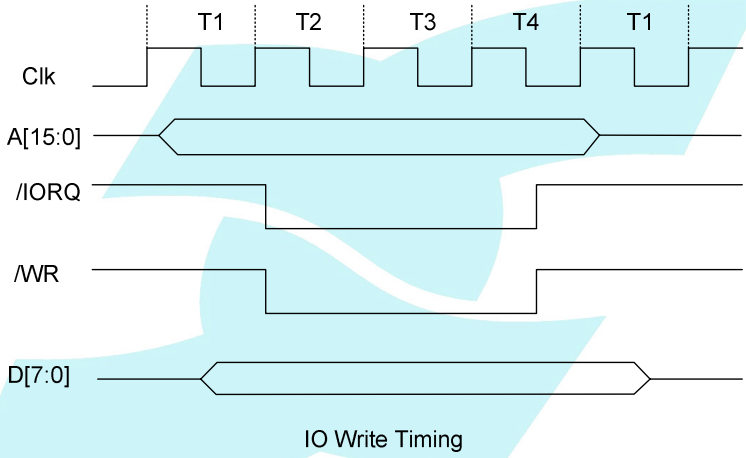
Memory Write Timing

IO Read Timing



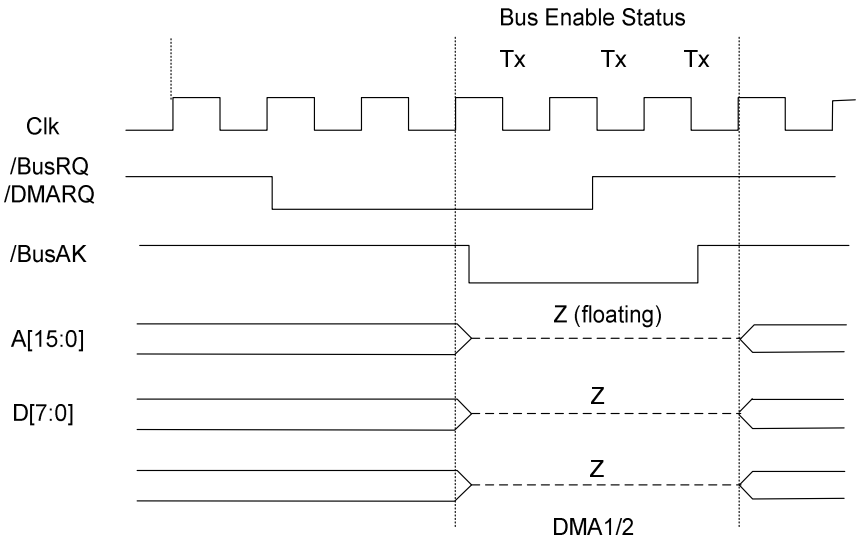
IO Read Timing

IO Write Timing



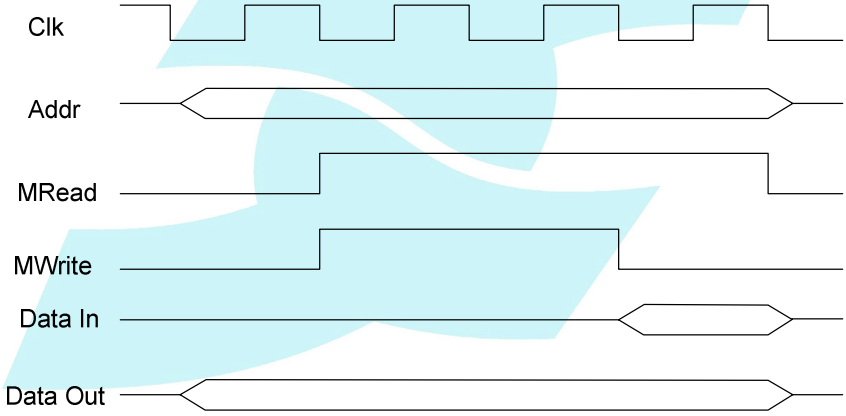
IO Write Timing

DMA1/2 Timing



DMA1/2 Timing

DSP Read/Write Timing



DSP Read/Write Timing

5.4.9 A/D Converter Characteristics

Characteristics	Min	Typ.	Max	Unit
Dynamic range		60		dB
Total Harmonic Distortion + Noise	50	53	55	dB
Frequency Response (20-13KHz)			±1	dB
Full Scale Input Voltage(Gain=0dB)		800		mVpp

5.4.10 Headphone Driver Characteristics Table

Characteristics	Min	Typ.	Max	Unit
Dynamic Range –60 dBFS Input		87		dB
Total Harmonic Distortion + Noise	70	73	75	dB
Frequency Response 20-20KHz			±0.6	dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.6	2.4	Vpp
Inter channel Isolation (1KHz)		91		dB
Inter channel Gain Mismatch(1KHz)		0.025		dB

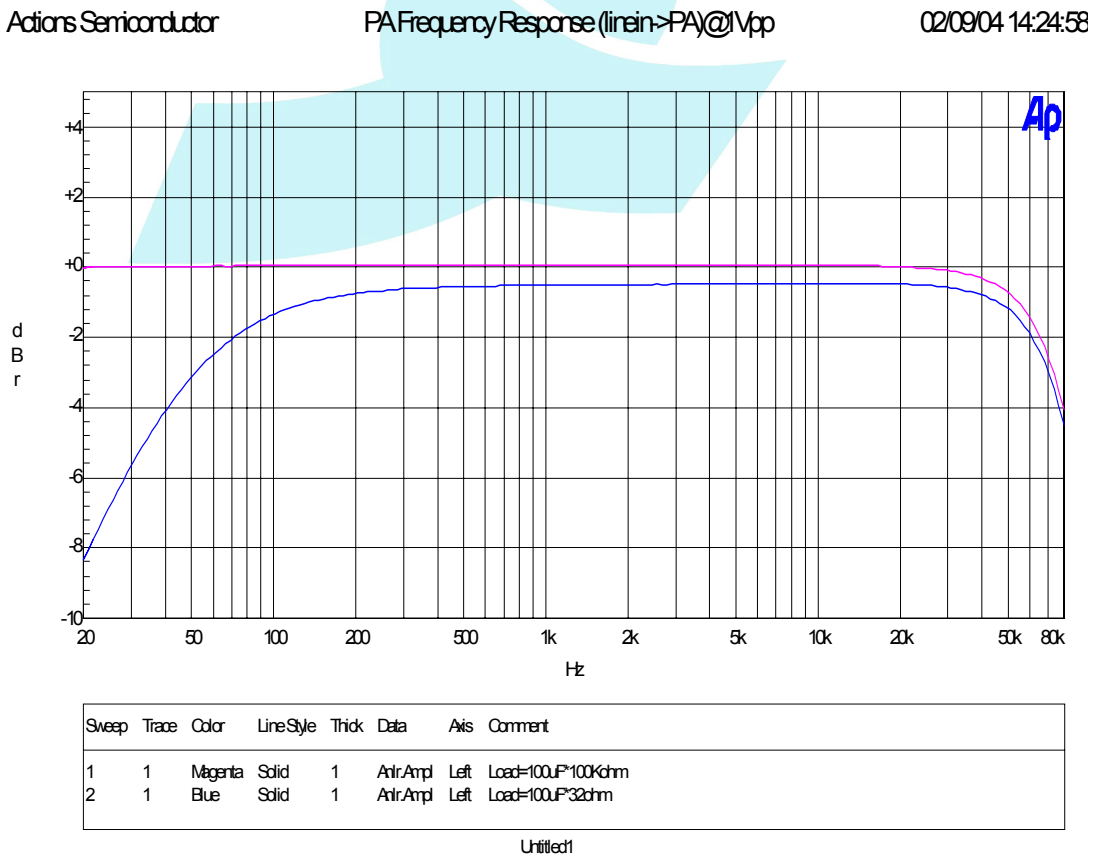
Note:1. T_A =-10 - +70℃, VDD = 2.0 V, VCC = 3.0 V

2. Sample Rate=32 KHz

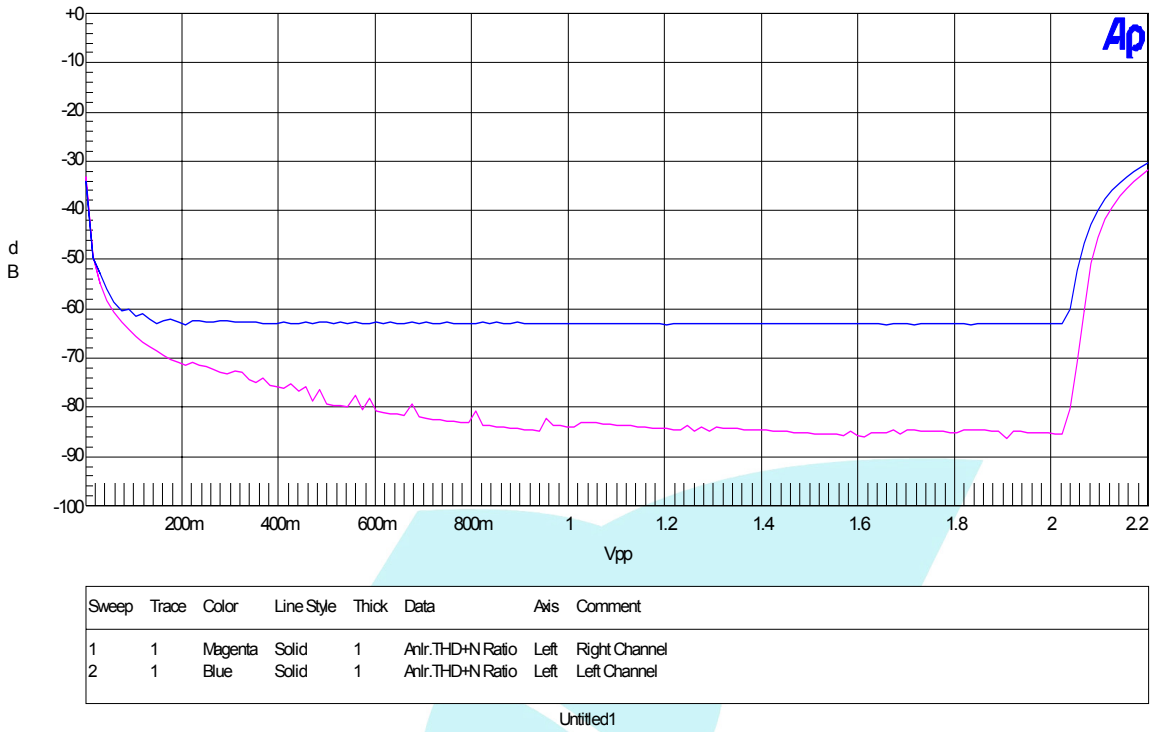
3. Bias Current=26uA

4. Volume Level=0x1F

Frequency Response Diagram of Headphone Driver



THD + N Amplitude Diagram of Headphone Driver



6. MCU/DSP Dissipation (IVDD VS. Frequency)

6.1 MCU Dissipation

(VBAT=1.5V, DSP under reset, VDD=2.0V, MCU runs in internal SRAM)

Clock Source	Divisor factor	IVDD(Max)
32.768KHZ	/(1—1024)	350uA
24.576MHz	/1	5.9mA
	/2	3.3mA
	/4	1.9mA
	/8	1.2mA
	/16	1.9mA
	/32	0.7mA

	/64	0.6mA
	/128	0.58mA
	/256	0.56mA
	/512	0.55mA
	/1024	0.54mA

6.2 DSP Dissipation (VBAT=1.5V, MCU run LOSC, VDD=2.0V, Vcc =3.0V)

DSP Speed (MIPS)	IVDD (Max)
6	3.49mA @ VDD=2.0V
12	6.52mA @ VDD=2.0V
24	11.24mA @ VDD=2.0V
36	16.24mA @ VDD=2.0V
48	21.08mA @ VDD=2.0V
60	28.5mA @ VDD=2.3V
72	33.6mA @ VDD=2.3V
84	38.7mA @ VDD=2.3V

7. Recommended Soldering Conditions

7.1 Soldering Conditions

Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions
Infrared ray reflow	Peak package's surface temperature: 235℃
	Reflow time: 30 seconds or less (210℃or more)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 3 days (10 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note: Maximum number of days during which the product can be stored at the temperature of 25℃ and relative humidity of 65% or less after dry-pack package is opened.

Caution: Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

7.2 Precaution against ESD for Semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

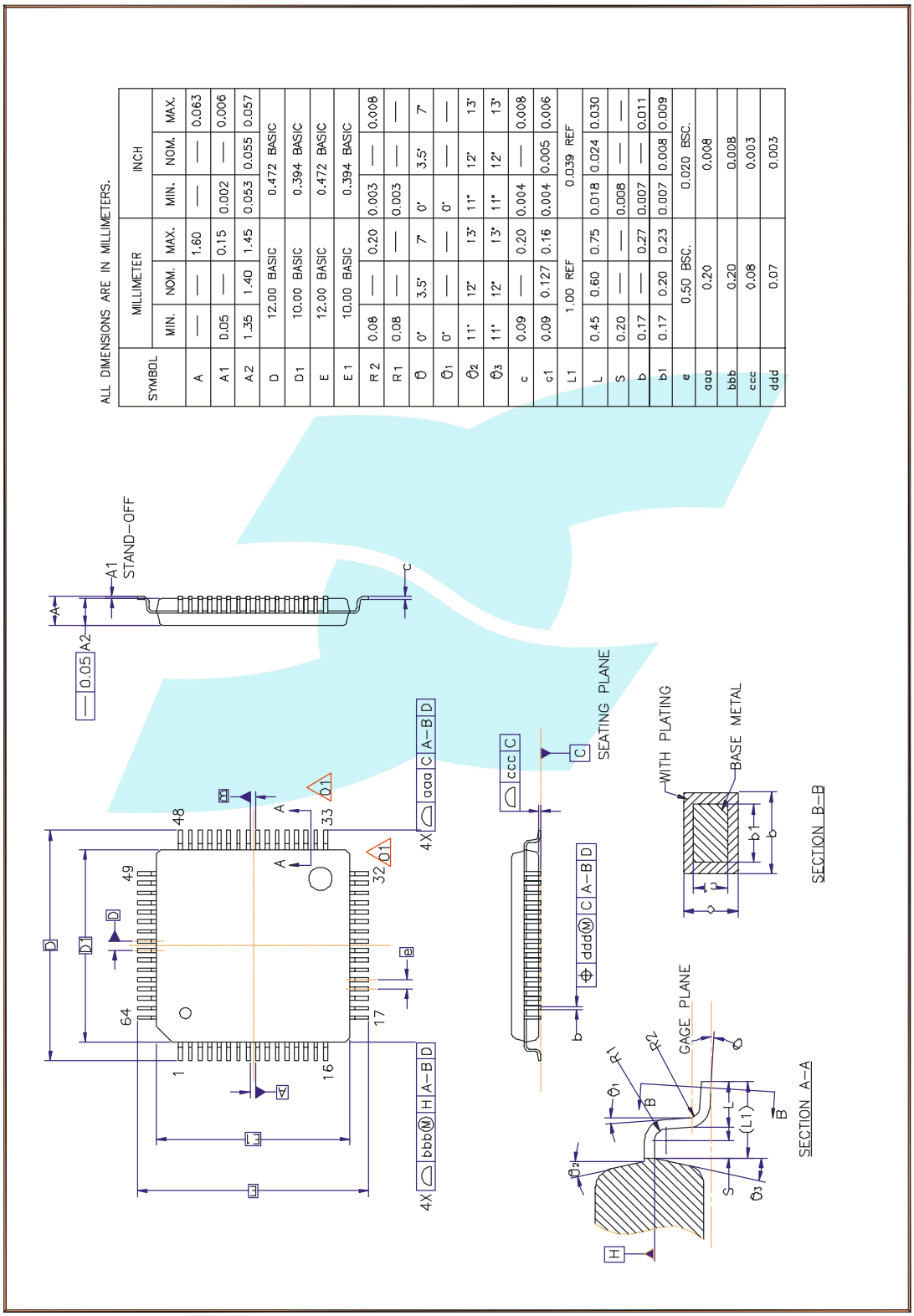
7.3 Handling of Unused Input Pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

7.4 Status before Initialization of MOS Devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

8. Package Drawings



ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	—	0.27	0.007	—	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.07			0.003	

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