ATJ2157 Datasheet

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Revision History

Version	Revision Content	Date
V1.0	Initial version	2020/9/23
V1.1	Modify PIN9 name from *VRBGR* to VREF	2020/11/2
V1.2	Fixed MFP function without I2S0_RX of GPIO6/7/8/9/15/30/31/32/33	2022/4/30

1 Introduction

The ATJ2157 is a new generation ultra-low power and highly-integrated single-chip of digital multimedia solution for devices such as audio and video players. It is a low-cost, low-power, high-efficiency digital multimedia chip which is based on M4F MCU with hardware accelerator. It is designed for portable audio/video product applications such as dedicated audio player, voice recoder, Car- audio player etc.

The ATJ2157 includes an audio decoder and a video decoder with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music or movie and uploading voice recordings. ATJ2157 also provides an interface to flash memory, SD/MMC card, LED/LCD, button and switch inputs, headphones, and microphone, and FM radio input and control. Its embedded audio codec supports almost all digital audio standards, and the embedded video codec supports Motion JPEG. For devices like USB-Disk or UAC device, it can act as a USB mass storage or USB HID slave device to personal computer system.

The ATJ2157 has low power consumption to allow long battery life and an efficient flexible on-chip DC-DC converter that supports Li-on battery only. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphone. The A/D includes inputs for both Microphone and Analog Audio in to support voice recording and FM radio integration features. The chip supports multi-task operation which allows user to hear song and look picture simultaneously. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio and video players.

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1.1 Key Features

1.2Features

System

- Up to 288MHz M4F processor Core
- Built-in 224KB RAM and 64KB ROM.
- Built-in 32KB Icache and 32KB Dcache.
- Support 24MHz OSC and 32.768KHz OSC
- Built-in Internal 32KHz RC oscillator
- Energy saving with dynamic power management, supporting Li-on only
- Support RTC and built-in 4 timers with timer capture.
- Support AES
- Support TRNG
- Support CHIP unique ID
- Support FFT/FIR/IIR hardware engine
- Integrated Motion JPEG Video Decoder, up to 30fps@QVGA resolution

Audio

- Three channels ADC, Two MIC/AUXIN/FM Analog ADC channels: SNR>98dB, THD<-86dB. And One AEC Analog ADC channel: SNR>80dB.
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/96kHz.
- Supports Single-Ended or full difference input analog microphone.
- Supports up to 4 PDM digital microphone.
- Supports PDM Rx and TX.
- Build in stereo sigma-delta DAC, In differential output mode SNR>100dB, THD+N<-85dB.
- DAC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/96k.
- Build in stereo 18mW PA (Power Amplifier) for headphone.
- Support two I2S TX and Two I2S Rx with master mode and slave mode.
- I2S Support Sample Rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96k/192K.

Storage

- Support up to 4CE NandFlash, including SLC, MLC, TLC and small block NandFlash with 8/24/40/60 bit ECC
- Support Managed NANDFLASH, Such as LBANAND, PBANAND, EFNAND, E2NAND eMMC eSD, etc.
- NAND interfaces: Support asynchronous; NV-DDR, NV-DDR2 (ONFI 3.0); toggle nand 2.0
- Support TLC and Randomizer Algorithmic
- Multi Media Card Specification Version 4.3(1/4/8 bit mode)
- Secure Digital Card Specification Version 3.0(1/4-bit mode)
- Support Booting up directly from NANDFLASH/eMMC/SPI NorFlash/SPI NandFlash.

Flexible I/O

- Support 50 GPIO at most
- Support 9 LRADC at most
- Support 9 PWM for lamp controller at most
- Support Uart, TWI and SPI
- Support USB2.0 HS, Compatible with EHCI.

Manufacture

- Package at QFN68 (7x7mm2)

1.3 Block Diagram

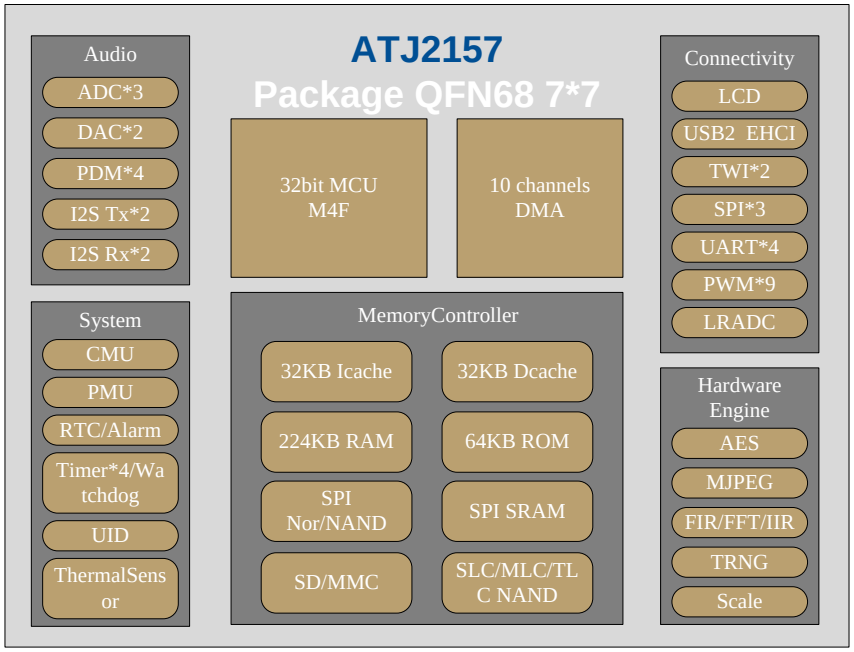


Figure 1-1 ATJ2157 Block Diagram

1.4 ATJ2157 Pin Assignment

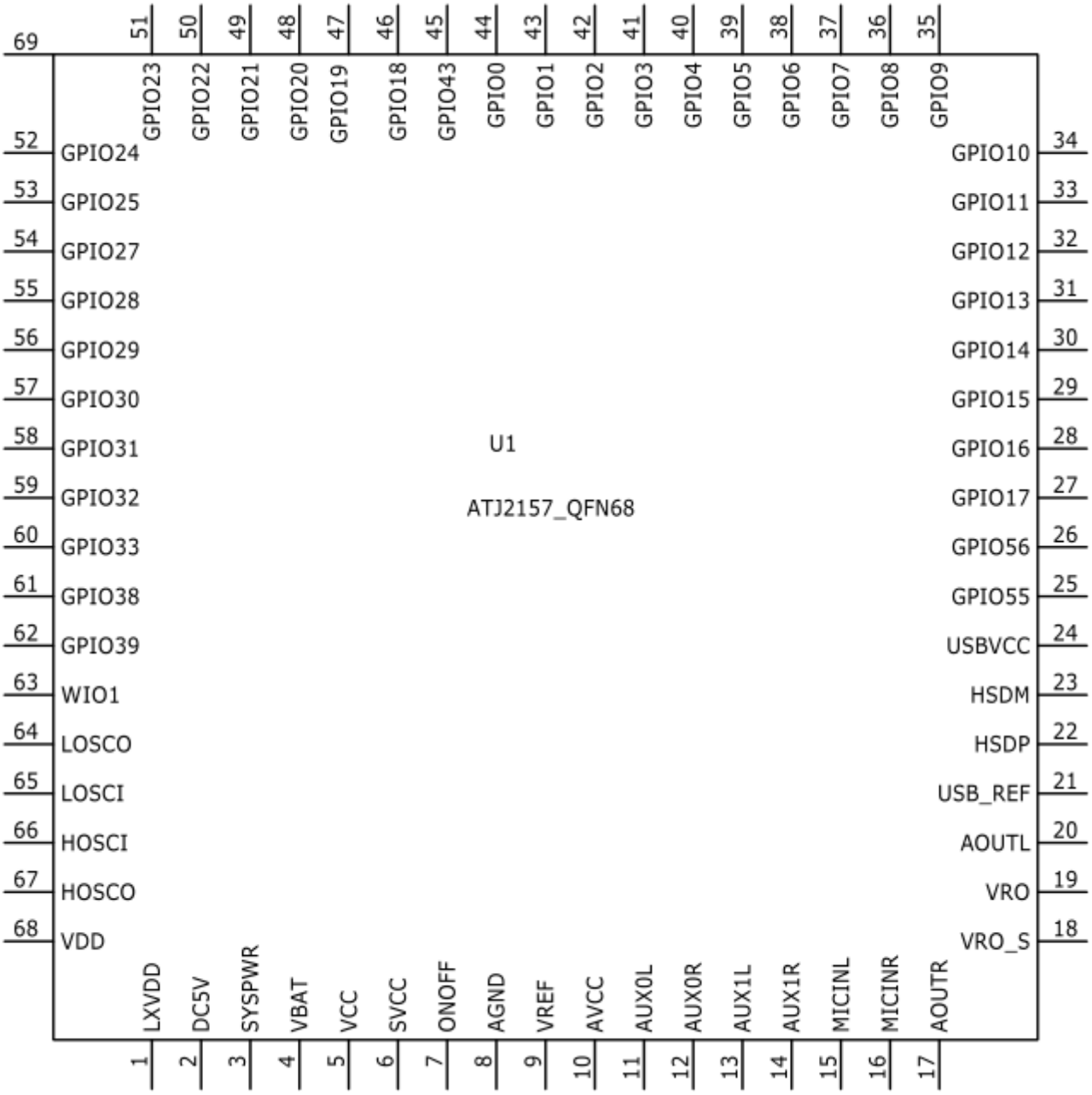


Figure 1-2 ATJ2157 schematic pin assignment

1.5 ATJ2157 Pin Description

Table 1-1 ATJ2157 PIN description

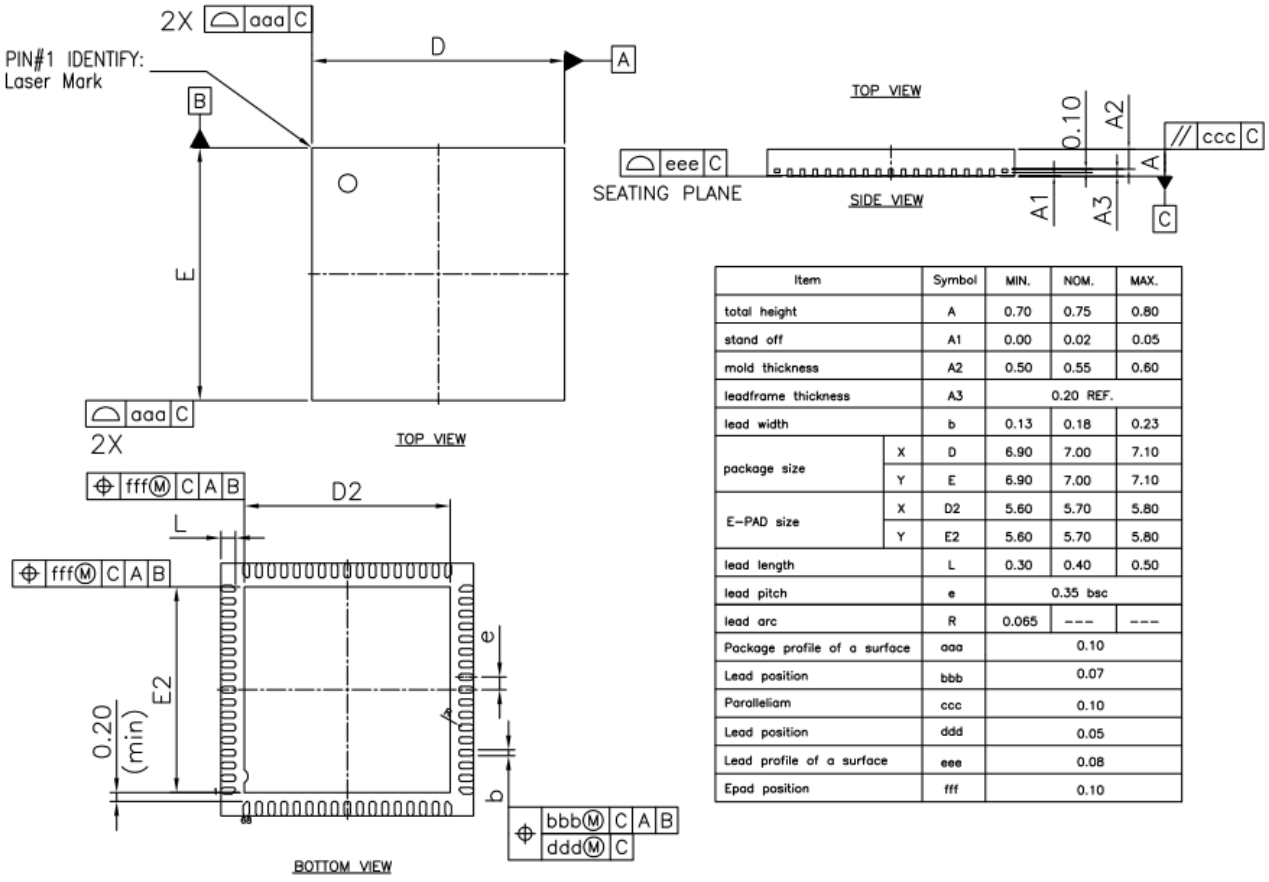
PIN No	PIN NAME	MFP	GPIO Initial state
1	LXVDD		
2	DC5V		

3	SYSPWR		
4	VBAT		
5	VCC		
6	SVCC		
7	ONOFF		
8	AGND		
9	VREF		
10	AVCC		
11	AUX0L	GPIO66/AUX0L/AUX0LP	*
12	AUX0R	GPIO67/AUX0R/AUX0LN	*
13	AUX1L	GPIO68/AUX1L/AUX0RN	*
14	AUX1R	GPIO69/AUX1R/AUX0RP	*
15	MICINL	GPIO64/MICINL/MICINLP/DMIC01_CLK	*
16	MICINR	GPIO65/MICINR/MICINLN/DMIC01_DAT	*
17	AOUTR	GPIO74/AOUTR/AOUTRP	*
18	VRO_S	GPIO75/VROS	*
19	VRO	GPIO73/VRO	*
20	AOUTL	GPIO72/AOUTL/AOUTLP	*
21	USB_RREF		
22	HSDP		
23	HSDM		
24	USBVCC		
25	GPIO55	GPIO55/SPI1_D7/SD1_DAT0/UART3_TX/PWM7/IIS1RX_BCLK/LRADC9	Z
26	GPIO56	GPIO56/SPI1_DQS/SD1_DAT1/UART3_RX/PWM8/IIS1RX_LRCLK	Z
27	GPIO17	GPIO17/NF_DQS/SPI1_MISO/UART3_TX/PWM7/IISORX_BCLK/DMIC23_CLK/LRADC6	*
28	GPIO16	GPIO16/NF_RB1/SPI1_MISO/UART3_TX/PWM7/IISORX_MCLKCLK/DMIC23_CLK/LRADC5/T3_CAP	*
29	GPIO15	GPIO15/NF_CE4/LCD_CE1/SPI0_SS/SD0_DAT0/UART3_RTS/TWI1_DAT/PWM6/IISORX_MCLKCLK/IIS1TX_DOUT/VMIC1	*
30	GPIO14	GPIO14/NF_CE3/LCD_CE0_HSYNC/SPI0_CLK/SD0_CMD/UART3_CTS/TWI1_CLK/PWM5/IISORX_DIN/LRADC10	*
31	GPIO13	GPIO13/NF_CE2/LCD_CE1/SPI0_MOSI/SD0_CLK0/UART3_RX/PWM4/IISORX_LRCLK/DMIC23_DAT/LRADC9/VMIC0	*
32	GPIO12	GPIO12/NF_CE1/SPI0_MISO/SD0_DAT0/UART3_TX/PWM3/IISORX_BCLK/DMIC23_CLK/LRADC8/T2_CAP	*
33	GPIO11	GPIO11/NF_WRB/LCD_WR_DCLK/SPI1_D2/SD0_CMD/UART2_RTS/TWI0_DAT/PWM2/IISORX_MCLK/DMIC23_DAT/LRADC7	*
34	GPIO10	GPIO10/NF_RDB/LCD_RDE_LDE/SPI1_D3/SD0_CLK1/UART2_CTS/TWI0_CLK/PWM1/IISOTX_DOUT/DMIC23_CLK/LRADC7	*
35	GPIO9	GPIO9/NF_ALE/LCD_TE/SPI2_MOSI/SD0_DAT7/UART2_RX/PWM0/IISOTX_LRCLK/IIS1TX_DOUT/DMIC01_DAT	*
36	GPIO8	GPIO8/NF_CLE/LCD_RS_VSYNC/SPI2_MISO/SD0_DAT6/UART2_TX/PWM8/IIS1TX_LRCLK/DMIC01_CLK/LRADC4	*
37	GPIO7	GPIO7/NF_D7/LCD_D7/SPI2_CLK/SD0_DAT5/UART1_RTS/TWI1_DAT/PWM7/IIS1TX_BCLK/DMIC01_DAT/LRADC3	*

38	GPIO6	GPIO6/NF_D6/LCD_D6/SPI2_SS/SD0_DAT4/UART1_CTS/TWI1_CLK/PWM6/IIS1TX_MCLK/DMIC01_CLK/LRADC2	*
39	GPIO5	GPIO5/NF_D5/LCD_D5/SPI0_D3/SDC0_DAT3/UART1_RX/PWM5/IIS0TX_BCLK/PDMTX_DAT/T3_CAP	*
40	GPIO4	GPIO4/NF_D4/LCD_D4/SPI0_D2/SDC0_DAT2/UART1_TX/PWM4/IIS0TX_MCLK/PDMTX_CLK/T2_CAP	*
41	GPIO3	GPIO3/NF_D3/LCD_D3/SPI0_MOSI/SDC0_DAT1/UART0_RTS/TWI0_DAT/PWM3/IIS1RX_DIN/SPI0_MISO	*
42	GPIO2	GPIO2/NF_D2/LCD_D2/SPI0_CLK/SDC0_DAT0/UART0_CTS/TWI0_CLK/PWM2/IIS1RX_LRCLK/SPI0_SS	*
43	GPIO1	GPIO1/NF_D1/LCD_D1/SPI0_MISO/SDC0_CLK0/UART0_RX/PWM1/IIS1RX_BCLK/SPI0_CLK	*
44	GPIO0	GPIO0/NF_D0/LCD_D0/SPI0_SS/SDC0_CMD/UART0_TX/PWM0/IIS1RX_MCLK/SPI_MOSI	*
45	GPIO43	GPIO43/LCD_CE0_HSYNC/SPI1_D2/SD0_DAT1/UART3_CTS/TWI1_CLK/PWM5/IIS0RX_DIN	Z
46	GPIO18	GPIO18/LCD_D8/SPI2_SS/SD1_CLK0/UART0_TX/PWM0/IIS0TX_MCLK/PDMTX_CLK	Z
47	GPIO19	GPIO19/LCD_D9/SPI2_CLK/SD1_CLK1/UART0_RX/PWM1/IIS0TX_BCLK/PDMTX_DAT	*
48	GPIO20	GPIO20/LCD_D10/SPI2_MISO/SD1_CMD/UART0_CTS/TWI0_CLK/PWM2/IIS0TX_LRCLK/LRADC7	Z
49	GPIO21	GPIO21/LCD_D11/SPI2_MOSI/SD1_DAT0/UART0_RTS/TWI0_DAT/PWM3/IIS0TX_DOUT/LRADC8	Z
50	GPIO22	GPIO22/LCD_D12/SPI1_SS/SD1_DAT4/UART1_TX/PWM4/IIS0RX_MCLK/DMIC01_CLK	Z
51	GPIO23	GPIO23/LCD_D13/SPI1_CLK/SD0_DAT4/SD1_DAT5/UART1_RX/PWM5/IIS0RX_BCLK/DMIC01_DAT	Z
52	GPIO24	GPIO24/LCD_D14/SPI1_MISO/SD0_DAT5/SD1_DAT6/UART1_CTS/TWI1_CLK/PWM6/IIS0RX_LRCLK/VMIC0/T2_CAP	Z
53	GPIO25	GPIO25/LCD_D15/SPI1_MOSI/SD0_DAT6/SD1_DAT7/UART1_RTS/TWI1_DAT/PWM7/IIS0RX_DIN/VMIC1	Z
54	GPIO27	GPIO27/LCD_D17/SPI0_CLK/SD0_DAT3/SD1_DAT2/UART0_RX/TWI0_DAT/PWM0/IIS1RX_BCLK/DMIC01_DAT	Z
55	GPIO28	GPIO28/LCD_D18/SPI0_MISO/SD0_DAT2/SD1_DAT3/UART1_TX/TWI1_CLK/PWM1/IIS1RX_LRCLK	Z
56	GPIO29	GPIO29/LCD_D19/SPI0_MOSI/SD0_DAT1/UART1_RX/TWI1_DAT/PWM2/IIS1RX_DIN/PDMTX_CLK	Z
57	GPIO30	GPIO30/LCD_D20/SD0_CLK0/SPI1_SS/SPI2_SS/UART2_TX/PWM3/IIS1TX_MCLK	Z
58	GPIO31	GPIO31/LCD_D21/SD0_CLK1/SPI1_CLK/SPI2_CLK/UART2_RX/PWM4/PDMTX_DAT/IIS1TX_BCLK	Z
59	GPIO32	GPIO32/LCD_D22/SD0_CMD/SPI1_MISO/SPI2_MISO/UART3_TX/PWM5/IIS1TX_LRCLK	Z
60	GPIO33	GPIO33/LCD_D23/SD0_DAT0/SPI1_MOSI/SPI2_MOSI/UART3_RX/PWM6/IIS1TX_DOUT	Z
61	GPIO38	GPIO38/LCD_D4/SPI1_D2/UART1_TX/PWM4/IIS0TX_MCLK/PDMTX_CLK/DMIC	Z

		23_CLK/LRADC6	
62	GPIO39	GPIO39/LCD_D5/SPI1_D3/SDO_CLK1/UART1_RX/PWM5/IISOTX_BCLK/PDMTX_DAT/DMIC23_DAT/LRADC9	Z
63	WIO1	WIO1/LRADC1/32KHz_IN	
64	LOSCO		
65	LOSCI		
66	HOSCI		
67	HOSCO		
68	VDD		
69	GND		

1.6 ATJ2157 Package Drawing



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3		0.20 REF.	
lead width		b	0.13	0.18	0.23
package size	X	D	6.90	7.00	7.10
	Y	E	6.90	7.00	7.10
E-PAD size	X	D2	5.60	5.70	5.80
	Y	E2	5.60	5.70	5.80
lead length		L	0.30	0.40	0.50
lead pitch		e		0.35 bsc	
lead arc		R	0.065	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Parallelism		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

Figure 1-3 ATJ2157 package drawing

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 2-1 Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage temperature	Tstg	-55		+150	℃
Supply voltage	DC5V	-0.3	5	6	V
	SYSPWR	-0.3		5	V
	BAT	-0.3	3.8	5	V
	VCC	-0.3	3.1	3.6	V
	SVCC	-0.3	2.6	3.3	V
	AVCC	-0.3	2.95	3.3	V
	USBVCC	-0.3	3.1	3.6	V
	VDD	-0.3	1.2	1.35	V
Input Voltage	+3.3V IO	-0.3	3.1	3.6	V
ESD HBM	Human body model	2000			V
ESD CDM	Charged Device Model	500			V

Note:

1) Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
2) All voltage values are with respect to GND

2.2 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 2-2 Recommended Operating Conditions

Supply Voltage	Min	Typ	Max	Unit
VCC/USBVCC	2.9	3.1	3.4	V
SVCC	2.5	2.6	2.7	V
AVCC	2.8	2.95	3.15	V
VREF	1.485	1.5	1.52	V
VDD	0.9	1.2	1.35	V
Ambient Temperature	TBD	25	TBD	℃

2.3 DC Characteristics

DC Parameters for +3.0V IO PIN

Table 2-3 DC Parameters

Parameter	Symbol	MIN.	MAX.	Unit	Condition
Low-level input voltage	VIL		0.8	V	VCC = 3.0V
High-level input voltage	VIH	2.0		V	

Low-level output voltage	VOL		0.4	V	Tamb = －10 to 70 ℃
High-level output voltage	VOH	2.4		V	

3 MCU

3.1 Overview

The ARM® Cortex™-M4F CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M4F CPU makes program execution simple and highly efficient.It is intended for deeply embedded applications that require optimal interrupt response features.
The required blocks are as follows:
• tight integration of system peripherals reduces area and development costs
• Thumb instruction set combines high code density with 32-bit performance
• IEEE754-compliant single-precision FPU
• code-patch ability for ROM system updates
• power control optimization of system components
• integrated sleep modes for low power consumption
• fast code execution permits slower processor clock or increases sleep mode time
Introduction, Reference Material
• hardware division and fast digital-signal-processing orientated multiply accumulate
• saturating arithmetic for signal processing
• deterministic, high-performance interrupt handling for time-critical applications
• memory protection unit (MPU) for safety-critical applications

3.2 NVIC

The ATJ2157 use Cortex-M4F processor, a Nested vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing.
The NVIC provides configurable interrupt handling abilities to the processor, facilitates low-latency exception and interrupt handling, and controls power management.
The NVIC supports up to 64 interrupts, each with up to 4 levels of priority that can be changed dynamically. The processor and NVIC can be put into a very low-power sleep mode, leaving the Wake Up Controller (WIC) to identify and prioritize interrupts. Also, the processor supports both level and pulse interrupts.
The NVIC and the processor core interface are closely couple, to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts.
Each peripheral device has one interrupt line connected to the NVIC. External interrupt can be programmed to generate an interrupt on rising edge, falling edge, or both.

3.2.1 Vector Table

When an exception takes place and is being handled by the Cortex-M4F, the processor will need to locate the starting address of the exception handler. This information is stored in the vector table.

Table 3-1 vector table

Interrupt ID	Interrupt source
0	-
1	WD_2Hz

2	TIMER0
3	TIMER1
4	TIMER2
5	TIMER3
6	RTC
7	I2SRX0
8	I2SRX1
9	NC
10	I2STX0
11	I2STX1
12	USB
13	SPI0
14	SPI1
15	SPI2
16	NAND
17	SDC
18	SDIO
19	TWI0
20	TWI1
21	UART0
22	UART1
23	UART2
24	UART3
25	NC
26	DMA0
27	DMA1
28	DMA2
29	DMA3
30	DMA4
31	DMA5
32	DMA6
33	DMA7
34	DMA8
35	DMA9
36	EXTIRQ
37	NC
38	NC

39	DAC
40	ADC01
41	ADC23
42	LCD
43	-
44	NC
45	-
46	NC
47	NC
48	MPU
49	-
50	SDMA

3.3 CACHE

- Support code runs directly in SPI nor/SRAM
- Caching data for code and read-only data in SPI Nor
- Caching data for data in SPI SRAM
- 32KB Icache of SPI Nor, with 4- ways associative and 8k bytes cache size of a way
- 32KB Dcache of SPI SRAM, with 4- ways associative and 8k bytes cache size of a way
- Support performance profile

3.4 Memory Map

Table 3-2 system memory map、

Start address	End address	Size	Function
IO Device			
0xC0000000	0xC000FFFF		RMU/-/CMU
0xC0010000	0xC001FFFF		PMU
0xC0020000	0xC002FFFF		-
0xC0030000	0xC003FFFF		Timer/RTC/WD
0xC0040000	0xC004FFFF		Memory controller
0xC0050000	0xC005FFFF		SPI Cache
0xC0060000	0xC006FFFF		SPI1 Cache
0xC0070000	0xC007FFFF		DMA
0xC0080000	0xC008FFFF		-
0xC0090000	0xC009FFFF		-
0xC00A0000	0xC00AFFFF		SPI0
0xC00B0000	0xC00BFFFF		SPI1
0xC00C0000	0xC00CFFFF		SPI2
0xC00D0000	0xC00DFFFF		UART0
0xC00E0000	0xC00EFFFF		UART1
0xC00F0000	0xC00FFFFF		UART2
0xC0100000	0xC010FFFF		UART3
0xC0110000	0xC011FFFF		TWI0
0xC0120000	0xC012FFFF		TWI1
0xC0140000	0xC014FFFF		USB
0xC0150000	0xC015FFFF		NAND
0xC0160000	0xC016FFFF		SD/MMC
0xC0170000	0xC017FFFF		SDIO
0xC0180000	0xC018FFFF		Audio
0xC0190000	0xC019FFFF		PWM
0xC01A0000	0xC01AFFFF		LCD
0xC01C0000	0xC01CFFFF		GPIO
0xC0200000	0xC020FFFF		-
SRAM Mapping (total:384K) (RAM Region)			
0x00100000	0x00107FFF	32KB	RAM0
0x00108000	0x0010FFFF	32KB	RAM1
0x00110000	0x00117FFF	32KB	RAM2
0x00118000	0x0011FFFF	32KB	RAM3
0x00120000	0x00127FFF	32KB	RAM4
0x00128000	0x0012FFFF	32KB	RAM5
0x00130000	0x00137FFF	32KB	RAM6
0x00150000	0x00157FFF	32KB	HW RAM
BROM Mapping (total:64K)			
0x00000000	0x0000FFFF	64KB	ROM

4 System Control

4.1 PMU

4.1.1 Features

The ATJ2157 integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery and 5V power supply;
- Integrate Linear battery charger;
- Integrated buck DC-DC output VDD, which can be switch to LDO mode.
- Linear regulators output SYSPWR, SVCC,VCC, AVCC

4.1.2 Module Description

4.1.2.1 DC-DC Accurate and Maximum Output Current

The output voltages are highly precise within ±2%, They provide large currents with a significantly small dropout voltage within ±5%. Table1 shows data of maximum output current.

Table 1 DC-DC Maximum Output Current

Output voltage (V)	Inductance (uH)	**Capacitance** (uF)	Load capacity (mA)
Typ 1.2, 0.7~1.35	4.7/10	10	100mA @Drop to 95% BAT=3.6V

4.1.2.2 Regulators Accurate and Maximum Output Current

The output voltages are highly precise within ±2%, They provide large currents with a significantly small dropout voltage within ±5%. Table2 shows data of maximum output current.

Table 2 Regulators Maximum Output Current

Name	Output voltage	Load capacity
VCC	2.9~3.4V	350 mA
VDD	0.9~1.35V	80 mA
AVCC	2.8~3.15V	30 mA@98%
SVCC	2.6V	10 mA

4.1.3 PMU Register List

PMU block base address

Name	Physical Base Address
PMU	0xC0010000

PMU Block Configuration Registers List

Offset	Register Name	Description
0x00	VOUT_CTL	voltage set Register
0x10	CHG_CTL	Charger control Register
0x14	CHG_DET	Charger status Register
0x1C	SYSTEM_SET	System set Register
0x20	POWER_CTL	POWER on/off control Register
0x24	WKEN_CTL	Wake up source select Register
0x28	WAKE_PD	Wake up source pending
0x2C	ONOFF_CTL	Onoff key control Register

4.1.4 Register Description

4.1.4.1 VOUT_CTL

Voltage set register (VDD) offset: 0x00

Bit(s)	Name	Description	R/W	Reset
31:30	-	Reseved for analog future use	R/W	0
29	USBVCC_EN	USBVCC enable： 0：disable 1：enalbe	R/W	1
28	USBVDD_EN	USBVDD enable： 0：disable 1：enalbe	R/W	1
27:23	-	- Reseved for future use	R/W	*
22	AVDD_EN	AVDD LDO enable 0: disable 1: enable	R/W	1
21:20	AVDD_VOL	AVDD voltage level 00 1.0V 01 1.1V 10 1.2V 11 1.3V	R/W	0x2
19:17	AVCC_SET	AVCC voltage level 000 2.8V 001 2.85V 010 2.9V *011 2.95V 100 3.0V 101 3.05V 110 3.1V 111 3.15V	R/W	0x3
16:13	VCCB	Should be 2’b1101	R/W	0xD

12:10	VCC_SET	VCC voltage level select 000 2.7V 001 2.8V 010 2.9V 011 3.0V *100 3.1V 101 3.2V 110 3.3V 111 3.4V	R/W	0x4
9:5	VDD_SET_S3VAD	VDD voltage coarse control 00000 0.7 00001 0.725 00010 0.75 00011 0.775 00100 0.8 00101 0.825 00110 0.85 00111 0.875 *01000 0.9 01001 0.925 01010 0.95 01011 0.975 01100 1 01101 1.025 01110 1.05 01111 1.075 10000 1.1 10001 1.125 10010 1.15 10011 1.175 10100 1.2	R/W	0x8
4:0	VDD_SET_S1	VDD voltage coarse control: 00000 0.7 00001 0.725 00010 0.75 00011 0.775 00100 0.8 00101 0.825 00110 0.85 00111 0.875 01000 0.9 01001 0.925 01010 0.95 01011 0.975 01100 1 01101 1.025 01110 1.05 01111 1.075 10000 1.1 10001 1.125 10010 1.15	R/W	0x14

		10011 1.175 *10100 1.2 10101 1.225 10110 1.25 10111 1.275 11000 1.3 11001 1.325 11010 1.35 11x1x 1.35		

4.1.4.2 CHG_CTL

Charging control register（VDD） **Offset = 0x10**

Bit(s)	Name	Description	R/W	Reset
31	DC5VOV_EN	DC5V Overvoltage detection enable bit 0:disable 1:enable	R/W	1
30:29	DC5VOV_SET	DC5V Overvoltage protection voltage value： 00：5.5V 01：6V 10：6.5V 11: 7V	R/W	0
28:22	-	Reserved for analog future use	R/W	*
21:20	BAT_PD	BAT Internal pull-down current control bit： 00：disable 01：2.5ma; 10: 5ma; 11: 15ma	R/W	0
19	-	Reserved	R/W	0
18	CHGEN	Enable Charge Circuit 0:disable 1:enable	R/W	0
17	ENTKLE	Trickle charging enable: 0: disable trickle charge. Whether battery voltage is below or up 3.0V, the charging current will be the value setting by CHG_CURRENT 1: enable trickle charge. When battery voltage is below 3.0V, the charging current is 1/10 of the value setting by CHG_CURRENT	R/W	0
16:14	CHG_CURRENT	Charger Current Configure 000:25mA 001:50mA 010:75mA 011:100mA 100:200mA 101:300mA 110:400mA 111:450mA	R/W	0
13	ENBATDT	Enable to detect the battery 0:disable 1:enable	R/W	0
12:7	CHG_VLOT	000000:4.1V	R/W	0

		000001:4.10625V ……. 010000:4.2V ……. 011000:4.25V ……. 100000:4.3V ……. 101000:4.35V ……. 110000:4.4V ……. 111111:4.49375V Step=6.25mV		
6:5	STOPV	Charging end voltage 00: 4.16V 01 :4.18V 10: 4.32V 11: 4.34V	R/W	1
4:2	-	Reserved for analog future use	R/W	*
1	ENCHGATDT	Automatic detection of charge termination 0:disable 1:enable	R/W	1
0	DTSEL	Time interval selection of charge termination detection 0:12min 1:20s	R/W	0

4.1.4.3 CHG_DET

Charging detect register（VDD） **Offset = 0x14**

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:9	-	Reserved for future use	R/W	0
8	DC5VOV_DET	Overvoltage detected of DC5V 0: normal 1: Overvoltage	R	X
7:6	CHGPHASE	Charge state 00: Reserved 01: trickle charging 10: Constant current charging 11: Constant voltage charging	R	x
5:3	CHG_STA	Charge Current detect 000....0~5%*I_{chg}, I_{chg} is set by register CHARGER_CTL. 001....5~10%*I_{chg} 010....10%~20%I_{chg} 011....20%~30%I_{chg} 100....30%~50%I_{chg} 101....50%~75%I_{chg} 110....75%~87.5%I_{chg} 111....87.5%I_{chg} 以上 You can see current charging current by these 3bits.	R	x
2	CHGEND	End of charge flag 0: charging 1: end	R	x

1	BATEXT	BAT flag 0: no battery 1: Battery placed	R	x
0	DTOVER	Battery detect end flag 0: detecting 1: end of detect	R	x

4.1.4.4 SYSTEM_SET

System set Register (SVCC) **Offset = 0x1C**

Bit(s)	Name	Description	R/W	Reset
32:15	-	RESERVED	R	0
14:10	-	RESERVED FOR FUTURE USE	R/W	0
9	LB_EN	LB automatically enters the standby mode function enable ： 0：disable 1：enable，entry the standby mode if BAT at low power	R/W	0
8:7	LB_VOL	LB (Low battery) voltage setting *00 2.7V 01 2.8V 10 3.0V 11 3.3V	R/W	0
6	OC_EN	VCC over current protection enable 0：disable 1：enable	R/W	1
5	LVPRO_EN	VCCVDD low voltage protection enable ： 0:disable 1:enable	R/W	1
4:2	-	RESERVED FOR FUTURE USE	R/W	0
1	DC5VON_T	Detection of debounce time adjustment of DC5VON： 0：4mS 1：16mS	R/W	1
0	DC5VRST_EN	DC5V reset enable 0:disable 1:enable	R/W	0

4.1.4.5 POWER_CTL

Power Control Register (SVCC) **Offset = 0x20**

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0
1	EN_S3	0:disable 1:enable	R/W	0
0	EN_S1	0:disable 1:enable	R/W	1

4.1.4.6 WKEN_CTL

Wake up source enable Register (SVCC) Offset:0x24

Bit(s)	Name	Description	R/W	Reset
31	-	Reserved for future use	R/W	0
30:28	BATLV_VOL	BATLV wake up voltage threshold： 000：3.4V 001：3.5V 010：3.6V 011：3.7V 100：3.8V 101：3.9V 110：4.0V 111：4.1V	R/W	0x2
27:25	DC5VLV_VOL	DC5VLV wake up voltage threshold ： 000：0.2V 001：0.5V 010：1.0V 011：1.5V 100：2.0V 101：2.5V 110：3.0V 111：3.5V	R/W	0x2
24	-	RESERVED	R/W	0
23	REMOTE_WKEN	Remote key(connect LRADC1) wake enble， voltage<0.9*SVCC 0: Disable 1: Enable	R/W	0
22	BATLV_WKEN	BAT low voltage detected wake enble 0: Disable 1: Enable	R/W	0
21	DC5VLV_WKEN	DC5V low voltage detected wake enble 0: Disable 1: Enable	R/W	0
20	WIO1LV_WKEN	WIO1 low voltage detected wake enble 0：diable 1：enable	R/W	0
19:18	WIO1LV_VOL	WIO1 low voltage selection 00：<0.66V; 01：<1V 10：<1.1V） 11：<1.17V	R/W	0x2
17	DC5VPD_EN	DC5V pull down enble 0：disable 1：enable	R/W	0
16:15	DC5VPD_SET	DC5V pull down current setting 00：2.5mA 01：5mA 10：10mA 11：20mA	R/W	0
14:12	-	RESERVED	R/W	0
11	WIO1_WKEN	WIO1 wake enable bit 0：disable 1：enable	R/W	0

10	-	RESERVED	R/W	0
9	CPUIRQ_WKEN	CPUIRQ wake enable bit 0：disable 1：enable	R/W	0
8:5	-	reserved	R/W	0
4	ALARM_WKEN	ALARM wake enable bit 0：disable 1：enable	R/W	0
3	DC5VOFF_WKEN	DC5V pull out wake enable bit 0：disable 1：enable	R/W	0
2	DC5VON_WKEN	DC5V push in wake enable bit 0：disable 1：enable	R/W	1
1	SHORT_WKEN	OMOFF key short press wake enable 0: disable 1: enable	R/W	0
0	LONG_WKEN	ONOFF key long press wake enable 0: disable 1: enable	R/W	1

4.1.4.7 WAKE_PD

WAKE up source pending Register (SVCC) Offset: 0x28

Bit(s)	Name	Description	R/W	Reset
31:	-	Reserved	R	0
30	DC5VON	DC5VON flag： 0：No DC5V 1：Push in DC5V,DC5V>BAT+0.08V	R	0
29:28				
27	OC_PD	Over current protection pending： 0: normal 1: Over current protection pending	R/W	0
26	LVPRO_PD	Low power protection of power supply pending： 0: normal 1: Low power protection of power supply	R/W	0
25	LB_PD	Battery low power protection pending： 0: normal 1: Battery low power protection	R/W	0
24	BATWK_PD	Battery Push in pending 0：normal 1：Battery insertion occurs	R/W	0
23	REMOTE_PD	Remote key(connect LRADC1) wake pending： 0：not 1：Remote key wake up occurred	R/W	0
22	BATLVWK_PD	BATLV wake pending 0：not 1：Low voltage of BAT wake up occurred	R/W	0
21	DC5VLVWK_PD	DC5VLV wake pending 0：not	R/W	0

		1：Low voltage of DC5V wake up occurred		
20	WIO1LV_PD	WIO1LV pending： 0：not 1：Low voltage of WIO1 detected	R/W	0
19:12	-	reserved	R/W	0
11	WIO1_PD	WIO1wakeup pending： 0：no 1：WIO1 wake up occurred	R/W	0
10	-	reserved	R/W	0
9	CPUIRQ_PD	CPUIRQ wakeup pending： 0: no 1: CPUIRQ wake up occurred	R/W	0
8:5	-	reserved	R/W	0
4	ALARM_PD	ALARM wakeup pending： 0: no 1: alarm wake-up occurred	R/W	0
3	DC5VOFF_PD	DC5Vpull out pending 0：No 1：DC5V pull out occurred	R/W	0
2	DC5VON_PD	DC5V push in pending 0：No 1：DC5V push in occurred	R/W	0
1	ONOFF_S_PD	ONOFF short press pending 0：No 1：ONOFF short press in occurred	R/W	0
0	ONOFF_L_PD	ONOFF long press pending 0：No 1：ONOFF long press in occurred	R/W	0

4.1.4.8 ONOFF_CTL

onoff key control & detect register (SVCC) **Offset = 0x2C**

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:9	-	Reserved for future use	R/W	0
8:6	ONOFF_PRESS_TIME	onoff key time setting: 000: 50ms <T< 0.125s is short key; t > = 0.125s is long key; 001: 50ms <T< 0.25s is short key; t > = 0.25s is long 010: 50ms <T< 0.5s is short key; t > = 0.5s is long key; 011: 50ms<T< 1s is short key; t> = 1s is long key; 100: 50ms<T< 1.5s is short key; t> = 1.5s is long key; 101: 50ms<T< 2s is short key; t> = 2s is long key; 110: 50ms<T< 3s is short key; t> = 3s is long key; 111: 50ms<T< 4s is short key; t> =4s is long key;	R/W	1
5:4	ONOFF_RST_EN	ONOFF Long press function setting： 00：Reserved 01：reset 10：restart 11: Reserved	R/W	1

3:2	ONOFF_RST_TIME	ONOFF Long press timer 00:8s 01:12s 10:16s 11:24s	R/W	0
1	ONOFF_PRESS	ONOFF status bit 0:The onoff key no press 1:The onoff is being pressed	R	0
0	PULLR_SEL	Level selection of onoff button 0: if he ONOFF key is pulled down, it means that the key is pressed 1: if he ONOFF key is pulled up, it means that the key is pressed	R/W	0

4.2 OSC

4.2.1 Features

- Support only one oscillator inputs: 24M;
- Supply 1 RC24M circuit which can be calibrated and 1 HOSC. CK24M clock source can be selected from the above RC24M or HOSC.
- Supply 1 LOSC as an option.

4.2.2 Register List

OSC Base Address

Name	Physical Base Address
OSC_REGISTER	0xC0000100

OSC Controller Registers List

Offset	Register Name	Description
0x00	HOSC_CTL	HOSC Control Register
0x04	LOSC_CTL	LOSC Control Register

4.2.3 Register Description

4.2.3.1 HOSC_CTL

HOSC control register.
Offset = 0x00(VDD domain)

Bit(s)	Name	Description	R/W	Reset
31:29	HOSCI_BC_SEL	HOSCI PAD base cap select: 000: 0p 001: 3p	R/W	0x4

		010: 6p 011: 9p 100: 12p** 101: 15p 110: 18p 111: 21p		
28:24	HOSCI_TC_SEL	HOSCI PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCI_TC_SEL	R/W	0x0
23:21	HOSCO_BC_SEL	HOSCO PAD base cap select: 000: 0p 001: 3p 010: 6p 011: 9p 100: 12p** 101: 15p 110: 18p 111: 21p	R/W	0x4
20:17	HOSCO_TC_SEL	HOSCO PAD trim cap select, range from 0pF to 3.1 pF Trim cap = 0.2pF * HOSCO_TC_SEL	R/W	0x0
16	HOSCO_CMOS_CAP	HOSCO PAD 15pF CMOS Cap Enable 0: disable 1: enable	R/W	0x0
15	-	Reserved	R/W	0x0
14:13	HOSC_AMPLMT	HOSC amplitude Adjust 00：450mV 01：500mV 10：550mV 11：600mV	R/W	0x3
12	HOSC_AMPLMT_EN	HOSC amplitude Adjust Enable: 0: disabled 1: enable	R/W	0x0
11:10	-	Reserved	R/W	0x0
9:8	HGMC	High Frequency crystal Oscillator GMMIN select bits	R/W	0x3
7:6	-	Reserved	R/W	0x0
5	HOSC_VDD_SEL	VDD_HOSC clock select: 0: select HOSC before GHR 1: select HOSC after GHR Glitch in HOSC low than 3ns will be remove by GHR. The glitch remove clock only provide to VDD power domain;	R/W	0x1
4	HOSC_BUF_SEL	HOSC clock output select: 0: HOSC clock select OP smiths trigger output. 1: HOSC clock select smiths trigger output. This bit is valid for HOSC from the source.	R/W	0x0
3:1	-	Reserved	R/W	0x0
0	HOSC_EN	HOSC enable: 0: disable 1: enable	R/W	0x0

4.2.3.2 LOSC_CTL

LOSC Control Register.
Offset = 0x04(SVCC domain)

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved, be read as zero.	R	0x0
24	LOSC_RDY	LOSC Status: 0: LOSC not Ready 1: LOSC ready	R	x
23:21	-	Reserved, be read as zero.	R/W	0
20:16	LOSCI_CAP	LOSCI PAD Capacitance select: 00000: 0pf 00001: 0.8pf 00010: 1.6pf 00011: 2.4pf … 10000: 12.8pf** … 11111: 24.8pf	R/W	0x19
15:13	-	Reserved, be read as zero.	R/W	0
12:8	LOSCO_CAP	LOSCO PAD Capacitance select: 00000: 0pf 00001: 0.8pf 00010: 1.6pf 00011: 2.4pf … 10000: 12.8pf** … 11111: 24.8pf	R/W	0x19
7	-	Reserved	R/W	0x0
6:4	LGMC	Low Frequency crystal Oscillator GMMIN select bits	R/W	0x7
3:1	-	Reserved	R/W	0x0
0	LOSC_EN	LOSC enable: 0: disable 1: enable	R/W	0x0

4.3 CMU

4.3.1 Features

(1) The CMU (Clock Management Unit) can select CK24M, CORE_PLL, DEV_PLL and RC32K as the clock of each peripheral.
(2) The clock sources of the memory blocks can be selected by CMU.

4.3.2 Register List

CMU Controller Base Address

Name	Physical Base Address
CMU_REGISTER	0xC0001000

CMU Digital Controller Registers List

Offset	Register Name	Description
0x0008	CMU_DEVCLKEN0	Device Clock Enable Register0
0x000C	CMU_DEVCLKEN1	Device Clock Enable Register1
0x0014	CMU_SD0CLK	SD0 Clock Control Register
0x0018	CMU_SD1CLK	SD1 Clock Control Register
0x0020	CMU_SPI0CLK	SPI0 Clock Control Register
0x0024	CMU_SPI1CLK	SPI1 Clock Control Register
0x0028	CMU_SPTWILK	SPI2 Clock Control Register
0x0034	CMU_LCDCLK	LCD Clock Control Register
0x0040	CMU_TIMER0CLK	TIMER0 Clock Control Register
0x0044	CMU_TIMER1CLK	TIMER1 Clock Control Register
0x0048	CMU_TIMER2CLK	TIMER2 Clock Control Register
0x004C	CMU_TIMER3CLK	TIMER3 Clock Control Register
0x0050	CMU_PWM0CLK	PWM0 Clock Control Register
0x0054	CMU_PWM1CLK	PWM1 Clock Control Register
0x0058	CMU_PWM2CLK	PWM2 Clock Control Register
0x005C	CMU_PWM3CLK	PWM3 Clock Control Register
0x0060	CMU_PWM4CLK	PWM4 Clock Control Register
0x0064	CMU_PWM5CLK	PWM5 Clock Control Register
0x0068	CMU_PWM6CLK	PWM6 Clock Control Register
0x006C	CMU_PWM7CLK	PWM7 Clock Control Register
0x0070	CMU_PWM8CLK	PWM8 Clock Control Register
0x007C	CMU_LRADCCLK	LRADC Clock Control Register
0x0080	CMU_ADC01CLK	ADC01 Clock Control Register
0x0084	CMU_ADC23CLK	ADC23 Clock Control Register
0x0088	CMU_DACCLK	DAC Clock Control Register
0x008C	CMU_I2STX0CLK	I2STX0 Clock Control Register
0x0090	CMU_I2STX1CLK	I2STX1 Clock Control Register
0x0094	CMU_I2SRX0CLK	I2SRX0 Clock Control Register
0x0098	CMU_I2SRX1CLK	I2SRX1 Clock Control Register

4.3.3 Register Description

4.3.3.1 CMU_DEVCLKEN0

Device Clock Enable Register0
Offset = 0x0008

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28	-	Reserved	R	0x0
27	LRADCCLKEN	LRADC Controller clock enable bit: 0: disable 1: enable	R/W	0x1
26	-	Reserved	R	0x0
25	PWMCLKEN	PWM clock enable bit: 0: disable 1: enable This bit controls all the clock gatings of PWMx	R/W	0x0
24	TIMERCLKEN	Timer0/1/2/3 controller clock: 0: disable 1: enable This bit controls all the clock gatings of TIMERx_CLK	R/W	0x0
23	UART3CLKEN	UART3 controller clock enable bit: 0: disable 1: enable	R/W	0x0
22	UART2CLKEN	UART2 controller clock enable bit: 0: disable 1: enable	R/W	0x0
21	UART1CLKEN	UART1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
20	UART0CLKEN	UART0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
19	TWI1CLKEN	TWI1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
18	TWI0CLKEN	TWI0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
17:16	-	Reserved	R	0x0
15	USBCLKEN	USB controller clock enable bit: 0: disable 1: enable	R/W	0x0
14	SECCLKEN	SEC clock enable bit: 0: disable; 1: enable;	R/W	0x0
13	LCDCLKEN	LCD controller clock enable bit: 0: disable 1: enable	R/W	0x0
12	-	Reserved	R/W	0x0

11	-	Reserved	R	0x0
10	SPI1CACHECLKEN	SPI1 CACHE Controller clock enable bit: 0: disable 1: enable	R/W	0x0
9	SPI0CACHECLKEN	SPI0 CACHE Controller clock enable bit: 0: disable 1: enable	R/W	0x0
8	SPTWILKEN	SPI2 controller clock enable bit: 0: disable 1: enable	R/W	0x0
7	SPI1CLKEN	SPI1 controller clock enable bit: 0: disable 1: enable	R/W	0x0
6	SPI0CLKEN	SPI0 controller clock enable bit: 0: disable 1: enable	R/W	0x0
5:4	-	Reserved	R	0x0
3	SD1CLKEN	SD1 card controller clock enable bit: 0: disable 1: enable	R/W	0x0
2	SD0CLKEN	SD0 card controller clock enable bit: 0: disable 1: enable	R/W	0x0
1	NANDFLASHCLKEN	NandFlash controller clock enable bit: 0: disable 1: enable	R/W	0x0
0	DMACLKEN	DMA clock enable bit: 0: disable 1: enable	R/W	0x0

Note:

4.3.3.2 CMU_DEVCLKEN1

Device Clock Enable Register1
Offset = 0x000C

Bit(s)	Name	Description	R/W	Reset
31	-	Reserved	R/W	0x1
30:14	-	Reserved	R	0x0
13	-	Reserved	R/W	0x0
12	-	Reserved	R	0x0
11	DACANACLKEN	DAC Analog Measurement Clock Enable bit 0: disable 1: enable	R/W	0x0
10:9	-	Reserved	R	0x0
8	I2SSRDCLKEN	I2SSRD Clock Enable bit: 0: disable 1: enable	R/W	0x0
7	I2SRX2MCLKEN	I2SRX2 Mclock enable bit: 0: disable 1: enable This bit will also enable the CK24M Clock which is sent to I2SRX2 module detecting LRCK	R/W	0x0

6	I2SRX1MCLKEN	I2SRX1 Mclock enable bit: 0: disable 1: enable This bit will also enable the CK24M Clock which is sent to I2SRX1 module detecting LRCK	R/W	0x0
5	I2SRX0MCLKEN	I2SRX0 Mclock enable bit: 0: disable 1: enable This bit will also enable the CK24M Clock which is sent to I2SRX0 module detecting LRCK	R/W	0x0
4	I2STX1MCLKEN	I2STX1 Mclock enable bit: 0: disable 1: enable This bit will also enables the CK24M Clock which is sent to I2STX1 module detecting LRCK	R/W	0x0
3	I2STX0MCLKEN	I2STX0 Mclock enable bit: 0: disable 1: enable This bit will also enables the CK24M Clock which is sent to I2STX0 module detecting LRCK	R/W	0x0
2	DACCLKEN	DAC controller clock enable bit: 0: disable 1: enable	R/W	0x0
1	ADC23CLKEN	ADC23 controller clock enable bit: 0: disable 1: enable	R/W	0x0
0	ADC01CLKEN	ADC01 controller clock enable bit: 0: disable 1: enable	R/W	0x0

4.3.3.3 CMU_SD0CLK

SD0 Clock Control Register
Offset = 0x0014

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9:8	SD0CLKSRC	SD0 Card Controller Clock Source Select: 00: CK24M 01: CORE_PLL 10: DEV_PLL 11: reserved	R/W	0x0
7	-	Reserved	R	0x0
6	SD0CLKPOSTDIV	SD0 Card Controller Clock Post-Divisor 0: /1 1: /128	R/W	0x0
5:4	-	Reserved	R	0x0
3:0	SD0CLKDIV	SD0 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6	R/W	0x0

		0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16		

4.3.3.4 CMU_SD1CLK

SD1 Clock Control Register
Offset = 0x0018

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9:8	SD1CLKSRC	SD1 Card Controller Clock Source Select: 00: CK24M 01: CORE_PLL 10: DEV_PLL 11: reserved	R/W	0x0
7	-	Reserved	R	0x0
6	SD1CLKPOSTDIV	SD1 Card Controller Clock Post-Divisor 0: /1 1: /128	R/W	0x0
5:4	-	Reserved	R	0x0
3:0	SD1CLKDIV	SD1 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16	R/W	0x0

4.3.3.5 CMU_SPI0CLK

SPI0 Clock Control Register
Offset = 0x0020

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9:8	SPI0CLKSRC	SPI0 Controller Clock Source:	R/W	0x0

		00: HCLK 01: CK24M 10: CORE_PLL 11: DEV_PLL		
7:4	-	Reserved	R	0x0
3:0	SPI0CLKDIV	SPI0 Clock Divisor: 0: /1 1: /2 2: /4 3: /6 4: /8 … 13: /26 14: /1.5 15: /2.5	R/W	0x0

4.3.3.6 CMU_SPI1CLK

SPI1 Clock Control Register
Offset = 0x0024

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	R	0x0
14:12	OPI2XCLKDIV	SPI1 OPI mode SPI1_2X_CLK divisor: 0: /1 1: /2 2: /4 3: /6 … 7: /14	R/W	0x0
11:10	-	Reserved	R	0x0
9:8	SPI1CLKSRC	SPI1 Controller Clock Source: 00: HCLK 01: CK24M 10: CORE_PLL 11: DEV_PLL	R/W	0x0
7:4	-	Reserved	R	0x0
3:0	SPI1CLKDIV	SPI1 Clock Divisor: 0: /1 1: /2 2: /4 3: /6 4: /8 … 13: /26 14: /1.5 15: /2.5	R/W	0x0

4.3.3.7 CMU_SPTWILK

SPI2 Clock Control Register
Offset = 0x0028

Bit(s)	Name	Description	R/W	Reset

31:10	-	Reserved	R	0x0
9:8	SPTWILKSRC	SPI2 Controller Clock Source: 00: HCLK 01: CK24M 10: CORE_PLL 11: DEV_PLL	R/W	0x0
7:4	-	Reserved	R	0x0
3:0	SPTWILKDIV	SPI2 Clock Divisor: 0: /1 1: /2 2: /4 3: /6 4: /8 … 13: /26 14: /1.5 15: /2.5	R/W	0x0

4.3.3.8 CMU_LCDCLK

LCD Clock Control Register
Offset = 0x0034

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9:8	LCDCLKSRC	LCD Controller Clock Source: 00: CK24M 01: CORE_PLL 10: DEV_PLL 11: reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	LCDCLKPREDIV	LCD Controller Clock PRE-divisor: 0: /1 1: /6	R/W	0x0
3:0	LCDCLKDIV	LCD Controller Clock Divisor: 0: /1 1: /2 2: /3 3: /4 4: /5 … 11: /12 Others: Reserved	R/W	0x0

4.3.3.9 CMU_TIMER0CLK

TIMER0 Clock Control Register
Offset = 0x0040

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0

1:0	TIMER0CLKSRC	Timer0 clock Source: 00: CK24M 01: CK24M/24 Others: Reserved	R/W	0x0

4.3.3.10 CMU_TIMER1CLK

TIMER1 Clock Control Register
Offset = 0x0044

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1:0	TIMER1CLKSRC	Timer1 clock Source: 00: CK24M 01: CK24M/24 Others: Reserved	R/W	0x0

4.3.3.11 CMU_TIMER2CLK

TIMER2 Clock Control Register
Offset = 0x0048

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1:0	TIMER2CLKSRC	Timer2 clock Source: 00: CK24M 01: CK24M/24 10: TIMER2_EXT 11: reserved	R/W	0x0

4.3.3.12 CMU_TIMER3CLK

TIMER3 Clock Control Register
Offset = 0x004C

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1:0	TIMER3CLKSRC	Timer3 clock Source: 00: CK24M 01: CK24M/24 10: TIMER3_EXT 11: reserved	R/W	0x0

4.3.3.13 CMU_PWM0CLK

PWM0 Clock Control Register
Offset = 0x0050

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM0CLKSRC	PWM0 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM0CLKDIV	PWM0 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.14 CMU_PWM1CLK

PWM1 Clock Control Register
Offset = 0x0054

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM1CLKSRC	PWM1 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM1CLKDIV	PWM1 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.15 CMU_PWM2CLK

PWM2 Clock Control Register
Offset = 0x0058

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM2CLKSRC	PWM2 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM2CLKDIV	PWM2 Controller Clock Divisor: 0: /1 1: /2 …	R/W	0x0

		255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved		

4.3.3.16 CMU_PWM3CLK

PWM3 Clock Control Register
Offset = 0x005C

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM3CLKSRC	PWM3 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM3CLKDIV	PWM3 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.17 CMU_PWM4CLK

PWM4 Clock Control Register
Offset = 0x0060

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM4CLKSRC	PWM4 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM4CLKDIV	PWM4 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.18 CMU_PWM5CLK

PWM5 Clock Control Register
Offset = 0x0064

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM5CLKSRC	PWM5 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM5CLKDIV	PWM5 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.19 CMU_PWM6CLK

PWM6 Clock Control Register
Offset = 0x0068

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM6CLKSRC	PWM6 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM6CLKDIV	PWM6 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.20 CMU_PWM7CLK

PWM7 Clock Control Register
Offset = 0x006C

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0

9	PWM7CLKSRC	PWM7 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM7CLKDIV	PWM7 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.21 CMU_PWM8CLK

PWM8 Clock Control Register
Offset = 0x0070

Bit(s)	Name	Description	R/W	Reset
31:10	-	Reserved	R	0x0
9	PWM8CLKSRC	PWM8 Controller Clock Source 0: RC32K 1: CK24M	R/W	0x0
8:0	PWM8CLKDIV	PWM8 Controller Clock Divisor: 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

4.3.3.22 CMU_LRADCCLK

LRADC Clock Control Register
Offset = 0x007C

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1:0	LRADCCLKSRC	LRADC Clock Source 00: CK24M/94 255KHz 01: CK24M/46 522KHz 10: CK24M/22 1091KHz 11: RC32K	R/W	0x0

4.3.3.23 CMU_ADC01CLK

ADC01 Clock Control Register
Offset = 0x0080

Bit(s)	Name	Description	R/W	Reset
31	ADC01FIRCLKRVS	ADC01 FIR Clock Reverse 0: normal 1: reversed	R/W	0x0
30	-	Reserved	R	0x0
29	ADC01FIRCLKDIV	ADC01 FIR Clock Divisor 0: /1 1: /2	R/W	0x0
28	ADC01FIRCLKEN	ADC01 FIR Clock Enable 0: disable 1: enable	R/W	0x0
27	ADC01CICCLKRVS	ADC01 CIC Clock Reverse 0: normal 1: reversed	R/W	0x0
26	-	Reserved	R	0x0
25	ADC01CICCLKDIV	ADC01 CIC Clock Divisor 0: /1 1: /2	R/W	0x0
24	ADC01CICCLKEN	ADC01 CIC Clock Enable 0: disable 1: enable	R/W	0x0
23	-	Reserved	R	0x0
22	DMIC01CLKSRC	DMIC01 Clock Source 0: ADC01 Analog Clock 1: ADC23 Analog Clock	R/W	0x0
21	DMIC01CLKDIV	DMIC01 Clock Divisor 0: /1 1: /2	R/W	0x0
20	DMIC01CLKEN	DMIC01 Clock Enable 0: disable 1: enable	R/W	0x0
19	ADC01ANACLKRVS	ADC01 Analog Clock Reverse 0: normal 1: reversed	R/W	0x0
18	LPADCANACLKSRC	LPADC Analog Clock Source 0: ADC01 Analog Clock 1: ADC23 Analog Clock	R/W	0x0
17	-	Reserved	R	0x0
16	LPADCANACLKEN	LPADC Analog Clock Enable 0: disable 1: enable	R/W	0x0
15	-	Reserved	R	0x0
14	ADCANACLKSRC	ADC Analog Clock Source 0: ADC01 Analog Clock 1: ADC23 Analog Clock	R/W	0x0
13	-	Reserved	R	0x0
12	ADCANACLKEN	ADC Analog Clock Enable 0: disable 1: enable	R/W	0x0

11:10	ADC01OVFSDIV	ADC01 Over Sample Divisor 00: /1 01: /2 10: /4 11: /3	R/W	0x0
9:8	ADC01CLKSRC	ADC01_CLK Source 00: ADCG0_CLK 01: I2STX0_MCLK 10: PDMCLK(from external PIN) 11: reserved	R/W	0x0
7:6	ADCG0CLKSRC	ADCG0_CLK Source 00: AudioPLL0 01: AudioPLL1 10: CK24M 11: reserved	R/W	0x0
5	-	Reserved	R	0x0
4	ADCG0CLKPREDIV	ADCG0_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	ADCG0CLKDIV	ADCG0_CLK Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: /5	R/W	0x0

Note:

1) The sample rate(ADCG0_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152M			45.1584M		
BIT[4]	BIT[2:0]	ratio	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1
0	110	12	4.0960	16	32	3.7632	--	--
CK24M frequency			24M					
0	111	5	4.8(CK24M)	16(300fs)	32(150fs)	4.8(CK24M)	16(300fs)	32(150fs)

AUDIO_PLL0/1 frequency			49.152M			45.1584M		
BIT[4]	BIT[2:0]	ratio	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	48	96	11.2896	44.1	88.2
1	010	6	8.192	32	64	7.5264	--	--
1	011	8	6.144	24	48	5.6448	22.05	44.1

1	100	12	4.096	16	32	3.7632	--	--
1	101	16	3.072	12	24	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
CK24M frequency			24M					
1	111	10	2.4(CK24M)	8(300fs)	16(150fs)	2.4(CK24M)	8(300fs)	16(150fs)

4.3.3.24 CMU_ADC23CLK

ADC23 Clock Control Register
Offset = 0x0084

Bit(s)	Name	Description	R/W	Reset
31	ADC23FIRCLKRVS	ADC23 FIR Clock Reverse 0: normal 1: reversed	R/W	0x0
30	-	Reserved	R	0x0
29	ADC23FIRCLKDIV	ADC23 FIR Clock Divisor 0: /1 1: /2	R/W	0x0
28	ADC23FIRCLKEN	ADC23 FIR Clock Enable 0: disable 1: enable	R/W	0x0
27	ADC23CICCLKRVS	ADC23 CIC Clock Reverse 0: normal 1: reversed	R/W	0x0
26	-	Reserved	R	0x0
25	ADC23CICCLKDIV	ADC23 CIC Clock Divisor 0: /1 1: /2	R/W	0x0
24	ADC23CICCLKEN	ADC23 CIC Clock Enable 0: disable 1: enable	R/W	0x0
23	-	Reserved	R	0x0
22	DMIC23CLKSRC	DMIC23 Clock Source 0: ADC01 Analog Clock 1: ADC23 Analog Clock	R/W	0x0
21	DMIC23CLKDIV	DMIC23 Clock Divisor 0: /1 1: /2	R/W	0x0
20	DMIC23CLKEN	DMIC23 Clock Enable 0: disable 1: enable	R/W	0x0
19	ADC23ANACLKRVS	ADC23 Analog Clock Reverse 0: normal 1: reversed	R/W	0x0
18:12	-	Reserved	R	0x0
11:10	ADC23OVFSDIV	ADC23 Over Sample Divisor 00: /1 01: /2 10: /4 11: /3	R/W	0x0

9:8	ADC23CLKSRC	ADC23_CLK Source 00: ADCG1_CLK 01: I2STX0_MCLK 10: PDMCLK(from external PIN) 11: reserved	R/W	0x0
7:6	ADCG1CLKSRC	ADCG1_CLK Source 00: AudioPLL0 01: AudioPLL1 10: CK24M 11: reserved	R/W	0x0
5	-	Reserved	R	0x0
4	ADCG1CLKPREDIV	ADCG1_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	ADCG1CLKDIV	ADCG1_CLK Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: /5	R/W	0x0

Note:
1) The sample rate(ADCG1_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152M			45.1584M		
BIT[4]	BIT[2:0]	ratio	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1
0	110	12	4.0960	16	32	3.7632	--	--
CK24M frequency			24M					
0	111	5	4.8(CK24M)	16(300fs)	32(150fs)	4.8(CK24M)	16(300fs)	32(150fs)

AUDIO_PLL0/1 frequency			49.152M			45.1584M		
BIT[4]	BIT[2:0]	ratio	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)	Clock (MHz)	Clock/ 256(kHz)	Clock/ 128(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	48	96	11.2896	44.1	88.2
1	010	6	8.192	32	64	7.5264	--	--
1	011	8	6.144	24	48	5.6448	22.05	44.1
1	100	12	4.096	16	32	3.7632	--	--
1	101	16	3.072	12	24	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
CK24M frequency			24M					

1	111	10	2.4(CK24M)	8(300fs)	16(150fs)	2.4(CK24M)	8(300fs)	16(150fs)

4.3.3.25 CMU_DACCLK

DAC Clock Control Register
Offset = 0x0088

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0x0
11	PDMCLKEN	DAC PDMTX 128FS Clock Enable 0: disable 1: enable	R/W	0x0
10	SDMCLKEN	DAC SDM 128FS Clock Enable 0: disable 1: enable	R/W	0x0
9	-	Reserved	R	0x0
8	DACCLKSRC	DAC 128FS Clock Source 0: DAC 256FS CLK 1: PDMCLK(from external PIN)	R/W	0x0
7	DACCLKPOSTDIV	DAC 128FS Clock Post-Divisor 0: /2; 1: /1	R/W	0x0
6	DAC256FSSRC	DAC 256FS Clock Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
5	-	Reserved	R	0x0
4	DAC256FSPREDIV	DAC 256FS Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	DAC256FSDIV	DAC 256FS Clock Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0

Note:
1) The sample rate (DAC_256FS_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152M			45.1584M		
BIT[4]	BIT[2:0]	ratio	Clock (MHz)	Clock/ 256fs(kHz)	Clock/ 128fs(kHz)	Clock (MHz)	Clock/ 256fs(kHz)	Clock/ 128fs(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1

0	110	12	4.0960	16	32	3.7632	--	--
0	111	--	--	--	--	--	--	--

AUDIO_PLL0/1 frequency			49.152M			45.1584M		
BIT[4]	BIT[2:0]	ratio	Clock (MHz)	Clock/ 256fs(kHz)	Clock/ 128fs(kHz)	Clock (MHz)	Clock/ 256fs(kHz)	Clock/ 128fs(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	48	96	11.2896	44.1	88.2
1	010	6	8.192	32	64	7.5264	--	--
1	011	8	6.144	24	48	5.6448	22.05	44.1
1	100	12	4.096	16	32	3.7632	--	--
1	101	16	3.072	12	24	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
1	111	--	--	--	--	--	--	--

4.3.3.26 CMU_I2STX0CLK

I2STX Clock Control register
Offset = 0x008C

Bit(s)	Name	Description	R/W	Reset
31:30	-	Reserved	R	0x0
29:28	I2SSRDCLKSRC	I2S SRD Clock Source 00: CK24M 01: Audiopll0/2 10: Audiopll1/2 11: reserved	R/W	0x0
27:13	-	Reserved	R	0x0
12	I2STX0MCLKEXTREV	I2STX0_MCLK EXT Reverse 0: Normal 1: Reversed	R/W	0x0
11:10	-	Reserved	R	0x0
9:8	I2STX0MCLKSRC	I2STX0_MCLK Source 00: DAC_256fs_CLK 01: DAC_256fs_CLK/2 10: I2STX0_CLK 11: I2STX0_MCLK_EXT	R/W	0x0
7	-	Reserved	R	0x0
6	I2STX0CLKSRC	I2STX0_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
5	-	Reserved	R	0x0
4	I2STX0CLKPREDIV	I2STX0_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	I2STX0CLKDIV	I2STX0_CLK Divisor. 000: /1 001: /2 010: /3 011: /4	R/W	0x0

		100: /6 101: /8 110: /12 111: /24		

Note:
1) Refer to CMU_DACCLK for more information.
2) The sample rate (I2STX0_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1
0	110	12	4.0960	16	32	3.7632	--	--
0	111	24	2.048	8	16	1.8816	--	--

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256(kHz)	MCLK/ 128(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	64	128	11.2896	44.1	88.2
1	010	6	8.1920	48	96	7.5264	--	--
1	011	8	6.1440	32	64	5.6448	22.05	44.1
1	100	12	4.0960	24	48	3.7632	--	--
1	101	16	3.0720	16	32	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
1	111	48	1.024	4	8	0.9408	--	--

4.3.3.27 CMU_I2STX1CLK

I2STX Clock Control register
Offset = 0x0090

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	I2STX1MCLKEXTREV	I2STX1_MCLK EXT Reverse 0: Normal 1: Reversed	R/W	0x0
11:10	-	Reserved	R	0x0
9:8	I2STX1MCLKSRC	I2STX1_MCLK Source 00: I2STX1_CLK 01: I2STX0_MCLK 10: ADC01_CLK 11: I2STX1_MCLK_EXT	R/W	0x0
7	-	Reserved	R	0x0
6	I2STX1CLKSRC	I2STX1_CLK Source	R/W	0x0

		0: AudioPLL0 1: AudioPLL1		
5	-	Reserved	R	0x0
4	I2STX1CLKPREDIV	I2STX1_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	I2STX1CLKDIV	I2STX1_CLK Divisor. 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: /24	R/W	0x0

Note:

1) Refer to CMU_I2STX0CLK/CMU_ADC01CLK for more information.
2) The sample rate (I2STX1_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1
0	110	12	4.0960	16	32	3.7632	--	--
0	111	24	2.048	8	16	1.8816	--	--

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	64	128	11.2896	44.1	88.2
1	010	6	8.1920	48	96	7.5264	--	--
1	011	8	6.1440	32	64	5.6448	22.05	44.1
1	100	12	4.0960	24	48	3.7632	--	--
1	101	16	3.0720	16	32	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
1	111	48	1.024	4	8	0.9408	--	--

4.3.3.28 CMU_I2SRX0CLK

I2SRX0 Clock Control register
Offset = 0x0094

Bit(s)	Name	Description	R/W	Reset

31:13	-	Reserved	R	0x0
12	I2SRX0MCLKEXTREV	I2SRX0_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
11:10	-	Reserved	R	0x0
9:8	I2SRX0MCLKSRC	I2SRX0_MCLK Source 00: I2SRX0_CLK 01: I2STX0_MCLK 10: ADC01_CLK 11: I2SRX0_MCLK_EXT	R/W	0x0
7	-	Reserved	R	0x0
6	I2SRX0CLKSRC	I2SRX0_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
5	-	Reserved	R	0x0
4	I2SRX0CLKPREDIV	I2SRX0_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	I2SRX0CLKDIV	I2SRX0_CLK Divisor. 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: /24	R/W	0x0

Note:

1) Refer to CMU_I2STX0CLK/CMU_ADC01CLK for more information.
2) The sample rate (I2SRX0_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1
0	110	12	4.0960	16	32	3.7632	--	--
0	111	24	2.048	8	16	1.8816	--	--

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	64	128	11.2896	44.1	88.2
1	010	6	8.1920	48	96	7.5264	--	--
1	011	8	6.1440	32	64	5.6448	22.05	44.1
1	100	12	4.0960	24	48	3.7632	--	--

1	101	16	3.0720	16	32	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
1	111	48	1.024	4	8	0.9408	--	--

4.3.3.29 CMU_I2SRX1CLK

I2SRX1 Clock Control register
Offset = 0x0098

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	I2SRX1MCLKEXTREV	I2SRX1_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
11:10	-	Reserved	R	0x0
9:8	I2SRX1MCLKSRC	I2SRX1_MCLK Source 00: I2SRX1_CLK 01: I2STX1_MCLK 10: I2SRX0_MCLK 11: I2SRX1_MCLK_EXT	R/W	0x0
7	-	Reserved	R	0x0
6	I2SRX1CLKSRC	I2SRX1_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
5	-	Reserved	R	0x0
4	I2SRX1CLKPREDIV	I2SRX1_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
3	-	Reserved	R	0x0
2:0	I2SRX1CLKDIV	I2SRX1_CLK Divisor. 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: /24	R/W	0x0

Note:
3) Refer to CMU_I2STX1CLK/CMU_I2SRX0CLK for more information.
4) The sample rate (I2SRX1_CLK) is listed below:

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
0	000	1	49.152	192	--	45.1584	176.4	--
0	001	2	24.576	96	192	22.5792	88.2	176.4
0	010	3	16.384	64	128	15.0528	--	--
0	011	4	12.288	48	96	11.2896	44.1	88.2
0	100	6	8.1920	32	64	7.5264	--	--
0	101	8	6.1440	24	48	5.6448	22.05	44.1
0	110	12	4.0960	16	32	3.7632	--	--

0	111	24	2.048	8	16	1.8816	--	--

AUDIO_PLL0/1 frequency			49.152MHz			45.1584MHz		
BIT[4]	BIT[2:0]	ratio	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)	MCLK (MHz)	MCLK/ 256fs(kHz)	MCLK/ 128fs(kHz)
1	000	2	24.576	96	192	22.5792	88.2	176.4
1	001	4	12.288	64	128	11.2896	44.1	88.2
1	010	6	8.1920	48	96	7.5264	--	--
1	011	8	6.1440	32	64	5.6448	22.05	44.1
1	100	12	4.0960	24	48	3.7632	--	--
1	101	16	3.0720	16	32	2.8224	11.025	22.05
1	110	24	2.048	8	16	1.8816	--	--
1	111	48	1.024	4	8	0.9408	--	--

4.4RMU

4.4.1 Features

The RMU Controller has following features:
(1) The RMU (Reset Management Unit) can reset all the peripherals.
(2) The MCU can enter power-saving mode by setting the registers of RMU.

4.4.2 RMU Register List

RMU base address

Name	Physical Base Address
RMU_digital	0xC0000000

RMU register list

Offset	Register Name	Description
0x00000000	**MRCR0**	**Module Reset Control Register0**
0x00000004	**MRCR1**	**Module Reset Control Register1**

4.4.3 Register Description

4.4.3.1 MRCR0

MRCR0 (Module Reset Control Register0, offset = 0x00000000)

Bit(s)	Name	Description	R/W	Reset
31:26	-	Reserved	R	0x0
25	PWMRESET	PWM reset bit: 0: reset 1: normal	R/W	0x0
24	TIMERRESET	Timer0/1/2/3 controller reset bit: 0: reset 1: normal	R/W	0x0
23	UART3RESET	UART3 controller reset bit: 0: reset 1: normal	R/W	0x0
22	UART2RESET	UART2 controller reset bit: 0: reset 1: normal	R/W	0x0
21	UART1RESET	UART1 controller reset bit: 0: reset 1: normal	R/W	0x0
20	UART0RESET	UART0 controller reset bit: 0: reset 1: normal	R/W	0x0
19	TWI1RESET	TWI1 controller reset bit: 0: reset	R/W	0x0

		1: normal		
18	TWI0RESET	TWI0 controller reset bit: 0: reset 1: normal	R/W	0x0
17	-	-	R/W	0x0
16	USBRESET2	USB controller reset2 bit: 0: reset 1: normal	R/W	0x0
15	USBRESET	USB controller reset bit: 0: reset 1: normal	R/W	0x0
14	-	-	R/W	0x0
13	LCDRESET	LCD controller clock enable bit: 0: disable 1: enable	R/W	0x0
12	-	-	R/W	0x0
11	-	Reserved	R	0x0
10	SPI1CACHERESET	SPI1 CACHE Controller reset bit: 0: reset 1: normal	R/W	0x0
9	SPI0CACHERESET	SPI0 CACHE Controller reset bit: 0: reset 1: normal	R/W	0x0
8	SPI2RESET	SPI2 controller reset bit: 0: reset 1: normal	R/W	0x0
7	SPI1RESET	SPI1 controller reset bit: 0: reset 1: normal	R/W	0x0
6	SPI0RESET	SPI0 controller reset bit: 0: reset 1: normal	R/W	0x0
5:4	-	Reserved	R	0x0
3	SD1RESET	SD1 card controller reset bit: 0: reset 1: normal	R/W	0x0
2	SD0RESET	SD0 card controller reset bit: 0: reset 1: normal	R/W	0x0
1	NANDFLASHRESET	NandFlash controller reset bit: 0: reset 1: normal	R/W	0x0
0	DMARESET	DMA reset bit: 0: reset 1: normal	R/W	0x0

4.4.3.2 MRCR1

MRCR1 (Module Reset Control Register1, offset = 0x00000004)

Bit(s)	Name	Description	R/W	Reset
31:14	-	Reserved	R	0x0
13	-	-	R/W	0x0
12	-	-	R/W	0x0

11	-	Reserved	R	0x0
10	-	-	R/W	0x0
9	-	-	R/W	0x0
8	-	-	R/W	0x0
7	-	-	R/W	0x0
6	I2SRX1RESET	I2SRX1 reset bit: 0: reset 1: normal	R/W	0x0
5	I2SRX0RESET	I2SRX0 reset bit: 0: reset 1: normal	R/W	0x0
4	I2STX1RESET	I2STX1 reset bit: 0: reset 1: normal	R/W	0x0
3	I2STX0RESET	I2STX0 reset bit: 0: reset 1: normal	R/W	0x0
2	DACRESET	DAC controller clock reset bit: 0: reset 1: normal	R/W	0x0
1	-	-	R/W	0x0
0	ADCRESET	ADC controller reset bit: 0: reset 1: normal	R/W	0x0

4.5RTC

4.5.1 Features

- A individual power supply pin: SVCC
- Internal oscillator, LOSC or HOSC optional
- Calendar with a alarm IRQ which can wake up the PMU
- Four Timers with IRQS
- A watch dog which for CPU can be configured optional as IRQ or Reset

4.5.2 RTC Register List

RTC block base address

Name	Physical Base Address
RTC	0xC0030000

RTC Controller Registers

Offset	Register Name	Description
0x00	RTC_CTL	RTC Control Register
0x04	RTC_REGUPDATA	RTC Register update Register
0x08	RTC_DHMSALM	RTC Day Hour Minute and Second Alarm Register
0x0C	RTC_DHMS	RTC Day Hour Minute and Second Register
0x10	RTC_YMD	RTC Year Month Date Register
0x14	RTC_ACCESS	RTC freely access Register
0x1c	WD_CTL	Watch Dog Control register

4.5.3 RTC Register Description

4.5.3.1 RTC_CTL

Calendar Control Register
Offset=0x0000（SVCC）

Bits	Name	Description	R/W	Reset
31:19	-	Reserved	R	0x0
18	HOSC_DIV_EN	HOSC Division Circuit Enable 0: disable 1: enable	R/W	0x0
17	RTC32K_DIV_EN	RTC32K Division Circuit Enable 0: disable 1: enable	R/W	0x0
16	RTC32K_SEL	RTC32K Clock select 0 : LOSC 1 : EXT_32K	R/W	0x0
15:8	-	Reserved	R	0x0
7	LEAP	RTC Leap Year bit 1: leap year	R	0x1

		0: not leap year		
6:5	-	Reserved	R	0x0
4	CAL_EN	Calendar Enable 1: Enable 0: Disable	R/W	0x0
3:2	CAL_CLK_SEL	00: reserved 01: RTC32K_division 10: HOSC_division 11: RTC32K_divisio	R/W	0x1
1	ALIE	Alarm IRQ Enable 1: Enable 0: Disable	R/W	0x0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	R/W	0x0

4.5.3.2 RTC_REGUPDATA

Offset=0x0004（SVCC）

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	UPDATA	The SVCC register update control Register.	R/W	0x5A69

4.5.3.3 RTC_DHMSALM

Offset=0x0008（SVCC）

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20:16	HOUEAL	Alarm hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0
13:8	MINAL	Alarm minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0x0

Note： When writing this register, updating the RTC_REGUPDATA register is needed.

4.5.3.4 RTC_DHMS

Offset=0x000C（SVCC）

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20:16	HOUR	Time hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0
13:8	MIN	Time minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0

5:0	SEC	Time second setting 00H – 3BH	R/W	0x0

Note： When writing this register, updating the RTC_REGUPDATA register is needed.

4.5.3.5 RTC_YMD

Offset=0x0010（SVCC）

Bits	Name	Description	R/W	Reset
31：23	-	Reserved	R	0x0
22:16	YEAR	Time year setting 00H – 63H	R/W	0x0
15:12	-	Reserved	R	0x0
11:8	MON	Time month setting 01H – 0CH	R/W	0x1
7:5	-	Reserved	R	0x0
4:0	DATE	Time day setting 01H – 1FH	R/W	0x1

Note： When writing this register, updating the RTC_REGUPDATA register is needed.

4.5.3.6 RTC_ACCESS

Offset=0x0014（SVCC）

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	ACCESS	These bits can be accessed by CPU freely.	R/W	0x0

Note： Writing this register needn’t updating the RTC_REGUPDATA register, but software should wait for 3 cycles of CK32K (about 100us)

4.5.3.7 WD_CTL

Offset=0x001C（VDD）

Bits	Name	Description	R/W	Reset
31..7	-	reserved	R	0x0
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	RW	0x0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Reset,1: irq-. 0：Send Reset signal when watchdog overflow. 1：Send IRQ signal when watchdog overflow.	RW	0x0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 1: Enable 0: Disable	RW	0x0
3..1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length The watch dog’s overflow value is 180. 000 1khz 176 ms 001 512hz 352 ms 010 256hz 703ms	RW	0x0

		011 128hz 1.4 s 100 64hz 2.8s 101 32hz 5.6 s 110 16hz 11.2s 111 10ms		
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0x0

4.5.4 TIMER Register List

RTC block base address

Name	Physical Base Address
TIMER	0xC0030100

RTC Controller Registers

Offset	Register Name	Description
0x00	T0_CTL	Timer0 Control register
0x04	T0_VAL	Timer0 Value register
0x08	T0_CNT	Timer0 count register
0x20	T1_CTL	Timer1 Control register
0x24	T1_VAL	Timer1 Value register
0x28	T1_CNT	Timer1 count register
0x40	T2_CTL	Timer2 Control register
0x44	T2_VAL	Timer2 Value register
0x48	T2_CNT	Timer2 count register
0x4c	T2_CAP	Timer2 capture value register
0x60	T3_CTL	Timer3 Control register
0x64	T3_VAL	Timer3 Value register
0x68	T3_CNT	Timer3 count register
0x6c	T3_CAP	Timer3 capture value register

4.5.5 TIMER Register Description

4.5.5.1 T0_CTL

Timer0 control register
Offset=0x00（VDD）

Bits	Name	Description	R/W	Reset
31:6	-	Reserved	R	0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0x0
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit.	RW	0x0

4.5.5.2 T0_VAL

Timer0 value register
Offset=0x04（VDD）

Bits	Name	Description	R/W	Reset
31:0	VAL	Read or write Timer/Counter value register Note: If set Tx_VAL=n, irq would cause after n+1 Tx_CLK.	RW	0x0

4.5.5.3 T0_CNT

Timer0 current counter register
Offset=0x08（VDD）

Bits	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

4.5.5.4 T1_CTL

Timer1 control register
Offset=0x20（VDD）

Bits	Name	Description	R/W	Reset
31:6	-	Reserved	R	0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0x0
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit.	RW	0x0

4.5.5.5 T1_VAL

Timer1 value register
Offset=0x24（VDD）

Bits	Name	Description	R/W	Reset
31:0	VAL	Read or write current Timer0 value Note: If set Tx_VAL=n, irq would cause after n+1 Tx_CLK.	RW	0x0

4.5.5.6 T1_CNT

Timer1 current counter register
Offset=0x28（VDD）

Bits	Name	Description	R/W	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

4.5.5.7 T2_CTL

Timer2 control register
Offset=0x40（VDD）

Bits	Name	Description	R/W	Reset
31:13	-	Reserved	R	0
12	LEVEL	Current input pulse level. Using for counter mode and capture mode	R	0x0
11	DIR	Timer Counting direction set: 0：down 1：up	RW	0x0
10:9	MODE_SEL	Timer mode select: 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	RW	0x0
8	CAPTURE_IP	Capture event irq pending Writing 1 to clear this bit.	RW	0x0
7:6	CAPTURE_SE	Capture signal edge select 00:falling edge 01:rising edge 1x:both falling edge and rising edge	RW	0x0
5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable In timer/counter mode: When this bit is enabled, Timer2_Zero_IRQ sent out the irq signal until the pending bit was cleared. If DIR='0', T2_CNT compare with ZERO If DIR='1', T2_CNT compare with T2_VAL. For more detail reference to timer2/3 block diagram In input capture mode Every trigger edge would cause a capture irq, which pending reference to CAPTURE_IP	RW	0x0
0	ZIPD	Timer IRQ Pending, Writing 1 to clear this bit.	RW	0x0

4.5.5.8 T2_VAL

Timer2 value register
Offset=0x44（VDD）

Bits	Name	Description	R/W	Reset
31:0	VAL	Set timer counter value.	RW	0x0

4.5.5.9 T2_CNT

Timer2 current counter register
Offset=0x48（VDD）

Bits	Name	Description	R/W	Reset
31:0	CNT	Timer current value registers.	R	0x0

4.5.5.10 T2_CAP

Timer3 current counter register
Offset=0x4C（VDD）

Bits	Name	Description	R/W	Reset
31:0	CAP	Capture value register Using in capture mode, when capture irq occurred, read this register to get counter of pulse width counter. It would be reload by every trigger edge set in Tx_CTL.	R	0x0

4.5.5.11 T3_CTL

Timer3 control register
Offset=0x60（VDD）

Bits	Name	Description	R/W	Reset
31:13	-	Reserved	R	0
12	LEVEL	Current input pulse level. Using for counter mode and capture mode	R	0x0
11	DIR	Timer Counting direction set: 0：down 1：up	RW	0x0
10:9	MODE_SEL	Timer mode select: 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	RW	0x0
8	CAPTURE_IP	Input Capture mode event irq pending Writing 1 to clear this bit.	RW	0x0
7:6	CAPTURE_SE	Input Capture mode signal edge select 00:falling edge 01:rising edge 1x:both falling edge and rising edge	RW	0x0

5	En	Timer Enable 0:Disable 1:Enable	RW	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer Reload enable 0:Not reload 1:Reload	RW	0x0
1	ZIEN	Timer IRQ Enable. Include timer mode and input capture mode. In timer mode, When this bit is enabled, Timer_IRQ sent out the irq signal until the pending bit was cleared. If DIR='0', T3_CNT compare with ZERO If DIR='1', T3_CNT compare with T2_VAL. For more detail reference to timer2/3 block diagram In input capture mode, this bit would set be '1'when every trigger edge was found, which was set in CAPTURE_SE	RW	0x0
0	ZIPD	Timer mode IRQ Pending, Writing 1 to clear this bit. If occurred a timer overflow or zero, this pending would be set to '1'	RW	0x0

4.5.5.12 T3_VAL

Timer3 value register
Offset=0x64（VDD）

Bits	Name	Description	R/W	Reset
31:0	VAL	Set timer counter value.	RW	0x0

4.5.5.13 T3_CNT

Timer3 current counter register
Offset=0x68（VDD）

Bits	Name	Description	R/W	Reset
31:0	CNT	Timer current value registers.	R	0x0

4.5.5.14 T3_CAP

Timer3 current counter register
Offset=0x6C（VDD）

Bits	Name	Description	R/W	Reset
31:0	CAP	Capture value register Using in capture mode, when capture irq occurred, read this register to get counter of pulse width counter. It would be reload by every trigger edge set in Tx_CTL.	R	0x0

5 DMA

5.1 Overview

- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory.
- 10-channel ordinary DMA, that supports for transmission in burst 8 mode or single mode. Only one of the ten DMA channels can transfer data at the same time.
- One SDMA channel for YUV mode transmission
- DMA0-7 transmission can be triggered on the occurrence of selected events
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
- Transmission width includes 8-bit, 16-bit, and 32-bit, which is determined by DMA transmission type.

5.2 DMA Register List

DMA Control Group Base Address

Name	Physical Base Address
DMAController	0xC0070000

DMA Controller Register List

Offset	Register Name	Description
0x00000000	DMAIP	DMA interrupt pending register
0x00000004	DMAIE	DMA interrupt enable register
0x00000100	DMA0CTL	DMA0 control register
0x00000104	DMA0START	DMA0 start register
0x00000108	DMA0SADDR0	DMA0 source address register0
0x0000010c	DMA0SADDR1	DMA0 source address register1
0x00000110	DMA0DADDR0	DMA0 destination address register0
0x00000114	DMA0DADDR1	DMA0 destination address register1
0x00000118	DMA0BC	DMA0 byte counter register
0x0000011c	DMA0RC	DMA0 remain counter register
0x00000200	DMA1CTL	DMA1 control register
0x00000204	DMA1START	DMA1 start register
0x00000208	DMA1SADDR0	DMA1 source address register0
0x0000020c	DMA1SADDR1	DMA1 source address register1
0x00000210	DMA1DADDR0	DMA1 destination address register0
0x00000214	DMA1DADDR1	DMA1 destination address register1
0x00000218	DMA1BC	DMA1 byte counter register
0x0000021c	DMA1RC	DMA1 remain counter register
0x00000300	DMA2CTL	DMA2 control register
0x00000304	DMA2START	DMA2 start register
0x00000308	DMA2SADDR0	DMA2 source address register0
0x0000030c	DMA2SADDR1	DMA2 source address register1
0x00000310	DMA2DADDR0	DMA2 destination address register0
0x00000314	DMA2DADDR1	DMA2 destination address register1
0x00000318	DMA2BC	DMA2 byte counter register
0x0000031c	DMA2RC	DMA2 remain counter register
0x00000400	DMA3CTL	DMA3 control register

0x00000404	DMA3START	DMA3 start register
0x00000408	DMA3SADDR0	DMA3 source address register0
0x0000040c	DMA3SADDR1	DMA3 source address register1
0x00000410	DMA3DADDR0	DMA3 destination address register0
0x00000414	DMA3DADDR1	DMA3 destination address register1
0x00000418	DMA3BC	DMA3 byte counter register
0x0000041c	DMA3RC	DMA3 remain counter register
0x00000500	DMA4CTL	DMA4 control register
0x00000504	DMA4START	DMA4 start register
0x00000508	DMA4SADDR0	DMA4 source address register0
0x0000050c	DMA4SADDR1	DMA4 source address register1
0x00000510	DMA4DADDR0	DMA4 destination address register0
0x00000514	DMA4DADDR1	DMA4 destination address register1
0x00000518	DMA4BC	DMA4 byte counter register
0x0000051c	DMA4RC	DMA4 remain counter register
0x00000600	DMA5CTL	DMA5 control register
0x00000604	DMA5START	DMA5 start register
0x00000608	DMA5SADDR0	DMA5 source address register0
0x0000060c	DMA5SADDR1	DMA5 source address register1
0x00000610	DMA5DADDR0	DMA5 destination address register0
0x00000614	DMA5DADDR1	DMA5 destination address register1
0x00000618	DMA5BC	DMA5 byte counter register
0x0000061c	DMA5RC	DMA5 remain counter register
0x00000700	DMA6CTL	DMA6 control register
0x00000704	DMA6START	DMA6 start register
0x00000708	DMA6SADDR0	DMA6 source address register0
0x0000070c	DMA6SADDR1	DMA5 source address register1
0x00000710	DMA6DADDR0	DMA6 destination address register0
0x00000714	DMA6DADDR1	DMA6 destination address register1
0x00000718	DMA6BC	DMA6 byte counter register
0x0000071c	DMA6RC	DMA6 remain counter register
0x00000800	DMA7CTL	DMA7 control register
0x00000804	DMA7START	DMA7 start register
0x00000808	DMA7SADDR0	DMA7 source address register0
0x0000080c	DMA7SADDR1	DMA7 source address register1
0x00000810	DMA7DADDR0	DMA7 destination address register0
0x00000814	DMA7DADDR1	DMA7 destination address register1
0x00000818	DMA7BC	DMA7 byte counter register
0x0000081c	DMA7RC	DMA7 remain counter register
0x00000900	DMA8CTL	DMA8 control register
0x00000904	DMA8START	DMA8 start register
0x00000908	DMA8SADDR0	DMA8 source address register0
0x0000090c	DMA8SADDR1	DMA8 source address register1
0x00000910	DMA8DADDR0	DMA8 destination address register0
0x00000914	DMA8DADDR1	DMA8 destination address register1
0x00000918	DMA8BC	DMA8 byte counter register
0x0000091c	DMA8RC	DMA8 remain counter register
0x00000a00	DMA9CTL	DMA9 control register
0x00000a04	DMA9START	DMA9 start register
0x00000a08	DMA9SADDR0	DMA9 source address register0
0x00000a0c	DMA9SADDR1	DMA9 source address register1
0x00000a10	DMA9DADDR0	DMA9 destination address register0
0x00000a14	DMA9DADDR1	DMA9 destination address register1

0x00000a18	DMA9BC	DMA9 byte counter register
0x00000a1c	DMA9RC	DMA9 remain counter register
0x00001000	SDMACTL	SDMA control register
0x00001004	SDMASTART	SDMA start register
0x00001008	SDMASADDR0	SDMA source address register0
0x0000100c	SDMASADDR1	SDMA source address register1
0x00001010	SDMASADDR2	SDMA source address register2
0x00001014	SDMALCDCFG	SDMA LCD configuration register
0x00001018	SDMABC	SDMA byte counter register
0x0000101c	SDMARC	SDMA remain counter register

5.3 DMA Register Description

5.3.1.1 DMAIP

DMAIP (DMA Interrupt Pending Register, offset = 0x00000000)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:27	Reserved	Reserved	R	x
26	SDMAHFIP	SDMA Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
25	DMA9HFIP	DMA9 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
24	DMA8HFIP	DMA8 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
23	DMA7HFIP	DMA7 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
22	DMA6HFIP	DMA6 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
21	DMA5HFIP	DMA5 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
20	DMA4HFIP	DMA4 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
19	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
18	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
17	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
16	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
15:11	Reserved	Reserved	R	x
10	SDMATCIP	SDMA Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
9	DMA9TCIP	DMA9 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
8	DMA8TCIP	DMA8 Transmission Complete IRQ Pending	RW	0x0

		This bit can be written '1' to clear.		
7	DMA7TCIP	DMA7 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
6	DMA6TCIP	DMA6 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
5	DMA5TCIP	DMA5 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
4	DMA4TCIP	DMA4 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0

5.3.1.2 DMAIE

DMAIE (DMA Interrupt Enable Register, offset = 0x00000004)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:26	Reserved	Reserved	R	x
25	DMA9HFIE	DMA9 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
24	DMA8HFIE	DMA8 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
23	DMA7HFIE	DMA7 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
22	DMA6HFIE	DMA6 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
21	DMA5HFIE	DMA5 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
20	DMA4HFIE	DMA4 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
19	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0

18	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
17	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
16	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
15:10	Reserved	Reserved	R	x
9	DMA9TCIE	DMA9 Transmission Complete IRQ Enable: 0: disable DMA9 Transmission Complete interrupt 1: enable DMA9 Transmission Complete interrupt	RW	0x0
8	DMA8TCIE	DMA8 Transmission Complete IRQ Enable: 0: disable DMA8 Transmission Complete interrupt 1: enable DMA8 Transmission Complete interrupt	RW	0x0
7	DMA7TCIE	DMA7 Transmission Complete IRQ Enable: 0: disable DMA7 Transmission Complete interrupt 1: enable DMA7 Transmission Complete interrupt	RW	0x0
6	DMA6TCIE	DMA6 Transmission Complete IRQ Enable: 0: disable DMA6 Transmission Complete interrupt 1: enable DMA6 Transmission Complete interrupt	RW	0x0
5	DMA5TCIE	DMA5 Transmission Complete IRQ Enable: 0: disable DMA5 Transmission Complete interrupt 1: enable DMA5 Transmission Complete interrupt	RW	0x0
4	DMA4TCIE	DMA4 Transmission Complete IRQ Enable: 0: disable DMA4 Transmission Complete interrupt 1: enable DMA4 Transmission Complete interrupt	RW	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	RW	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	RW	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	RW	0x0

5.3.1.3 DMA0CTL

DMA0CTL (DMA0 control Register, offset = 0x00000100)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit 2:8bit 3:reserved	RW	0
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5’b00000: memory 5’b00001: UART0 TX FIFO 5’b00010: UART1 TX FIFO 5’b00011: UART2 TX FIFO 5’b00100: UART3 TX FIFO 5’b00101: SDIO FIFO 5’b00110: SD/MMC FIFO 5’b01000: SPI0 TX FIFO 5’b01001: SPI1 TX FIFO 5’b01010: SPI2 TX FIFO 5’b01011: DAC(PDMTX) FIFO0 5’b01100: DAC(PDMTX) FIFO1 5’b01101: IIS TX0 FIFO 5’b01110: IIS TX1 FIFO 5’b10001: - 5’b10011: TWI0 TX FIFO 5’b10100: TWI1 TX FIFO 5’b10101: PWM FIFO 5’b10110: LCD FIFO 5’b11000: NAND 5’b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5’b00000: memory 5’b00001: UART0 RX FIFO 5’b00010: UART1 RX FIFO	RW	0

		5’b00011: UART2 RX FIFO 5’b00100: UART3 RX FIFO 5’b00101: SDIO FIFO 5’b00110: SD/MMC FIFO 5’b01000: SPI0 RX FIFO 5’b01001: SPI1 RX FIFO 5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.4 DMA0START

DMA0START (DMA0 Interrupt Pending Register, offset = 0x00000104)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.5 DMA0SADDR0

DMA0SADDR0 (DMA0 Source Address Register0, offset = 0x00000108)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.6 DMA0SADDR1

DMA0SADDR1 (DMA0 Source Address Register1, offset = 0x0000010c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit.	RW	0x0

		The bit[1..0] is no effect if data width is 32-bit.		

5.3.1.7 DMA0DADDR0

DMA0DADDR0 (DMA0 Destination Address Register0, offset = 0x00000110)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.8 DMA0DADDR1

DMA0DADDR1 (DMA0 Destination Address Register1, offset = 0x00000114)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.9 DMA0BC

DMA0BC (DMA0 BYTE Counter Register, offset = 0x00000118)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.10 DMA0RC

DMA0RC (DMA0 Remain Counter Register, offset = 0x0000011c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.11 DMA1CTL

DMA1CTL (DMA1 control Register, offset = 0x00000200)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select	RW	0

		0:32bit 1:16bit 2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO	RW	0

		5’b01000: SPI0 RX FIFO 5’b01001: SPI1 RX FIFO 5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.12 DMA1START

DMA1START (DMA1 Interrupt Pending Register, offset = 0x00000204)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.13 DMA1SADDR0

DMA1SADDR0 (DMA1 Source Address Register0, offset = 0x00000208)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.14 DMA1SADDR1

DMA1SADDR1 (DMA1 Source Address Register1, offset = 0x0000020c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.15 DMA1DADDR0

DMA1DADDR0 (DMA1 Destination Address Register0, offset = 0x00000210)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.16 DMA1DADDR1

DMA1DADDR1 (DMA1 Destination Address Register1, offset = 0x00000214)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.17 DMA1BC

DMA1BC (DMA1 BYTE Counter Register, offset = 0x00000218)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.18 DMA1RC

DMA1RC (DMA1 Remain Counter Register, offset = 0x0000021c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.19 DMA2CTL

DMA2CTL (DMA2 control Register, offset = 0x00000300)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.20 DMA2START

DMA2START (DMA2 Interrupt Pending Register, offset = 0x00000304)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.21 DMA2SADDR0

DMA2SADDR0 (DMA2 Source Address Register0, offset = 0x00000308)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.22 DMA2SADDR1

DMA2SADDR1 (DMA2 Source Address Register1, offset = 0x0000030c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.23 DMA2DADDR0

DMA2DADDR0 (DMA2 Destination Address Register0, offset = 0x00000310)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.24 DMA2DADDR1

DMA2DADDR1 (DMA2 Destination Address Register1, offset = 0x00000314)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.25 DMA2BC

DMA2BC (DMA2 BYTE Counter Register, offset = 0x00000318)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.26 DMA2RC

DMA2RC (DMA2 Remain Counter Register, offset = 0x0000031c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.27 DMA3CTL

DMA3CTL (DMA3 control Register, offset = 0x00000400)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.28 DMA3START

DMA3START (DMA3 Interrupt Pending Register, offset = 0x00000404)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.29 DMA3SADDR0

DMA3SADDR0 (DMA3 Source Address Register0, offset = 0x00000408)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.30 DMA3SADDR1

DMA3SADDR1 (DMA3 Source Address Register1, offset = 0x0000040c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.31 DMA3DADDR0

DMA3DADDR0 (DMA3 Destination Address Register0, offset = 0x00000410)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.32 DMA3DADDR1

DMA3DADDR1 (DMA3 Destination Address Register1, offset = 0x00000414)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.33 DMA3BC

DMA3BC (DMA3 BYTE Counter Register, offset = 0x00000418)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.34 DMA3RC

DMA3RC (DMA3 Remain Counter Register, offset = 0x0000041c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.35 DMA4CTL

DMA4CTL (DMA4 control Register, offset = 0x00000500)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.36 DMA4START

DMA4START (DMA4 Interrupt Pending Register, offset = 0x00000504)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.37 DMA4SADDR0

DMA4SADDR0 (DMA4 Source Address Register0, offset = 0x00000508)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.38 DMA4SADDR1

DMA4SADDR1 (DMA4 Source Address Register1, offset = 0x0000050c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.39 DMA4DADDR0

DMA4DADDR0 (DMA4 Destination Address Register0, offset = 0x00000510)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.40 DMA4DADDR1

DMA4DADDR1 (DMA4 Destination Address Register1, offset = 0x00000514)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.41 DMA4BC

DMA4BC (DMA4 BYTE Counter Register, offset = 0x00000518)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.42 DMA4RC

DMA4RC (DMA4 Remain Counter Register, offset = 0x0000051c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.43 DMA5CTL

DMA5CTL (DMA5 control Register, offset = 0x00000600)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.44 DMA5START

DMA5START (DMA5 Interrupt Pending Register, offset = 0x00000604)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.45 DMA5SADDR0

DMA5SADDR0 (DMA5 Source Address Register0, offset = 0x00000608)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.46 DMA5SADDR1

DMA5SADDR1 (DMA5 Source Address Register1, offset = 0x0000060c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.47 DMA5DADDR0

DMA5DADDR0 (DMA5 Destination Address Register0, offset = 0x00000610)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.48 DMA5DADDR1

DMA5DADDR1 (DMA5 Destination Address Register1, offset = 0x00000614)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.49 DMA5BC

DMA5BC (DMA5 BYTE Counter Register, offset = 0x00000618)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.50 DMA5RC

DMA5RC (DMA5 Remain Counter Register, offset = 0x0000061c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.51 DMA6CTL

DMA6CTL (DMA6 control Register, offset = 0x00000700)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.52 DMA6START

DMA6START (DMA6 Interrupt Pending Register, offset = 0x00000704)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.53 DMA6SADDR0

DMA6SADDR0 (DMA6 Source Address Register0, offset = 0x00000708)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.54 DMA6SADDR1

DMA6SADDR1 (DMA6 Source Address Register1, offset = 0x0000070c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.55 DMA6DADDR0

DMA6DADDR0 (DMA6 Destination Address Register0, offset = 0x00000710)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.56 DMA6DADDR1

DMA6DADDR1 (DMA6 Destination Address Register1, offset = 0x00000714)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.57 DMA6BC

DMA6BC (DMA6 BYTE Counter Register, offset = 0x00000718)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.58 DMA6RC

DMA6RC (DMA6 Remain Counter Register, offset = 0x0000071c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.59 DMA7CTL

DMA7CTL (DMA7 control Register, offset = 0x00000800)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.60 DMA7START

DMA7START (DMA7 Interrupt Pending Register, offset = 0x00000804)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.61 DMA7SADDR0

DMA7SADDR0 (DMA7 Source Address Register0, offset = 0x00000808)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.62 DMA7SADDR1

DMA7SADDR1 (DMA7 Source Address Register1, offset = 0x0000080c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.63 DMA7DADDR0

DMA7DADDR0 (DMA7 Destination Address Register0, offset = 0x00000810)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.64 DMA7DADDR1

DMA7DADDR1 (DMA7 Destination Address Register1, offset = 0x00000814)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.65 DMA7BC

DMA7BC (DMA7 BYTE Counter Register, offset = 0x00000818)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.66 DMA7RC

DMA7RC (DMA7 Remain Counter Register, offset = 0x0000081c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.67 DMA8CTL

DMA8CTL (DMA8 control Register, offset = 0x00000900)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.68 DMA8START

DMA8START (DMA8 Interrupt Pending Register, offset = 0x00000904)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.69 DMA8SADDR0

DMA8SADDR0 (DMA8 Source Address Register0, offset = 0x00000908)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.70 DMA8SADDR1

DMA8SADDR1 (DMA8 Source Address Register1, offset = 0x0000090c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.71 DMA8DADDR0

DMA8DADDR0 (DMA8 Destination Address Register0, offset = 0x00000910)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.72 DMA8DADDR1

DMA8DADDR1 (DMA8 Destination Address Register1, offset = 0x00000914)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.73 DMA8BC

DMA8BC (DMA8 BYTE Counter Register, offset = 0x00000918)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.74 DMA8RC

DMA8RC (DMA8 Remain Counter Register, offset = 0x0000091c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.75 DMA9CTL

DMA9CTL (DMA9 control Register, offset = 0x00000a00)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
21:20	TWS	Transmit data width select 0:32bit 1:16bit	RW	0

		2:8bit 3:reserved		
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0
17	TRM	0:Burst8 1:Single	RW	0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S, and DMA-ASRC transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15	DAM	Destination address mode 0: increment 1: constant	RW	0
14:13	-	Reserved	-	0
12:8	DSTSL	Destination select: 5'b00000: memory 5'b00001: UART0 TX FIFO 5'b00010: UART1 TX FIFO 5'b00011: UART2 TX FIFO 5'b00100: UART3 TX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 TX FIFO 5'b01001: SPI1 TX FIFO 5'b01010: SPI2 TX FIFO 5'b01011: DAC(PDMTX) FIFO0 5'b01100: DAC(PDMTX) FIFO1 5'b01101: IIS TX0 FIFO 5'b01110: IIS TX1 FIFO 5'b10001: - 5'b10011: TWI0 TX FIFO 5'b10100: TWI1 TX FIFO 5'b10101: PWM FIFO 5'b10110: LCD FIFO 5'b11000: NAND 5'b11101: - Other: Reserved	RW	0
7	SAM	Source address mode 0: increment 1: constant	RW	0
6:5	-	Reserved	-	0
4:0	SRCSL	Source Select: 5'b00000: memory 5'b00001: UART0 RX FIFO 5'b00010: UART1 RX FIFO 5'b00011: UART2 RX FIFO 5'b00100: UART3 RX FIFO 5'b00101: SDIO FIFO 5'b00110: SD/MMC FIFO 5'b01000: SPI0 RX FIFO 5'b01001: SPI1 RX FIFO	RW	0

		5’b01010: SPI2 RX FIFO 5’b01011: ADC01 FIFO 5’b01100: ADC23 FIFO (I2S RX0) 5’b01101: IIS RX0 FIFO 5’b01110: IIS RX1 FIFO 5’b10001: - 5’b10011: TWI0 RX FIFO 5’b10100: TWI1 RX FIFO 5’b11000: NAND 5’b11101: - Other: Reserved		

5.3.1.76 DMA9START

DMA9START (DMA9 Interrupt Pending Register, offset = 0x00000a04)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written ‘0’ to abort DMAx transmission.	RW	0x0

5.3.1.77 DMA9SADDR0

DMA9SADDR0 (DMA9 Source Address Register0, offset = 0x00000a08)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.78 DMA9SADDR1

DMA9SADDR1 (DMA9 Source Address Register1, offset = 0x00000a0c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.79 DMA9DADDR0

DMA9DADDR0 (DMA9 Destination Address Register0, offset = 0x00000a10)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.80 DMA9DADDR1

DMA9DADDR1 (DMA9 Destination Address Register1, offset = 0x00000a14)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMADADDR	The destination address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.81 DMA9BC

DMA9BC (DMA9 BYTE Counter Register, offset = 0x00000a18)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.82 DMA9RC

DMA9RC (DMA9 Remain Counter Register, offset = 0x00000a1c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

5.3.1.83 SDMACTL

SDMACTL (SDMA control Register, offset = 0x00001000)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:22	-	Reserved	-	0
19	-	Reserved	-	0
18	reload	Reload the DMA controller registers and start DMA transmission after current DMA	RW	0

		transmission is complete: 0: disable reload mode 1: enable reload mode		
17:16	LCDMODE	The transfer mode while LCD DRQ is selected: 00: RGB 01: reserved 10: YUV444_one_buffer 11: YUV420_one_buffer	RW	0x0
15:0	-	Reserved	-	0

5.3.1.84 SDMASTART

SDMASTART (SDMA Interrupt Pending Register, offset = 0x00001004)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:1	Reserved	-	-	-
0	DMASTART	DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	RW	0x0

5.3.1.85 SDMASADDR0

SDMASADDR0 (SDMA Source Address Register0, offset = 0x00001008)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.86 SDMASADDR1

SDMASADDR1 (SDMA Source Address Register1, offset = 0x0000010c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.87 SDMASADDR2

SDMASADDR2(SDMA Source Address Register2, offset = 0x00001010)

Bit	Bit	Function	Access	Reset

Number	Mnemonic			
31:0	DMASADDR	The source address of DMA transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	RW	0x0

5.3.1.88 SDMALCDCFG

SDMALCDCFG (SDMA LCD configuration register, offset = 0x00001014)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:11	Reserved	Be read as 23-zeros	-	-
26:16	IMAGWIDTH	The data width of IMAG buffer.	R/W	0
15:11	Reserved	Be read as 23-zeros	-	-
10:0	LCDWIDTH	The data width of LCD buffer.	R/W	0

5.3.1.89 SDMABC

SDMABC (SDMA BYTE Counter Register, offset = 0x00001018)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	Reserved	R	x
17:0	DMABYTECOUNTER	The frame length of DMA transmission.	RW	0x0

5.3.1.90 SDMARC

SDMARC (SDMA Remain Counter Register, offset = 0x0000101c)

Bit Number	Bit Mnemonic	Function	Access	Reset
31:18	Reserved	-	-	-
17:0	DMARemainCounterH	The Remain Counter of DMA transmission.	R	0x0

6 Storage

6.1 NANDFLASH Controller

6.1.1 Features

- 8bit/24bit/40bit/60bit Error Correction support
- multiple NAND interfaces: asynchronous; NV-DDR, NV-DDR2 (ONFI 3.0); toggle nand 2.0
- Data error Corrected by HW automatically
- Seven bytes address support for new NAND Flash support
- SLC、MLC & TLC NAND Flash support
- 8 bit wide NAND support
- Monitor the NAND flash Ready/Busy signal by HW support

6.2 SD/MMC card controller

6.2.1 Features

- Fully compliant with MMC Specification 4.41
- Fully compliant with SD card Specification 2.0
- Fully compliant with SDIO 3.0
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for input Signal, Output Delay Chain for output signal.。
- Integrated Watchdog Timeout Counter to report Exception happening.
- Integrated Pull up resistance (value 51Komh) for Data and CMD line.
- Integrated CRC calculate and check circuit.
- Send continuous clock to support SDIO card.
- Support 3.1/1.8V CLK PAD voltage.
- Support 3.1/1.8V CMD PAD voltage.
- Support 3.1V/1.8 DAT PAD voltage.
- Band Width: 50Mbyte/S
- Maximal SD interface Clock: 100MHz

7 Transfer and Communication

7.1SPI0

7.1.1 Features

SPI is a combination module which includes conventional SPI and SPI_Cache interface.

- Only support master mode
- Support mode0 and mode3
- Support AHB and Cache access SPI and no DMA interface
- Only Support 8bit transfer mode
- Support 32 bit seed 8bit randomize
- Support 3wire
- Support 16 level delay chain, 1ns/step
- Support 1x/2x/dual/4x/quad access SPI NOR
- Support 16bit CRC only when Cache access fifo, not support CRC when AHB access fifo
- Support cache abort
- Support 100MHz spi_clk as highest speed
- Let R = spi_clk/cpu_clk. In 1x mode, R < 256; In 2x/dual mode, R < 128; In 4x/quad mode, R <64

7.1.2 Function Description

7.1.2.1 SPI Mode Timing

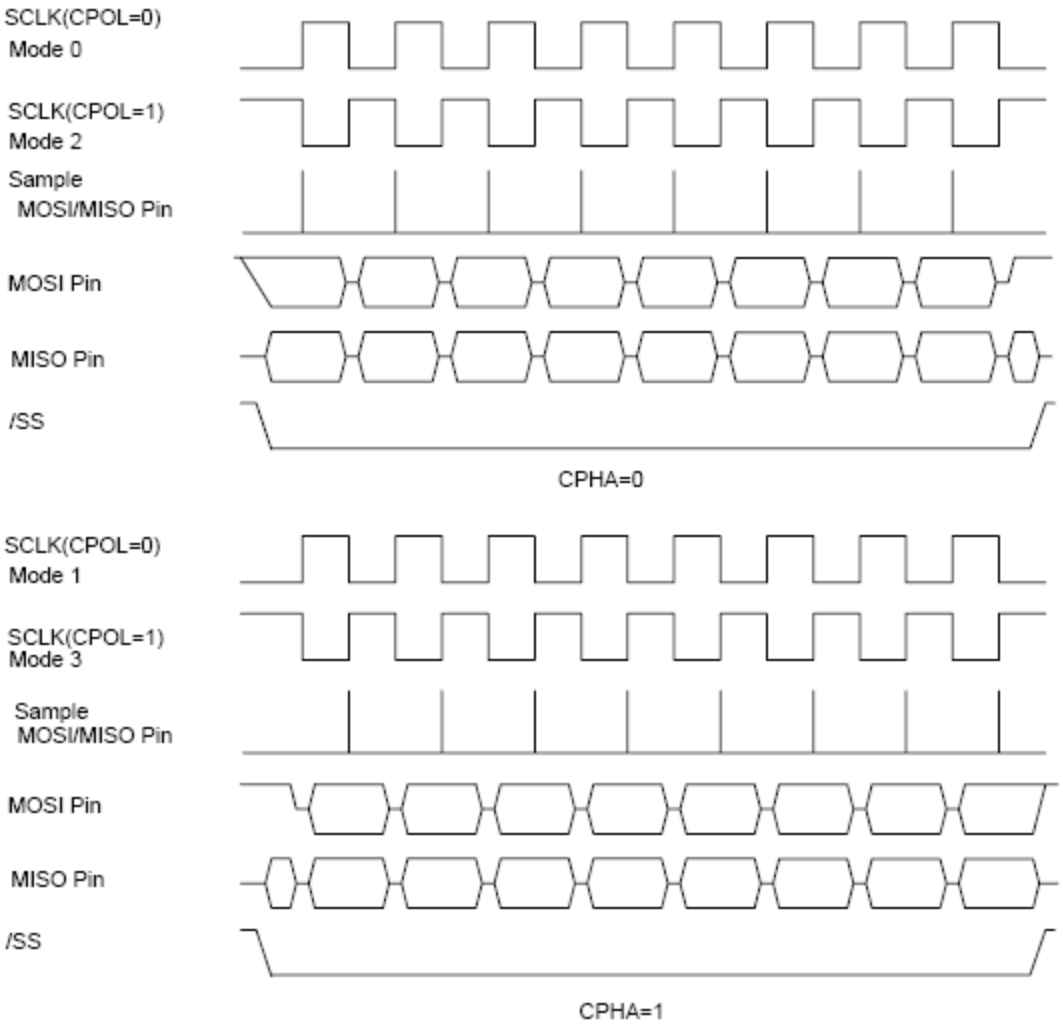


Figure 7-1 SPI Mode Timing

7.1.2.2 Page Programme Timing

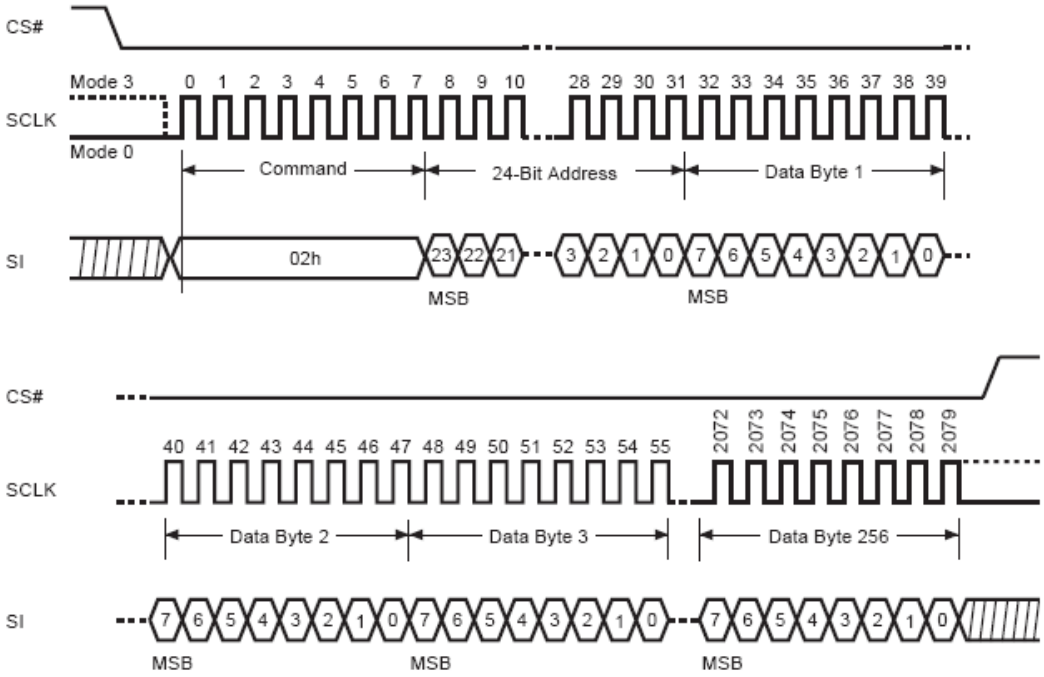


Figure 7-2 Page Programme Timing

7.1.2.3 Dual Read Timing (Dual output read)

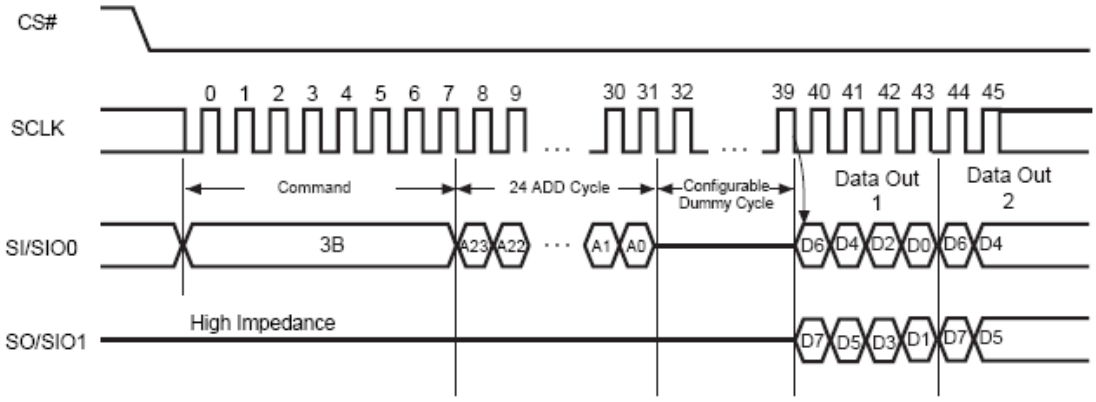


Figure 7-3 Dual Read Timing

7.1.2.4 2x Read Timing (Dual Input Output Read)

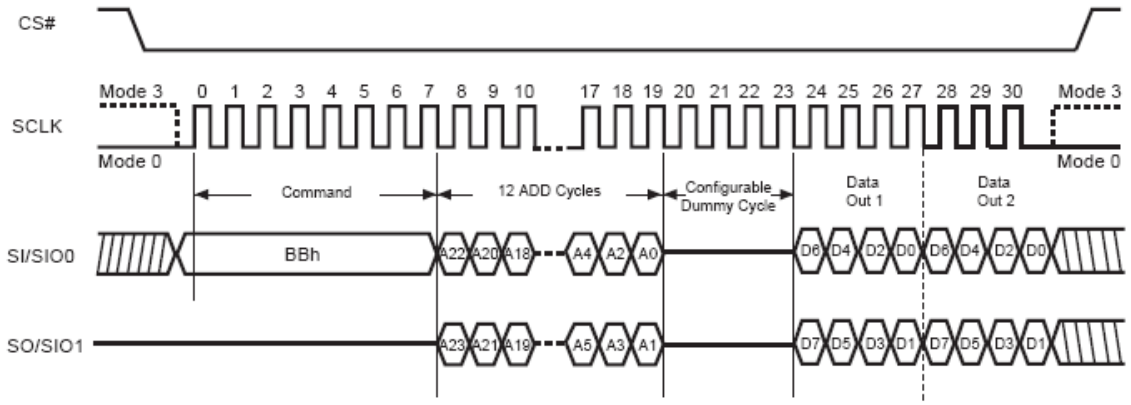


Figure 7-4 2x Read Timing

7.1.2.5 Quad Read Timing

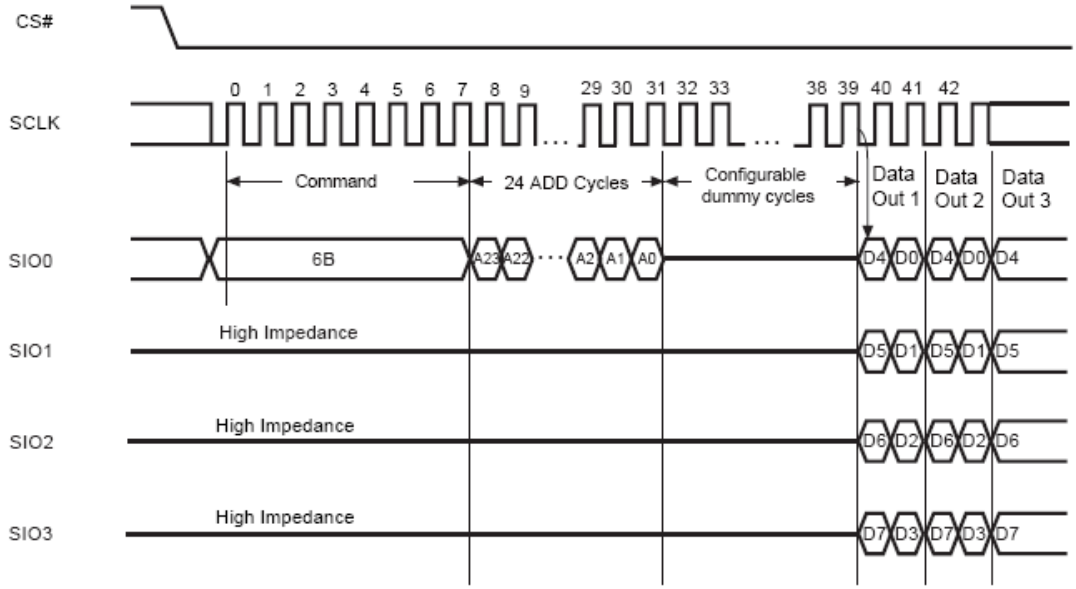


Figure 7-5 Quad Read Timing

7.1.2.6 4x Read Timing

When in 4x mode，spi_mosi is used as spi_io0，and spi_miso is used as spi_io1.
The 4x mode instruction is “EBh”, and there are eight “dummy” clocks after the 24-bit address。

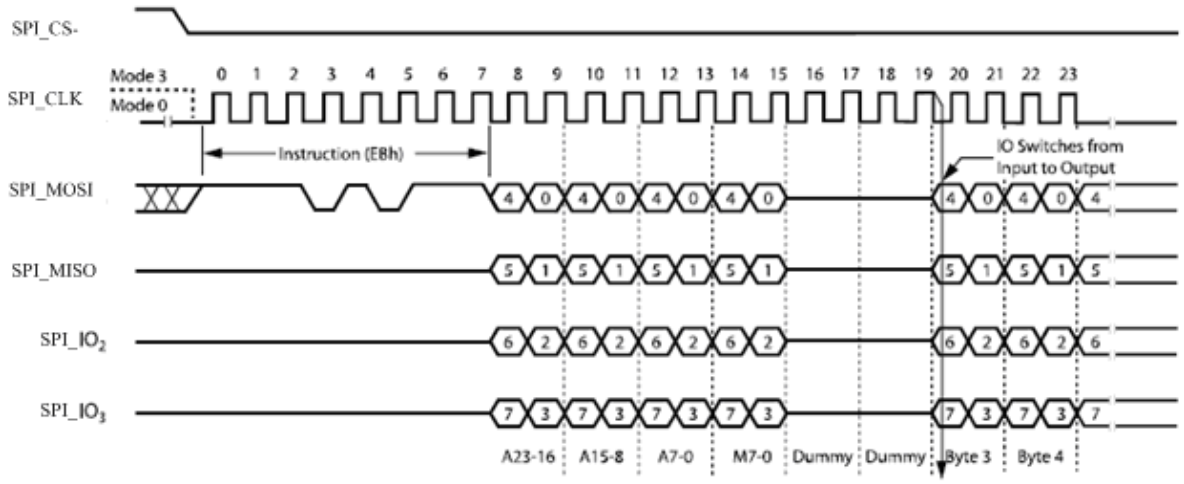


Figure 7-6 4x Read Timing(1)

The Mode bits (M7-0) equals “A5”hex,so the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown blow. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low.

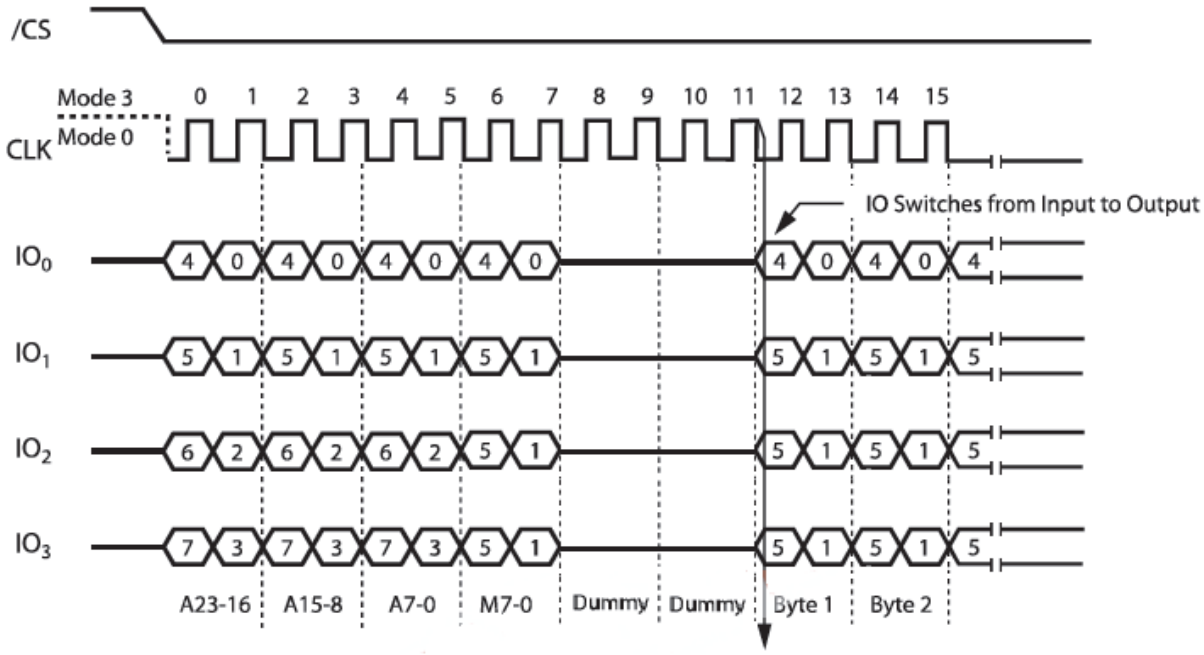


Figure 7-7 4x Read Timing(2)

7.1.2.7 3 Wire Mode

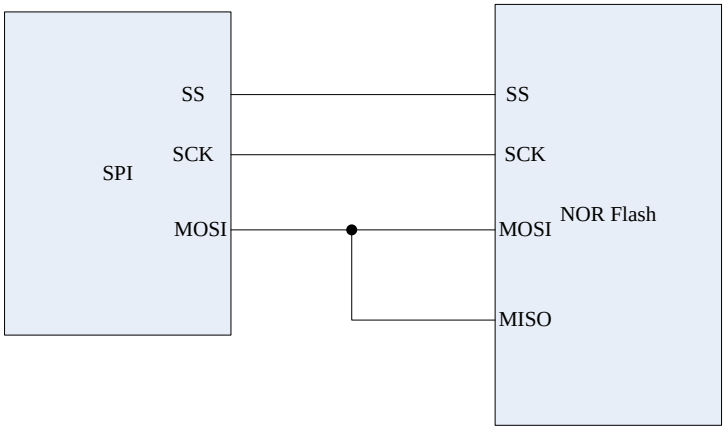


Figure 7-8 3 Wire Mode

7.1.3 Operation Manual

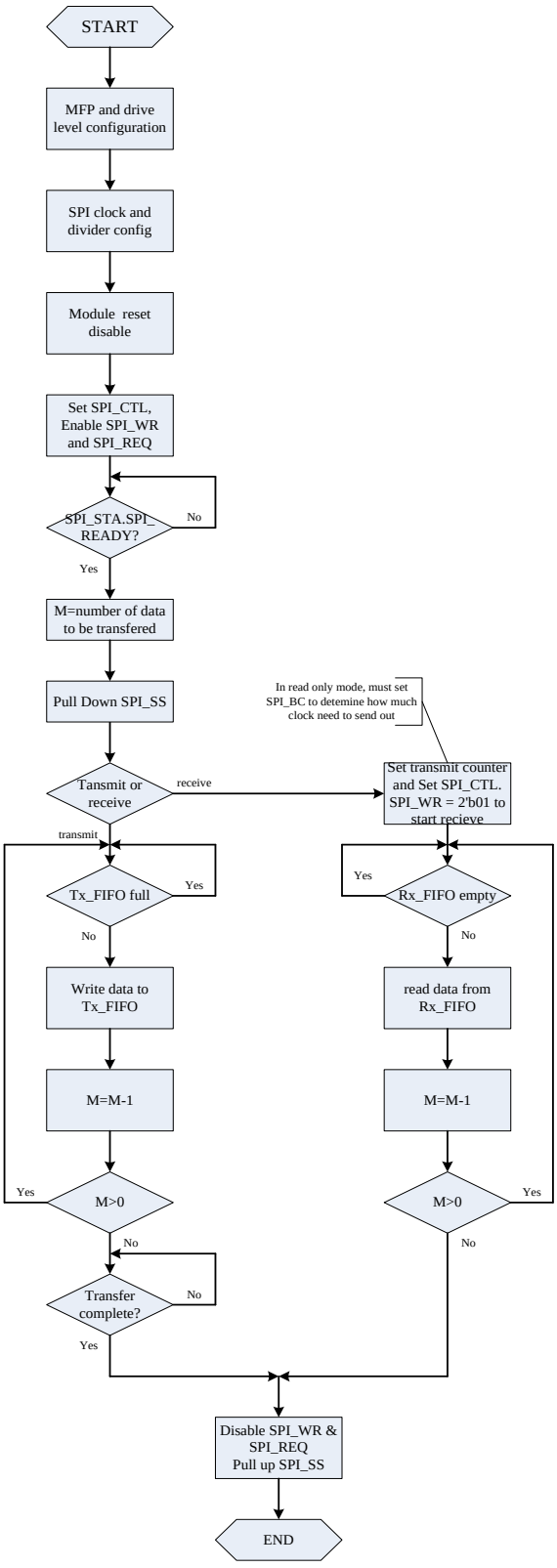


Figure 7-9 SPI0 master operation flow

7.1.4 Register List

SPI0 Controller Base Address

Name	Physical Base Address
SPI0_REGISTER	0xC00A0000

SPI0 Controller Registers List

Offset	Register Name	Description
0x0000	SPI0_CTL	SPI0 Control Register
0x0004	SPI0_STA	SPI0 Status Register
0x0008	SPI0_TXDAT	SPI0 Transmit FIFO Data Register
0x000C	SPI0_RXDAT	SPI0 Receive FIFO Data Register
0x0010	SPI0_BC	SPI0 Byte Counter Register
0x0018	CACHE_ERROR_ADDR	Cache address for cpu to inquire
0x001C	CACHE_MODE	Cache Mode configure register
0x0030	SPI0_CHECKRB_COUNTER	SPI0 auto check RB counter register
0x0034	SPI0_SNOR_CRM	SPI0 SNOR continue read mode register

7.1.5 Register Description

7.1.5.1 SPI0_CTL

SPI0 Control Register
Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	-	Reserved	R/W	0x0
29	NO_CRC_RAND_RXEN	NO CRC Area Rx Randomizer Enable (Cache Interface Only) No CRC area will enable rx randomize function when enable SPI0_CTL[12] and this bit simultaneously. 0: Disable 1: Enable	R/W	0x0
28	SPI_MODE_SELECT	SPI0 Mode Select 0: Mode3 1: Mode0 Note: to change the mode must disable SPI then enable SPI	R/W	0x0
27	DUAL_QUAD_SELECT	SPI Dual/Quad Mode Select It works only when SPI_IO_MODE select 2x IO mode or 4x IO mode 0: 2x/4x mode 1: dual/quad mode	R/W	0x0
26	RX_WRITE_SEL	SPI0 Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0

25:24	TIME_OUT_CTRL	Time Out Control (Cache Interface Only) 00: wait 16 cycles 01: wait 32 cycles 10: wait 64 cycles 11: wait 128 cycles	R/W	0x0
23:22	CRC_ERROR_TIME	CRC Error Times (Cache Interface Only) 00: 2times 01: 4times 10: 8times 11: 16times	R/W	0x0
21	CRC_IRQ_EN	CRC Error IRQ Enable (Cache Interface Only) SPI will set CRC Error pending when CRC_Error_TIME times consecutive error occurs 0: Disable 1: Enable	R/W	0x0
20	CRC_EN	CRC Enable (Cache Interface Only) 0: Disable 1: Enable	R/W	0x0
19:16	SPI_DELAY	SPI0 Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: delay 1 ns 0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns 1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns 1110: delay 14 ns 1111: delay 15 ns	R/W	0x0
15:14	-	Reserved	R/W	0x0
13	RAND_TXEN	SPI0 Master TX Randomizer enable 0: disable 1: enable	R/W	0x0
12	RAND_RXEN	SPI0 Master RX Randomizer enable 0: disable 1: enable	R/W	0x0
11:10	SPI_IO_MODE	SPI0 data I/O mode select 00: 1x I/O mode select 01: 1x I/O mode select 10: 2x I/O mode select 11: 4x I/O mode select	R/W	0x0
9	SPI_3WIRE	SPI0 Master 3-wire mode enable 0:disable 1:enable use 3-wire mode only in master read only or write only mode.	R/W	0x0
8	SPI_REQ	SPI0 Bus Request (AHB Interface Only, Please reference operation manual) 0:disable 1:enable	R/W	0x0

7	SPI_TDRQ_EN	SPI0 TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 8 level empty; 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI0 RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 8 level full. 0: disable 1: enable	R/W	0x0
5	SPI_TX_FIFO_EN	SPI0 Tx FIFO Enable (AHB Interface Only) 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI0 Rx FIFO Enable (AHB Interface Only) 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI0 NSS pin control output (AHB Interface Only) 0: output low 1: output high	R/W	0x1
2	SPI_LOOP	SPI0 Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI0 Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

7.1.5.2 SPI0_STA

SPI0 Status Register
Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	SPI_READY	SPI0 Ready (AHB Interface Only, please reference operation manual) 0: not ready 1: ready	R	0x0
7	CRC_PD	CRC Error Pending, Write 1 to this bit will clear it. (Cache Interface Only) 0: No CRC Error Pending 1: CRC Error Pending.	R/W	0x0
6	SPI_BUSY	SPI0 master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0
5	SPI_TXFU	SPI0 TX FIFO Full (AHB Interface Only) 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI0 TX FIFO Empty (AHB Interface Only) 0: not empty 1: empty	R	0x1
3	SPI_RXFU	SPI0 RX FIFO Full (AHB Interface Only)	R	0x0

		0: not full 1: full		
2	SPI_RXEM	SPI0 RX FIFO Empty (AHB Interface Only) 0: not empty 1: empty	R	0x1
1	CRC_ERROR	CRC Error Status, Write 1 to this bit will clear it. (Cache Interface Only) 0: No CRC Error 1: CRC Error.	R/W	0x0
0	-	Reserved	R	0x0

7.1.5.3 SPI0_TXDAT

SPI0 Transmit FIFO Data Register
Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	SPI_TXDAT	SPI0 Tx Data[7:0] Writing this field will send 1 byte to 8bitx16 levels depth SPI0 TX FIFO	W	0x0

7.1.5.4 SPI0_RXDAT

SPI0 Receiver FIFO Data Register
Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	SPI_RXDAT	SPI0 Rx Data[7:0] Writing this field will fetch 1 byte to 8bitx16 levels depth SPI0 RX FIFO only when SPI_CTL. RAND_RXEN disable	R	0x0

7.1.5.5 SPI0_BC

SPI0 Bytes Count Register, this register is used for setting SPI bytes counter bits in SPI master read only mode
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be recieved	R	0x0
15:0	SPI_BC	Bytes Counter [15: 0]	R/W	0x0

7.1.5.6 CACHE_ERROR_ADDR

SPI0 Cache Error Addr register
Offset=0x0018

Bit(s)	Name	Description	R/W	Reset

31:24	-	Reserved	R	0x0
23:5	CACHE_ERROR_ADDR	Cache read ERROR Address, only for cpu to inquire	R	0x7FFFF
4:0	-	Reserved	R	0x0

7.1.5.7 CACHE_MODE

SPI0 MODE register
Offset=0x001C

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	RB	SNOR RB status bit 0: not busy 1: busy	R	0x0
7:2	-	Reserved	R	0x0
1	-	Reserved	W/R	0x0
0	CHECKRB	SNOR auto check RB start bit 0: disable auto check RB 1: start auto check RB	W/R	0x0

7.1.5.8 SPI0_CHECKRB_COUNTER

SPI0 auto check RB counter register
Offset=0x0030

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0x0
11:0	RBCOUNTER	Auto check RB counter	W/R	0xFFF

7.1.5.9 SPI0_SNOR_CRM

SPI0 SNOR continue read mode register
Offset=0x0034

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	CRM	SNOR continue read mode	W/R	0xA5

7.2SPI1

7.2.1 Features

- Support SPI normal mode: mode 0/1/2/3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data
- Support D-cache Interface
- Support 16 level delay chain, 1ns/step
- Support 1x/2x/dual/4x/quad access SPI NOR
- Support slave mode
- Support 100MHz spi_clk as highest speed

7.2.2 Function Description

7.2.2.1 SPI Write Timing

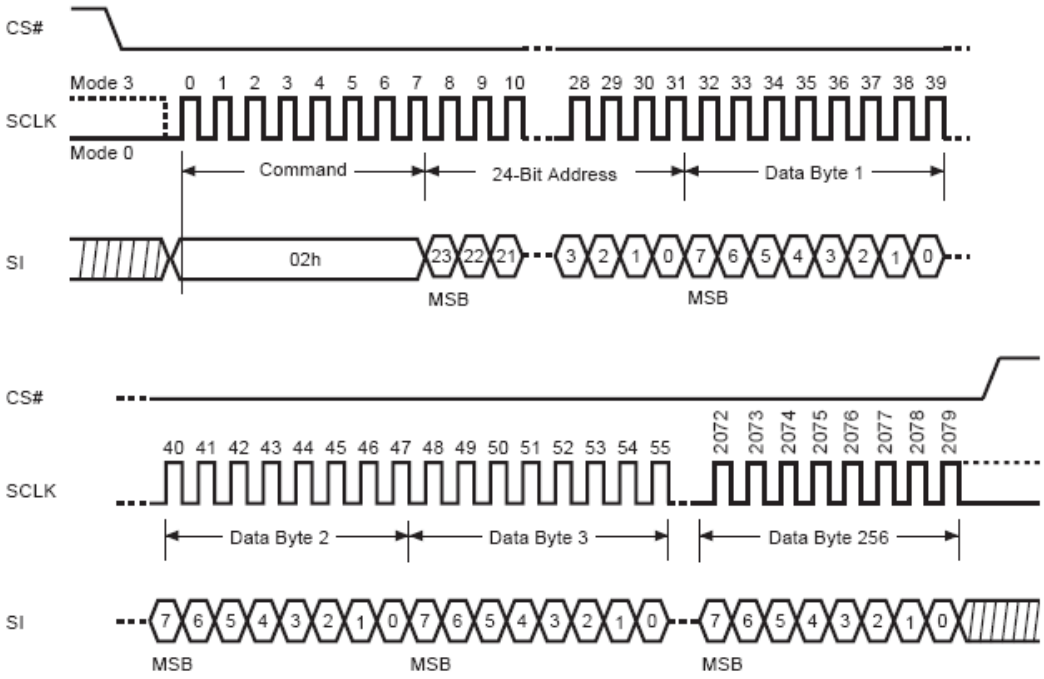
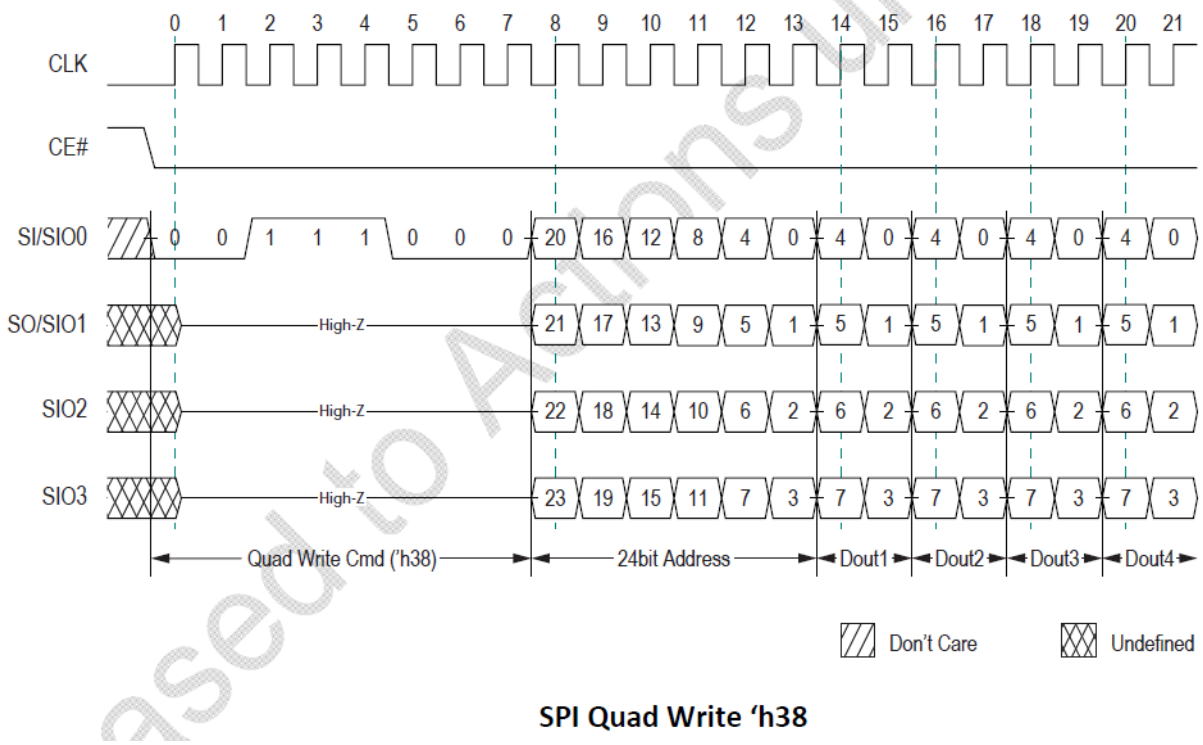


Figure 7-10 Page Programme Timing@single wire



SPI Quad Write 'h38

Figure 7-11 Page Programme Timing@four wires

7.2.2.2 Dual Read Timing (Dual output read)

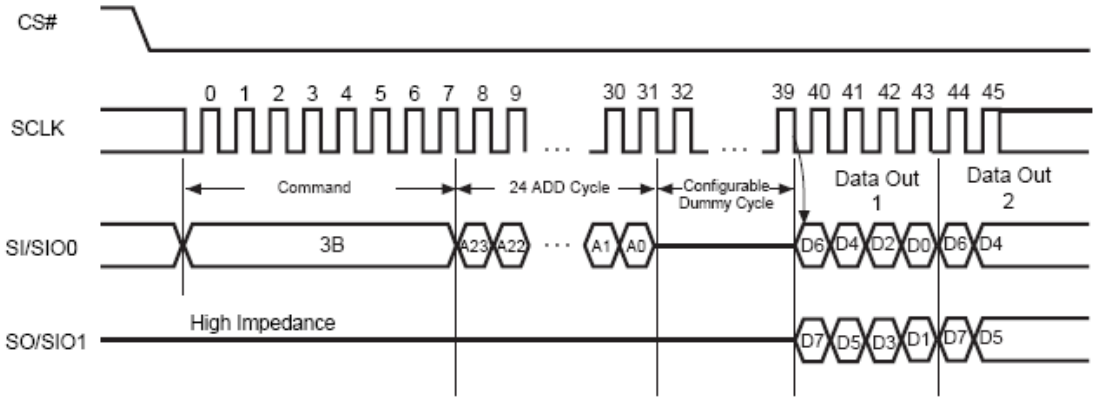


Figure 7-12 Dual Read Timing

7.2.2.3 2x Read Timing (Dual Input Output Read)

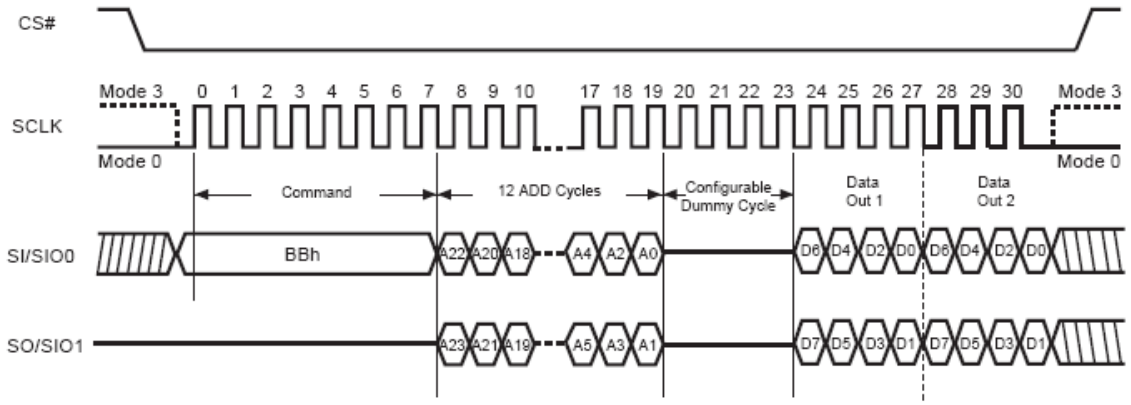


Figure 7-13 2x Read Timing

7.2.2.4 Quad Read Timing

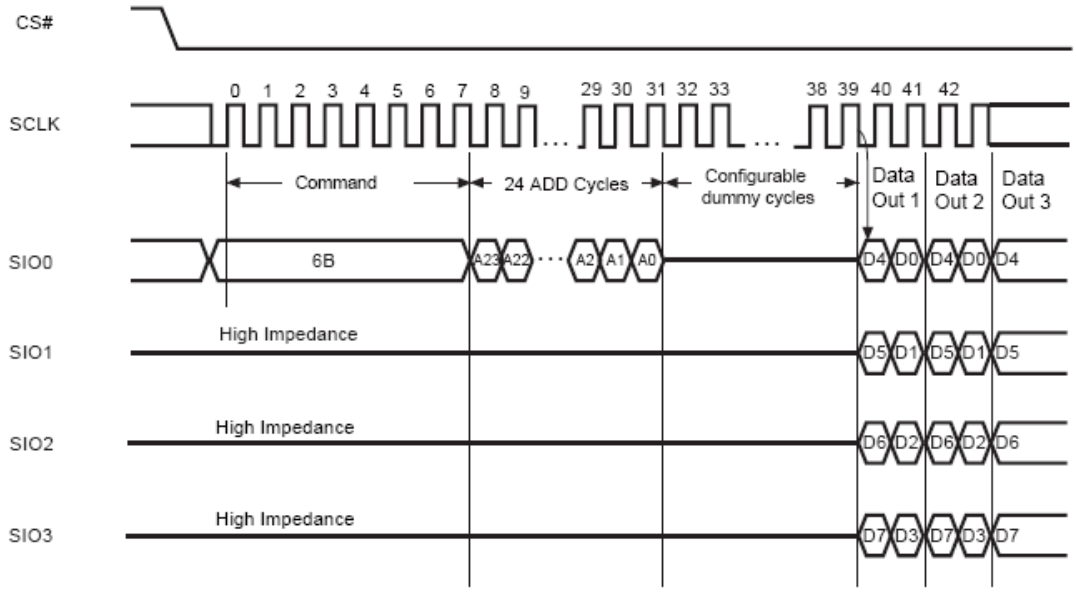


Figure 7-14 Quad Read Timing

7.2.2.5 4xIO Read Timing

When in 4x mode，spi_mosi is used as spi_io0，and spi_miso is used as spi_io1.

The 4x mode instruction is “EBh”, and there are six “dummy” clocks after the 24-bit address。

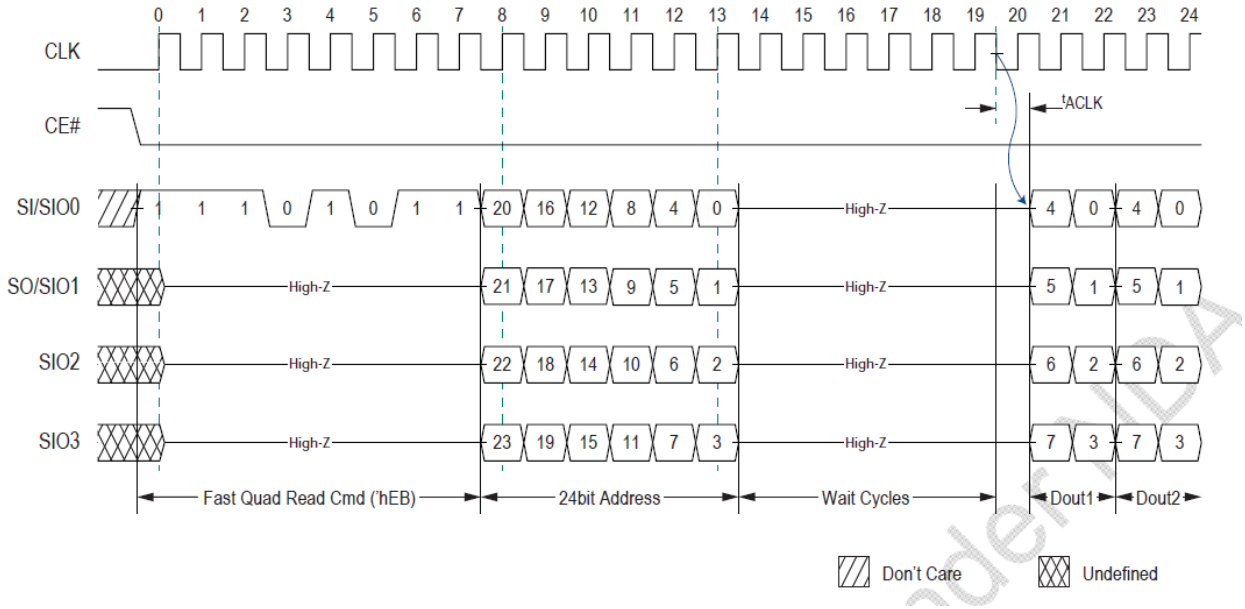


Figure 7-15 4x Read Timing

7.2.2.6 Full Quad SPI mode

QPI mode, full quad spi function, the command and the address and data, all use four IO.

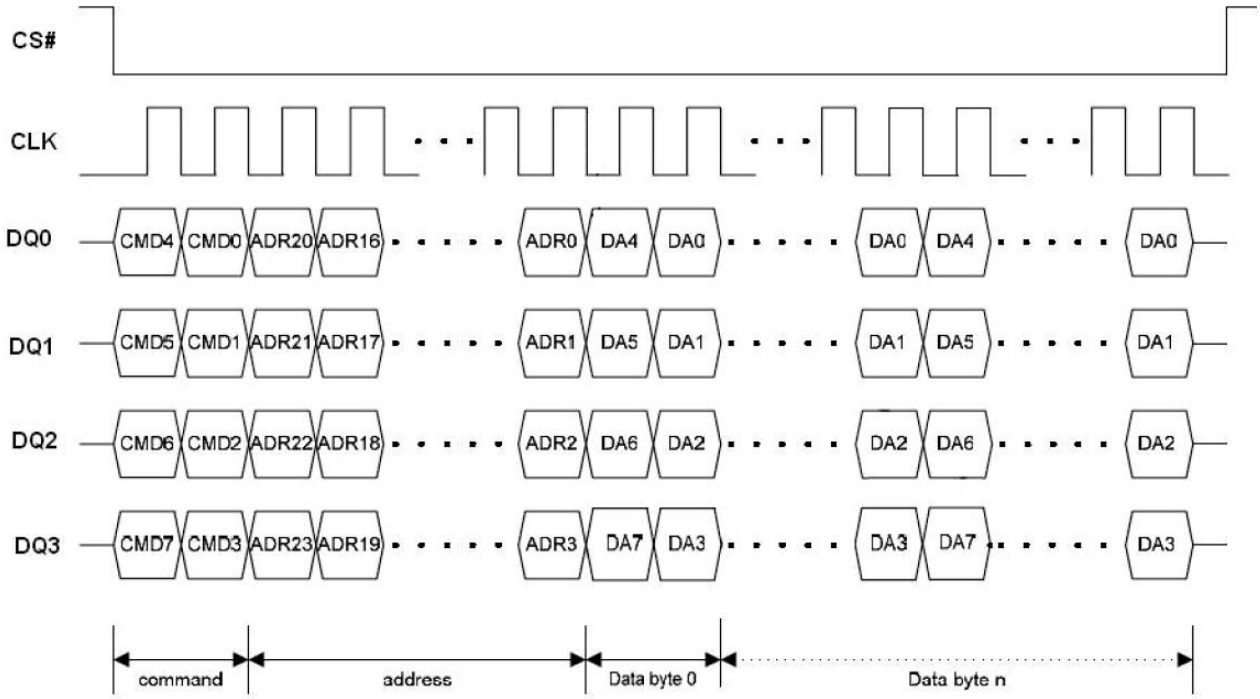


Figure 7-15 Quad SPI Timing

7.2.2.7 OPI PSRAM Interface

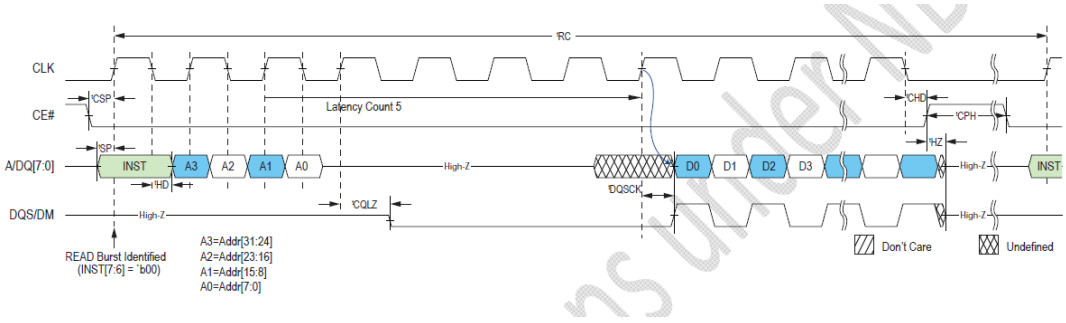


Figure 7-16 QSPI PSRAM read Timing

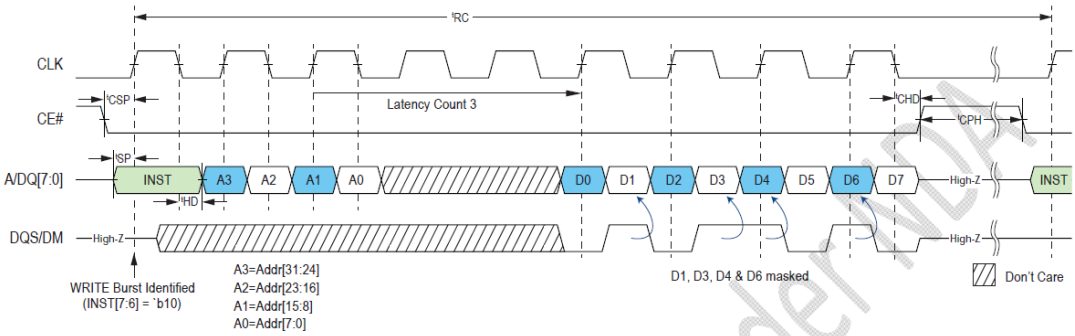


Figure 7-17 QSPI PSRAM synchronous write followed by any opreration

Register write:

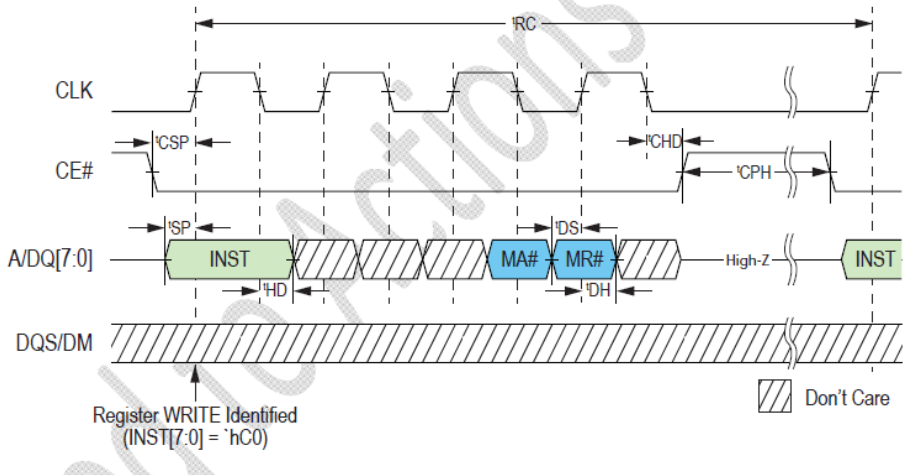
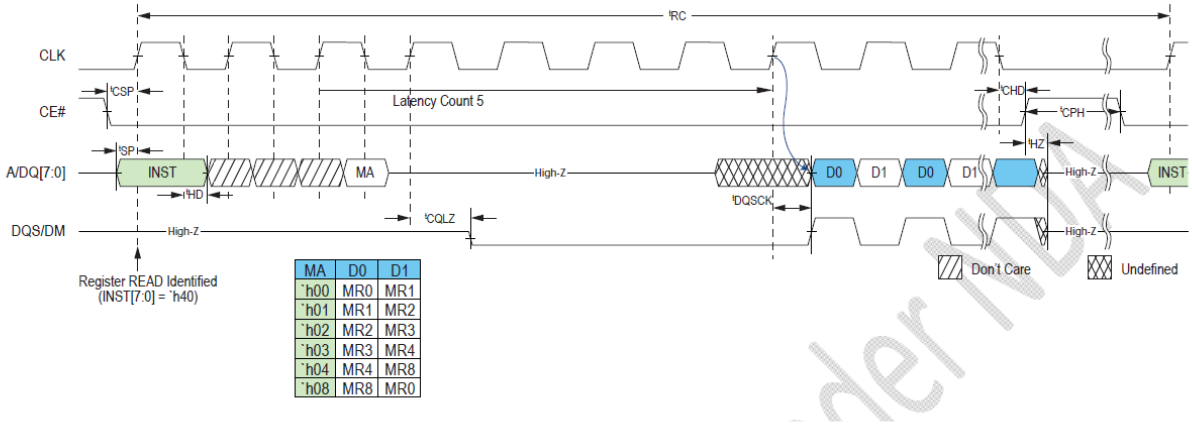


Figure 7-18 QSPI register write



MA	D0	D1
'h00	MR0	MR1
'h01	MR1	MR2
'h02	MR2	MR3
'h03	MR3	MR4
'h04	MR4	MR8
'h08	MR8	MR0

Figure 7-19 QSPI register read

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time (^{t}CHD +^{t}HZ> ^{t}DQSCK) for a sufficient data window.

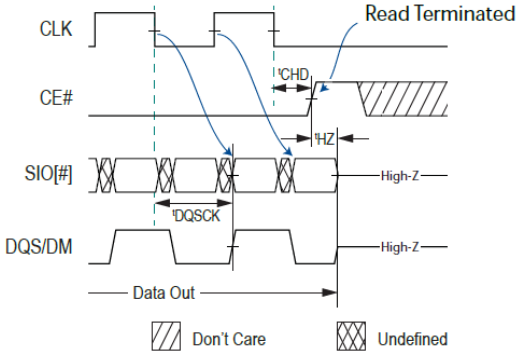


Figure 7-19 QSPI read command Termination

7.2.2.8 DDR QPI PSRAM Interface

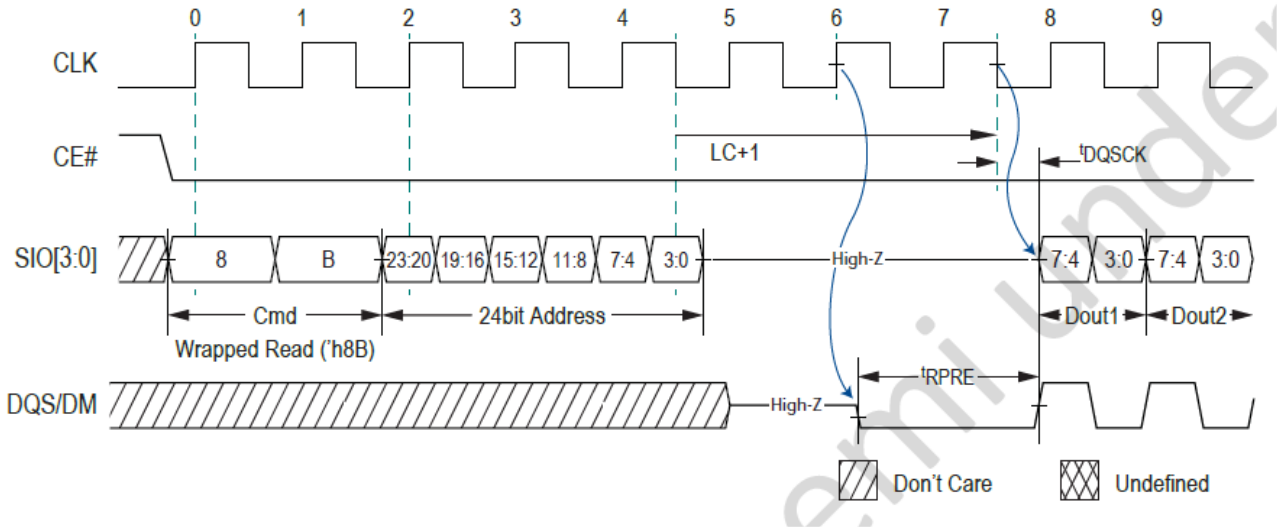


Figure 7-20 QSPI Fast Quad Read 'h88(Latency Code 2 Shown)

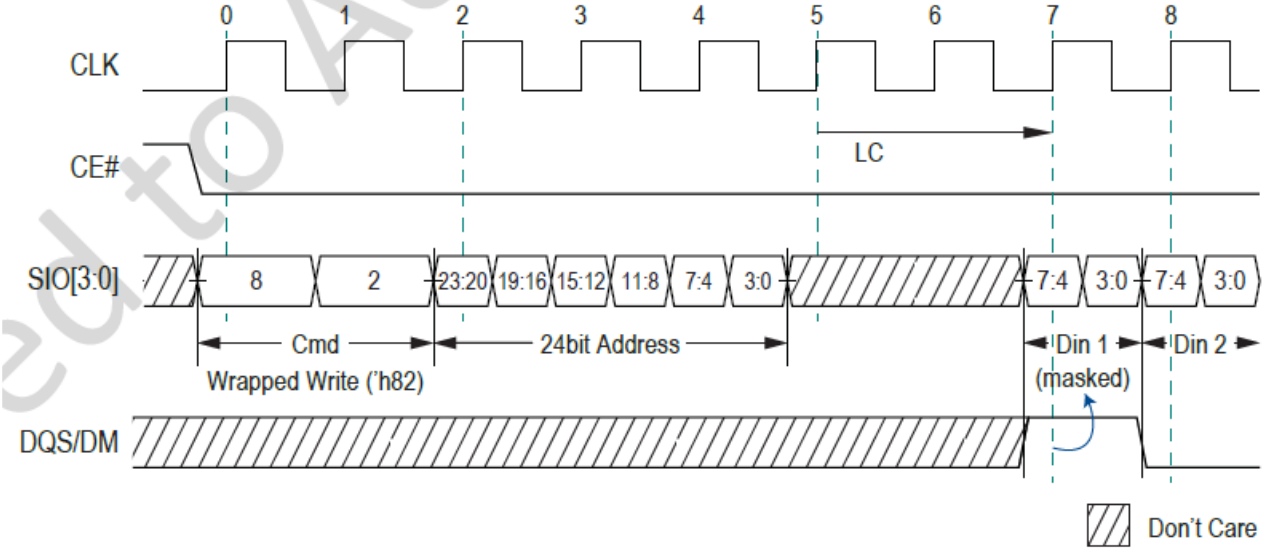


Figure 7-21 QSPI Write 'h82(Latency Code 2 shown)

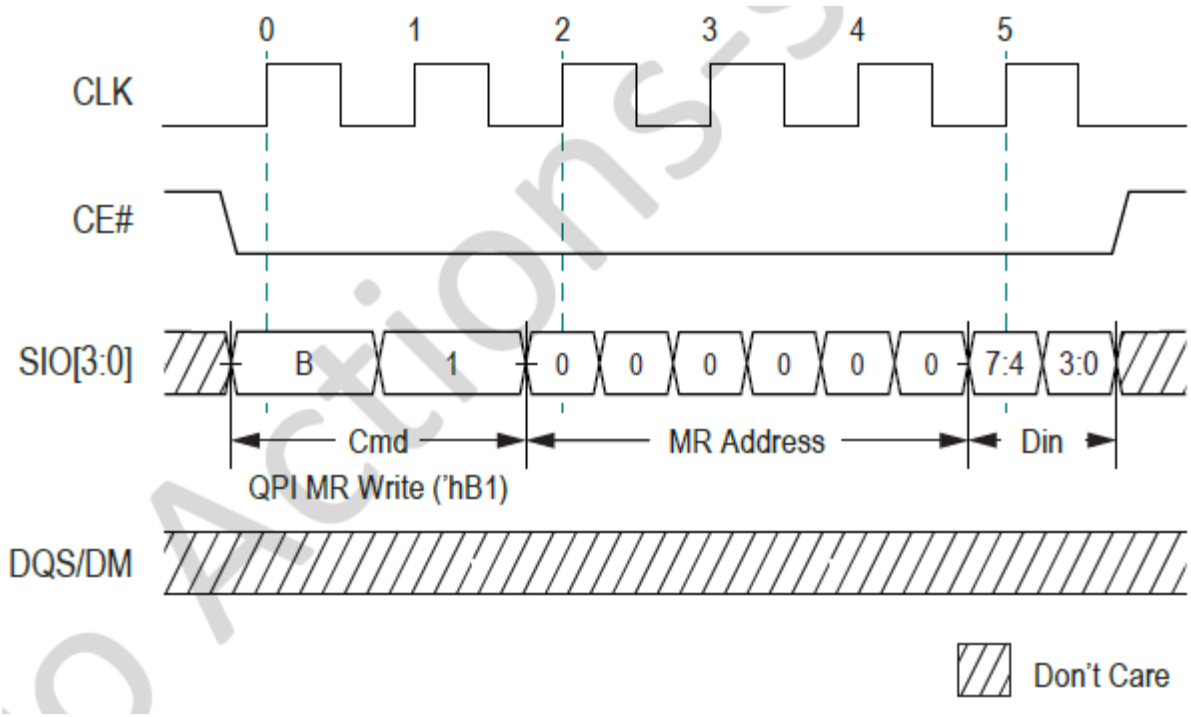


Figure 7-22 QSPI MR Write 'hB1

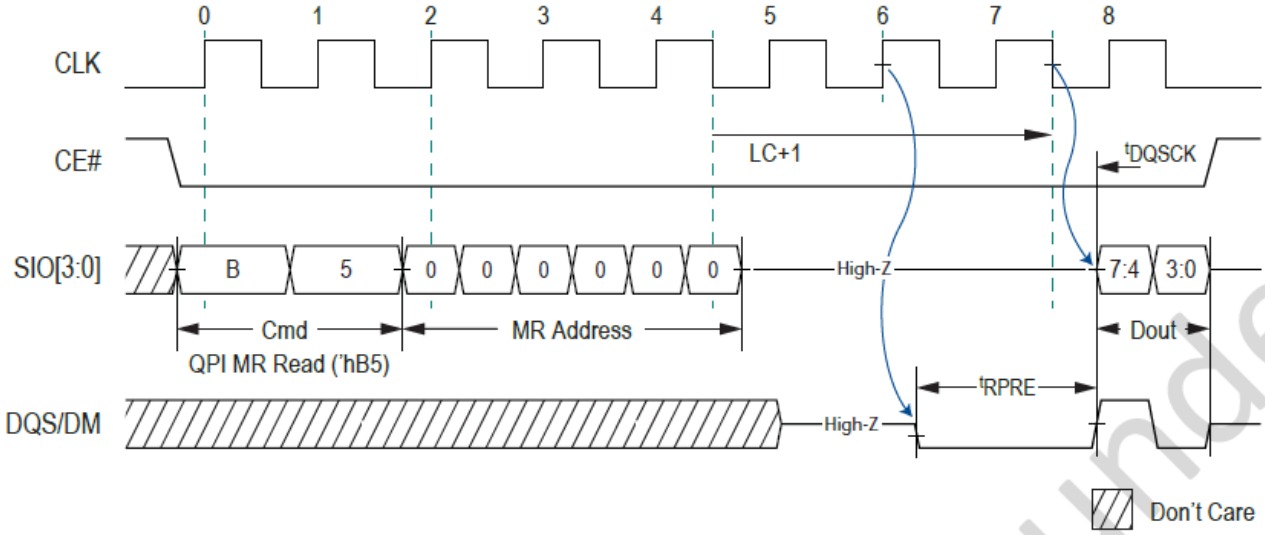


Figure 7-23 QSPI MR read 'hB5(latency Code 2 shown)

Table 5: Latency Configuration Codes MR0[4:2]

Latency Codes (LC)			*Max Input CLK Freq (MHz)*	
MR0[4:2]	*Write Latency (LC)*	*Read Latency (LC+1)*	*Standard*	*Extended*
010	2	3	84	84
011	3	4	104	104
100 (default)	4	5	133	133
101	5	6	166	166
others	reserved	-	-	-

7.2.3 Operation Manual

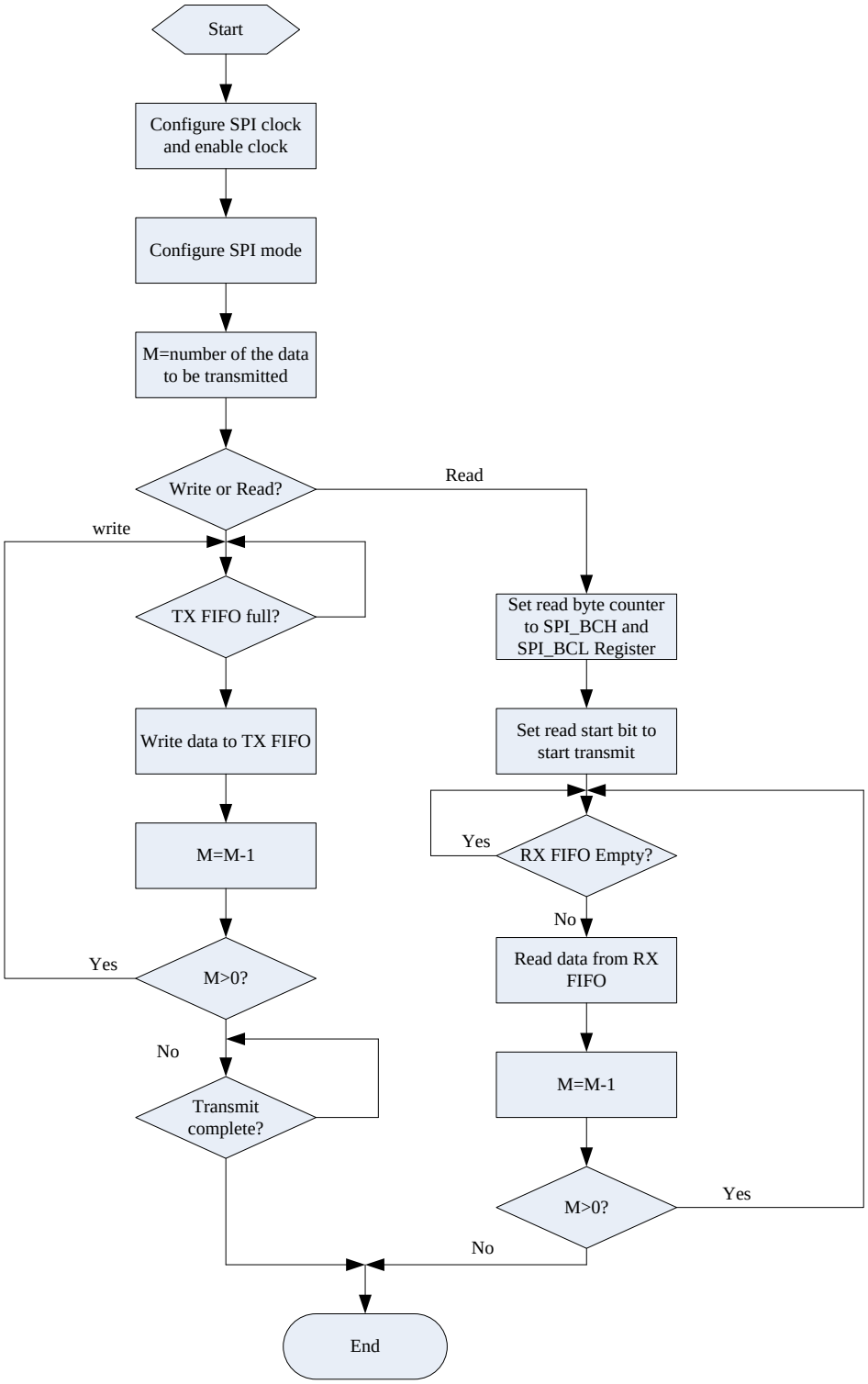


Figure 7-24 SPI1 Operation flow

7.2.4 Register List

SPI1 Controller Base Address

Name	Physical Base Address	KSEG1 Base Address
SPI1_REGISTER	0xC00B0000	0xC0110000

SPI1 Controller Registers List

Offset	Register Name	Description
0x0000	SPI1_CTL	SPI1 Control Register
0x0004	SPI1_STA	SPI1 Status Register
0x0008	SPI1_TXDAT	SPI1 Transmit FIFO Data Register
0x000C	SPI1_RXDAT	SPI1 Receive FIFO Data Register
0x0010	SPI1_BC	SPI1 Byte Counter Register
0x0018	SPI1_DDR_MODE_CTL	SPI1 DDR Mode select register

7.2.5 Register Description

7.2.5.1 SPI1_CTL

SPI1 Control Register
Offset=0x0000

Bit(s)	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0x0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27	DUAL_QUAD_SELECT	**SPI1 Dual/Quad Mode Select** It works only when SPI_IO_MODE select 2x IO mode or 4x IO mode 0: 2x/4x mode 1: dual/quad mode	R/W	0x0
26	RX_WRITE_SEL	**SPI1 Rx Write Select,** Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0

25	DMS	DMA transmit mode select 0: burst8 mode 1: single mode	R/W	0x0
24	TXCEB	TX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
23	RXCEB	RX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0x0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0x0
20	RILS	RX IRQ Level select 0: RX FIFO not empty, generate IRQ 1: RX FIFO at least 8 level data, generate IRQ Note: this bit have no effect when SPI_RIRQ_EN is disable, SPI1_CTL[8].	R/W	0x0
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: delay 1 ns 0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns 1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns	R/W	0x0

		1110: delay 14 ns 1111: delay 15 ns		
15	SPI_REQ	SPI Bus Request (AHB Interface Only) 0:disable 1:enable	R/W	0x1
14	QPIEN	Full Quad mode enable 0: full quad spi mode disable 1: full quad spi mode enable	R/W	0x0
13:12	TIME_OUT_CTRL	Time Out Control (Cache Interface Only) 00: no wait 01: wait 32 cycles 10: wait 64 cycles 11: wait 128 cycles	R/W	0x0
11:10	SPI_IO_MODE	SPI data I/O mode select 00: 1x I/O mode select 01: 1x I/O mode select 10: 2x I/O mode select 11: 4x I/O mode select	R/W	0x0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO at least 8 level empty 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, this trigger of SPI RX IRQ controlled by SPI1_CTL[20]. 0: disable 1: enable	R/W	0x0
7	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 8 level empty; When DMA remain counter < 8, trigger DRQ until all data transfer completely; 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 8 level full.; When DMA remain counter < 8, trigger DRQ until all data received completely; 0: disable 1: enable	R/W	0x0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI NSS pin control output	R/W	0x1

		0: output low 1: output high		
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

7.2.5.2 SPI1_STA

SPI1 Status Register

Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0x0
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	R/W	0x0
10	-	Reserved	R	0x0
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	R/W	0x0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	R/W	0x0
7	SPI_RXFU	SPI1 RX FIFO Full 0: not full 1: full	R	0x0
6	SPI_RXEM	SPI1 RX FIFO Empty 0: not empty 1: empty	R	0x1
5	SPI_TXFU	SPI1 TX FIFO Full 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI1 TX FIFO Empty 0: not empty	R	0x1

		1: empty		
3	SPI_TIRQ_PD	SPI1 TX IRQ Pending, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0x0
2	SPI_RIRQ_PD	SPI1 RX IRQ Pending, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0x0
1	SPI_READY	SPI1 Ready (AHB Interface Only, please reference operation manual) 0: not ready 1: ready	R	0x1
0	SPI_BUSY	SPI1 master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0

7.2.5.3 SPI1_TXDAT

SPI1 Transmit FIFO Data Register
Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:0	SPI1_TXDAT	SPI1 TX FIFO, 32bitx16 levels When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0x0

7.2.5.4 SPI1_RXDAT

SPI1 Receive FIFO Data Register
Offset=0x000C

Bit(s)	Name	Description	R/W	Reset
31:0	SPI1_RXDAT	SPI RX FIFO, When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx16 levels	R	0x0

7.2.5.5 SPI1_BC

SPI1 Bytes Count Register, this register is used for setting SPI1 bytes counter bits in the SPI read mode only.
Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be received, only use in master mode	R	0x0
15:0	SPI1_BC	Bytes Counter [15: 0]	R/W	0x0

7.2.5.6 SPI1_DDR_MODE_CTL

SPI1 OPI Control register
Offset=0x0018

Bit(s)	Name	Description	R/W	Reset
31:20	-	Reserved	R	0x0
19:16	WLC	Write Latency Count value	W/R	0x0
15:12	RLC	Read Latency Count value read Variable Latency should 3～7， Read Fixed Latency should 6～14.	W/R	0x0
11:8	CLKOUT_DELAY	Clock out delay: 0000: no delay 0001: delay 0.5 ns 0010: delay 1 ns 0011: delay 1.5 ns 0100: delay 2 ns 0101: delay 2.5 ns 0110: delay 3 ns 0111: delay 3.5 ns … 1111: delay 7.5ns	R/W	0x0
7:4	DQS_DELAY	DQS_ delay: 0000: no delay 0001: delay 0.5 ns 0010: delay 1 ns 0011: delay 1.5 ns 0100: delay 2 ns 0101: delay 2.5 ns 0110: delay 3 ns	R/W	0x0

		0111: delay 3.5 ns … 1111: delay 7.5ns		
3:2	-	Reserved	R/W	0x0
1:0	DMSLT	DDR MODE select 00: disable OPI mode 01: select OPI DDR mode 10: select QPI DDR mode 11: Reserved	R/W	0x0

7.3SPI2

7.3.1 Features

- Support SPI normal mode: mode 0\1\2\3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data
- Support 16 level delay chain, 1ns/step
- Support slave mode
- Support 100MHz spi_clk as highest speed

7.3.2 Operation Manual

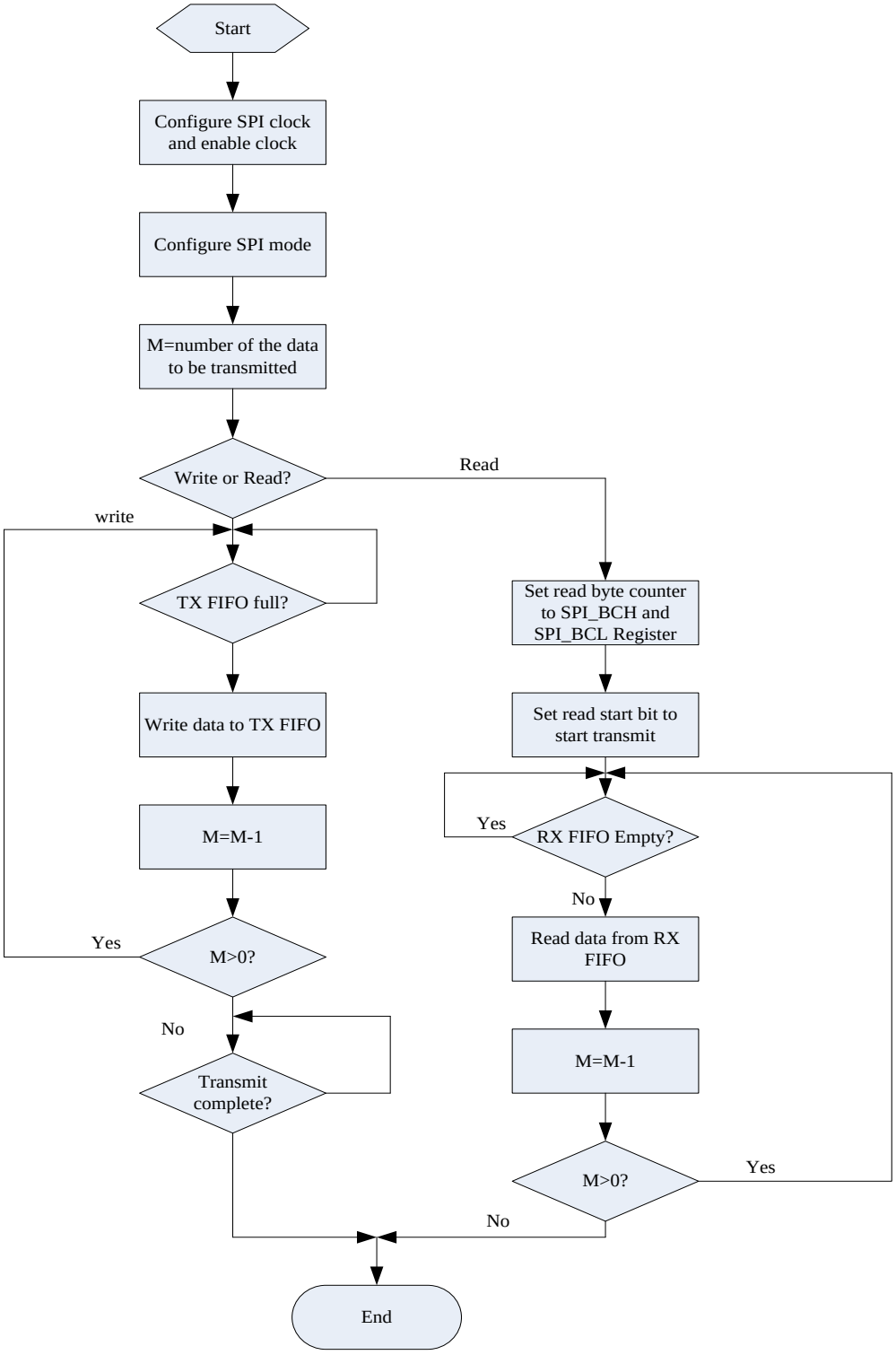


Figure 7-25 SPI2 Operation flow

7.3.3 Register List

SPI Registers Block Base Address

Name	Physical Base Address
SPI2	0xC00C0000

SPI Registers Offset Address

Offset	Register Name	Description
0x0000	SPI2_CTL	SPI Control Register
0x0004	SPI2_STA	SPI Status Register
0x0008	SPI2_TXDAT	SPI Transmit FIFO Data Register
0x000C	SPI2_RXDAT	SPI Receive FIFO Data Register
0x0010	SPI2_BC	SPI Byte Counter Low Register

7.3.4 Register Description

7.3.4.1 SPI2_CTL

SPI2 Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27	-	Reserved	R/W	0
26	RX_WRITE_SEL	SPI2 Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000)	R/W	0x0

		1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)		
25	DMS	DMA transmit mode select 0: burst8 mode 1: single mode	R/W	0x0
24	TXCEB	TX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
23	RXCEB	RX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0
20	RILS	RX IRQ Level select 0: RX FIFO not empty, generate IRQ 1: RX FIFO at least 8 level data, generate IRQ Note: this bit have no effect when SPI_RIRQ_EN is disable, SPI2_CTL[8].	R/W	0x0
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: delay 1 ns 0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns	R/W	0000

		1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns 1110: delay 14 ns 1111: delay 15 ns		
15:10	-	Reserved	R/W	0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO at least 8 level empty 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, this trigger of SPI RX IRQ controlled by SPI2_CTL[20]. 0: disable 1: enable	R/W	0x0
7	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 8 level empty; When DMA remain counter < 8, trigger DRQ until all data transfer completely; 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 8 level full.; When DMA remain counter < 8, trigger DRQ until all data received completely; 0: disable 1: enable	R/W	0x0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only	R/W	00

		11: Read and Write		

7.3.4.2 SPI2_STA

SPI2 Status Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:12	Reserved	Reserved	R	x
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0
10	Reserved	Reserved	R	x
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Write 1 to clear this bit	RW	0
7	SPI_RXFU	SPI RX FIFO Full 0: not full 1: full	R	0
6	SPI_RXEM	SPI RX FIFO Empty 0: not empty 1: empty	R	1
5	SPI_TXFU	SPI TX FIFO Full 0: not full 1: full	R	0
4	SPI_TXEM	SPI TX FIFO Empty 0: not empty 1: empty	R	1
3	SPI_TIRQ_PD	SPI TX IRQ Pending, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0
2	SPI_RIRQ_PD	SPI RX IRQ Pending, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0

1	Reserved	Reserved	R	x
0	SPI_BUSY	SPI master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0

7.3.4.3 SPI2_TXDAT

SPI2 Transmit FIFO Data Register

Offset=0x008

Bit(s)	Name	Description	R/W	Reset
31:0	SPI2_TXDAT	SPI2 TX FIFO, 32bitx16 levels When SPI2_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI2_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0x0

7.3.4.4 SPI2_RXDAT

SPI2 Receive FIFO Data Register

Offset=0x00c

Bit(s)	Name	Description	R/W	Reset
31:0	SPI2_RXDAT	SPI RX FIFO, When SPI2_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI2_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx16 levels	R	0x0

7.3.4.5 SPI2_BC

SPI Bytes Count Register, this register is used for setting SPI bytes counter bits in the SPI read mode only.

Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be received, only use in master mode	R	0x0
15:0	SPI_BC	Bytes Counter [15: 0]	R/W	0

7.4UART

7.4.1 Features

ATJ2157 Platform contains four UART interfaces: UART0/1/2/3. UART0/1/2/3 has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Capable of speeds up to 6Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX Support DMA single mode
- Add UART RX DMA counter for valid data in RAM。
- RX BaudRate tolerance≤±2%

7.4.2 Function Description

UART（Universal Asynchronous Receiver/Transmitter）is usually an individual (or part of an)integrated circuit used for serial communications over a computer or peripheral device serial port. UART are now commonly included in microcontrollers.

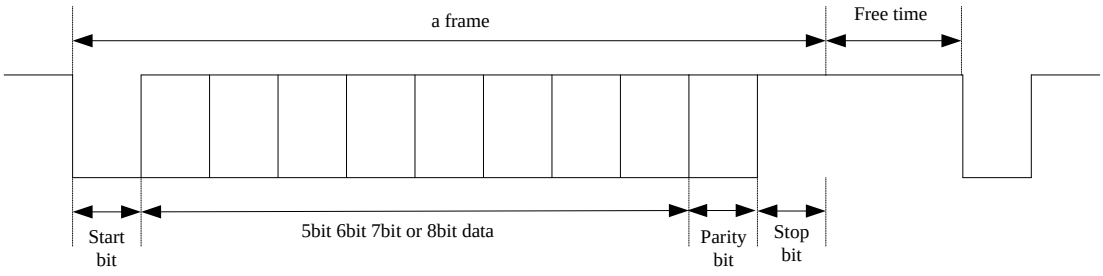


Figure 7-26 uart timing

RTS/CTS hardware Autoflow control flow description:
When the receiver FIFO level reaches the trigger level of 14 bytes, RTS- will be pulled up to invalid state. The sending UART may send an additional byte after the trigger level is reached (in case the sending UART has another byte to send) because it may not recognize the invalid state of RTS- until after it has begun sending the additional byte. RTS- is automatically reasserted once the receiver FIFO is less than 14 bytes by reading the receiver buffer register. The reassertion signals the sending UART to continue transmitting data.

The transmitter checks CTS- before sending the next data byte. When CTS- is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, CTS- must be released before the middle of the

last stop bit that is currently being sent.

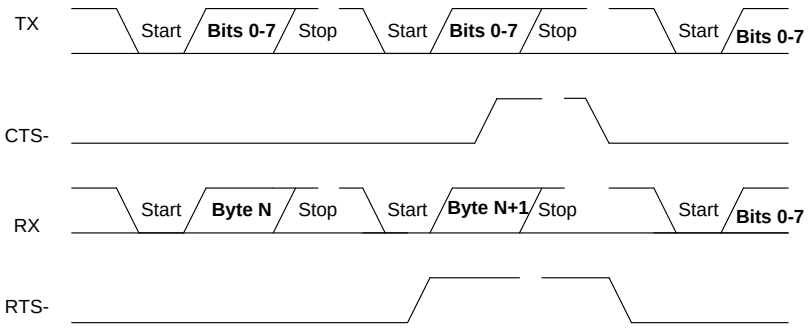


Figure 7-27 uart CTS/RTS autoflow control timing

The clock to drive UART controller is HOSC. The UART1 Baud Rate can be selected by UARTx_BR register.

Special Note:
When receive data by IRQ mode, if the FIFO number received not meet the trigger level, wait until the time is out of the trigger level data bytes.

7.4.3 Operation Manual

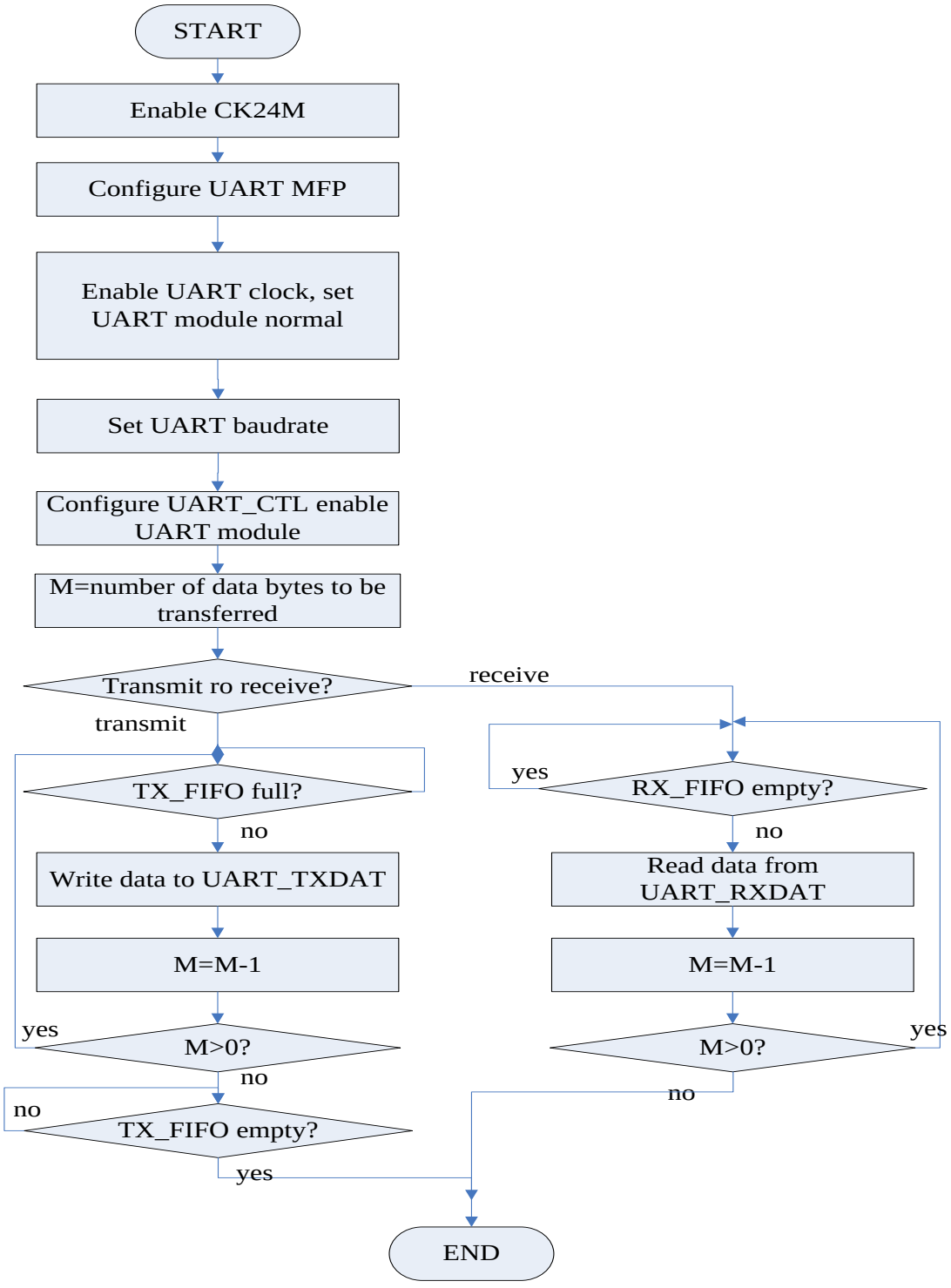


Figure 7-28 UART operation flow

7.4.4 Register List

UART Registers Block Base Address

Name	Physical Base Address
UART0	0xC00D0000
UART1	0xC00E0000
UART2	0xC00F0000
UART3	0xC0100000

UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UARTx Control Register
0x0004	UARTx_RXDAT	UARTx Receive FIFO Data Register
0x0008	UARTx_TXDAT	UARTx Transmit FIFO Data Register
0x000c	UARTx_STA	UARTx Status Register
0x0010	UARTx_BR	UARTx BAUDRATE divider Register

7.4.5 Register Description

7.4.5.1 UARTx_CTL

UART Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31	RXENABLE	UART RX disable 1：normal 0：disable	R/W	0x0
30	TXENABLE	UART TX disable 1：normal 0：disable	RW	0x0
29	TX_FIFO_EN	UART TX FIFO enable: 0: Disable 1: Enable	R/W	0x0
28	RX_FIFO_EN	UART RX FIFO enable: 0: Disable 1: Enable	R/W	0x0
27	-	Reserved	RW	0x0
26	TX_FIFO_SEL	UART TX FIFO Input Select. 0: From CPU 1: From DMA	RW	0x0
25	-	Reserved	RW	0x0
24	RX_FIFO_SEL	UART RX FIFO Output Select. 0: To CPU 1: To DMA	RW	0x0

23:22	AFL	Level for triggle RTS to high in autoflow when the flowauto bit is set 00:14byte 01:12byte 10:8byte 11:4byte	**RW**	**0x0**
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0x0
19	TXIE	UART TX IRQ Enable. 0: Disable 1: Enable	RW	0x0
18	RXIE	UART RX IRQ Enable. 0: Disable 1: Enable	RW	0x0
17	TXDE	UART TX DRQ Enable. 0: Disable 1: Enable	RW	0x0
16	RXDE	UART RX DRQ Enable. 0: Disable 1: Enable	RW	0x0
15	EN	UART Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable	RW	0x0
14	-	Reserved	RW	0x0
13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0:no request 1: request to send data	RW	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	RW	0x0

11:10	RDIC	UART RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00,01 because at least 8 bytes necessary. In DMA single mode (special DMA), DO set 00 for 1 Bytes transfer for each DRQ.	RW	0x0
9:8	TDIC	UART TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ/DRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA burst mode (normal DMA), DO not set 00,01 because at least 8 bytes necessary. In DMA single mode (special DMA), DO set 00 for 1 Bytes transfer for each DRQ.	RW	0x0
7	CTSE	CTS Enable. When this bit is set, request to receive data. 0:no request 1: request to receive data	RW	0x
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	0x0
3	WUEN	Wake up enable 0：disable 1：enable UART0 used only.	RW	0

2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0：1 stop bit 1：2 stop bit	RW	0x0
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	0x0

7.4.5.2 UARTx_RXDAT

UART Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:8	Reserved		R	0x0
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	x

7.4.5.3 UARTx_TXDAT

UART Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:8	Reserved		R	0
7:0	TXDAT	Transmite**d** Data. The depth of FIFO is 8bit×16 levels	W	0

7.4.5.4 UARTx_STA

UART Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:25	Reserved		R	0
24	WSTA	UART0 wake up status bit 0: sleep 1: wake up UART0 used only.	R	0

23	PAER	Parity Status. 0: Parity OK 1: Parity error. Writing 1 to the bit will clear the bit. When parity error.	R/W	0x0
22	STER	Stop Status. 0: Stop OK 1: Stop error. Writing 1 to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
20:16	TXFL	TX FIFO Level. The field indicates the current TX FIFO empty level.	R	10000
15:11	RXFL	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS-pin.	R	0
7	CTSS	CTS Status. The bit reflects the status of the external CTS-pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error.	RW	0

		0: No Error 1: Error Writing 1 to the bit will clear the bit.		
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	1
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

7.4.5.5 UARTx_BR

UART BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:16	TXBRDIV	UART TX BAUDRATE divider BaudRate= Colck_source/BaudRate divider Clock_source=HOSC	R/W	0x028
15:0	RXBRDIV	UART RX BAUDRATE divider BaudRate= Colck_source/BaudRate divider Clock_source=HOSC	R/W	0x028

7.5 TWI

7.5.1 Features

- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Both master and slave supports DMA mode
- Only 7-bit address mode support
- Two TWI modules with TWI0/1
- 8 Bit x8 TX FIFO and 8Bit x8 RX FIFO
- Supports general call

Pull-up resistors are required on both of the TWI signal lines as the TWI drivers are open drain typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal pull-Up resistor in standard and fast mode.

7.5.2 Register List

TWI Block Base Address

Name	Physical Base Address
TWI0	0xC0110000
TWI1	0xC0120000

TWI Block Configuration Registers List

Offset	Register Name	Description
0x00	TWIx_CTL	TWI Control Register
0x04	TWIx_CLKDIV	TWI Clock Divide Register
0x08	TWIx_STAT	TWI Status Register
0x0c	TWIx_ADDR	TWI Address Register
0x10	TWIx_TXDAT	TWI TX Data Register
0x14	TWIx_RXDAT	TWI RX Data Register
0x18	TWIx_CMD	TWI Command Register
0x1c	TWIx_FIFOCTL	TWI FIFO control Register
0x20	TWIx_FIFOSTAT	TWI FIFO status Register
0x24	TWIx_DATCNT	TWI Data transmit counter
0x28	TWIx_RCNT	TWI Data transmit remain counter

7.5.3 Register Description

7.5.3.1 TWIx_CTL

TWI Control Register
Offset=0x00

Bits	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	IRQC	TWI IRQ Control 0: set when RX FIFO received 1 bytes data in IRQ mode 1: set when RX FIFO received 4 bytes data in IRQ mode	RW	0x0
9	DRQTE	TX DRQ enable 0：disable 1：enable	RW	0x0
8	DRQRE	RX DRQ enable 0：disable 1：enable	RW	0x0
7	BUSSEL	TX/RX FIFO Bus select 0: AHB. 1: DMA	RW	0x0
6	IRQE	IRQ Enable. 0: Disable 1: Enable	RW	0x0
5	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	RW	0x0
4	-	Reserved	RW	0x0
3:2	GBCC	Generating Bus Control Condition (only for master mode).	RW	0x0
1	RB	Release Bus. Write 1 to this bit will release the bus.	RW	0x0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0x0

7.5.3.2 TWIx_CLKDIV

TWI Clock Divide Control Register
Offset=0x04

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	CLKDIV	Clock Divider Factor (only for master mode). TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=HOSC/(CLKDIV*16)	RW	0x0

7.5.3.3 TWIx_STAT

TWI Status Register

Offset=0x08

Bits	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	SRGC	Slave receive general call 0: not receive a general call 1: receive a general call	R	0x0
9	SAMB	Slave address match bit 0: slave address not match 1: slave address match	R	0x0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0x0
7	TCB	Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing 1 to this bit will clear it.	RW	0x0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0x0
5	STAD	Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0x0
4	STPD	Stop detect bit The bit is clear when the TWI module is disable or when	RW	0x0

		the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected		
3	-	Reserved	RW	0x0
2	IRQP	IRQ Pending Bit. 1: IRQ 0: No IRQ Clear condition: Writing 1 to this bit will clear it.	RW	0x0
1	BEB	Bus error bit 0: No error occur 1: Bus error occur Write “1” to clear this bit The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data.	RW	0x0
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived	R	0x0

7.5.3.4 TWIx_ADDR

TWI Address Register

Offset=0x0c

Bits	Name	Description	R/W	Reset
31：8	-	Reserved	R	0x0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. TWI_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master.	RW	0x0
0	-	Reserved.	R	0x0

7.5.3.5 TWIx_TXDAT

TWI Data Register

Offset=0x10

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	DA	The registers of Data or address to be transfer, or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave TWI device address while the LSB is the Read/Write bit.	W	0x0

7.5.3.6 TWIx_RXDAT

TWI receive Data Register

Offset=0x14

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	DA	The Receive data Register	R	0x0

7.5.3.7 TWIx_CMD

TWI Command Register

Offset=0x18

Bits	Name	Description	R/W	Reset
31：16	-	Reserved	R	0x0
15	SECL	Start to execute the command list 0: not execute 1: execute command	RW	0x0
14:13	-	Reserved	R	0x0
12	WRS	Write or Read select 0: write 1: read This bit only used in Slave mode.	RW	0x0
11	MSS	Master or slave mode select 0: slave mode 1: Master mode	RW	0x0
10	SE	Stop enable	RW	0x0

		0: disable 1: enable		
9	NS	NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data	RW	0x0
8	DE	Data enable 0: disable 1: enable The counts of data transmitted depend on the TWIx_CNT register.	RW	0x0
7:5	SAS	Second address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address	RW	0x0
4	RBE	Restart bit enable 0: not send restart bit 1: send restart bit	RW	0x0
3:1	AS	Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address include slave address and slave internal memory address.	RW	0x0
0	SBE	Start bit enable 0: not send start bit 1: send start bit	RW	0x0

7.5.3.8 TWIx_FIFOCTL

TWI FIFO control Register

Offset=0x1c

Bits	Name	Description	R/W	Reset
31:3	-	Reserved	R	0x0
2	TFR	TX FIFO reset bit Write 1 to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	RW	0x0
1	RFR	RX FIFO reset bit Write 1 to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	RW	0x0
0	NIB	NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute，generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	RW	0x0

7.5.3.9 TWIx_FIFOSTAT

TWI FIFO status Register

Offset=0x20

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:12	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0x0
11:8	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0x0
7	-	Reserved	R	0x0
6	WRS	Write or read status bit when acts as slave， used only in FIFO mode 0: master write to slave 1: master read from slave	R	0x0
5	TFF	TX FIFO full bit 0: not full 1: full	R	0x0
4	TFE	TX FIFO empty bit 1: empty 0: not empty	R	0x1
3	RFF	RX FIFO full bit 0: not full	R	0x0

		1: full		
2	RFE	RX FIFO empty bit 1: empty 0: not empty	R	0x1
1	RNB	Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data Write 1 to clear this bit	RW	0x0
0	CECB	Command Execute Complete bit 0: not complete 1: complete	R	0x1

7.5.3.10 TWIx_DATCNT

TWI data Counter Register

Offset=0x24

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Data Transmit counter	RW	0x0

7.5.3.11 TWIx_RCNT

TWI remain Counter Register

Offset=0x28

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Remain counter	R	0x0

7.6USB

7.6.1 Features

- Compliant with USB Specification, Revision 2.0;
- Compliant with ON-THE_GO supplement to USB 2.0 Specification, Revision 1.3;
- Supports UTMI+ Level3 compliant transceiver;
- Compatible with EHCI 1.0;
- Built-in PVCI-compatible system bus and optional AMBA AHB interface;
- Optional AMBA AXI 32-bit or 64-bit data bus width interface;
- Supports OTG SRP and HNP protocols
- Supports point-to-point communications with one HS, FS, or LS device
- Supports HS or FS Hub
- Hardware configurable endpoints(four data endpoint and one pair controller endpoint) as HS/FS device
- Supports ISO/INT/CTRL/BULK transfers for both host and device
- Compatible with EHCI data structures (FSTN and SITD back points are not supported)
- Supports embedded DMA access to FIFO
- Supports SRAM interface for FIFO
- Supports Suspend, Resume and Remote-wakeup Functions
- USB OTG software subsystem

8 Audio

8.1DAC

8.1.1 Features

- Stereo sigma-delta DAC, SNR>98dB, SNR (A-WEIGHTING)>100dB, THD<-85dB.
- 24bit*32Levels DAC FIFO0 and FIFO1, accessed by CPU, DMA, when 16 level filled, a IRQ is send. Data of FIFO0 and FIFO1 can be added with overflow process.
- Digital volumes of 256 steps with zero cross detection.
- Sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48kHz/88.2KHz/96kHz.
- ADC and DAC sound mixing.
- DACFIFO0/1 Output samples counter.
- Mult-Device linkage mode.
- Auto Mute function description.
- DAC VOLUME soft stepping controller.
- Stereo PDMTX.
- Build in stereo 20mW PA (Power Amplifier) for headphone. PA output supports traditional mode an

d direct drive mode（for earphone）.

- An anti-pop circuit for suppressing noise of PA when enable and disable.

8.1.2 DAC performance

fs=48k，single-end mode ，RL=16R，output mode=1.6vpp					
Parameter	Condition	min	typ	max	unit
Max Amplitude	Input = 0dBFS@1kHz		525		mVrms
Noise	Input PCM=0 A-weighted		5		uVrms
signal-to-noise ratio: SNR	A-weighted		100		db
Dynamic Range	Input= -48 dBFS @1khz		100		db
Total Harmonic distortion plus noise: THD+N	Input=0dBFS @1khz			-85	db

8.1.3 Register List

Table DAC Controller Registers Address

Name	Physical Base Address
DAC_Control_Register	0xC0180000

Table DAC Controller Registers

Offset	Register Name	Description
0x00	DAC_DIGCTL	DAC Digital Control Register
0x04	DAC_FIFOCTL	DAC FIFO Control Register
0x08	DAC_FIFOSTA	DAC FIFO State Register
0x0c	DAC_DAT_FIFO0	DAC FIFO0 Data Register
0x10	DAC_DAT_FIFO1	DAC FIFO1 Data Register
0x14	VOL_LCH	Left Channel Volume Control Register
0x18	VOL_RCH	Right Channel Volume Control Register
0x1c	PDMTX_CTL	PDMTX Control Register
0x20	DAC_FIFO0_CNT	DAC FIFO0 Out Counter Register
0x24	DAC_FIFO1_CNT	DAC FIFO1 Out Counter Register

8.1.4 Register Description

8.1.4.1 DAC_DIGCTL

DAC Digital Control Register

Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
31:28	-	Reserved	R	0x0
27	AMEN	Auto Mute Enable: 0：disable; 1：enable;	RW	0x0
26	AMDP	Auto-Mute Detect Pending bit 0：detect invalid or AMEN=0; 1：detect valid;	R	0x0
25:24	AMCNT	Auto Mute 00：512 (10ms at 48ksr)； 01：1024 (20ms at 48ksr)； 10：2048 (40ms at 48ksr)； 11：4096 (80ms at 48ksr)；	RW	0x0
23	-	Reserved	R	0x0
22:21	MULT_DEVICE	Mult-devices select: 00:disable 01:**DAC** with I2STX0； Others:reseverd Note: mult-device linkage mode	RW	0x0
20	SDMCNT	SDM Mute： 0x0:256 0x1:512	RW	0x0
19:18	SDMNDTH	SDM noise detection threshold 0x0：-84dbFS 0x1：-78dbFS 0x2：-72dbFS 0x3：-66dbFS	RW	0x2
17	SDMREEN	Reset SDM after has detect noise 0x0：disable 0x1：enable	RW	0x0
16	AUDIO_128FS_256FS	128fs and 256fs 0x0: 128fs device and 256fs device do not exist at the same time 0x1: 128fs device and 256fs device exist at the same time	RW	0x0

		Note： SPDIFTX（128fs）and I2STX（256fs） SPDIFTX（128fs）and DAC（256fs）		
15:13	-	Reserved for future use		
12	AD2DALPEN_L	ADC Digital CH0/CH2 and DAC Digital Left channel Mix Enable: 0x0: Disable 0x1: Enable	RW	0x0
11	AD2DALPEN_R	ADC Digital CH1/CH3 and DAC Digital Right channel Mix Enable: 0x0: Disable 0x1: Enable	RW	0x0
10	ADC_LRMIX	ADC CH0/CH2 channel mix CH1/CH3 channel enable 0x0: Disable 0x1: Enable	RW	0x0
9	AD2DA_CHSEL	ADC Channel mix to DAC Digital channel select: 0: CH0，CH1 mix DAC 1: CH2，CH3 mix DAC	RW	0x1
8	SDM_EN	DAC SDM Enable. 0x0: Disable 0x1: Enable	RW	0x0
7:6	-	Reserved for future use	R	0x0
5	DAF1M2DAEN	DAC FIFO1 Mix to DAC Enable: 0x0: Disable 0x1: Enable	RW	0x0
4	DAF0M2DAEN	DAC FIFO0 Mix to DAC Enable: 0x0: Disable 0x1: Enable	RW	0x0
3:2	OSRDA	DAC Over Sample Rate: 0x0: 16X 0x1: 32X 0x2: 64X 0x3: 128X Fix INTFRS as 8X.	RW	0x2
1	ENDITH	DAC Dither Enable: 0x0: disable 0x1: enable	RW	0x0
0	DDEN	DAC Digital Enable. 0x0: Disable 0x1: Enable	RW	0x0

8.1.4.2 DAC_FIFOCTL

DAC FIFO Control Register

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
31:14	-	Reserved	R	0x0
13:12	DAF1_IS	DAC FIFO1 Input Select: 0x00: CPU 0x01: DMA 0x02: reserved 0x03:reserved	RW	0x0
11	-	Reserved	RW	0x0
10	DAF1_IEN	DAC FIFO1 Half-Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
9	DAF1_DEN	DAC FIFO1 Half-Empty DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
8	DAF1_RST	DAC FIFO1 Reset. 0: Reset FIFO 1: Enable FIFO	RW	0x0
7	DACFIFO01_ DMAWIDTH	DACFIFO0/DACFIFO1 DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . DACFIFO0/DACFIFO1need not to support 8bit and 64bit DMA data width.	RW	0x0
6	-	Reserved	RW	0x0
5:4	DAF0_IS	DAC FIFO0 Input Select: 0x00: CPU 0x01: DMA 0x02:-reserved 0x03:reserved	RW	0x0
3	-	Reserved	RW	0x0
2	DAF0_IEN	DAC FIFO0 Half-Empty IRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
1	DAF0_DEN	DAC FIFO0 Half-Empty DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	DAF0_RST	DAC FIFO0 Reset. 0x0: Reset FIFO	RW	0x0

		0x1: Enable FIFO		

8.1.4.3 DAC_FIFOSTA

DAC FIFO State Register

Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	0x0
24	DAF1_ER	DAC FIFO1 error 0 : no error 1 : error If fifo was empty, system bus read DAC FIFO1 would cause fifo error. Writing 1 to the bit will clear it	RW	0x0
23	DAF1_IP	DAC FIFO1 half-Empty IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
22	DAF1_FULL	DAC FIFO1 Full Flag. 0x0: Not Full 0x1: Full	R	0x0
21	-	Reserved for DAF1_STATUS.	R	0x0
20:16	DAF1_STATUS	DAC FIFO1 Status. These 6 bits shows how many sample pairs fifo not filled. For example, when read as 6, means cpu can write 12 samples to fifo. If no DAC_CLK register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0
15:9	-	Reserved	R	0x0
8	DAF0_ER	DAC FIFO0 error 0 : no error 1 : error If fifo was empty, system bus read DAC FIFO0 would cause fifo error. Writing 1 to the bit will clear it	RW	0x0
7	DAF0_IP	DAC FIFO0 half-Empty IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it. When CMU_DEVCLKEN_DACCLKEN & (DAC_DIG_EN or I2STX0_EN or SPDIFTX_EN) =1, pending read as ok.	RW	0x0

6	DAF0_FULL	DAC FIFO0 Full Flag. 0x0: Not Full 0x1: Full	R	0x0
5	-	Reserved for DAF0_STATUS.	R	0x0
4:0	DAF0_STATUS	DAC FIFO0 Status These 6 bits shows how many sample pairs fifo not filled. For example, when read as 6, means CPU can write 12 samples to fifo. If no DAC_CLK register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0

8.1.4.4 DAC_DAT_FIFO0

DAC FIFO0 Data Register

Offset = 0x0c

Bit(s)	Name	Description	R/W	Reset
31:8	DAF0DAT	DAC FIFO0 Data FIFO is 24bit x 32 levels. FIFO read pairing. If wrote FIFO level was 2n+1, there was one FIFO data left in FIFO.	W	x
7:0	-	Reserved	R	0x0

8.1.4.5 DAC_DAT_FIFO1

DAC FIFO1 Data Register

Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
31:8	DAF1DAT	DAC FIFO1 Data FIFO is 24bit x 32 levels. If wrote FIFO level was 2n+1, there was one FIFO data left in FIFO.	W	x
7:0	-	Reserved	R	0x0

8.1.4.6 VOL_LCH

Volume Left Channel Control Register

Offset = 0x14

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20	TO_CNT	TO_CNT setting: 0 : 8*ADJ_CNT 1 : 128*ADJ_CNT	RW	0x0
19:12	ADJ_CNT	ADJ_CNT = reg_num It is recommended to set it to be consistent with the sampling rate, and the default value is 48 KFS.	RW	0x30
11	SOFT_STEP_DONE	Dac volume left channel soft stepping gain reach target set status： 0 : marching 1 : done	R	0x1
10	SOFT_STEP_EN	Dac volume left channel soft stepping gain control enable 0 : disable 1 : enable For more detail see chapter DAC VOLUME soft stepping controller Sugguest VOLLZCEN was enable if Dac volume Soft stepping was enable,	RW	0x0
9	VOLLZCTOEN	Volume Left Channel Zero Cross Detection Time Out Enable: 0x0: Disable 0x1: Enable Note: When VOLLZCEN ==1 & VOLLZCTOEN ==1, and zero cross is not detected. After 100ms@48ksr, Volume change will be set.	RW	0x0
8	VOLLZCEN	Volume Left Channel Zero Cross Detection Enable: 0x0: Disable 0x1: Enable Note: When the sign bit of the sample changed, zero cross is detected.	RW	0x0
7:0	VOLL	Volume Left Channel Control (step:0.375dB): 0xff: +24.0dB 0xfe: +23.625dB 0xfd: +23.25dB . . 0xbf: 0dB 0xbe: -0.375dB . . 0x00: mute	RW	0xbf

8.1.4.7 VOL_RCH

Volume Right Channel Control Register

Offset = 0x18

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20	TO_CNT	TO_CNT setting: 0 : 8*ADJ_CNT 1 : 128*ADJ_CNT	RW	0x0
19:12	ADJ_CNT	ADJ_CNT = reg_num It is recommended to set it to be consistent with the sampling rate, and the default value is 48 KFS.	RW	0x30
11	SOFT_STEP_DONE	Dac volume right channel soft stepping gain reach target set status： 0 : marching 1 : done	R	0x1
10	SOFT_STEP_EN	Dac volume right channel soft stepping gain control enable 0 : disable 1 : enable For more detail see chapter DAC VOLUME soft stepping controller Sugguest VOLRZCEN was enable if Dac volume Soft stepping was enable,	RW	0x0
9	VOLRZCTOEN	Volume Right Channel Zero Cross Detection Time Out Enable: 0x0: Disable 0x1: Enable Note: When VOLRZCEN ==1 & VOLRZCTOEN ==1, and zero cross is not detected. After 100ms@48ksr, Volume change will be set.	RW	0x0
8	VOLRZCEN	Volume Right Channel Zero Cross Detection Enable: 0x0: Disable 0x1: Enable Note: When the sign bit of the sample changed, zero cross is detected.	RW	0x0
7:0	VOLR	Volume Right Channel Control (step:0.375dB): 0xff: +24.0dB 0xfe: +23.625dB 0xfd: +23.25dB . . 0xbf: 0dB	RW	0xbf

		0xbe: -0.375dB . . 0x00: mute		

8.1.4.8 PDMTX_CTL

PDMTX Control Register

Offset = 0x1C

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	RW	0x0
14	DMIC_BYPASS	When PDMTX output source is DMIC01 or DMIC23，DMIC data Bypass mode select： 0: Correct the phase relation between data and CLK, delay sending out one DMIC cycle 1：Bypass	RW	0x0
13:12	PDMTX_CH_SET	PDMTX data output set: 00：disable (hi-z) 01：channel-0 enalbe (channel-1 hi-z) 10：channel-1 enalbe (channel-0 hi-z) 11：channel-0, channel-1 enalbe	RW	0x0
11:10	-	Reserved	R	0x0
9:8	PDMTX_SRC	PDMTX output source select: 0x0: DAC 0x1: LPADC analog 1bit data bypass 0x2: DMIC01 1bit data bypass 0x3: DMIC23 1bit data bypass	RW	0x0
7:4	-	Reserved	R	0x0
3	PDM1_ARST_EN	PDMTX1 Auto Reset: 0：normal mode； 1：Auto reset mode：When 64 zeros or ones are output continuously, reset pdmtx module to prevent deadlock		
2	PDM0_ARST_EN	PDMTX0 Auto Reset: 0：normal mode； 1：Auto reset mode：When 64 zeros or ones are output continuously, reset pdmtx module to prevent deadlock		
1	PDM1_EN	PDM1 (Right channel) enable: 0: disable. 1: enable.		

0	PDM0_EN	PDM0 (Left channel) enable: 0: disable. 1: enable.	RW	0x0

8.1.4.9 DAC_FIFO0_CNT

DAC FIFO0 Out Counter Register

Offset = 0x20

Bit(s)	Name	Description	R/W	Reset
31:19	-	Reserved		
18	IP	DAC sample counter overflow irq pending 0: no pending 1:pending Write '1' to clear this bit	RW	0x0
17	IE	DAC sample counter overflow irq enable: 0:disable 1:enable If CNT overflow, it would cause an interrupt.	RW	0x0
16	EN	DAC sample counter enable 0:disable 1:enable Disable this function could reset the whole counter.	RW	0x0
15:0	CNT	DAC FIFO0 sample counter FIFO read as pairing,	R	0x0

8.1.4.10 DAC_FIFO1_CNT

DAC FIFO1 Out Counter Register

Offset = 0x24

Bit(s)	Name	Description	R/W	Reset
31:19	-	Reserved		
18	IP	DAC sample counter overflow irq pending 0: no pending 1:pending Write '1' to clear this bit	RW	0x0
17	IE	DAC sample counter overflow irq enable: 0:disable 1:enable If CNT overflow, it would cause an interrupt.	RW	0x0

16	EN	DAC sample counter enable 0:disable 1:enable Disable this function could reset the whole counter.	RW	0x0
15:0	CNT	DAC FIFO1 sample counter FIFO read as pairing	R	0x0

8.2 ADC

8.2.1 Features

- Three channels ADC
- Two MIC/AUXIN/FMIN Analog ADC channels; SNR>98dB, THD<-86dB.
- One channel AEC Analog ADC channel; SNR>80dB.
- AMIC Support Single-Ended or full difference input.
- Support 4 DMIC input;
- Support 3 pairs AUXIN 0/1; each pair can be formed as mix or difference input.
- Programmable HPF.
- Programmable frequency response curve.
- Automatic Amplitude Limitation.
- ADC Gain Zero Crossing.
- Stereo 24bit *32Level ADC FIFO, accessed by CPU, DMA when 16 level filled a IRQ is send.
- Supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48kHz.

8.2.2 Programmable HPF

The high pass filter used to attenuate the frequency below the configured frequency, and allows the frequency above the configured frequency to pass through without phase shift. It is mainly used to remove low-frequency noise. The configured frequency known as cut-off frequency(fp)。

In order to cover different applications, ATJ2157 designed a configurable high pass filter。

HPF has two parts configurations：

Cut-off frequency (-3dB) band select for HPF, list in register CHx_DIGCTL[18]

Cut-off frequency (-3dB) points select for HPF, list in register CHx_DIGCTL[17:12]

Under different sampling rates and the same configuration, the -3dB frequency is inconsistent. The table below lists the configuration frequency relationships of different frequency segments of 16K / 48K / 96K：

Sampling rate	Low frequence section		high frequence section	
	section(Hz)	step(Hz)	section(Hz)	step(Hz)
16K	0.375~20	0.375	10~620	10
48K	1~60	1	30~1860	30

96K	1.875~120	1.875	60~3700	60

At the same sampling rate, the HPF will setting fast and stabilize at a lower the cutoff frequency.

. At the same cut-off frequency, the HPF will setting fast and stabilize at a higher sampling rate.

8.2.3 Programmable frequency response

ATJ2157 provides three optional frequency response curves. Their data are as follows:

Fir mode select	pass band ripple(db)	Stopband attenuation(db)	-1db cutoff frequency(Hz)
Fir mode A	**-0.04~0.06**	-71	-0.436
Fir mode B	**-0.09~0.00**	-82	-0.449
Fir mode C	**-0.04~0.08**	-71	-0.235

8.2.4 ADC performance

fs=48k，single-end input mode，1FFS=1Vrms，gain=0db					
Parameter	Condition	min	typ	max	unit
Full Scale Input Voltage	THD+N=1% input=1khz		1		FFS
Noise	Input = 0V A-weighted		12		uFFS
signal-to-noise ratio: SNR	THD+N=1% A-weighted		98		db
Dynamic Range	Input= -40dBFS @1khz A-weighted		98		db
Total Harmonic distortion plus noise: THD+N	Input=0dBFS @1khz			-86	db

8.2.5 Register List

Table ADC Controller Registers Address

Name	Physical Base Address
ADC_Control_Register	0xC0181000

Table ADC Controller Registers

Offset	Register Name	Description
0x00	ADC_DIGCTL	ADC Digital Control Register
0x04	ADC_GRPCTL	ADC Group Control Register
0x08	ADC01_FIFOCTL	ADC01 FIFO Control Register
0x0c	ADC23_FIFOCTL	ADC23 FIFO Control Register

0x10	ADC01_FIFOSTA	ADC01 FIFO State Register
0x14	ADC23_FIFOSTA	ADC23 FIFO State Register
0x18	ADC01_DAT_FIFO	DAC01 FIFO Data Register
0x1c	ADC23_DAT_FIFO	DAC23 FIFO Data Register
0x20	AAL_CTL	Auto Amplitude Limit Control Register
0x24	CH0_DIGCTL	CH0 Digital Control Register
0x28	CH1_DIGCTL	CH1 Digital Control Register
0x2c	CH2_DIGCTL	CH2 Digital Control Register
0x30	CH3_DIGCTL	CH3 Digital Control Register
0x34	ADC_MAPPING	ADC Digital Mapping Control Register
0x38	ADC_AUX_CTL	ADC AUX Control Register
0x3c	ADC_MIC_MIX_CTL	ADC MIC PAOUT MIX Control Register
0x40	ADC_AEC_CTL	AEC Channel ADC Control Register
0x44	ADC_CTL	ADC Control Register
0x48	ADC_BIAS0	ADC BIAS0 Control Register
0x4c	ADC_BIAS1	ADC BIAS1 Control Register
0x54	VMIC_CTL	VMIC Control Register

8.2.6 Register Description

8.2.6.1 ADC_DIGCTL

ADC Digital Control Register

Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
31:4	-	Reserved	R	0x0
3	CH3_DIG_EN	CH3 digital enable 0:disable 1:enable	RW	0x0
2	CH2_DIG_EN	CH2 digital enable 0:disable 1:enable	RW	0x0
1	CH1_DIG_EN	CH1 digital enable 0:disable 1:enable	RW	0x0
0	CH0_DIG_EN	CH0 digital enable 0:disable 1:enable	RW	0x0

8.2.6.2 ADC_GRPCTL

ADC Group Control Register
Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	R	0x0
14:12	DMIC_PRE_GAIN	Pre-Gain control for DMIC 000 : 1x 001 : 2x 010 : 4x 011 : 8x 100 : 16x 101 : 32x 110 : 63x 111 : 63x for all DMIC interface if CHx data select DMIC and CHx_DIG_EN was enable channel x DMIC interface was enable.	RW	0x0
11	-	Reserved	R	0x0
10:9	ADC23_OVFS_SEL	ADC23 oversampling rate control: 00 : 128fs 01 : 64fs 10 : 150fs 11 : 50fs for AMIC and DMIC interface	RW	0x0
8:7	ADC23_FIR_MD_SEL	FIR mode select 00 : FIR mode A 01 : FIR mode B 10 : FIR mode C 11 : Reserved This configuration reference to frequency response.	RW	0x0
6	-	Reserved	R	0x0
5:4	ADC01_OVFS_SEL	ADC01 oversampling rate control: 00 : 128fs 01 : 64fs 10 : 150fs 11 : 50fs for AMIC and DMIC interface	RW	0x0
3:2	ADC01_FIR_MD_SEL	FIR mode select 00 : FIR mode A 01 : FIR mode B 10 : FIR mode C	RW	0x0

		11 : Reserved This configuration reference to frequency response.		
1:0	-	Reserved	R	0x0

8.2.6.3 ADC01_FIFOCTL

ADC01 FIFO Control Register

Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	FIFO_DMAWIDTH	ADC FIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . ADCFIFO need not to support 8bit and 64bit DMA data width.	RW	0x0
6	-	Reserved	R	0x0
5:4	FIFO_OS	ADC FIFO Output Select: 0x00: CPU 0x01: DMA 0x02: reserved 0x03:reserved	RW	0x0
3	-	Reserved	RW	0x0
2	FIFO_IEN	ADC FIFO Half-Filled IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	FIFO_DEN	ADC FIFO Half-Filled DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	FIFO_RST	ADC FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

8.2.6.4 ADC23_FIFOCTL

ADC23 FIFO Control Register

Offset = 0x0c

Bit(s)	Name	Description	R/W	Reset

31:8	-	Reserved	R	0x0
7	FIFO_DMAWIDTH	ADC FIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . ADCFIFO need not to support 8bit and 64bit DMA data width.	RW	0x0
6	-	Reserved	R	0x0
5:4	FIFO_OS	ADC FIFO Output Select: 0x00: CPU 0x01: DMA 0x02: reserved 0x03:reserved	RW	0x0
3	-	Reserved	RW	0x0
2	FIFO_IEN	ADC FIFO Half-Filled IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	FIFO_DEN	ADC FIFO Half-Filled DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	FIFO_RST	ADC FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

8.2.6.5 ADC01_FIFOSTA

ADC01 FIFO State Register

Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FIFO_ER	FIFO error 0 : no error 1 : error When fifo was full, system bus wirte ADCFIFO would cause error Writing 1 to the bit will clear it	RW	0
7	FIFO_IP	ADC FIFO Half-Filled IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
6	FIFO_EMPTY	ADC FIFO Empty Flag. 0x0: Not Empty	R	0x1

		0x1: Empty		
5	-	Reserved for FIFO_STATUS.	R	0x0
4:0	FIFO_STATUS	ADC FIFO Status.	R	0x0

8.2.6.6 ADC23_FIFOSTA

ADC23 FIFO State Register

Offset = 0x14

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FIFO_ER	FIFO error 0 : no error 1 : error When fifo was full, system bus wirte ADCFIFO would cause error Writing 1 to the bit will clear it	RW	0
7	FIFO_IP	ADC FIFO Half-Filled IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
6	FIFO_EMPTY	ADC FIFO Empty Flag. 0x0: Not Empty 0x1: Empty	R	0x1
5	-	Reserved for FIFO_STATUS.	R	0x0
4:0	FIFO_STATUS	ADC FIFO Status.	R	0x0

8.2.6.7 ADC01_DAT_FIFO

DAC01 FIFO Data Register

Offset = 0x18

Bit(s)	Name	Description	R/W	Reset
31:8	ADDAT	ADC Data FIFO is 24bit x 32 levels.	R	x
7:0	-	Reserved	R	0x0

8.2.6.8 ADC23_DAT_FIFO

DAC23 FIFO Data Register
Offset = 0x1c

Bit(s)	Name	Description	R/W	Reset
31:8	ADDAT	ADC Data FIFO is 24bit x 32 levels.	R	x
7:0	-	Reserved	R	0x0

8.2.6.9 AAL_CTL

Auto Amplitude Limit Control Register
Offset = 0x20

Bit(s)	Name	Description	R/W	Reset
31:18	-	Reserved, read as zero	R	0x0
17	AAL_EN	Automatic amplitude limiter controller enable 0 : disable 1 : enable	RW	0x0
16	AAL_RECOVER_MODE	AAL recover mode 0: When the amplitude of a frame is less than vt0, the gain recovers to one level 1: When the amplitude of a frame is less than vt0, the original gain is restored immediately	RW	0x0
15:14	AAL_FL	AAL frame length select Length ratio 96ksr 48ksr 32ksr 16ksr 0: 1 5.46 10.92 16.38 32.77 1: 1/2 2.73 5.46 8.19 16.38 2: 1/3 1.82 3.64 5.46 10.92 3: 1/6 0.91 1.82 2.73 5.46	RW	0x3
13:12	AAL_VT1	AAL VT1 level select high level threshold: 00 : -0.4dbFS 01 : -1.8dbFS 10 : -5.3dbFS 11 : -11.3dbFS	RW	0x0
11	reserved		RW	0x0
10:8	AAL_VT0	AAL gain recovery level selection (low level threshold) 0x0 : off 0x1 : -49.3dbFS 0x2 : -39.3dbFS	RW	0x0

		0x3 : -29.3dbFS 0x4 : -19.3dbFS 0x5 : -9.3dbFS 0x6 : -5.3dbFS 0x7 : -2.3dbFS		
7:4	AAL_MAX	Maximum gain adjustment range	RW	0xf
3:0	AAL_CNT	Actual gain adjustment，<=AAL_MAX	R	0x0

8.2.6.10 CH0_DIGCTL

CH0 Digital Control Register

Offset = 0x24

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved, read as zero	R	0x0
21	AAL_CH_EN	Channel AAL enable 0 : disable 1 : enable	RW	0x0
20	DATA_OUT_EN	channel FIFO timing slot enable 0 : disable 1 : enable	RW	0x0
19	HPF_EN	High pass filter control 0:disable 1:enable	RW	0x0
18	HPF_S	HPF frequency fc0 & s0 select 0: low frequency range 1: high frequency range For more detail seeing chapter Programmable HFP	RW	0x0
17:12	HPF_N	HPF frequency fc select 0000-111111 For more detail seeing chapter Programmable HFP Fc = fc0+N*s0	RW	0x0
11	MIC_SEL	CH0 data source select 0:ADC Analog part 1:Digital MIC interface	RW	0x0
10	-	Reserved for future use	RW	0x0
9:8	SGAIN	SGAIN select 00: 0db 01: 6db 10: 12db 11: 18db	RW	0x0

7	ZERO_CROSS_EN	Wait zero cross before new FGAIN takes effect 0:disable 1:enable	RW	0x0
6:0	FGAIN	final gain， set bit[5:0]: 0x00: 0db ***** 0x01: 0.526db … (0.526db/step) 0x3b: 31.034db 0x3c ~ 0x7f Reserved, not to set.	RW	0x0

8.2.6.11 CH1_DIGCTL

CH1 Digital Control Register

Offset = 0x28

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved, read as zero	R	0x0
21	AAL_CH_EN	Channel AAL enable 0 : disable 1 : enable	RW	0x0
20	DATA_OUT_EN	channel FIFO timing slot enable 0 : disable 1 : enable	RW	0x0
19	HPF_EN	High pass filter control 0:disable 1:enable	RW	0x0
18	HPF_S	HPF frequency fc0 & s0 select 0: low frequency range 1: high frequency range For more detail seeing chapter Programmable HFP	RW	0x0
17:12	HPF_N	HPF frequency fc select 0000-111111 For more detail seeing chapter Programmable HFP Fc = fc0+N*s0	RW	0x0
11	MIC_SEL	CH0 data source select 0:ADC Analog part 1:Digital MIC interface	RW	0x0
10	-	Reserved for future use	RW	0x0
9:8	SGAIN	SGAIN select 00: 0db 01: 6db 10: 12db	RW	0x0

		11: 18db		
7	ZERO_CROSS_EN	Wait zero cross before new FGAIN takes effect 0:disable 1:enable	RW	0x0
6:0	FGAIN	final gain，set bit[5:0]: 0x00: 0db ***** 0x01: 0.526db … (0.526db/step) 0x3b: 31.034db 0x3c ~ 0x7f Reserved, not to set.	RW	0x0

8.2.6.12 CH2_DIGCTL

CH2 Digital Control Register

Offset = 0x2c

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved, read as zero	R	0x0
20	DATA_OUT_EN	channel FIFO timing slot enable 0 : disable 1 : enable	RW	0x0
19	HPF_EN	High pass filter control 0:disable 1:enable	RW	0x0
18	HPF_S	HPF frequency fc0 & s0 select 0: low frequency range 1: high frequency range For more detail seeing chapter Programmable HFP	RW	0x0
17:12	HPF_N	HPF frequency fc select 0000-111111 For more detail seeing chapter Programmable HFP Fc = fc0+N*s0	RW	0x0
11	MIC_SEL	CH0 data source select 0:ADC Analog part 1:Digital MIC interface	RW	0x0
10	-	Reserved for future use	RW	0x0
9:8	SGAIN	SGAIN select 00: 0db 01: 6db 10: 12db 11: 18db	RW	0x0
7	ZERO_CROSS_EN	Wait zero cross before new FGAIN takes effect	RW	0x0

		0:disable 1:enable		
6:0	FGAIN	final gain，set bit[5:0]: 0x00: 0db ***** 0x01: 0.526db … (0.526db/step) 0x3b: 31.034db 0x3c ~ 0x7f Reserved, not to set.	RW	0x0

8.2.6.13 CH3_DIGCTL

CH3 Digital Control Register

Offset = 0x30

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved, read as zero	R	0x0
20	DATA_OUT_EN	channel FIFO timing slot enable 0 : disable 1 : enable	RW	0x0
19	HPF_EN	High pass filter control 0:disable 1:enable	RW	0x0
18	HPF_S	HPF frequency fc0 & s0 select 0: low frequency range 1: high frequency range For more detail seeing chapter Programmable HFP	RW	0x0
17:12	HPF_N	HPF frequency fc select 0000-111111 For more detail seeing chapter Programmable HFP Fc = fc0+N*s0	RW	0x0
11	MIC_SEL	CH0 data source select 0:ADC Analog part 1:Digital MIC interface	RW	0x0
10	-	Reserved for future use	RW	0x0
9:8	SGAIN	SGAIN select 00: 0db 01: 6db 10: 12db 11: 18db	RW	0x0
7	ZERO_CROSS_EN	Wait zero cross before new FGAIN takes effect 0:disable 1:enable	RW	0x0

6:0	FGAIN	final gain，set bit[5:0]: 0x00: 0db ***** 0x01: 0.526db … (0.526db/step) 0x3b: 31.034db 0x3c ~ 0x7f Reserved, not to set.	RW	0x0

8.2.6.14 ADC_MAPPING

ADC Digital Mapping Control Register

Offset = 0x34

Bit(s)	Name	Description	R/W	Reset
31:15	-	Reserved	R	0x0
14:12	CH3_MAP	000: DMIC0 001: DMIC1 010: DMIC2 011: DMIC3 100: Analog L channel 101: Analog R channel * 110: Low power Analog channel 111: reserved	RW	0x5
11	-	Reserved	R	0x0
10:8	CH2_MAP	000: DMIC0 001: DMIC1 010: DMIC2 011: DMIC3 100: Analog L channel * 101: Analog R channel 110: Low power Analog channel 111: reserved	RW	0x4
7	-	Reserved	R	0x0
6:4	CH1_MAP	000: DMIC0 001: DMIC1 * 010: DMIC2 011: DMIC3 100: Analog L channel 101: Analog R channel 110: Low power Analog channel 111: reserved	RW	0x1
3	-	Reserved	R	0x0
2:0	CH0_MAP	000: DMIC0 *	RW	0x0

		001: DMIC1 010: DMIC2 011: DMIC3 100: Analog L channel 101: Analog R channel 110: Low power Analog channel 111: reserved		

8.2.6.15 ADC_AUX_CTL

ADC AUX Control Register

Offset = 0x38

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:16	Reserved	Reserved	RW	0x0
15:14	AUX1L_EN	AUX1L to ADC L channel input enable 00: disable 01: disable with input pd function(15kR pd res) 10: disable with input voltage set to VR 11: enable channel	RW	0x0
13:12	AUX1R_EN	AUX1R to ADC R channel input enable 00: disable 01: disable with input pd function(15kR pd res) 10: disable with input vol set to VR 11: enable channel	RW	0x0
11	AUX1_IN_MODE	AUX1 input mode select 1: single end input mode：AUX1L to ADC L channel，AUX1R to ADC R channel; 0: differential input mode：AUX1L and AUX1R form the differential input to ADC R channel;	RW	0x0
10	AUX1LRMIX	AUX1L and AUX1R mix to ADC R en 0:disable 1:enable Should set to se mode.	RW	0x0
9:8	AUX1_IRS	AUX1 input resistor select 00: 120k 01:60k 10:30k 11:6k	RW	0x0
7:6	AUX0L_EN	AUX0L to ADC L channel input enable 00: disable 01: disable with input pd function(15kR pd res)	RW	0x0

		10: disable with input voltage set to VR 11: enable channel		
5:4	AUX0R_EN	AUX0R to ADC R channel input enable 00: disable 01: disable with pd function(15kR pd res) 10: disable with input vol set to VR 11: enable channel	RW	0x0
3	AUX0_IN_MODE	AUX0 input mode select 1: single end input mode: AUX0L to ADC L channel，AUX0R to ADC R channel; 0: differential input mode: AUX0L and AUX0R form the differential input to ADC L channel	RW	0x0
2	AUX0LRMIX	AUX0L and AUX0R mix to ADCL en 0:disable 1:enable Should set to se mode.	RW	0x0
1:0	AUX0_IRS	AUX0 input resistor select 00: 120k 01:60k 10:30k 11:6k	RW	0x0

8.2.6.16 ADC_MIC_MIX_CTL

ADC MIC PAOUT MIX Control Register

Offset = 0x3c

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15	-	Reserved	RW	0x0
14	PAR2ADL_EN	PA OUTR mix to ADC L channel 0:disable 1:enable	RW	0x0
13	PAL2ADL_EN	PA OUTL mix to ADC L channel 0:disable 1:enable	RW	0x0
12	PAR2ADR_EN	PA OUTR mix to ADC R channel 0:disable 1:enable	RW	0x0
11	PAL2ADR_EN	PA OUTL mix to ADC R channel 0:disable 1:enable	RW	0x0

10	PAR_PD_EN	PA OUTR mix to ADC channel pull down 0:disable 1:enable	RW	0x0
9	PAL_PD_EN	PA OUTL mix to ADC channel pull down 0:disable 1:enable	RW	0x0
8	MICGRSEL	MIC input gain res select: If [5]MIC_IRMS=0 0:60k 1:6k else if [5]MIC_IRMS=1 0:5k 1:2k Gain calculated a preamp_pg	RW	0x0
7:6	GMIRSEL	Gm input mode filter res select : (also as gm mode input res) 00: 10k 01:50k 10:250k 11:500k	RW	0x0
5	MIC_IRMS	MIC input res mode select: 0: res mode: input res select by[8], gain as preamp_pg; 1: GM input mode: res select by [7:6]GMIRSEL.this bit also enable/disable the GM OP. for gm input mode , FDBUF OP should be enable . FDBUF_IRS should set to 0.	RW	0x0
4	MIC_IN_MODE	MIC input mode select 1: single end input mode: MICINL to ADC L channel， MICINR to ADC R channel; 0: differential input mode: MICINL and MICINR form the differential input to ADC L/R channel; *For L channel, MICINL is positive end, MICINR is negative end; FOR R channel ,invert.*	RW	0x0
3:2	MICL_EN	MIC L channel enable 00: disable 01: disable with input pd function(5kohm pd res) 10: disable with input voltage set to VR 11: enable channel	RW	0x0
1:0	MICR_EN	MIC R channel enable 00: disable 01: disable with input pd function(5kohm pd res) 10: disable with input voltage set to VR	RW	0x0

		11: enable channel		

8.2.6.17 ADC_AEC_CTL

AEC Channel ADC Control Register

Offset = 0x40

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:13	-	Reserved	RW	0x0
12	AECCLK_DIV	AEC ADC clock divide select: 0:/2; 1: /1; /2 means input clock of aec adc is 256fs; /1 means 128fs;	RW	0x0
11	AECADC_BINV	AEC ADC channel output bits invert,to make the phase right: 0:disable 1:enable	RW	0x0
10	AECVRDA_EN	AEC channel VRDA OP enable 0:disable 1:enable	RW	0x0
9	ADC_VAD_EN	ADC VAD channel enable 0:disable 1:enable	RW	0x0
8	AEC_DSS	AEC channel data source select 0:from AEC channel preamp 1:from ADC L channel preamp	RW	0x0
7	AECICCEN	AEC channel input cap charge enable 0:disable 1:enable	RW	0x0
6:4	AEC_GAIN	AEC channel GAIN RES control 000: 120kR, -6db 001: 170kR, -3db 010: 240kR, 0db 011: 338kR, 3db 100-111:480kR, 6db	RW	0x0
3	AECL_PDEN	AUX0L to AEC channel pull down enable 0:disable 1:enable If AUX0L channel is used in ADC L/R channel, this should not pd.	RW	0x0
2	AECR_PDEN	AUX0R to AEC channel Pull down enable 0:disable	RW	0x0

		1:enable If AUX0R channel is used in ADC L/R channel, this should not pd.		
1	AECL_EN	AUX0L to AEC channel enable 0: disable 1: enable, input res 120kR	RW	0x0
0	AECR_EN	AUX0R to AEC channel enable 0:disable 1:enable, input res 120kR	RW	0x0

8.2.6.18 ADC_CTL

ADC Control Register

Offset = 0x44

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28	ADCCLK_DIV	main ADC clock divide select: 0: /2; 1: /1; /2 means input clock of aec adc is 256fs; /1 means 128fs;	RW	0x0
27	-	Reserved	RW	0x0
26	BIASEN	BIAS enable 0:disable 1:enable	RW	0x0
25	ADR_CAPFC_EN	input cap to ADC R channel fast charge enable 0:disable 1:enable	RW	0x0
24	ADL_CAPFC_EN	input cap to ADC L channel fast charge enable 0:disable 1:enable	RW	0x0
23	-	Reserved	RW	0x0
22	-	Reserved	RW	0x0
21	ADCL_BINV	ADC L channel output bits invert, to make the phase right; 0:disable 1:enable	RW	0x0
20	ADCR_BINV	ADC R channel output bits invert, to make the phase right; 0:disable 1:enable For R channel diff input, invert the output bits, to make the phase the same as L channel	RW	0x0
19	-	Reserved	RW	0x0
18:16	FDBUFL_IRS	FDBUFL input resistor select	RW	0x0

<table>
<tr><td></td><td></td><td>0xx: not connect,disable
100:120k
101:60k
110:30k
111:6k</td><td></td><td></td></tr>
<tr><td>15</td><td>-</td><td>Reserved</td><td>RW</td><td>0x0</td></tr>
<tr><td>14:12</td><td>FDBUFR_IRS</td><td>FDBUFR input resistor select
0xx: not connect,disable
100:120k
101:60k
110:30k
111:6k</td><td>RW</td><td>0x0</td></tr>
<tr><td>11:8</td><td>PREAM_PG</td><td>PREAMP OP feedback res select to form different gain with different input res:
0000:30K
0001:42.4K
0010:60K
0011:67.3K
0100:75.5K
0101:84.8K
0110:95.1K
0111:106.7K
1000:120K
1001:134.3K
1010:150.7k
1011:169K
1100:189.7K
1101:212.8K
1110:238.8K
1111:267.9K
For use, first select inputmode and input res, then select preamp feedback res ,then gain is fixed.
For diff mode (se mode -6db)
<table>
<tr><td></td><td>120k</td><td>60k</td><td>30k</td><td>6k</td></tr>
<tr><td>0000</td><td>-12db</td><td>-6db</td><td>0db</td><td>14db</td></tr>
<tr><td>0001</td><td>-9db</td><td>-3db</td><td>3db</td><td>17db</td></tr>
<tr><td>0010</td><td>-6db</td><td>0db</td><td>6db</td><td>20db</td></tr>
<tr><td>0011</td><td>-5db</td><td>1db</td><td>7db</td><td>21db</td></tr>
<tr><td>0100</td><td>-4db</td><td>2db</td><td>8db</td><td>22db</td></tr>
<tr><td>0101</td><td>-3db</td><td>3db</td><td>9db</td><td>23db</td></tr>
<tr><td>0110</td><td>-2db</td><td>4db</td><td>10db</td><td>24db</td></tr>
<tr><td>0111</td><td>-1db</td><td>5db</td><td>11db</td><td>25db</td></tr>
<tr><td>1000</td><td>0db</td><td>6db</td><td>12db</td><td>26db</td></tr>
<tr><td>1001</td><td>1db</td><td>7db</td><td>13db</td><td>27db</td></tr>
</table></td><td>RW</td><td>0x0</td></tr>
</table>

		1010	2db	8db	14db	28db		
		1011	3db	9db	15db	29db		
		1100	4db	10db	16db	30db		
		1101	5db	11db	17db	31db		
		1110	6db	12db	18db	32db		
		1111	7db	13db	19db	33db		
7	FDBUFL_EN	FD BUF OP L enable for SE mode 0:disable 1:enable					RW	0x0
6	FDBUFR_EN	FD BUF OP R enable for SE mode 0:disable 1:enable					RW	0x0
5	PREOPL_EN	PREOP L enable 0:disable 1:enable					RW	0x0
4	PREOPR_EN	PREOP R enable 0:disable 1:enable					RW	0x0
3	VRDAL_EN	VRDAL OP enable 0:disable 1:enable					RW	0x0
2	VRDAR_EN	VRDAR OP enable 0:disable 1:enable					RW	0x0
1	ADCL_EN	ADC L channel enable 0:disable 1:enable					RW	0x0
0	ADCR_EN	ADC R channel enable 0:disable 1:enable					RW	0x0

8.2.6.19 VMIC_CTL

VMIC Control Register

Offset = 0x54

Bit(s)	Name	Description	R/W	Reset
31:2	-	Reserved	R	0x0
1	VMIC1_EN	VMIC1 enable 0:disable 1:enable	RW	0x0
0	VMIC0_EN	VMIC0 enable	RW	0x0

		0:disable 1:enable		

8.3I2S

8.3.1 Features

- 2OUT+2IN I2S (I2STX0 / I2STX1 / I2SRX0 / I2SRX1).
- Support with master mode and slave mode.
- Support sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/96k/192k.
- 24 bit *32 level*5 fifos for I2Sx，accessed by CPU, DMA, when 16 level empty/full, a irq is sent.
- Support I2S/ left-justified/ right-justified/ TDM format, with 16/20/24 bit datawidth.
- Support TDM 4/8 channel, with A/B mode.
- Support sample rate auto detect in slave mode. (TMD Mode：Bclk up to12.288MHz).
- Support I2Sx share clocks mode.

8.3.2 I2STXx Register List

Table I2STX Controller Registers Address

Name	Physical Base Address
I2STX	0xC0182000

Table I2STX Controller Registers

Offset	Register Name	Description
0x0000	I2STX0_CTL	I2STX0 Control Register
0x0004	I2STX0_FIFOCTL	I2STX0 FIFO control register
0x0008	I2STX0_FIFOSTA	I2STX0 FIFO state register
0x000c	I2STX0_DAT_FIFO	I2STX0 FIFO data register
0x0010	I2STX0_SRDCTL	I2STX0 sample rate detect control register
0x0014	I2STX0_SRDSTA	I2STX0 sample rate detect status register
0x0018	I2STX0_FIFO_CNT	I2STX0 FIFO Out Counter Register
0x0100	I2STX1_CTL	I2STX1 Control Register
0x0104	I2STX1_FIFOCTL	I2STX1 FIFO control register
0x0108	I2STX1_FIFOSTA	I2STX1 FIFO state register
0x010c	I2STX1_DAT_FIFO	I2STX1 FIFO data register
0x0110	I2STX1_SRDCTL	I2STX1 sample rate detect control register
0x0114	I2STX1_SRDSTA	I2STX1 sample rate detect status register
0x0118	I2STX1_FIFO_CNT	I2STX1 FIFO Out Counter Register
0x0200	I2STX_MODE	I2S TX mode Register

8.3.3 I2STXx Register Description

8.3.3.1 I2STX0_CTL

I2S TX0 Control Registe
Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20	TDMTX_CHAN	0:4 channel 1:8 channel	RW	0x0
19	TDMTX_MODE	0:TDM-A (I2S data format) 1:TDM-B (left-justified data format)	RW	0x0
18:17	TDMTX_SYNC	at the beginning of the data frame, the type of LRCLK set: 00: at the rising edge of LRCLK with a pulse(duration of one BCLK) 01: at the rising edge of LRCLK with a 50% duty cycle; 10: at the falling edge of LRCLK with a 50% duty cycle; 11: Reserved	RW	0x0
16:8	-	Reserved	RW	0x0
7	TXMODE	I2S mode select: 0:I2S Master mode; 1:I2S Slave mode	RW	0x0
6	TX_SMCLK	MCLK(256FS) source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only.	RW	0x1
5:4	TXWIDTH	Effective width 00: data are 16 bit effective 01: data are 20 bit effective 10: data are 24 bit effective 11: reserved	RW	0x2
3	TXBCLKSET	Set the bit width of each channel: 0:32bit 1:16bit	RW	0x0
2:1	TXMODELSEL	I2S transfer format select: 00 : I2S format	RW	0x0

		01 : left-justified format 10 : right-justified format (when TXBCLKSET=1, this mode is invalid) 11 : TDM		
0	TXEN	I2S TX Enable. 0: Disable 1: Enable	RW	0x0

8.3.3.2 I2STX0_FIFOCTL

I2STX0 FIFO control register

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	FIFO_ DMAWIDTH	I2STX FIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . I2STXFIFO need not to support 8bit and 64bit DMA data width.	RW	0x0
6	-	Reserved	RW	0x0
5:4	**FIFO_IS**	I2STX_FIFO Input Select: 0x00: CPU 0x01: DMA 0x02:-reserved 0x03:reserved	RW	0x0
3	FIFO_SEL	I2STX0 module FIFO select: 0 : I2STX0_FIFO 1 : DAC FIFO0/1	RW	0x0
2	FIFO_IEN	I2STX_FIFO Half-Empty IRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
1	FIFO_DEN	I2STX_FIFO Half-Empty DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	FIFO_RST	I2STX_FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

8.3.3.3 I2STX0_FIFOSTA

I2STX0 FIFO state register

Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FIFO_ER	I2STX_FIFO error 0 : no error 1 : error If fifo was empty, system bus read TX FIFO would cause fifo error. Writing 1 to the bit will clear it	RW	0x0
7	FIFO_IP	I2STX_FIFO Half-Empty IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
6	FIFO_FULL	I2STX_FIFO Full Flag. 0x0: Not Full 0x1: Full	R	0x0
5	-	Reserved	R	0x0
4:0	FIFO_STATUS	I2STX_FIFO Status Indicate how many fifo level can be written into fifo. If no I2STX_CLK register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0

8.3.3.4 I2STX0_DAT_FIFO

I2STX0 FIFO data register

Offset = 0x0c

Bit(s)	Name	Description	R/W	Reset
31:8	DAT	I2STX_FIFO Data FIFO is 24bit x 32 levels.	W	x
7:0	-	Reserved	R	0x0

8.3.3.5 I2STX0_SRDCTL

I2STX0 sample rate detect control register

Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the TX output as 0. 0:not mute 1:mute	RW	0x0
11:6	-	Reserved	RW	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0:disable 1:enable	RW	0x0
7:6	-	reserved	RW	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0:2 LRCLK cycle 1:4 LRCLK cycle Other: reserved	RW	0x0
3:1	SRD_TH	Threshold of sampling rate detection 0: 8 1: 16 … 6:56 7:64 Value=(SRD_TH+1)*8	RW	0x0
0	SRD_EN	Slave mode sample rate detect enable: 0:disable 1:enable	RW	0x0

8.3.3.6 I2STX0_SRDSTA

I2STX0 sample rate detect status register

Offset = 0x14

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by SRDCLK. CNT= SRDCLK / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	sample rate changing detection timeout interrupt pending 0:no irq 1:irq	RW	0x0
10	SRC_PD	sample rate changing detection interrupt pending 0:no irq	RW	0x0

		1:irq Write '1' to clean this bit.		
9	-	Reserved for future use	R	0x0
8	CHW_PD	channel width change interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
7:3	-	Reserved	R	0x0
2:0	WL	Channel width length(the rate of BCLK to LRCLK): 000： 32 rate(I2S: 16*2bit) 001： 64 rate(I2S: 32*2bit; TDM4: 16*4bit) 010：128 rate(TDM8: 16*8bit; TDM4: 32*4bit) 011：256 rate(TDM8: 32*8bit) 1xx：error value	R	0x0

8.3.3.7 I2STX0_FIFO_CNT

I2STX0 FIFO Out Counter Register
Offset = 0x18

Bit(s)	Name	Description	R/W	Reset
31:19	-	Reserved		
18	IP	I2STXx FIFO counter overflow irq pending 0: no pending 1: pending Write '1' to clear this bit	RW	0x0
17	IE	I2STXx FIFO counter overflow irq enable: 0:disable 1:enable If CNT overflow, it would cause an interrupt.	RW	0x0
16	EN	I2STXx FIFO counter enable 0:disable 1:enable Disable this function could reset the whole counter.	RW	0x0
15:0	CNT	I2STXx FIFO counter	R	0x0

8.3.3.8 I2STX1_CTL

I2S TX1 Control Registe
Offset = 0x100

Bit(s)	Name	Description	R/W	Reset
31:21	-	Reserved	R	0x0
20	TDMTX_CHAN	0:4 channel 1:8 channel	RW	0x0
19	TDMTX_MODE	0:TDM-A (I2S data format) 1:TDM-B (left-justified data format)	RW	0x0
18:17	TDMTX_SYNC	at the beginning of the data frame, the type of LRCLK set: 00: at the rising edge of LRCLK with a pulse(duration of one BCLK) 01: at the rising edge of LRCLK with a 50% duty cycle; 10: at the falling edge of LRCLK with a 50% duty cycle; 11: Reserved	RW	0x0
16:8	-	Reserved	RW	0x0
7	TXMODE	I2S mode select: 0:I2S Master mode; 1:I2S Slave mode	RW	0x0
6	TX_SMCLK	MCLK(256FS) source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only.	RW	0x1
5:4	TXWIDTH	Effective width 00: data are 16 bit effective 01: data are 20 bit effective 10: data are 24 bit effective 11: reserved	RW	0x2
3	TXBCLKSET	Set the bit width of each channel: 0:32bit 1:16bit	RW	0x0
2:1	TXMODELSEL	I2S transfer format select: 00 : I2S format 01 : left-justified format 10 : right-justified format(when TXBCLKSET=1, this mode is invalid) 11 : TDM	RW	0x0
0	TXEN	I2S TX Enable. 0: Disable 1: Enable	R/W	0x0

8.3.3.9 I2STX1_FIFOCTL

I2STX1 FIFO control register

Offset = 0x104

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	FIFO_ DMAWIDTH	I2STX FIFO DMA transfer width configured 0 : 32bit 1 : 16bit	RW	0x0
6	-	Reserved	RW	0x0
5:4	**FIFO_IS**	I2STX_FIFO Input Select: 0x00: CPU 0x01: DMA 0x02:-reserved 0x03:reserved	RW	0x0
~~3~~	-	Reserved	RW	0x0
2	FIFO_IEN	I2STX_FIFO Half-Empty IRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
1	FIFO_DEN	I2STX_FIFO Half-Empty DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	FIFO_RST	I2STX_FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

8.3.3.10 I2STX1_FIFOSTA

I2STX1 FIFO state register

Offset = 0x108

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FIFO_ER	I2STX_FIFO error 0 : no error 1 : error If fifo was empty, system bus read TX FIFO would cause fifo error. Writing 1 to the bit will clear it	RW	0x0
7	FIFO_IP	I2STX_FIFO Half-Empty IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
6	FIFO_FULL	I2STX_FIFO Full Flag. 0x0: Not Full 0x1: Full	R	0x0

5	-	Reserved	R	0x0
4:0	FIFO_STATUS	I2STX_FIFO Status	R	0x0

8.3.3.11 I2STX1_DAT_FIFO

I2STX1 FIFO data register

Offset = 0x10c

Bit(s)	Name	Description	R/W	Reset
31:8	DAT	I2STX_FIFO Data FIFO is 24bit x 32 levels.	W	x
7:0	-	Reserved	R	0x0

8.3.3.12 I2STX1_SRDCTL

I2STX1 sample rate detect control register

Offset = 0x110

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the TX output as 0. 0:not mute 1:mute	RW	0x0
11:9	-	Reserved	RW	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0:disable 1:enable	RW	0x0
7:6	-	reserved	RW	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0:2 LRCLK cycle 1:4 LRCLK cycle Other: reserved	RW	0x0
3:1	SRD_TH	Threshold of sampling rate detection 0: 8 1: 16 … 6:56 7:64 Value=(SRD_TH+1)*8	RW	0x0
0	SRD_EN	Slave mode sample rate detect enable:	RW	0x0

		0:disable 1:enable		

8.3.3.13 I2STX1_SRDSTA

I2STX1 sample rate detect status register

Offset = 0x114

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by SRDCLK. CNT= SRDCLK / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	sample rate changing detection timeout interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
10	SRC_PD	sample rate changing detection interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
9	-	Reserved for future use	R	0x0
8	CHW_PD	channel width change interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
7:3	-	Reserved	R	0x0
2:0	WL	Channel width length(the rate of BCLK to LRCLK)： 000： 32 rate(I2S: 16*2bit) 001： 64 rate(I2S: 32*2bit; TDM4: 16*4bit) 010：128 rate(TDM8: 16*8bit; TDM4: 32*4bit) 011：256 rate(TDM8: 32*8bit) 1xx：Reserved	R	0x0

8.3.3.14 I2STX1_FIFO_CNT

I2STX1 FIFO Out Counter Register

Offset = 0x118

Bit(s)	Name	Description	R/W	Reset
31:19	-	Reserved		

18	IP	I2STXx FIFO counter overflow irq pending 0: no pending 1: pending Write '1' to clear this bit	RW	0x0
17	IE	I2STXx FIFO counter overflow irq enable: 0:disable 1:enable If CNT overflow, it would cause an interrupt.	RW	0x0
16	EN	I2STXx FIFO counter enable 0:disable 1:enable Disable this function could reset the whole counter.	RW	0x0
15:0	CNT	I2STXx FIFO counter	R	0x0

8.3.3.15 I2STX_MODE

I2S TX MODE Registe
Offset = 0x200

Bit(s)	Name	Description	R/W	Reset
31:11	-	Reserved	R	0x0
10	LPEN0	I2STX0 and I2SRX0 data loopback enable 0：disable 1：enable	RW	0x0
9	LPEN1	I2STX1 and I2SRX1 data loopback enable 0：disable 1：enable	RW	0x0
8:5	-	Reserved	R	0x0
4	SC_T0R0_EN	I2STX0,I2SRX0 share I2STX0_MCLK, BCLK, LRCLK enable： 0：disable 1：enable	RW	0x0
3	SC_T1R1_EN	I2STX1,I2SRX1 share I2STX1_MCLK, BCLK, LRCLK enable： 0：disable 1：enable	RW	0x0
2	SC_T0T1_EN	I2STX0,I2STX1 share I2STX0_MCLK, BCLK, LRCLK enable： 0：disable 1：enable	RW	0x0
1	SC_R0R1_EN	I2SRX0,I2SRX1 share I2SRX0_MCLK, BCLK, LRCLK enable：	RW	0x0

		0：disable 1：enable		
0	-	Reserved	RW	0x0

8.3.4 I2SRX Register List

Table I2S Controller Registers Address

Name	Physical Base Address
I2SRX	0xC0183000

Table I2SRX Controller Registers

Offset	Register Name	Description
0x0000	I2SRX0_CTL	I2S RX0 Control Register
0x0004	I2SRX0_FIFOCTL	I2S RX0 FIFO Control Register
0x0008	I2SRX0_FIFOSTA	I2S RX0 FIFO State Register
0x000c	I2SRX0_DAT_FIFO	I2S RX0 FIFO Data Register
0x0010	I2SRX0_SRDCTL	I2S RX0 sample rate detect control register
0x0014	I2SRX0_SRDSTA	I2S RX0 sample rate detect status register
0x0100	I2SRX1_CTL	I2S RX1 Control Register
0x0104	I2SRX1_FIFOCTL	I2S RX1 FIFO Control Register
0x0108	I2SRX1_FIFOSTA	I2S RX1 FIFO State Register
0x010c	I2SRX1_DAT_FIFO	I2S RX1 FIFO Data Register
0x0110	I2SRX1_SRDCTL	I2S RX1 sample rate detect control register
0x0114	I2SRX1_SRDSTA	I2S RX1 sample rate detect status register

8.3.5 I2SRXx Register Description

8.3.5.1 I2SRX0_CTL

I2S RX0 Control Register

Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
31:17	-	Reserved	R	0x0
16	TDMRX_CHAN	0:4 channel 1:8 channel	RW	0x0
15	TDMRX_MODE	0:TDM-A (I2S format) 1:TDM-B (left-justified format)	RW	0x0
14:13	TDMRX_SYNC	at the beginning of the data frame, the type of LRCLK set:	RW	0x0

		00: at the rising edge of LRCLK with a pulse(duration of one BCLK) 01: at the rising edge of LRCLK with a 50% duty cycle; 10: at the falling edge of LRCLK with a 50% duty cycle; 11: Reserved		
12:8	-	Reserved	R	0x0
7	RXMODE	I2S mode select: 0:I2S Master mode; 1:I2S Slave mode	RW	0x0
6	RX_SMCLK	MCLK source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only.	RW	0x1
5:4	RXWIDTH	Effective width 00:datas are 16 bit effective 01: datas are 20 bit effective 10: dates are 24 bit effective 11: reserved	RW	0x2
3	RXBCLKSET	Set the bit width of each channel: 0x00:32bit 0x01:16bit	RW	0x0
2:1	RXMODELSEL	I2S transfer format select: 0 0:i2s model 01: left-justified 10: right-justified (when TXBCLKSET=1, this mode is invalid) 11: TDM	RW	0x0
0	RXEN	I2S RX Enable. 0: Disable 1: Enable	R/W	0x0

8.3.5.2 I2SRX0_FIFOCTL

I2S RX0 FIFO Control Register

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	FIFO_ DMAWIDTH	I2SRX0FIFO DMA transfer width configured 0 : 32bit 1 : 16bit	RW	0x0
6	-	Reserved	R	0x0

5:4	FIFO_OS	RX FIFO Output Select: 0x00: CPU 0x01: DMA 0x02: reserved 0x03:reserved	RW	0x0
3	-	Reserved	RW	0x0
2	FIFO_IEN	RX FIFO Half-Filled IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	FIFO_DEN	RX FIFO Half-Filled DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	FIFO_RST	RX FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

8.3.5.3 I2SRX0_FIFOSTA

I2S RX0 FIFO State Register

Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FIFO_ER	FIFO error 0 : no error 1 : error When fifo was full, system bus wirte RX FIFO would cause error Writing 1 to the bit will clear it	RW	0
7	FIFO_IP	RX FIFO Half-Filled IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
6	FIFO_EMPTY	RX FIFO Empty Flag. 0x0: Not Empty 0x1: Empty	R	0x1
5	-	Reserved	R	0x0
4:0	FIFO_STATUS	RX FIFO Status.	R	0x0

8.3.5.4 I2SRX0_DAT_FIFO

I2S RX0 FIFO Data Register
Offset = 0x0C

Bit(s)	Name	Description	R/W	Reset
31:8	RXDAT	RX Data FIFO is 24bit x 32 levels.	R	x
7:0	-	Reserved	R	0x0

8.3.5.5 I2SRX0_SRDCTL

I2S RX0 sample rate detect control register
Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the TX output as 0. 0:not mute 1:mute **Mute would continue until SRC_PD was clear.**	RW	0x0
11:9	-	Reserved	RW	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0:disable 1:enable	RW	0x0
7:6	-	reserved	RW	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0:2 LRCLK cycle 1:4 LRCLK cycle Other: reserved	RW	0x0
3:1	SRD_TH	Threshold of sampling rate detection 0: 8 1: 16 … 6:56 7:64 Value=(SRD_TH+1)*8	RW	0x0
0	SRD_EN	Slave mode sample rate detect enable: 0:disable 1:enable	RW	0x0

8.3.5.6 I2SRX0_SRDSTA

I2S RX0 sample rate detect status register

Offset = 0x14

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by SRDCLK. CNT= SRDCLK / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	sample rate changing detection timeout interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
10	SRC_PD	sample rate changing detection interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
9	-	Reserved for future use	R	0x0
8	CHW_PD	channel width change interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
7:3	-	Reserved	R	0x0
2:0	WL	Channel width length (the rate of BCLK to LRCLK)： 000： 32 rate(I2S: 16*2bit) 001： 64 rate(I2S: 32*2bit; TDM4: 16*4bit) 010：128 rate(TDM8: 16*8bit; TDM4: 32*4bit) 011：256 rate(TDM8: 32*8bit) 1xx：error value	R	0x0

8.3.5.7 I2SRX1_CTL

I2S RX1 Control Register

Offset = 0x100

Bit(s)	Name	Description	R/W	Reset
31:17	-	Reserved	R	0x0
16	TDMRX_CHAN	0:4 channel 1:8 channel	RW	0x0
15	TDMRX_MODE	0:TDM-A (I2S format) 1:TDM-B (left-justified format)	RW	0x0
14:13	TDMRX_SYNC	at the beginning of the data frame, the type of LRCLK set:	RW	0x0

		00: at the rising edge of LRCLK with a pulse(duration of one BCLK) 01: at the rising edge of LRCLK with a 50% duty cycle; 10: at the falling edge of LRCLK with a 50% duty cycle; 11: Reserved		
12:8	-	Reserved	R	0x0
7	RXMODE	I2S mode select: 0:I2S Master mode; 1:I2S Slave mode	RW	0x0
6	RX_SMCLK	MCLK source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only.	RW	0x1
5:4	RXWIDTH	Effective width 00:datas are 16 bit effective 01: datas are 20 bit effective 10: dates are 24 bit effective 11: reserved	RW	0x2
3	RXBCLKSET	Set the bit width of each channel: 0x00:32bit 0x01:16bit	RW	0x0
2:1	RXMODELSEL	I2S transfer format select: 0 0:i2s model 01: left-justified 10: right-justified(when TXBCLKSET=1, this mode is invalid) 11: TDM	RW	0x0
0	RXEN	I2S RX Enable. 0: Disable 1: Enable	R/W	0x0

8.3.5.8 I2SRX1_FIFOCTL

I2S RX1 FIFO Control Register

Offset = 0x104

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	FIFO_ DMAWIDTH	I2SRX1FIFO DMA transfer width configured 0 : 32bit 1 : 16bit	RW	0x0
6	-	Reserved	R	0x0
5:4	FIFO_OS	RX FIFO Output Select:	RW	0x0

		0x00: CPU 0x01: DMA 0x02: reserved 0x03:reserved		
3	-	Reserved	RW	0x0
2	FIFO_IEN	RX FIFO Half-Filled IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	FIFO_DEN	RX FIFO Half-Filled DRQ Enable. 0x0: Disable 0x1: Enable	RW	0x0
0	FIFO_RST	RX FIFO Reset. 0x0: Reset FIFO 0x1: Enable FIFO	RW	0x0

8.3.5.9 I2SRX1_FIFOSTA

I2S RX1 FIFO State Register

Offset = 0x108

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FIFO_ER	FIFO error 0 : no error 1 : error When fifo was full, system bus wirte RX FIFO would cause error Write '1' to clear this bit.	RW	0
7	FIFO_IP	RX FIFO Half-Filled IRQ Pending Bit. 0x0: No IRQ 0x1: IRQ Writing 1 to the bit is clear it.	RW	0x0
6	FIFO_EMPTY	RX FIFO Empty Flag. 0x0: Not Empty 0x1: Empty	R	0x1
5	-	Reserved	R	0x0
4:0	FIFO_STATUS	RX FIFO Status.	R	0x0

8.3.5.10 I2SRX1_DAT_FIFO

I2S RX1 FIFO Data Register
Offset = 0x10C

Bit(s)	Name	Description	R/W	Reset
31:8	RXDAT	RX Data FIFO is 24bit x 32 levels.	R	x
7:0	-	Reserved	R	0x0

8.3.5.11 I2SRX1_SRDCTL

I2S RX1 sample rate detect control register
Offset = 0x110

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the TX output as 0. 0:not mute 1:mute	RW	0x0
11:9	-	Reserved	RW	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0:disable 1:enable	RW	0x0
7:6	-	reserved	RW	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0:2 LRCLK cycle 1:4 LRCLK cycle Other: reserved	RW	0x0
3:1	SRD_TH	Threshold of sampling rate detection 0: 8 1: 16 … 6:56 7:64 Value=(SRD_TH+1)*8	RW	0x0
0	SRD_EN	Slave mode sample rate detect enable: 0:disable 1:enable	RW	0x0

8.3.5.12 I2SRX1_SRDSTA

I2S RX1 sample rate detect status register
Offset = 0x114

Bit(s)	Name	Description	R/W	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by SRDCLK. CNT= SRDCLK / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	sample rate changing detection timeout interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
10	SRC_PD	sample rate changing detection interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
9	-	Reserved for future use	R	0x0
8	CHW_PD	channel width change interrupt pending 0:no irq 1:irq Write '1' to clean this bit.	RW	0x0
7:3	-	Reserved	R	0x0
2:0	WL	Channel width length (the rate of BCLK to LRCLK)： 000： 32 rate(I2S: 16*2bit) 001： 64 rate(I2S: 32*2bit; TDM4: 16*4bit) 010：128 rate(TDM8: 16*8bit; TDM4: 32*4bit) 011：256 rate(TDM8: 32*8bit) 1xx：error value	R	0x0

9 Man-Machine Interface

9.1LCD Module

9.1.1 Features

- RGB888、RGB666、RGB565、aBGR888、YCbCr444 source data format
- Source data Transfer Via DMA to FIFO
- Support 8/9/16 bit active (TFT) LCD panels with digital CPU interface

- Support 8/16/24 bit active (TFT) LCD panels with RGB interface
- Support read and write operation
- Support Dual RGB display
- Support YCbCr444 to RGB888

9.1.2 Register List

Table LCD Controller Base Address

Name	Physical Base Address
LCDC_REGISTER	0xC01A0000

Table LCD Controller Registers List

Offset	Register Name	Description
0x0000	LCD_CTL	LCD Control Register
0x0004	DISP_SIZE	LCD pixel size cfg Register
0x0008	LCDC_CLK	LCD Clock adjust Register for CPU IF
0x000c	EXT_CLK	EM clock control register for CPU IF
0x0010	DEFAULT_COLOR	RGB IF DEFAULT COLOR Register
0x0014	LCD_DATA	DATA Register
0x0018	LCD_TIM0	LCD0 RGB Timing0 register
0x001c	LCD_TIM1	LCD0 RGB Timing1 register
0x0020	LCD_TIM2	LCD0 RGB Timing2 register
0x0024	LCD_IF_PCS	LCD parity register
0x0028	LCD_IMG_XPOS	LCD image x position in the screen
0x002c	LCD_IMG_YPOS	LCD image y position in the screen
0x0030	GAMMA_IDX	Gamma memory address and status
0x0034	PATH_GAMMA_RAM	Gamma memory data
0x0038	PATH_DITHER	Dither control module
0x0040	LCD_DATA1	LCD DATA Register 1

9.1.3 Register Description

9.1.3.1 LCD_CTL

LCD controller control register

Offset = 0x0000

Bit(s)	Name	Description	R/W	Reset
31	CLK_GAT_EN	Clock gate enable bit 0: Disable	R/W	0x0

		1: Enable		
30	PC_EN	Parity Check enable bit 0: Disable 1: Enable	R/W	0x0
29	RB_SWAP	Swap R,B for input data 0：R,B NO SWAP 1：R,B SWAP	R/W	0x0
28	CESEL	Choose the Chip Select of extended memory Interface 0: CE0 1: CE1	R/W	0x0
27	IN_BUS	Inside transfer bus mode。 0: AHB Transfer Mode 1: DMA Transfer Mode	R/W	0x0
26	TEFUNCEN	TE detect function enable 0：disable 1：Enable	R/W	0x0
25	TEINV	TE Intput Polarity Inversion 0：Disable 1：Enable	R/W	0x0
24	STARTT	Start Transfer 0：Disable 1：Enable **Note:** before setting this bit all other setting of LCDC should be set. This bit would be cleared by hardware after AHB Clock is synchronized with LCD Clock.	R/W	0x0
23	ODD_EVEN_L	Odd and Even Line function Enable 0：Disable 1：Enable	R/W	0x0
22	RGB_DR	Choose RGB IF Transfer Data source 0：DRAM 1：DEFAULT COLOR REG	R/W	0x0
21	RGB565_FORMAT	Rgb565 input format selection: 1) AHB mode 0: R is bit [23:19], G is bit [15:10], B is bit [7:3]，other bit is reseved 1: bit[31:16] is reseved, bit [15:0] = g [2:0] B [4:0] R [4:0] g [5:3] 2) DMA mode 0: 32 bit contains two pixels, such as bit [31:0] = G1 [2:0] B1 [4:0] R1 [4:0] G1 [5:3] G0 [2:0] B0 [4:0] R0 [4:0] G0 [5:3] 1: 32 bit contains two pixels, such as bit [31:0] = R1 [4:0] G1 [5:0] B1 [4:0] R0 [4:0] G0 [5:0] B0 [4:0]	R/W	0x0

		See LCD for details_ Data register description.		
20	AHB_CFG_DATA	Select whether AHB write data is display data or configuration data (only CPU if) 0: display data 1: Configuration data	R/W	0x0
19:18	DQBITS	Choose the 8bits/9bit/16bits /24bits bus interface 0: 8bit 1: 16bit 2: 24bit 3: 9bit	R/W	0x0
17	-	reseved	R	0x0
16:14	CC_ODD	LCD color sequence configuration for odd line(active only at IFSEL==2 and ODD_EVEN_L==1) 000: BGR 001:RBG 010:GRB 011:GBR 100:BRG 101: RGB Other: reserved This function is only used for RGB IF	R/W	0x0
13:11	CC_EVEN	LCD color sequence configuration for even line(active only at IFSEL==2 and ODD_EVEN_L==1) 000: BGR 001:RBG 010:GRB 011:GBR 100:BRG 101: RGB Other: Reserved This function is only used for RGB IF	R/W	0x0
10:8	SDT	Source Data Type select 0: RGB565 Data Transfer 1: RGB666/BGR666 Data Transfer 2: RGB888/BGR888 Data Transfer 3: aBGR888 Data Transfer 4: YCbCr444 Data Transfer (auto open YCbCr444toRGB888) 5: YCbCr444 Data Transfer (close YCbCr444toRGB888,) Others: Reserved For RGB888/BGR888 and RGB666/BGR666 source data，they are stored contiguously in RAM in 24bit mode, so you must read 3Word(4Pixel) data every time, otherwise you will cause display errors.	R/W	0x0

		RGB for AHB interface, BGR for DMA interface, see LCD_DATA for more information.		
7	EMDE	FIFO Empty DRQ Enable. 0: Disable 1: Enable This bit should be enabled when DMA is used to transmit the LCD data.	R/W	0x0
6	RS	RS select 0: RS output low voltage level 1: RS output high voltage level RS is low or high voltage in the case of writing INDEX/DATA/REG in different LCM	R/W	0x0
5:4	DDT	IF RGB Format Select 0: RGB 565 1: RGB 666 2: RGB 888 3: Reserved	R/W	0x0
3	MLS	When LCD_CTL[19:18] is '0' and LCD_CTL[5:4] is '0', or LCD_CTL[19:18] is '3' and LCD_CTL[5:4] is '1', this bit is used to control output order. 0: first byte is RG, second byte is GB, … 1: first byte is GB, second byte is RG, …	R/W	0x0
2:1	IFSEL	Mode select 0: I8080 Interface 1: M6800 Interface 2: RGB Interface 3: Reserved	R/W	0x0
0	EN	LCD controller Enable. 0: Disable 1: Enable	R/W	0x0

9.1.3.2 DISP_SIZE

LCD pixel size cfg Register

Offset=0x0004

Bit(s)	Name	Description	R/W	Reset
31:27	-	Reserved	R	0x0
26:16	Y	Screen Height (in lines) for RGB IF/ frame size HEIGHT for CPU IF Panel height is Y+1	R/W	0x0
15:11	reserved	Reserved	R	0x0
10: 0	X	Screen Width (in pixels) for RGB IF/ frame size width for	R/W	0x0

		CPU IF Panel width is X+1		

Note: For RGB565 and ARGB888 data sources, the frame width of the RGB interface must be 4 bytes aligned. For RGB666 and RGB888 data sources, the frame width of the RGB interface must be 4pxiel (the size of each pixel is 3byte) aligned.

9.1.3.3 LCDC_CLK

LCD Clock adjust Register for CPU IF (for DMA transfer data)
Offset=0x0008

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	0x0
21:16	CLKHDU	Clock High Level Duration (from LCD_CLK). from 1 to 64 (CLKHDU +1)	R/W	0xf
15:14	-	Reserved	R	0x0
13:8	CLKL2DU	Clock Low Level Duration (from LCD_CLK) (active only at CPU 6800 IF) from 1 to 64 (CLKL2DU +1)	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	CLKLDU	Clock Low Level Duration (from LCD_CLK) from 1 to 64 (CLKLDU +1)	R/W	0xf

Note: when send RGB data to LCDM, this register should be set to obtain perfect operation clock for LCDM from LCD_CLK.

9.1.3.4 EXT_CLK

EM Clock control Register for CPU IF (for AHB transfer data)
Offset=0x000c

Bit(s)	Name	Description	R/W	Reset
31:22	-	Reserved	R	0x0
21:16	EXCLKH	Clock High Level Duration (from AHB_CLK). from 1 to 64 (EXCLKH +1)	R/W	0xf
15:14	-	Reserved	R	0x0
13:8	EXCL2KL	Clock Low Level Duration (from AHB_CLK) from 1 to 64 (EXCL2KL +1)	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	EXCLKL	Clock Low Level Duration (from AHB_CLK) from 1 to 64 (EXCLKL +1)	R/W	0xf

Note: EXT_CLK use clock from AHB_CLK, when use EXTMEM to sent command to LCDM or read data from LCDM, this register should be set to obtain perfect operation clock.

9.1.3.5 DEFAULT_COLOR

RGB IF Default Color Register

Offset=0x0010

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:16	R	panel’s default color R for RGB888	R/W	0x0
15:8	G	panel’s default color G for RGB888	R/W	0x0
7:0	B	panel’s default color B for RGB888	R/W	0x0

Data format for RGB888

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:18	R	panel’s default color R for RGB666	R/W	0x0
17:16	-	Reserved	R/W	0x0
15:10	G	panel’s default color G for RGB666	R/W	0x0
9:8	-	Reserved	R/W	0x0
7:2	B	panel’s default color B for RGB666	R/W	0x0
1:0	-	Reserved	R/W	0x0

Data format for RGB666

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:19	R	panel’s default color R for RGB565	R/W	0x0
18:16	-	Reserved	R/W	0x0
15:10	G	panel’s default color G for RGB565	R/W	0x0
9:8	-	Reserved	R/W	0x0
7:3	B	panel’s default color B for RGB565	R/W	0x0
2:0	-	Reserved	R/W	0x0

Data format for RGB565

9.1.3.6 LCD_DATA

LCD Data Register

Offset=0x0014

(1) For AHB mode (LCD_CTL.IN_BUS=0):

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:16	R	panel’s color R for RGB888	R/W	0x0
15:8	G	panel’s color G for RGB888	R/W	0x0
7:0	B	panel’s color B for RGB888	R/W	0x0

Data format for RGB888

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:18	R	panel's color R for RGB666	R/W	0x0
17:16	-	Reserved	R/W	0x0
15:10	G	panel's color G for RGB666	R/W	0x0
9:8	-	Reserved	R/W	0x0
7:2	B	panel's color B for RGB666	R/W	0x0
1:0	-	Reserved	R/W	0x0

Data format for RGB666

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:19	R	panel's color R for RGB565	R/W	0x0
18:16	-	Reserved	R/W	0x0
15:10	G	panel's color G for RGB565	R/W	0x0
9:8	-	Reserved	R/W	0x0
7:3	B	panel's color B for RGB565	R/W	0x0
2:0	-	Reserved	R/W	0x0

Data format for RGB565 (LCD_CTL. RGB565_FORMAT =0)

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:13	G	panel's color G[2:0] for RGB565	R/W	0x0
12:8	B	panel's color B for RGB565	R/W	0x0
7:3	R	panel's color R for RGB565	R/W	0x0
2:0	G	panel's color G[5:3] for RGB565	R/W	0x0

Data format for RGB565 (LCD_CTL. RGB565_FORMAT =1)

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:16	Y	panel's color Y for YCbCr444	R/W	0x0
15:8	Cb	panel's color Cb for YCbCr444	R/W	0x0
7:0	Cr	panel's color Cr for YCbCr444	R/W	0x0

Data format for YCbCr444

Bit(s)	Name	Description	R/W	Reset
31:16	-	Reserved	R	0x0
15:0	CMD	Transmitted as a command	R/W	0x0

Data register [15:0] when transmitted as a command

(2)For DMA mode (LCD_CTL.IN_BUS=1):

RGB565 (LCD_CTL. RGB565_FORMAT =0)

G1[2:0]	B1[4:0]	R1[4:0]	G1[5:3]	G0[2:0]	B0[4:0]	R0[4:0]	G0[5:3]

31bit 24 23 16 15 8 7 0bit

RGB565 (LCD_CTL. RGB565_FORMAT =1)

R1[4:0]	G1[5:3]	G1[2:0]	B1[4:0]	R0[4:0]	G0[5:3]	G0[2:0]	B0[4:0]

31bit 24 23 16 15 8 7 0bit

BGR666

R1[5:0]	2b00	B0[5:0]	2b00	G0[5:0]	2b00	R0[5:0]	2b00
G2[5:0]	2b00	R2[5:0]	2b00	B1[5:0]	2b00	G1[5:0]	2b00
B3[5:0]	2b00	G3[5:0]	2b00	R3[5:0]	2b00	B2[5:0]	2b00

31bit 24 23 16 15 8 7 0bit

BGR888

R1[7:0]	B0[7:0]	G0[7:0]	R0[7:0]
G2[7:0]	R2[7:0]	B1[7:0]	G1[7:0]
B3[7:0]	G3[7:0]	R3[7:0]	B2[7:0]

31bit 24 23 16 15 8 7 0bit

aBGR888

a0[7:0]	B0[7:0]	G0[7:0]	R0[7:0]
a1[7:0]	B1[7:0]	G1[7:0]	R1[7:0]
a2[7:0]	B2[7:0]	G2[7:0]	R2[7:0]

31bit 24 23 16 15 8 7 0bit

YCbCr444

0x0	Cr0[7:0]	Cb0[7:0]	Y0[7:0]
0x0	Cr1[7:0]	Cb1[7:0]	Y1[7:0]
0x0	Cr2[7:0]	Cb2[7:0]	Y2[7:0]

31bit 24 23 16 15 8 7 0bit

9.1.3.7 LCD_TIM0

LCD RGB Timing0 register

Offset=0x0018

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	VSYNC_INV	Vsync Output Polarity Inversion 0: Vsync Pulse active high; 1: Vsync Pulse active low	R/W	0x0
6	HSYNC_INV	Hsync Output Polarity Inversion 0: Hsync Pulse active high; 1: Hsync Pulse active low	R/W	0x0
5	DCLK_INV	DCLK Output Polarity Inversion 0: send data at rising edge	R/W	0x0

		1: send data at fall edge		
4	LDE_INV	LDE Output Polarity Inversion 0: LDE Pulse active high; 1: LDE Pulse active low	R/W	0x0
3:0	-	Reserved	R	0x0

9.1.3.8 LCD_TIM1

LCD RGB Timing1 register
Offset=0x001c

Bit(s)	Name	Description	R/W	Reset
31:30	-	Reserved	R	0x0
29:20	HSPW	Horizontal Sync Pulse Width (in pixels) Thspw = (HSPW+1) * Tpclk	R/W	0x0
19:10	HFPD	Horizontal Front Porch Delay (in pixels) Thfp = (HFP +1) * Tpclk	R/W	0x0
9:0	HBPD	Horizontal Back Porch Delay (in pixels) Thbp = (HBP +1) * Tpclk	R/W	0x0

9.1.3.9 LCD_TIM2

LCD RGB Timing2 register
Offset=0x0020

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28:20	VSPW	Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Thsync	R/W	0x0
19:10	VFPD	Vertical Front Porch Delay (in lines) Tvfp = (VFP +1) * Thsync	R/W	0x0
9:0	VBPD	Vertical Back Porch Delay (in lines) Tvbp = (VBP +1) * Thsync	R/W	0x0

9.1.3.10 LCD_IF_PCS

LCD Status register
Offset=0x0024

Bit(s)	Name	Description	R/W	Reset

31	LCDFI	LCD Data translate Finish 0: busy 1: finish Write 1 to clear the bit.	R/W	0x0
30	FRAME_END	Frame translate finish flag（Only valid on RGB interface） 0: busy 1: finish Write 1 to clear the bit.	R/W	0x0
29	VBI	Vertical Blanking pending（Only valid on RGB interface） Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period Write 1 to clear the bit.	R/W	0x0
28:18	-	Reserved	R	0x0
17	UNDER_F	Underflow Pending Bit.（Only valid on RGB interface） 0: Not overflow 1: overflow Write 1 to clear the bit and reset the FIFO.	R/W	0x0
16	-	Reserved	R	0x0
15	VBI_INTEN	Vertical Blanking Interrupt Enable Bit. 0: Disable 1: Enable	R/W	0x0
14	LCDFI_INTEN	LCD Data translate Finish Interrupt Enable Bit 0: Disable 1: Enable	R/W	0x0
13	FRAME_END_INTEN	Frane End Interrupt Enable Bit. 0: Disable 1: Enable	R/W	0x0
12	UNDER_F_INTEN	Underflow Interrupt Enable Bit. 0: Disable 1: Enable	R/W	0x0
11	-	Reserved	R	0x0
10	FIFOET	FIFO Empty Status 0: Not Empty 1: Empty	R	0x0
9	-	Reserved	R	0x0
8	TE_STATUS	TE signal status bit。 0: invalid 1: activity	R	0x1
7:0	PCS	Parity Check Sum. The Parity Check Sum of the LCD parallel interface (both 8 bit and 16bit). Only CPU	R	0x0

9.1.3.11 LCD_IMG_XPOS

LCD image x position in the screen

Offset=0x0028

Bit(s)	Name	Description	R/W	Reset
31:27	-	Reserved	R	0x0
26:16	XSTART	At which pixel per line does the image begin, XSTART+1	R/W	0x0
15:11	-	Reserved	R	0x0
10:0	XEND	At which pixel per line does the image end, XEND+1	R/W	0x0

Note: For RGB565 and ARGB888 data sources, the frame width of the RGB interface must be 4 bytes aligned. For RGB666 and RGB888 data sources, the frame width of the RGB interface must be 4pxiel (the size of each pixel is 3byte) aligned.

9.1.3.12 LCD_IMG_YPOS

LCD image y position in the screen

Offset=0x002c

Bit(s)	Name	Description	R/W	Reset
31:27	-	Reserved	R	0x0
26:16	YSTART	At which column does the image begin, YSTART+1	R/W	0x0
15:11	-	Reserved	R	0x0
10:0	YEND	At which column does the image end, YEND+1	R/W	0x0

9.1.3.13 GAMMA_IDX

Gamma memory address and status

Offset=0x0030

Bit(s)	Name	Description	R/W	Reset
31:17	-	Reserved	R	0x0
16	GAMMA_EN	Gamma enable	R/W	0x0
15:9	-	Reserved	R	0x0
8	GTD_EN	0: only gamma function 1: gamma and dither enable	R/W	0x0
7:0	RAM_IDX	0x00-0xbf，by words	R/W	0x0

Note: Using gamma function operationsequence: First configure filling in PAT_GAMMA_RAM table by setting RAM_IDX memory pointer, then enable GAMMA_EN.

9.1.3.14 PATH_GAMMA_RAM

Gamma memory data

Offset=0x0034

Bit(s)	Name	Description	R/W	Reset
31:0	RAM_DATA	0x000 R3R2R1R0 0x004 R7R6R5R4 …… 0x100 G3G2G1G0 0x104 G7G6G5G4 …… 0x200 B3B2B1B0 0x204 B7B6B5B4 …… 0x2FC B255B254	R/W	0x0

9.1.3.15 PATH_DITHER

Dither control module

Offset=0x0038

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0x0
11:9	START_YPOS	If STRENGTH=0: 4x4mode, The data range is 0-3; If STRENGTH=1: 8x8mode, The data range is 0-7;	R/W	0x0
8:6	START_XPOS	If STRENGTH=0: 4x4mode, The data range is 0-3; If STRENGTH=1: 8x8mode, The data range is 0-7;	R/W	0x0
5	POS_EN	Coordinate configurable function enable 0: Disable 1: Enable	R/W	0x0
4	STRENGTH	0:4x4 ordered dither 1:8x8 ordered dither	R/W	0x0
3:1	-	Reserved	R	0x0
0	ENABLE	Dither module enable 1: Enable 0: Disable	R/W	0x0

9.1.3.16 LCD_DATA1

LCD Data1 Register

Offset=0x0040

For AHB mode (LCD_CTL.IN_BUS=0):

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:16	R	panel's color R for RGB888	R/W	0x0
15:8	G	panel's color G for RGB888	R/W	0x0
7:0	B	panel's color B for RGB888	R/W	0x0

Data format for RGB888

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:18	R	panel's color R for RGB666	R/W	0x0
17:16	-	Reserved	R/W	0x0
15:10	G	panel's color G for RGB666	R/W	0x0
9:8	-	Reserved	R/W	0x0
7:2	B	panel's color B for RGB666	R/W	0x0
1:0	-	Reserved	R/W	0x0

Data format for RGB666

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved	R	0x0
23:16	Y	panel's color Y for YCbCr444	R/W	0x0
15:8	Cb	panel's color Cb for YCbCr444	R/W	0x0
7:0	Cr	panel's color Cr for YCbCr444	R/W	0x0

Data format for YCbCr444

Note：

To complete the transmission of RGB666 and RGB888, The LCD_DATA1 register is used to satisfy the transmission for the RGB/YCbCr data of two pixels need to be transmitted for three times,The specific usage is as follows:

1) Configure AHB interface (LCD_ CTL.IN_ BUS=0）、16bit DQ BUS（LCD_ CTL.DQBITS=1 ）、The transmission data is display data (LCD_ CTL.AHB_CFG_ Data = 0), and the output interface is rgb666 or rgb888 (LCD_ CTL. DDT=1/2）;

2) Writes the RGB/YCbCr data of the first pixel to be transmitted in the LCD_DATA1;

3) And then writes RGB/YCbCr data of the second pixel to be transmitted in the LCD_DATA;

4) Loop Step2 and 3 until data transfer is complete.

The matters needing attention:

1) For LCD_Data register to be written will start the transfer, so please write LCD_DATA1 at first, and then write to LCD_ Data register.

2) Only supports even pixel transmission.

9.2PWM

9.2.1 Features

- Support frequency and duty ratio adjustable
- Support 9 channel PWM channel, independent adjustable
- Support 3 modes: Fixed mode, Breath mode and programmable mode.
- The Fixed mode maximum supports 64K duty; duty can be configured arbitrarily by RAM, and can output PWM waveform with fixed frequency and duty cycle.
- The Breath mode supports the duty cycle gradient, enabling the breathing lamp to become brighter or darker.
- The programmable mode supports duty cycle in real time with RAM. Generate arbitrary waveform.
- Support multiple PWM and programmable mode at the same time

9.2.2 Fixed Mode Timing

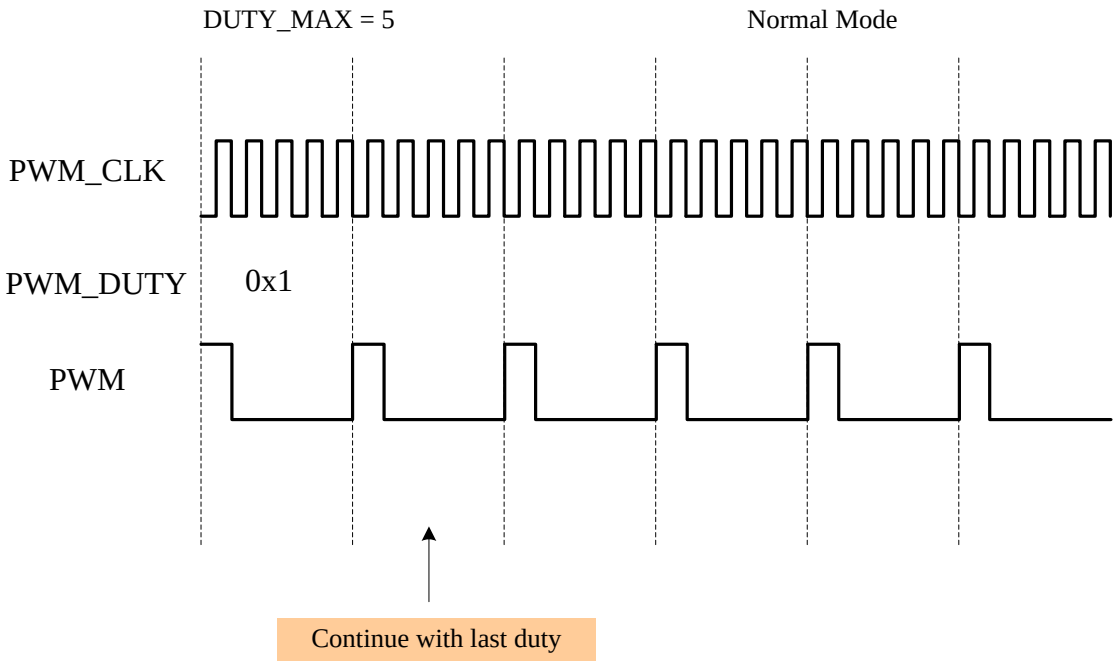


Figure9-1 Fixed mode simple example

9.2.3 Breath Mode Timing

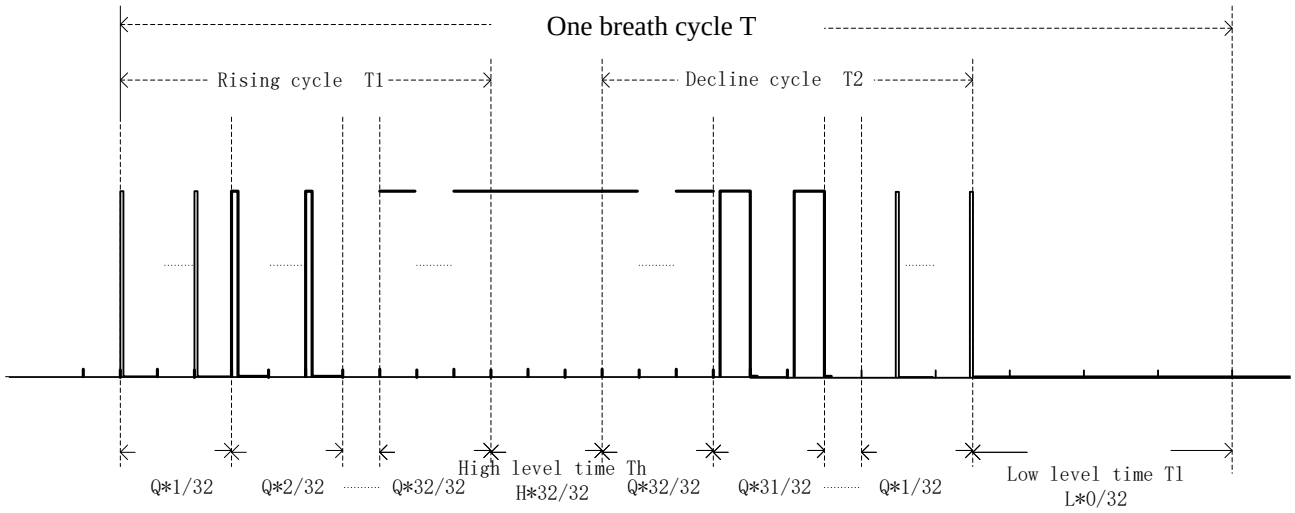


Figure 9-2 Breath mode simple example

9.2.4 Programmable Mode Timing

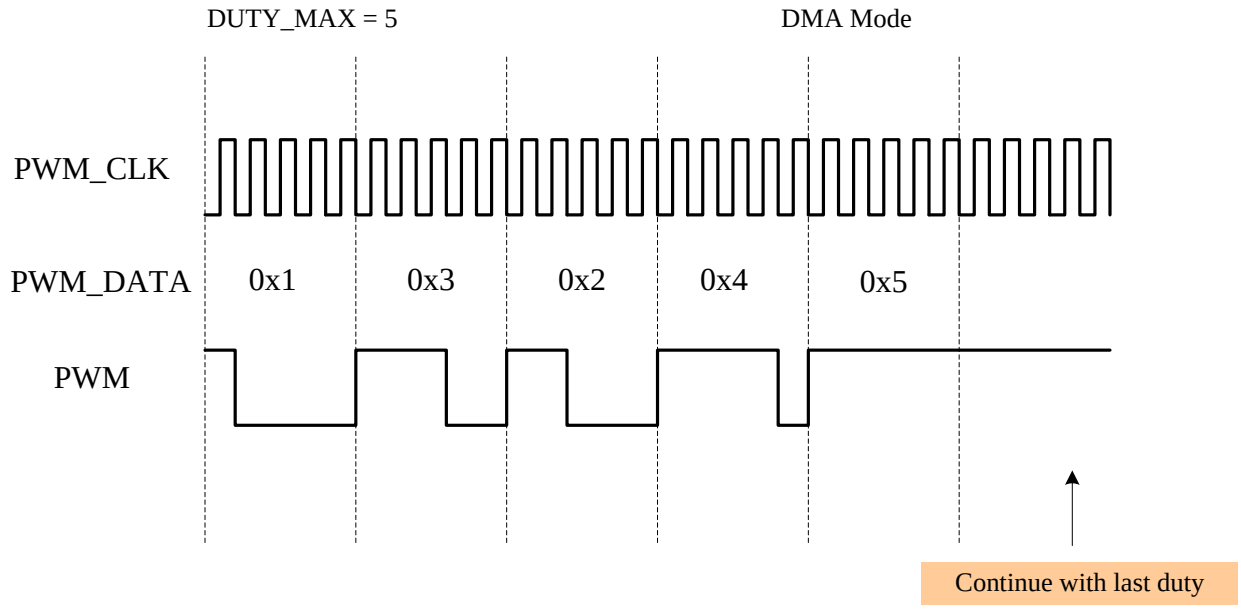


Figure9-3 Programmable mode example used DMA transmission

Note：PWM_DUTY_MAX > (DMA_WAIT_CYCLE + 6) * (PWM_CLK / DMA_CLK)

9.2.5 Register List

Table PWM Controller Registers Address

Name	Physical Base Address
PWM	0xC0190000

Table PWM Controller Registers

Offset	Register Name	Description
0x000	PWMx_CTL	PWM0 Output Control register
0x004	PWMx_C	PWM0 breath mode C register
0x008	PWMx_Q	PWM0 breath mode Q register
0x00c	PWMx_H	PWM0 breath mode H register
0x010	PWMx_L	PWM0 breath mode L register
0x014	PWMx_DUTYMAX	PWM0 Duty Max register
0x018	PWMx_DUTY	PWM0 Duty register
0xf00	PWM_DMACTL	PWM Enable Control register
0xf04	PWM_FIFODAT	PWM FIFO Data register
0xf08	PWM_FIFOSTA	PWM FIFO Status register

9.2.6 **Register** Description

9.2.6.1 PWMx_CTL

PWMx Output Control Register

Offset = 0x000 + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:5	Reserved	Reserved	R	0x0
4	CH_START	PWM0 Channel start 0: stop after this PWM wave period 1: PWM start	RW	0x0
3	CH_EN	PWM0 Channel Enable 0: disable 1: enable	RW	0x0
2	POL_SEL	Polarity select: 0:PWM0 low voltage level active 1:PWM0 high voltage level active Active in fixed Mode and Breath Mode	RW	0x0
1:0	MODE_SEL	PWM0 Mode Select: 0: Fixed Mode 1: Breath Mode 2: Programmable Mode 3: Reserved	RW	0x0

Note: CH_START write 0 will take effect after a complete PWM cycle，When CH_EN writes 0, it will take effect

immediately, and the PWM output level will be changed by POL_SEL decided.

9.2.6.2 PWMx_C

PWMx Breath mode C configuration Register
Offset = 0x004 + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:24	Reserved	Reserved	R	0x0
7:0	C	Counter Top of PWM Duty For Example: In Breath Mode if C = 32， The PWM Duty is 1/32, 2/32, .. , 32/32	RW	0x20

Note: Rising and DeclineTime→High Level Time→Low Level Time, there will be a small time slot(t, one period of CMU_PWM ,not affect) in the gap between the 3 state transitions.

9.2.6.3 PWMx_Q

PWMx Breath mode Q configuration Register
Offset = 0x008 + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:24	Reserved	Reserved	R	0x0
23:16	QD	Time of Every Duty =C/C …1/C: Fall time T2=QD*C*C*t t is the period of CMU_PWM C*t is the period of PWM Wave Only Active in Breath Mode	RW	0x0
15:8	Reserved	Reserved	R	0x0
7:0	QU	Time of Every Duty =1/C …C/C: rise time T1=QU*C*C*t t is the period of CMU_PWM C*t is the period of PWM Wave Only Active in Breath Mode	RW	0x0

9.2.6.4 PWMx_H

PWMx Breath mode H/L configuration Register
Offset = 0x00c + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	R	0x0
15:0	H	Time of Duty =C/C :	RW	0x0

		High Level Time = H*C*t t is the period of CMU_PWM\ C*t is the period of PWM Wave Only Active in Breath Mode		

9.2.6.5 PWMx_L

PWMx Breath mode H/L configuration Register
Offset = 0x010 + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	R	0x0
15:0	L	Time of Duty =0/C: Low Level Time = L*C*t t is the period of CMU_PWM C*t is the period of PWM Wave Only Active in Breath Mode	RW	0x0

9.2.6.6 PWMx_DUTYMAX

PWMx Duty Max Register
Offset = 0x014 + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	R	0x0
15:0	DUTYMAX	Configurable maximum duty. PWM period = PWM_CLK period * DUTY_MAX Note: PWM_ CLK period is PWM clock period DUTYMAX >= 0x1	RW	0x1

9.2.6.7 PWMx_DUTY

PWMx Duty Register
Offset = 0x018 + 0x100*x

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	R	0x0
15:0	DUTY	PWM DUDY = DUTY / DUTY_MAX Only Active in Normal Mode	RW	0x0

9.2.6.8 PWM_DMACTL

PWM Module Enable Register

Offset = 0xf00

Bit(s)	Name	Description	R/W	Reset
31:1	Reserved	Reserved	R	0x0
7:4	PWM_FIFO_CLK_SEL	0000:PWM0 0001:PWM1 0010:PWM2 0011:PWM3 0100:PWM4 0101:PWM5 0110:PWM6 0111:PWM7 1000:PWM8 Other: Reserved	RW	0x0
3:1	-	-	RW	0x0
0	START	PWM DMA START 0: disable 1: enable	RW	0x0

Note：PWM DMA channel is selected by bit [7:4]

9.2.6.9 PWM_FIFODAT

PWM FIFO Data Register

Offset = 0xf04

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	R	0x0
15:0	DATA	DUTY DATA PWM DUDY = DUTY / DUTY_MAX Only Active in programmable Mode	R	0x0

Note: DUTY must be configured ≤ (DUTY_MUX), failing to do so may result in unpredictable behavior.

9.2.6.10 PWM_FIFOSTA

PWM FIFO Status Register

Offset = 0xf08

Bit(s)	Name	Description	R/W	Reset
31:5	Reserved	Reserved	R	0x0
4:3	LEVEL	PWM FIFO level	R	0x2

		This field indicates pwm fifo empty level		
2	EMPTY	PWM FIFO empty status: 0: not empty 1: empty	R	0x1
1	FULL	PWM FIFO full status: 0: not full 1: full	R	0x0
0	ERROR	PWM FIFO error status: 0: no error 1: error Writing 1 to the bit is clear	RW	0x0

9.3SARADC

9.3.1 Features

The ATJ2157 integrates one 10-bit muti-channals ADC module, which can be used to sample BAT/DC5V/AVCC/SVCC, temperature and 11 external analog inputs.

9.3.2 A/D Converters

ADC input range：

channal	range
DC5VADC	input voltage range is 0~6V
BATADC	input voltage range is 2~4.5V
SENSOR	Temperature range is -40~120℃
AVCCADC	input voltage range is 0~AVCC
SVCCADC	input voltage range is 0~SVCC
LRADC1	input voltage range is 0~SVCC
LRADC2/3/4/5/6/7/8/9/10	input voltage range is 0~AVCC

Table 3 ADC input range

The output data of ADC can be calculated as the following formula：

BATADC：

1 LSB= $\frac{4.8}{2^{10}} * \frac{Vref}{1.5}$ ， When the battery voltage equals VBAT, the ADC data n= $\frac{Vbat}{\frac{4.8}{2^{10}} * \frac{Vref}{1.5}}$

Where Vref is the value of the reference voltage actually value.

For example: Vref=1.5V, 1LSB=4.69mV， So the corresponding data from 0v to 0.00469V is 000h .

DC5VADC：

1 LSB= $\frac{6}{2^{10}} * \frac{Vref}{1.5}$， When the battery voltage equals V, the ADC data n= $\frac{V}{\frac{6}{2^{10}} * \frac{Vref}{1.5}}$

Where Vref is the value of the reference voltage actually value.

For example: Vref=1.5V, 1LSB=5.86mV， So the corresponding data from 0v to 0.00586V is 000h .

SENSADC:

1 LSB= $\frac{1.2}{2^{10}} * \frac{Vref}{1.5}$， When the voltage of TEMP SENSOR equals V, the ADC data n= $\frac{V}{\frac{1.2}{2^{10}} * \frac{Vref}{1.5}}$

Where Vref is the value of the reference voltage actually value.

Temperature range is -40~120℃

T=(1.2/1024*data(decimal)*Vref/1.5-0.7691)/(-0.001707) ℃。

AVCCADC/LRADC1/2/3/4/5/6/7/8/9/10/11/SVCCADC

1 LSB= $\frac{3.6}{2^{10}} * \frac{Vref}{1.5}$， When theinput voltage equals V, the ADC data n= $\frac{V}{\frac{3.6}{2^{10}} * \frac{Vref}{1.5}}$

9.3.3 SARADC Register List

SARADC block base address

Name	Physical Base Address
SARADC	0xC0010000

PMU Block Configuration Registers List

Offset	Register Name	Description
0x38	PMUADC_CTL	PMUADC Control Register
0x3C	BATADC_DATA	BAT ADC data Register
0x40	DC5VADC_DATA	DC5V ADC data Register
0x44	SENSADC_DATA	SENSOR ADC data Register
0x48	AVCCADC_DATA	AVCCADC data Register
0x50	LRADC1_DATA	LRADC1 data Register
0x54	LRADC2_DATA	LRADC2 data Register

0x58	LRADC3_DATA	LRADC3 data Register
0x5C	LRADC4_DATA	LRADC4 data Register
0x60	LRADC5_DATA	LRADC5 data Register
0x64	LRADC6_DATA	LRADC6 data Register
0x68	LRADC7_DATA	LRADC7 data Register
0x6C	LRADC8_DATA	LRADC8 data Register
0x70	LRADC9_DATA	LRADC9 data Register
0x74	LRADC10_DATA	LRADC10 data Register
0x7C	SVCCADC_DATA	SVCCADC data Register

9.3.4 Register Description

9.3.4.1 PMUADC_CTL

PMUADC Control Register （VDD） default: 0x1001B **Offset = 0x38**

Bit(s)	Name	Description	R/W	Reset
31:24	-	Reserved for analog future use	R/W	0
23:20	FASTMODE_SET	ADC single channel fast mode channel select: 0000：DC5VADC 0001：BATADC 0010：SENSORADC 0011：AVCCADC 0100：LRADC1ADC 0101：LRADC2ADC 0110：LRADC3ADC 0111：LRADC4ADC 1000：LRADC5ADC 1001：LRADC6ADC 1010：LRADC7ADC 1011：LRADC8ADC 1100：LRADC9ADC 1101：LRADC10ADC 1110：reserved 1111：SVCCADC	R/W	0000
19	FASTMODE_EN	ADC single channel fast mode enable: 0：Disable 1：Enable	R/W	0
18	-	Reserved for analog future use	R/W	0
17	I_COMP_SET	ADC COMP current set	R/W	0

		0: 0.5uA 1: 1uA		
16	RESERVED	RESERVED	R /W	1
15	SVCCADC_EN	SVCCADC A/D enable. 0: Disable 1: Enable	R/W	0
14	-	reserved	R/W	0
13	LRADC10_EN	LRADC10 A/D enable. 0: Disable 1: Enable	R/W	0
12	LRADC9_EN	LRADC9 A/D enable. 0: Disable 1: Enable	R/W	0
11	LRADC8_EN	LRADC8 A/D enable. 0: Disable 1: Enable	R/W	0
10	LRADC7_EN	LRADC7 A/D enable. 0: Disable 1: Enable	R/W	0
9	LRADC6_EN	LRADC6 A/D enable. 0: Disable 1: Enable	R/W	0
8	LRADC5_EN	LRADC5 A/D enable. 0: Disable 1: Enable	R/W	0
7	LRADC4_EN	LRADC4 A/D enable. 0: Disable 1: Enable	R/W	0
6	LRADC3_EN	LRADC3 A/D enable. 0: Disable 1: Enable	R/W	0
5	LRADC2_EN	LRADC2 A/D enable. 0: Disable 1: Enable	R/W	0
4	LRADC1_EN	LRADC1 A/D enable. 0: Disable 1: Enable If S1 has configured the corresponding WIO as LRADC1 function, when entering S4, set the WIO register as IO function, and then proceed to S4 to prevent SVCC leakage	R/W	1

3	AVCCADC_EN	AVCC A/D enable 0: Disable 1: Enable	R/W	1
2	SENSORADC_EN	Sensor A/D enable 0: Disable, sensor circuit and output disable 1: Enable, sensor circuit and output enable	R/W	0
1	BATADC_EN	Battery A/D enable 0: Disable 1: Enable	R/W	1
0	DC5VADC_EN	DC5V A/D enable 0: Disable 1: Enable	R/W	1

9.3.4.2 BATADC_data

BATADC DATA Register（VDD） **Offset = 0x3C**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	BATADC	10bit Voltage ADC，used to detect Battery voltage。	R	Xx

9.3.4.3 DC5VADC_DATA

DC5V ADC DATA Register (VDD) **Offset = 0x40**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	DC5VADC	10bit Voltage ADC，used to detect DC5V voltage。 Input voltage range is: 0-6V	R	Xx

9.3.4.4 SENSADC_data

Sensor ADC DATA Register (VDD) **Offset = 0x44**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	SENSADC	10bit Voltage ADC，used to detect TEMP。	R	xx

9.3.4.5 AVCCADC_DATA

AVCCADC DATA Register (VDD) **Offset = 0X48**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	AVCCADC	AVCC ADC data.	R	xx

9.3.4.6 LRADC1_DATA

LRADC1 DATA Register(VDD) **Offset = 0x50**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC1	LRADC1 data LRADC1 input voltage range is from 0 to SVCC.	R	xx

9.3.4.7 LRADC2_DATA

LRADC2 DATA Register(VDD) **Offset = 0x54**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC2	LRADC2 data.	R	xx

9.3.4.8 LRADC3_data

LRADC3 DATA Register (VDD) **Offset = 0x58**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC3	LRADC3data	R	xx

9.3.4.9 LRADC4_data

LRADC4 DATA Register (VDD) **Offset = 0x5C**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC4	LRADC4 data	R	xx

9.3.4.10 LRADC5_DATA

LRADC5 DATA Register(VDD) **Offset = 0x60**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC5	LRADC5 data.	R	xx

9.3.4.11 LRADC6_data

LRADC6 DATA Register(VDD) **Offset = 0x64**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC6	LRADC6 data.	R	xx

9.3.4.12 LRADC7_data

LRADC7 DATA Register (VDD) **Offset = 0x68**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC7	LRADC7 的数据输出.	R	xx

9.3.4.13 LRADC8_data

LRADC8 DATA Register (VDD) **Offset = 0X6C**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC8	LRADC8 data.	R	xx

9.3.4.14 LRADC9_data

LRADC9 DATA Register(VDD) **Offset = 0X70**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC9	LRADC9 data	R	xx

9.3.4.15 LRADC10_data

LRADC10 DATA Register (VDD) **Offset = 0X74**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	LRADC10	LRADC10 data	R	xx

9.3.4.16 SVCCADC_data

SVCCADC DATA Register (VDD) **Offset = 0x7C**

Bit(s)	Name	Description	R/W	Reset
31:10	-	RESERVED	R	0
9:0	SVCCADC	SVCCADC data.	R	xx

10 GPIO/MFP

10.1 Features

- Each IO can configure input and output port, which can output 0 or 1. It can also detect the level signal input by external circuit, and read 0 or 1 through internal registers.
- Schmitt can be configured to open or close
- Built-in upper/down pull resistance,could be selected
- The driving ability is adjustable. 4 levels

10.2 Function Description

A PAD can be configured muti-function by MFP_CTL, to pay attention to its priority relationship

10.2.1 IO Output

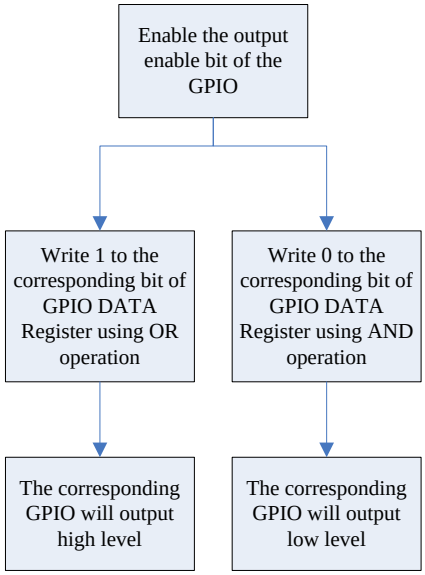


Figure 10-1 IO config output

10.2.2 IO Input

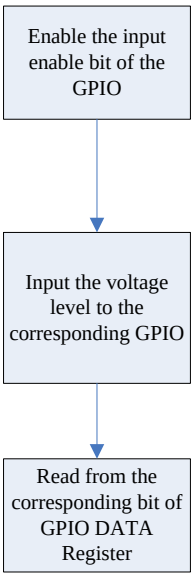


Figure 10-2 IO config input

10.2.3 GPIO[75:64] OUTPUT SET

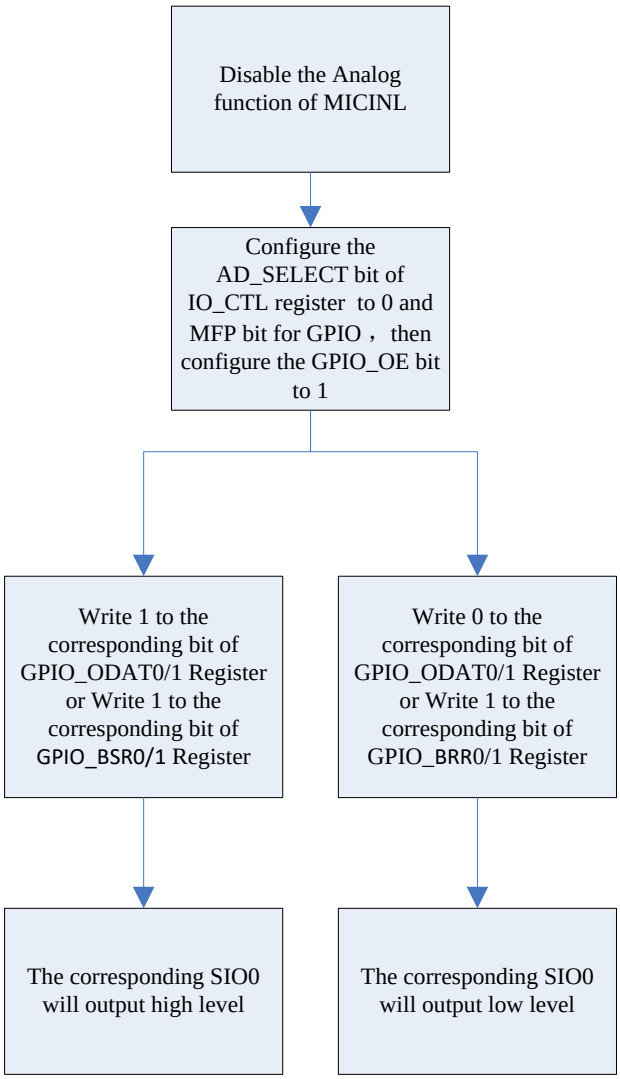


Figure 10-3 GPIO[75:64] output configure

10.2.4 GPIO[75:64] INPUT SET

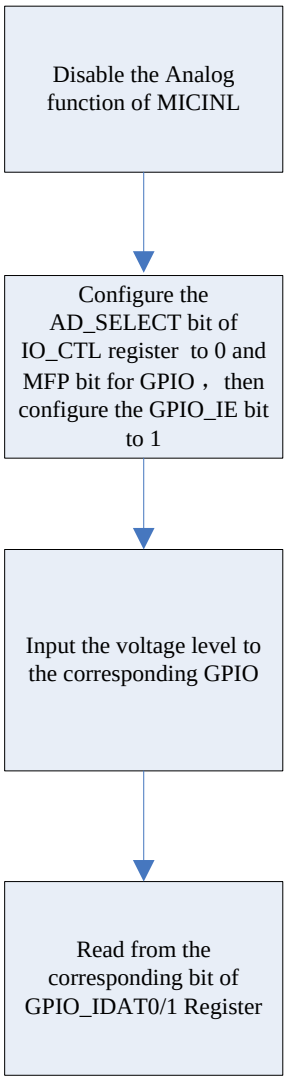


Figure 10-4 GPIO[75:64] input configure

10.2.5 GPIO INTC

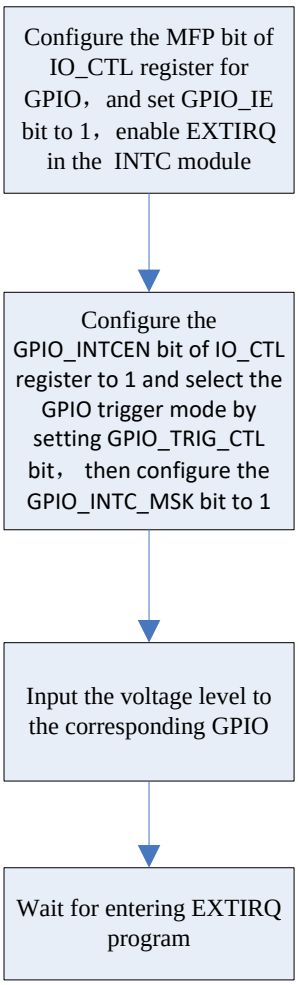


Figure 10-5 GPIO interrupt configure

10.3 Register List

Table GPIO_MFP Controller Registers Address

Name	Physical Base Address
GPIO_MFP	0xC01C0000

Table GPIO&MFP Controller Registers

Offset	Register Name	Description
0x0004	GPIO0_CTL	GPIO0 control Register
0x0008	GPIO1_CTL	GPIO1 control Register
0x000C	GPIO2_CTL	GPIO2 control Register
0x0010	GPIO3_CTL	GPIO3 control Register
0x0014	GPIO4_CTL	GPIO4 control Register

0x0018	GPIO5_CTL	GPIO5 control Register
0x001C	GPIO6_CTL	GPIO6 control Register
0x0020	GPIO7_CTL	GPIO7 control Register
0x0024	GPIO8_CTL	GPIO8 control Register
0x0028	GPIO9_CTL	GPIO9 control Register
0x002C	GPIO10_CTL	GPIO10 control Register
0x0030	GPIO11_CTL	GPIO11 control Register
0x0034	GPIO12_CTL	GPIO12 control Register
0x0038	GPIO13_CTL	GPIO13 control Register
0x003C	GPIO14_CTL	GPIO14 control Register
0x0040	GPIO15_CTL	GPIO15 control Register
0x0044	GPIO16_CTL	GPIO16 control Register
0x0048	GPIO17_CTL	GPIO17 control Register
0x004C	GPIO18_CTL	GPIO18 control Register
0x0050	GPIO19_CTL	GPIO19 control Register
0x0054	GPIO20_CTL	GPIO20 control Register
0x0058	GPIO21_CTL	GPIO21 control Register
0x005C	GPIO22_CTL	GPIO22 control Register
0x0060	GPIO23_CTL	GPIO23 control Register
0x0064	GPIO24_CTL	GPIO24 control Register
0x0068	GPIO25_CTL	GPIO25 control Register
0x006C	GPIO26_CTL	GPIO26 control Register
0x0070	GPIO27_CTL	GPIO27 control Register
0x0074	GPIO28_CTL	GPIO28 control Register
0x0078	GPIO29_CTL	GPIO29 control Register
0x007C	GPIO30_CTL	GPIO30 control Register
0x0080	GPIO31_CTL	GPIO31 control Register
0x0084	GPIO32_CTL	GPIO32 control Register
0x0088	GPIO33_CTL	GPIO33 control Register
0x009C	GPIO38_CTL	GPIO38 control Register
0x00a0	GPIO39_CTL	GPIO39 control Register
0x00B0	GPIO43_CTL	GPIO43 control Register
0x00E0	GPIO55_CTL	GPIO55 control Register
0x00E4	GPIO56_CTL	GPIO56 control Register
0x0104	GPIO64_CTL	GPIO64 control Register
0x0108	GPIO65_CTL	GPIO65 control Register
0x010C	GPIO66_CTL	GPIO66 control Register
0x0110	GPIO67_CTL	GPIO67 control Register
0x0114	GPIO68_CTL	GPIO68 control Register
0x0118	GPIO69_CTL	GPIO69 control Register
0x0124	GPIO72_CTL	GPIO72 control Register

0x0128	GPIO73_CTL	GPIO73 control Register
0x012C	GPIO74_CTL	GPIO74 control Register
0x0130	GPIO75_CTL	GPIO75 control Register
0x0200	GPIO_ODAT0	GPIO Output Data register0
0x0204	GPIO_ODAT1	GPIO Output Data register1
0x0208	GPIO_ODAT2	GPIO Output Data register2
0x0210	GPIO_BSR0	GPIO Output Data bit set register0
0x0214	GPIO_BSR1	GPIO Output Data bit set register1
0x0218	GPIO_BSR2	GPIO Output Data bit set register2
0x0220	GPIO_BRR0	GPIO Output Data bit set register0
0x0224	GPIO_BRR1	GPIO Output Data bit set register1
0x0228	GPIO_BRR2	GPIO Output Data bit set register2
0x0230	GPIO_IDAT0	GPIO Output Data register0
0x0234	GPIO_IDAT1	GPIO Output Data register1
0x0238	GPIO_IDAT2	GPIO Output Data register2
0x0240	GPIO_PD0	GPIO IRQ Pending register0
0x0244	GPIO_PD1	GPIO IRQ Pending register1
0x0304	WIO1_CTL	Wake up IO1 control Register

10.4 Register Description

10.4.1 GPIO0_CTL

GPIO0 control Register

Offset=0x04

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level	R/W	0x0

		Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO	R/W	0x0

		1:NF_D0 2:LCD_D0 4:SDC0_CMD 6:SPI0_SS 9:UART0_TX 16:PWM0 20:IISRX1_MCLK 31:SPI0_MOSI OTHER: Reserved		

10.4.2 GPIO1_CTL

GPIO1 control Register

Offset=0x08

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control	R/W	0x1

		000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_D1 2:LCD_D1 4:SDC0_CLK0 6:SPI0_MISO 9:UART0_RX 16:PWM1 20:IISRX1_BCLK 31:SPI0_CLK OTHER: Reserved	R/W	0x0

10.4.3 **GPIO2_CTL**

GPIO2 control Register

Offset=0x0C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0

8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_D2 2:LCD_D2 4:SDC0_DAT0 6:SPI0_CLK 9:UART0_CTS 13:TWI0_CLK 16:PWM2 20:IISRX1_LRCLK 31:SPI0_SS OTHER: Reserved	R/W	0x0

10.4.4 GPIO3_CTL

GPIO3 control Register

Offset=0x10

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level	R/W	0x0

		100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO	R/W	0x0

		0:GPIO 1:NF_D3 2:LCD_D3 4:SDC0_DAT1 6: SPI0_MOSI 9:UART0_RTS 13:TWI0_DAT 16:PWM3 20:IISRX1_DIN 31:SPI0_MISO OTHER: Reserved		

10.4.5 GPIO4_CTL

GPIO4 control Register

Offset=0x14

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0

14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_D4 2:LCD_D4 4:SDC0_DAT2 6:SPI0_D2 10:UART1_TX 16:PWM4 17:IISTX0_MCLK 24:PDMTX_CLK 28: T2_CAP OTHER: Reserved	R/W	0x0

10.4.6 GPIO5_CTL

GPIO5 control Register

Offset=0x18

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0

10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_D5 2:LCD_D5 4:SDC0_DAT3 6:SPI0_D3 10:UART1_RX 16:PWM5 17:IISTX0_BCLK 24:PDMTX_DAT 28: T3_CAP OTHER: Reserved	R/W	0x0

10.4.7 GPIO6_CTL

GPIO6 control Register

Offset=0x1C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode	R/W	0x0

		000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0

5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_D6 2:LCD_D6 4:SD0_DAT4 8:SPI2_SS 10:UART1_CTS 14:TWI1_CLK 16:PWM6 18:IISTX1_MCLK 25:DMIC01_CLK 27:LRADC2 OTHER: Reserved	R/W	0x0

10.4.8 GPIO7_CTL

GPIO7 control Register

Offset=0x20

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when	R/W	0x0

		GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_D7 2:LCD_D7 4:SD0_DAT5 8:SPI2_CLK 10:UART1_RTS 14:TWI1_DAT 16:PWM7 18:IISTX1_BCLK	R/W	0x0

		25:DMIC01_DAT 27:LRADC3 OTHER: Reserved		

10.4.9 GPIO8_CTL

GPIO8 control Register

Offset=0x24

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6	R/W	0x1

		110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_CLE 2:LCD_RS_VSYNC 4:SD0_DAT6 8:SPI2_MISO 11:UART2_TX 16:PWM8 18:IISTX1_LRCLK 25:DMIC01_CLK 27:LRADC4 OTHER: Reserved	R/W	0x0

10.4.10 **GPIO9_CTL**

GPIO9 control Register

Offset=0x28

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt	R/W	0x0

		to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect		
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable.	R/W	0x0

		0: Disable 1: Enable		
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_ALE 2:LCD_TE 4:SD0_DAT7 8:SPI2_MOSI 11:UART2_RX 16:PWM0 17:IISTX0_LRCLK 18:IISTX1_DOUT 25:DMIC01_DAT OTHER: Reserved	R/W	0x0

10.4.11 **GPIO10_CTL**

GPIO10 control Register

Offset=0x2C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable;	R/W	0x0

		Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_RDB 2:LCD_RDE_LDE 4:SD0_CLK1	R/W	0x0

		7:SPI1_D3 11:UART2_CTS 13:TWI0_CLK 16:PWM1 17:IISTX0_DOUT 25:DMIC23_CLK 27:LRADC7 OTHER: Reserved		

10.4.12 GPIO11_CTL

GPIO11 control Register

Offset=0x30

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1	R/W	0x1

		001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_WRB 2:LCD_WR_DCLK 4:SD0_CMD 7:SPI1_D2 11:UART2_RTS 13:TWI0_DAT 16:PWM2 19:IISRX0_MCLK 25:DMIC23_DAT 27:LRADC7 OTHER: Reserved	R/W	0x0

10.4.13 **GPIO12_CTL**

GPIO12 control Register

Offset=0x34

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable	R/W	0x0

		1: Enable		
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_CE1 4:SD0_DAT0 7:SPI0_MISO 12;UART3_TX 16:PWM3 19:IISRX0_BCLK 25:DMIC23_CLK 27:LRADC8 28: T2_CAP OTHER: Reserved	R/W	0x0

10.4.14 GPIO13_CTL

GPIO13 control Register

Offset=0x38

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge	R/W	0x0

		011: hight level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0

4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_CE2 2:LCD_CE1 4:SD0_CLK0 7:SPI0_MOSI 12:UART3_RX 16:PWM4 19:IISRX0_LRCLK 25:DMIC23_DAT 27:LRADC9 29:VMIC0 OTHER: Reserved	R/W	0x0

10.4.15 GPIO14_CTL

GPIO14 control Register

Offset=0x3C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS	R/W	0x0

		0: Disable; 1: Enable;		
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_CE3 2:LCD_CE0_HSYNC 4:SD0_CMD 7:SPI0_CLK 12:UART3_CTS 14:TWI1_CLK 16:PWM5 19:IISRX0_DIN 27:LRADC10 OTHER: Reserved	R/W	0x0

10.4.16 GPIO15_CTL

GPIO15 control Register

Offset=0x40

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0

10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_CE4 2:LCD_CE1 4:SD0_DAT0 7:SPI0_SS 12:UART3_RTS 14:TWI1_DAT 16:PWM6 18:IISTX1_DOUT 19:IISRX0_MCLK 29:VMIC1 OTHER: Reserved	R/W	0x0

10.4.17 **GPIO16_CTL**

GPIO16 control Register

Offset=0x44

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0

23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable	R/W	0x0

		1: Enable		
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_RB1 7:SPI1_MISO 12:UART3_TX 16:PWM7 19:IISRX0_MCLK 25:DMIC23_CLK 27:LRADC5 28: T3_CAP OTHER: Reserved	R/W	0x0

10.4.18 GPIO17_CTL

GPIO17 control Register

Offset=0x48

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0

19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 1:NF_DQS 7:SPI1_MISO 12:UART3_TX 16:PWM7 19;IIS0RX_BCLK 25:DMIC23_CLK 27:LRADC6 OTHER: Reserved	R/W	0x0

10.4.19 GPIO18_CTL

GPIO18 control Register

Offset=0x4C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0

10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D8 5:SD1_CLK0 8:SPI2_SS 9:UART0_TX 16:PWM0 17:IISTX0_MCLK 24:PDMTX_CLK OTHER: Reserved	R/W	0x0

10.4.20 GPIO19_CTL

GPIO19 control Register

Offset=0x50

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge	R/W	0x0

		010:dual edge 011: hight level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable	RW	0x0

		1: Enable		
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D9 5:SD1_CLK1 8:SPI2_CLK 9:UART0_RX 16:PWM1 17:IISTX0_BCLK 24:PDMTX_DAT OTHER: Reserved	R/W	0x0

10.4.21 GPIO20_CTL

GPIO20 control Register

Offset=0x54

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable;	R/W	0x0

		1: Enable;		
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D10 5:SD1_CMD 8:SPI2_MISO 9:UART0_CTS 13:TWI0_CLK 16:PWM2 17:IISTX0_LRCLK 27:LRADC7 OTHER: Reserved	R/W	0x0

10.4.22 GPIO21_CTL

GPIO21 control Register

Offset=0x58

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0

10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D11 5:SD1_DAT0 8:SPI2_MOSI 9:UART0_RTS 13:TWI0_DAT 16:PWM3 17:IISTX0_DOUT 27:LRADC8 OTHER: Reserved	R/W	0x0

10.4.23 GPIO22_CTL

GPIO22 control Register

Offset=0x5C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge	R/W	0x0

		001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO:	RW	0x0

		0: Disable 1: Enable		
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D12 7:SPI1_SS 5:SD1_DAT4 10:UART1_TX 16:PWM4 19:IISRX0_MCLK 25:DMIC01_CLK OTHER: Reserved	R/W	0x0

10.4.24 GPIO23_CTL

GPIO23 control Register

Offset=0x60

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS	R/W	0x0

		0: Disable; 1: Enable;		
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D13 4:SD0_DAT4 5:SD1_DAT5 7:SPI1_CLK 10:UART1_RX 16:PWM5 19:IISRX0_BCLK 25:DMIC01_DAT OTHER: Reserved	R/W	0x0

10.4.25 GPIO24_CTL

GPIO24 control Register

Offset=0x64

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0

10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D14 7:SPI1_MISO 4:SD0_DAT5 5:SD1_DAT6 10:UART1_CTS 14:TWI1_CLK 16:PWM6 19:IISRX0_LRCLK 28: T2_CAP 29:VMIC0 OTHER: Reserved	R/W	0x0

10.4.26 **GPIO25_CTL**

GPIO25 control Register

Offset=0x68

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0

23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable	R/W	0x0

		1: Enable		
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D15 7:SPI1_MOSI 4:SD0_DAT6 5:SD1_DAT7 10:UART1_RTS 14:TWI1_DAT 16:PWM7 19:IISRX0_DIN 29:VMIC1 OTHER: Reserved	R/W	0x0

10.4.27 GPIO26_CTL

GPIO26 control Register

Offset=0x6C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when	R/W	0x0

		GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D16 4:SD0_DAT7 5:SD1_DAT1 6:SPI0_SS 9:UART0_TX 13:TWI0_CLK 16:PWM8 20:IISRX1_MCLK	R/W	0x0

		25:DMIC01_CLK 28: T3_CAP OTHER: Reserved		

10.4.28 GPIO27_CTL

GPIO27 control Register

Offset=0x70

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6	R/W	0x1

		110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D17 6:SPI0_CLK 4:SD0_DAT3 5:SD1_DAT2 9:UART0_RX 13;TWI0_DAT 16:PWM0 20:IISRX1_BCLK 25:DMIC01_DAT OTHER: Reserved	R/W	0x0

10.4.29 **GPIO28_CTL**

GPIO28 control Register

Offset=0x74

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt	R/W	0x0

		to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect		
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable.	R/W	0x0

		0: Disable 1: Enable		
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D18 4:SD0_DAT2 5:SD1_DAT3 6:SPI0_MISO 10:UART1_TX 14:TWI1_CLK 16:PWM1 20;IISRX1_LRCLK OTHER: Reserved	R/W	0x0

10.4.30 GPIO29_CTL

GPIO29 control Register

Offset=0x78

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send	R/W	0x0

		IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D19 4:SD0_DAT1 6:SPI0_MOSI 10:UART1_RX	R/W	0x0

		14:TWI1_DAT 16:PWM2 20:IISRX1_DIN 24:PDMTX_CLK OTHER: Reserved		

10.4.31 GPIO30_CTL

GPIO30 control Register

Offset=0x7C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4	R/W	0x1

		100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D20 4:SD0_CLK0 7:SPI1_SS 8:SPI2_SS 11:UART2_TX 16:PWM3 18:IISTX1_MCLK OTHER: Reserved	R/W	0x0

10.4.32 **GPIO31_CTL**

GPIO31 control Register

Offset=0x80

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt	R/W	0x0

		to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect		
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable.	R/W	0x0

		0: Disable 1: Enable		
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D21 4:SD0_CLK1 7:SPI1_CLK 8:SPI2_CLK 11:UART2_RX 16:PWM4 18:IISTX1_BCLK 24:PDMTX_DAT OTHER: Reserved	R/W	0x0

10.4.33 GPIO32_CTL

GPIO32 control Register

Offset=0x84

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send	R/W	0x0

		IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D22 4:SD0_CMD 7:SPI1_MISO 8:SPI2_MISO	R/W	0x0

		12:UART3_TX 16:PWM5 18:IISTX1_LRCLK OTHER: Reserved		

10.4.34 GPIO33_CTL

GPIO33 control Register

Offset=0x88

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5	R/W	0x1

		101: Level 6 110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D23 4:SD0_DAT0 7:SPI1_MOSI 8:SPI2_MOSI 12:UART3_RX 16:PWM6 18:IISTX1_DOUT OTHER: Reserved	R/W	0x0

10.4.35 **GPIO38_CTL**

GPIO38 control Register

Offset=0x9C

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module;	R/W	0x0

		1: Send interrupt to the INTC，when the GPIO trigger event is detect		
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable	R/W	0x0

		1: Enable		
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D4 7:SPI1_D2 10:UART1_TX 16:PWM4 17:IISTX0_MCLK 24:PDMTX_CLK 25:DMIC23_CLK 27:LRADC6 OTHER: Reserved	R/W	0x0

10.4.36 GPIO39_CTL

GPIO39 control Register

Offset=0xA0

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC.	R/W	0x0

		1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_D5 4:SD0_CLK1 7:SPI1_D3 10:UART1_RX 16:PWM5	R/W	0x0

		17:IISTX0_BCLK 24:PDMTX_DAT 25:DMIC23_DAT 27:LRADC9 OTHER: Reserved		

10.4.37 GPIO43_CTL

GPIO43 control Register

Offset=0xB0

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4	R/W	0x1

		100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 2:LCD_CE0_HSYNC 4:SD0_DAT1 7:SPI1_D2 12:UART3_CTS 14:TWI1_CLK 16:PWM5 19:IISRX0_DIN OTHER: Reserved	R/W	0x0

10.4.38 **GPIO55_CTL**

GPIO55 control Register

Offset=0XE0

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt	R/W	0x0

		to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect		
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable.	R/W	0x0

		0: Disable 1: Enable		
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 5:SD1_DAT0 7:SPI1_D7 12:UART3_TX 16:PWM7 20:IISRX1_BCLK 27: LRADC9 OTHER: Reserved	R/W	0x0

10.4.39 GPIO56_CTL

GPIO56 control Register

Offset=0XE4

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask. 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	Reserved	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable;	R/W	0x0

		Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:16	Reserved	Reserved	R	0x0
15	DNMOS	Double NMOS 0: Disable; 1: Enable;	R/W	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4:0	MFP	Multi-Function of GPIO 0:GPIO 5:SD1_DAT1 7:SPI1_DQS 12:UART3_RX 16:PWM8 20:IIS1RX_LRCLK OTHER: Reserved	R/W	0x0

10.4.40 GPIO64_CTL

GPIO64 control Register

Offset=0x104

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(MICINL/MICINLP)	R/W	0x1
3:0	Reserved	0:GPIO 1:DMIC01_CLK OTHER:Reserved	R	0x0

10.4.41 GPIO65_CTL

GPIO65 control Register

Offset=0x108

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: DMIC01_DAT 1: Analog Function(MICINR/MICINLN)	R/W	0x1
3:0	Reserved	0:GPIO 1: DMIC01_DAT OTHER:Reserved	R	0x0

10.4.42 GPIO66_CTL

GPIO66 control Register

Offset=0x10C

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(AUX0L/AUX0LP)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.43 GPIO67_CTL

GPIO67 control Register

Offset=0x110

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(AUX0R/AUX0LN)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.44 GPIO68_CTL

GPIO68 control Register

Offset=0x114

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(AUX1L/AUX0RN)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.45 GPIO69_CTL

GPIO69 control Register

Offset=0x118

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(AUX1R/AUX0RP)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.46 GPIO72_CTL

GPIO74 control Register

Offset=0x124

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(AOUTL/AOUTLP)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.47 GPIO73_CTL

GPIO75 control Register

Offset=0x128

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(VRO)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.48 GPIO74_CTL

GPIO76 control Register

Offset=0x12C

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(AOUTR/AOUTRP)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.49 GPIO75_CTL

GPIO75 control Register

Offset=0x130

Bit(s)	Name	Description	R/W	Reset
31:15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIOInput Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIOOutput Enable. 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO: 0: Disable 1: Enable	RW	0x0
4	AD_Select	GPIO Analog/Digital Select Register 0: MFP 1: Analog Function(VROS)	R/W	0x1
3:0	Reserved	0:GPIO Other: Reserved	R	0x0

10.4.50 GPIO_ODAT0

GPIO Output Data register0

Offset = 0x200

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_ODAT	GPIO[31:0] Output Data.	R/W	0x0

10.4.51 GPIO_ODAT1

GPIO Output Data register1

Offset = 0x204

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_ODAT	GPIO[63:32] Output Data.	R/W	0x0

10.4.52 GPIO_ODAT2

GPIO Output Data register2

Offset = 0x208

Bit(s)	Name	Description	R/W	Reset
31:14	-	-	R	0x0
13:0	GPIO_ODAT	GPIO[77:64] Output Data.	R/W	0x0

10.4.53 GPIO_BSR0

GPIO Output Data bit set register0

Offset = 0x210

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_BSR0	GPIO[31:0] Output Data bit set register 0: there is no effect on the corresponding GPIO_ODAT0 position. 1: the corresponding GPIO_ODAT0 bit was set to 1. And the position of the register itself is automatically cleared 0 after writing 1.	R/W	0x0

10.4.54 GPIO_BSR1

GPIO Output Data bit set register1

Offset = 0x214

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_BSR1	GPIOB[63:32] Output Data bit set register 0: there is no effect on the corresponding GPIO_ODAT1 position. 1: the corresponding GPIO_ODAT1 bit was set to 1. And the position of the register itself is automatically cleared 0 after writing 1.	R/W	0x0

10.4.55 GPIO_BSR2

GPIO Output Data bit set register2

Offset = 0x218

Bit(s)	Name	Description	R/W	Reset
31:14	-	-	R	0x0
13:0	GPIO_BSR2	GPIOB[63:32] Output Data bit set register 0: there is no effect on the corresponding GPIO_ODAT2 position. 1: the corresponding GPIO_ODAT2 bit was set to 1. And the position of the register itself is automatically cleared 0 after writing 1.	R/W	0x0

10.4.56 GPIO_BRR0

GPIO Output Data bit reset register0

Offset = 0x220

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_BRR0	GPIOA[31:0] Output Data bit reset register 0: there is no effect on the corresponding GPIO_ODAT0 position. 1: the corresponding GPIO_ODAT0 bit was set to 0. And the position of the register itself is automatically cleared 0 after writing 1.	R/W	0x0

10.4.57 GPIO_BRR1

GPIO Output Data bit reset register1

Offset = 0x224

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_BRR1	GPIOB[63:32] Output Data bit reset register 0: there is no effect on the corresponding GPIO_ODAT1 position. 1: the corresponding GPIO_ODAT1 bit was set to 0. And the position of the register itself is automatically cleared 0 after writing 1.	R/W	0x0

10.4.58 GPIO_BRR2

GPIO Output Data bit reset register2

Offset = 0x228

Bit(s)	Name	Description	R/W	Reset
31:14	-	-	R	0x0
13:0	GPIO_BRR2	GPIOB[77:64] Output Data bit reset register 0: there is no effect on the corresponding GPIO_ODAT2 position. 1: the corresponding GPIO_ODAT2 bit was set to 0. And the position of the register itself is automatically cleared 0 after writing 1.	R/W	0x0

10.4.59 GPIO_IDAT0

GPIO Input Data register0

Offset = 0x230

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_IDAT	GPIO[31:0] Input Data.	R	0x0

10.4.60 GPIO_IDAT1

GPIO Input Data register1

Offset = 0x234

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_IDAT	GPIO[63:32] Input Data.	R	0x0

10.4.61 GPIO_IDAT2

GPIO Input Data register2

Offset = 0x238

Bit(s)	Name	Description	R/W	Reset
31:14	-	-	R	0x0
13:0	GPIO_IDAT	GPIO[77:64] Input Data.	R	0x0

10.4.62 GPIO_PD0

GPIO IRQ Pending register0

Offset = 0x240

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_PD	GPIO[31:0] IRQ Pending register. ‘0’: No IRQ ‘1’: IRQ Writing 1 to the bit is clear it.	R/W	0x0

10.4.63 GPIO_PD1

GPIO IRQ Pending register1

Offset = 0x244

Bit(s)	Name	Description	R/W	Reset
31:0	GPIO_PD	GPIO[63:32] IRQ Pending register. ‘0’: No IRQ ‘1’: IRQ Writing 1 to the bit is clear it.	R/W	0x0

10.4.64 WIO1_CTL

WIO1 control Register (SVCC)

Offset=0x304

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	R	0x0
25	WIO_INTC_MSK	WIO INTC mask.	R/W	0x0

		0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the WIO trigger event is detect		
24	WIO_INTC_PD	WIO INTC Pending. 0: no pending; 1: pending Write 1 to clear	R/W	0x0
23:21	WIO_TRIG_CTL	WIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: hight level 100: low level Others: Reserved	R/W	0x0
20	WIO_INTCEN	WIO INTC Enable. 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when WIO_INTC_MSK is ‘1’.	R/W	0x0
19:17	Reserved	Reserved	R	0x0
16	WIODAT	WIO Input/Output Data.	R/W	0x0
15	Reserved	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x0
11	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	Reserved	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable. 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO 10K PU Enable.	R/W	0x0

		0: Disable 1: Enable		
7	WIOINEN	WIO Input Enable.(it needs to be enabled when it is used as WIO function) 0: Disable 1: Enable	R/W	0x0
6	WIOOUTEN	WIO Output Enable. 0: Disable 1: Enable	R/W	0x0
5	Reserved	Reserved	R	0x0
5	Reserved	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0:GPIO 1:LRADC1 2:32KHz_IN Other: Reserved	R/W	0x0

Note: the IO is SVCC domain IO, and the register is SVCC domain. the register does not power down in S3/S4 state,

11 Ordering information

Part Number	Package	Package Size	MOQ(tray)
ATJ2157	QFN68	7mm x 7mm x 0.75mm	4160 pcs

12 Appendix

12.1 Acronym and Abbreviations

BLE: Bluetooth Low Energy
HCI: Host Controller Interface
ADC: Analog-to-Digital Converter
AMIC: Analog Micphone
DMIC: Digital Micphone
RF: Radio Frequency
GPIO: General Purpose Input Output
RoHS: Restriction of Hazardous Substances
SPI: Serial Peripheral Interface
TWI: Two-Wire Interface
UART: Universal Asynchronous Receiver Transmitter
dB: Decibel
DC: Direct Current
FIR: Fast Infrared
I2S: Inter-IC Sound
IR: Infrared
IRQ: Interrupt Request
LRADC: Low Resolution ADC
PA: Power Amplifier
PLL: Phase-Locked Loop
PMU: Power Management Unit
PWM: Pulse Width Modulation
RISC: Reduced Instruction Set Computing
RTC: Real-Time Clock
SOC: System on a Chip
SPEC: Specification
THD: Total Harmonic Distortion

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