ATJ2256/ATJ2257/ ATJ2257B Datasheet

Latest Version: 1.0

2009-12-10

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Contents

Revision History

Date	Revision	Description
2009-12-10	1.0	Initial version released;

1 Introduction

1.1 Overview

ATJ2256/ATJ2257/ATJ2257B is a highly integrated 32bit RISC-based SoC for digital media solution. The RISC architecture and high speed bus controller are capable of achieving high performance with low power consumption. With a built-in JPEG co-processor, this media platform is capable of processing both JPEG and MJPEG format with higher efficiency. The integrated high-speed USB 2.0 SIE enables the platform to act as a mass storage device at the speed up to 480Mbps. The audio codec in the SoC is based on sigma-delta modulation, providing high performance with low power consumption as well as allowing the flexible adjustment of sample rates from 8k to 96k. The built-in audio codec is able to switch inputs within headphones, microphones, FM radios and direct drive for low impedance earphones.

ATJ2256/ATJ2257/ATJ2257B also provides integrated SDRAM and Flash interfaces; IIC, IR and UART etc. interfaces for changeable control and transfer modes, therefore the chips can provide a true “ALL-IN-ONE” solution that is ideally suited for highly optimized digital media devices.

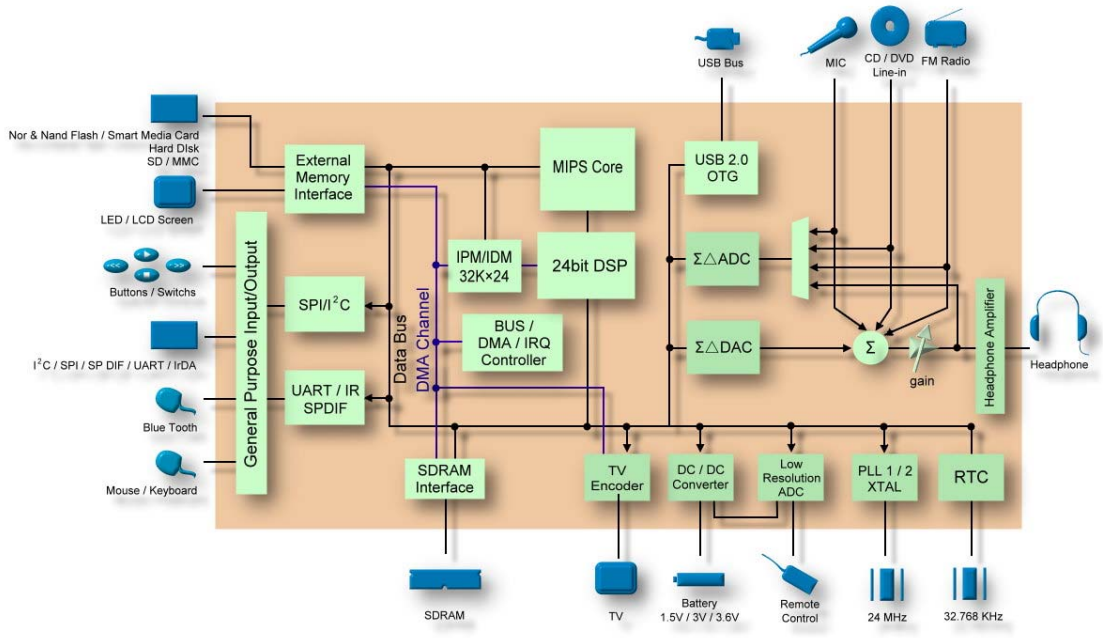
1.2 Features

- Audio playing support: WMA, OGG, APE, WAV, ASF, FLAC
- Audio recording support: WAV
- Video playing support: AMVB, XVID, WMV, FLV, MJPEG QVGA
- Image view support: JPEG, BMP, GIF, PNG
- High-speed USB 2.0 Device
- High-Speed NAND I/F
- Support SLC & MLC NAND FLASH with 8-bit Error Correction
- Support SD/MMC FLASH Card
- Support OLED, TFT, STN
- Integrated stereo DAC & ADC
- Li-Ion battery charger
- 6bit battery monitoring ADC

	ATJ2256	ATJ2257	ATJ2257B
Package	LQFP128 （14mmX14mm）	LQFP144 （20mmX20mm）	TFBGA144 （10.2mm×10.2mm）
Memory	Nand, SD/MMC	Nand, SD/MMC	Nand, SD/MMC
Display	CPU Interface LCM	TVOUT/CPU Interface LCM	TVOUT/CPU Interface LCM
Extension Interface	I2C/UART1/IR/SPI	I2C/UART1/IR/SPI	I2C/UART1&2/IR/SPI
Key-press	4×3/Remote	3×3/Remote	4×3/Remote
USB	Slave	OTG/Host/Slave	OTG/Host/Slave
CMOS sensor	Not supported	Supported	Supported
TV OUT	Supported	Supported	Supported
TV IN	Not supported	Supported	Supported
TP	External	External	External

2 Functional Block and Memory Map

2.1 Functional Block Diagram



2.2 Memory Map

Altogether 4G memory map; user mode 512M: 00000000～1FFFFFFF

Physical Memory Map			
Start	**End**	**Size（M）**	**Function**
0x00000000	0x0FFFFFFF	256	SDRAM Space
0x10000000	0x11FFFFFF	32	IO Device
0x12000000	0x13FFFFFF	32	Reserved
0x14000000	0x17FFFFFF	64	IO Device/MEM

0x18000000	0x1FFFFFFF	128	MEM (boot)
IO Map			
Start	End	Size（K）	Function
0x10000000	0x1000FFFF	64	PMU/LRADC
0x10010000	0x10017FFF	32	CMU/HOSC
0x10018000	0x1001FFFF	32	RTC/LOSC/WD
0x10020000	0x1002FFFF	64	Interrupt Controller
0x10030000	0x10037FFF	32	SRAM on Chip
0x10038000	0x1003BFFF	16	Reserved
0x1003C000	0x1003FFFF	16	32BitRisc Core Performance CNT
0x10040000	0x1004FFFF	64	Reserved
0x10050000	0x1005FFFF	64	DSP Control
0x10060000	0x1006FFFF	64	DMA Controller
0x10070000	0x1007FFFF	64	SDRAM Controller
0x10080000	0x1008FFFF	64	SPI controller
0x10090000	0x1009FFFF	64	Reserved
0x100A0000	0x100AFFFF	64	FLASH I/F
0x100B0000	0x100BFFFF	64	SD IF
0x100C0000	0x100CFFFF	64	MHA(MJPEG)
0x100D0000	0x100DFFFF	64	BT656 Port
0x100E0000	0x100EFFFF	64	USBOTG
0x100F0000	0x100FFFFF	64	YVU2RGB
0x10100000	0x1010FFFF	64	DAC＋PA
0x10110000	0x1011FFFF	64	ADC
0x10120000	0x1012FFFF	64	Reserved
0x10130000	0x1013FFFF	64	Reserved
0x10140000	0x1014FFFF	64	SPDIF
0x10150000	0x1015FFFF	64	Reserved
0x10160000	0x1016FFFF	64	UART-2
0x10160000			IR
0x10170000	0x1017FFFF	64	Reserved
0x10180000	0x1018FFFF	64	IIC
0x10190000	0x1019FFFF	64	Reserved
0x101A0000	0x101AFFFF	64	Key Scan
0x101B0000	0x101BFFFF	64	Reserved

0x101C0000	0x101CFFFF	64	GPIO
0x101D0000	0x101DFFFF	64	Reserved
0x101E0000	0x101EFFFF	64	Reserved
0x101F0000	0x101FFFFF	64	Reserved
		2048	SUM
0x10200000	0x11FFFFFF		Reserved
IO/MEM Map			
Start	**End**	**Size（K）**	**Function**
0x14000000	0x1403FFFF	256k	Reserved
0x14040000	0x1405FFFF	128k/96k	DSP mode 24bit Wide (128k) MIPS mode 32bit Wide (96k)
0x140600000	0x17FFFFFF		Reserved
MEM (LCD and LAN) Map			
Start	**End**	**Size（M）**	**Function**
0x18000000	0x18FFFFFF	16M	Reserved
0x19000000	0x19FFFFFF	16M	Reserved
0x1A000000	0x1AFFFFFF	16M	Reserved
0x1B000000	0x1BFFFFFF	16M	Reserved
0x1C000000	0x1CFFFFFF	16M	CE3 (LCD)
0x1D000000	0x1DFFFFFF	16M	CE2
0x1E000000	0x1EFFFFFF	16M	CE1
0x1F000000	0x1FFFFFFF	16M	CE0 (BROM)

3 Clock Management Unit (CMU)

The chips support two oscillator inputs: 24M and 32.768K.

Clock Management Unit (CMU) can be driven by a 24M high oscillator and a 32.768k low oscillator.

It provides:

- Four main clocks: MIPS core clock, DSP clock, AHB bus clock, APB bus clock;
- A low oscillator and a real time clock (RTC) module with alarm function.

The chips have a built-in Watch-Dog circuit.

Two 24bit timers are integrated in this IC. User may select either low or high oscillator as the source.

3.1 CMU/HOSC Register List

CMU Base Address

Block Name	Physical Base Address	KSEG1 Base Address
CMU	0x10010000	0xB0010000

HOSC/CMU Register Address

REG Name	Offset	Description
CMU_COREPLL	0x0000	Core PLL Control Register
CMU_DSPPLL	0x0004	DSP PLL Control Register
CMU_AUDIOPLL	0x0008	Audio PLL Control Register
CMU_BUSCLK	0x000C	Bus CLK Control Register
CMU_SDRCLK	0x0010	SDRAM Interface CLK Control Register
–	0x0014	Reserved
CMU_NANDCLK	0x0018	NAND Interface CLK Control Register
CMU_SDCLK	0x001C	SD Interface CLK Control Register
CMU_MHACLK	0x0020	MHA CLK Control Register
CMU_BTCLK	0x0024	BT Clk Control Register
CMU_UART1CLK	0x0028	Uart1 Clk Control Register
CMU_UART2CLK	0x002C	Uart2 CLK Control Register
CMU_DMACLK	0x0030	DMA CLK Control Register
CMU_FMCLK	0x0034	FM CLK Control Register

–	0x0038	Reserved
CMU_DEVCLKEN	0x0080	Device CLK Enable Control Register
CMU_DEVRST	0x0084	Device Reset Control Register

3.1.1 CMU_COREPLL

Core PLL Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9:8	CPBI	Core PLL Bias	RW	0
7	CPEN	Core PLL Enable 0: Disable, 1: Enable	RW	0
6	HOEN	High Oscillator Enable. 0: Disable, 1: Enable	RW	1
5:0	COREPLLCLK	Core PLL Clock Control Formula: 6M* CPCK, Range: 12~ 378M, Definition: 6M If CPCK is less than 0x02, the Core PLL will be unstable. DPCK value must be more than 0x02.	RW	0

3.1.2 CMU_DSPPLL

DSP PLL Control Register

Offset=0x0004

Bit	Name	Description	RW	Reset
31:9	-	Reserved	R	0
8:7	DPBI	DSP PLL Bias	RW	0
6	DPEN	DSP PLL Enable 0: Disable, 1: Enable	RW	0

5:0	DSPPLLCLK	DSP PLL Clock Control Formula: 6M* DPCK, Range:12~378M, Definition: 6M DPCK value must be more than 0x02.	RW	0

3.1.3 CMU_AUDIOPLL

Audio PLL Control Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:13	-	Reserved	RW	0
12	SRSEL	Audiopll 44.1kHz series Div Ratio selection: 0: 24M×32/34 1: 24M×47/50	RW	0
11	ADCPLL	Audio PLL CLk Control, 0: 24.576M 1: 22.5792M	RW	0
10:8	ADCCLK	ADC Clock Divisor, output is FS*256 PLL CLK: 24.576M, 22.5792M 000:/1 96k 000: useless 001:/2 48k 001: 44.1k 010:/3 32k 010: useless 011:/4 24k 011: 22.05k 100:/6 16k 100: useless 101:/8 12k 101:11.025k 110:/12 8k 110: Useless 111: Reserved 111: Useless		0
7	-	Reserved	R	0
6:5	APBI	Audio PLL Bias	RW	0
4	APEN	Audio PLL Enable 0: Disable, 1: Enable	RW	0
3	DACPLL	DAC PLL CLk Control, 0: 24.576M 1: 22.5792M	RW	0

2:0	DACCLK	DAC Clock Divisor, output is FS*256 PLL CLK: 24.576M, 22.5792M 000:/1 96k 000: useless 001:/2 48k 001:44.1k 010:/3 32k 010: useless 011:/4 24k 011:22.05k 100:/6 16k 100: useless 101:/8 12k 101: 11.025k 110:/12 8k 110: useless 111: reserved 111: useless	RW	0

Note:

1. AUDIOPLLCLK maps to DSP port 3FEE DAC_FREQ_SELECT and ADC_FREQ_SELECT field. The other field will be changed when operating one of these fields,
2. DSP & MIPS can both operate ADCCLK & DACCLK. The latter operation will decide register's value.

3.1.4 CMU_BUSCLK

Bus CLK Control Register

Offset=0x000C

Note: it may take a while before MCU Clock Changes. When the MCU clock is DC_En, there are several ways to recover the clock to non-divided LOSC clock (32kHz) source:

1. Push Reset button
2. POWER ON RESET
3. Key Board IRQ
4. Alarm IRQ
5. SIRQ
6. USB wake up IRQ

Bits	Name	Description	R/W	Reset
31	KEYE	Key Wakeup Enable	R/W	0
30	ALME	Alarm Wakeup Enable	R/W	0
29	SIRE	SIRQ Wakeup Enable	R/W	0
28	-	Reserved	R/W	0
27	USBE	Usb Wakeup Enable	R/W	0
26:12	-	Reserved	R	0

11:8	PCLKDIV	Peripheral CLK Divisor Div 2~16 0, 1: /2 2: /3 3: /4 ..... 15: /16	RW	0
7:6	CORECLKS	Core Clock Selection 00: 32.768k 01: 24M 10: Core_Clk 11: DSP PLL	RW	01
5:4	SCLKDIV	System CLK Divisor 0 0 /1 0 1 /2 1 0 /3 1 1 /4 Duty 50%	RW	0
3:2	CCLKDIV	CPU Clock Divisor 0 0 /1 (default) 0 1 /2 1 0 /3 1 1 /4 duty 50%	RW	0
1	DCEN	Core CLK DC Enable 1: enable DC When set 1, Core_Clk equal DC.	RW	0
0	—	Reserved	R	0

3.1.5 CMU_SDRCLK

SDRAM Interface CLK Control Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:2	-	Reserved	R	0

1:0	SDRDIV	SDRAM Clock Divisor 0 0 /1 (default) 0 1 /2 1 0 /3 1 1 /4	RW	0

3.1.6 CMU_NANDCLK

NAND Interface CLK Control Register

Offset=0x0018

Bit	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3:0	NANDDIV	NAND Interface Clock Division 0: /1 1: /2 2: /3 ..... 15: /16	RW	0

3.1.7 CMU_SDCLK

SD Interface CLK Control Register

Offset=0x001C

Bit	Name	Description	R/W	Reset
31:6	-	Reserved	R	0
5	CKEN	SD Interface Clock Enable 1: Enable 0: Disable	RW	0
4	D128	Enable Divide 128 circuit 1: Enable Div 128 0: Disable Div 128	RW	0

3:0	SDDIV	SD Interface Clock Divisor 0: /1 1: /2 2: /3 ..... 15: /16	RW	0

3.1.8 CMU_MHACLK

MHA CLK Control Register

Offset=0x0020

Bit	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3:0	MHADIV	MHA Clock Divisor 0: /1 1: /2 2: /3 ..... 15:/16	RW	0

3.1.9 CMU_BTCLK

BT Clk Control Register

Offset=0x0024

Bits	Name	Description	R/W	Reset
31..6	-	Reserved	R	0
5..4	BTCSSEL	BT Interface Clock Source Selection 0: Core_Clk 1: D_CLK 2: HOSC 3: reserved	RW	0
3..0	BTDIV	BT Clock Division 0: /1 1: /2 2: /3 ..... 15:/16	R	0

3.1.10 CMU_UARTxCLK

Uart1 Clk Control Register
Offset=0x0028
Uart2 Clk Control Register
Offset=0x002C

Bit	Name	Description	R/W	Reset
31:17	-	Reserved	R	0
16	UxEN	Uartx Clock Enable 1: Enable 0: Disable	RW	0
15:0	UARTxDIV	Uartx Clock Divisor Uartx_CLK*8=C_CLK/(UARTxDIV +1)	RW	0

3.1.11 CMU_DMACLK

DMA CLK Control Register
Offset=0x0030

Bit	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3	D7EN	DMA 7 (Special Channel) Clock Enable 1: Enable 0: Disable	R/W	0
2	D6EN	DMA 6 (Special Channel) Clock Enable 1: Enable 0: Disable	R/W	0
1	D5EN	DMA 5 (Special Channel) Clock Enable 1: Enable 0: Disable	R/W	0
0	D4EN	DMA 4 (Special Channel) Clock Enable 1: Enable 0: Disable	R/W	0

NOTE: DMA controller bus clock control bit is in CMU_DEVCLEEN register

3.1.12 CMU_FMCLK

FM CLK Control Register

Offset= 0x0034

Bits	Name	Description	R/W	Reset
31..6	-	reserved	R	0
5	BCKE	PWM Back Light clock Enable 0:disable 1:enable	RW	0
4	BCKS	Back Light CLK source select 0:LOSC 32k 1:HOSC/8 3M	RW	0
3:2	BCKCON	Divided PWM Back Light Special Clock Control LOSC HOSC/8 00: 32k 3M 01: 16k 1.5M 10: 8k 750k 11: 4k 375k	RW	0
1	CLKS	FM Clock Output Selection 0:32.768k 1:24M	RW	00
0	OUTE	FM Clock Output Enable(From Test Pin) 1:Enable test pin output Clock 0:Disable test pin output	RW	00

Note: Test pin can be configured to output oscillator clock 32k or 24M.

When OUTE is set to 0, test pin has the “test” function. When it is set to 1, test pin has the clock out function.

3.1.13 CMU_DEVCLKEN

Device CLK Control Register

Offset=0x0080

Bits	Name	Description	R/W	Reset
31..27	-	Reserved	R	0
26	GPIO	GPIO control reg clock enable. Switch APB clock	RW	0

25	Key	KEY control reg clock enable. Switch APB clock.	RW	0
24	SPI	SPI control reg clock enable. Switch AHB clock.	RW	0
23	IIC	IIC control reg clock enable. Switch APB clock.	RW	0
22	UART	UART control reg clock enable. Switch APB clock and UART special clock.	RW	0
21	-	Reserved	RW	0
20	SPDF	SPDIF control reg clock enable. Switch APB clock and Audio special clk.	RW	0
19	__	Reserved	RW	0
18	ADC	ADC control reg clock enable. Switch APB clock and Audio special clk.	RW	0
17	DAC	DAC control reg clock enable. Switch APB clock and Audio special clk.	RW	0
16	DSPC	DSP control reg clock enable. Switch APB clock and dsp special clk.	RW	0
15	-	Reserved	RW	0
14	MHA	MHA interface clock enable. Switch AHB clock and MHA special clk.	RW	0
13	USBC	USB Controler interface clock enable. Switch AHB clock.	RW	0
12	BT	BT656 interface clock enable. Switch AHB clock and Bt656 special clk.	RW	0
11	SD	SD interface clock enable. Switch AHB clock and SD special clk.	RW	0
10	–	Reserved	RW	0
9	NAND	Nand Flash interface clock enable. Switch AHB clock and FLASH special clk.	RW	0
8	DMAC	DMA control block clock enable Switch AHB clock and DMAC clock.	RW	0
7	–	Reserved	RW	0
6	SDRM	SDRAM mem block clock enable. Switch AHB Clock And sdram special clk.	RW	0
5	SDRC	Sdram Control reg clock enable Switch AHB Clock.	RW	0

4	DSPM	Dsp mem block clock enable Switch AHB clock	RW	1
3	-	Reserved	R	0
2	RMOC	Sram on chip Control reg clcok enable Switch AHB clock.	RW	1
1	YUV	YUV2RGB block clock enable. Switch AHB clock.	RW	0
0	–	Reserved	RW	1

NOTE: Some other clocks are always on, including APB_En (APB bridge clock), PMU_En, CMU_En, RTC_En, INTC_En.

3.1.14 CMU_DEVRST

Device Reset Control Register

Offset＝0x0084

Bits	Name	Description	R/W	Reset
31	-	Reserved	R	1
30	GPIO	GPIO control Block reset	RW	1
29	Key	KEY control Block reset.	RW	1
28	SPI	SPI Block reset.	RW	1
27	IIC	IIC control Block reset.	RW	1
26	UART	UART control Block reset.	RW	1
25	-	Reserved	RW	1
24	SPDF	SPDIF control reg Block reset.	RW	1
23	_	Reserved	RW	1
22	ADC	ADC control Block reset k.	RW	1
21	DAC	DAC control Block reset	RW	1
20	DSPC	DSP control block reset.	RW	1
19	INTC	Interrupt control Reset	RW	1
18	RTC	RTC block Reset	RW	1
17	PMU	PMU block Reset	RW	1
16..15	-	Reserved	R	1
14	OTG	OTG PHY reset		
13	DSPM	SRAM dspmem reset	RW	1
12	TVEC	TVENC reset	RW	1

11	YUV	YUV2RGB block Reset.	RW	1
10	-	Reserved	RW	1
9	USB	USB interface Reset	RW	1
8	BT	BT656 interface Reset.	RW	1
7	MHA	MHA interface Reset.	RW	1
6	SD	SD interface Reset.	RW	1
5	NAND	Flash interface Reset.	RW	1
4	–	Reserved	RW	1
3	DMAC	DMA control block Reset	RW	1
2	–	Reserved	RW	1
1	-	Reserved	RW	1
0	SDR	Sdram Control Reg and sdram block Reset,	RW	1

Note: Write '0' to reset the block

3.2 RTC/LOSC/Watch Dog/Timers Block Description

The chips have a low frequency oscillator, which can choose a built-in source or an external one. Meanwhile the chip also has RTC (Real Time Clock) with alarm IRQ. The alarm IRQ can wake up the system. For this purpose, the chip also has the watch dog circuit.

There are two Timers, namely, Timer0 and Timer1, which can only count down. The clock of the Timer is P_Clk.

3.3 RTC/LOSC/Watch Dog Register List

RTC Base Address

Name	Physical Base Address	KSEG1 Base Address
RTC	0x10018000	0xB0018000

HOSC/CMU Register Address

Control Register Name	Offset Address	Description
RTC_CTL	0x0000	RTC Control Register
RTC_DHMS	0x0004	RTC Day Hour Minute and Second Register
RTC_YMD	0x0008	RTC Year Month Date Register

RTC_DHMSALM	0x000C	RTC Day Hour Minute and Second Alarm Register
RTC_YMDALM	0x0010	RTC Year Month Date Alarm Register
RTC_WDCTL	0x0014	RTC Watch Dog Control register
RTC_T0CTL	0x0018	RTC Timer0 Control register
RTC_T0	0x001C	RTC Timer0 Value
RTC_T1CTL	0x0020	RTC Timer1 Control register
RTC_T1	0x0024	RTC Timer1 Value

NOTE 1: When reading Register DAY_HOUR_MIN_SEC, YEAR_MON_DATE YEAR_MON_DATE, the program can get the real value until reading the same value for 3 successive times.
NOTE 2: When setting the RTC, WD, COUNT0/1, the program shall disable the corresponding enable bit at first and then enable it after setting the value.

3.3.1 RTC_CTL

RTC Control Register
Offset=0x0000

Bit	Name	Description	R/W	Reset
31..12	-	Reserved	R	0
11	RST	RTC Reset 1: Normal 0: Reset	RW	1
10	-	Reserved	RW	0
9	LEAP	RTC Leap Year bit 1: leap year 0: non leap year	R	1
8:7	–	Reserved.	RW	0
6	EOSC	External Crystal OSC enable, 0: Disable, 1: Enable	RW	1
5	CKSS	Low Frequency Clock Source Select, 0: Built-in OSC (about 32K), 1: External Crystal OSC	RW	0
4	RTCE	RTC Enable, 0: Disable, 1: Enable	RW	1
3	2HIE	2Hz IRQ Enable 0: Disable, 1: Enable	RW	0

2	ALIE	Alarm IRQ Enable, 0: Disable, 1: Enable (POR- RESET)	RW	0
1	2HIP	2Hz IRQ Pending bit, writing 1 to this bit will clear it	RW	0
0	ALIP	Alarm IRQ Pending bit (POR- RESET),writing 1 to this bit will clear it	RW	0

Note: To changing RTC register, it must set RTCE to "0" first and then set it back to "1". Alarm Irq in order to wake the system.

3.3.2 RTC_DHMS

RTC Day Hour Minute and Second Register

Offset=0x0004

Bit	Name	Description Binary code	R/W	Reset
31:27	-	Reserved	R	0
26:24	DAY	01H-07H	RW	-
23:21	-	Reserved	R	0
20:16	HOUR	00H-17H	RW	-
15:14	-	Reserved	R	0
13:8	MIN	00H-3BH	RW	-
7:6	-	Reserved	R	0
5:0	SEC	00H-3BH	RW	-

Note: This register is reset by RST bit in RTC_Con Register.

3.3.3 RTC_YMD

RTC Year Month Date Register

Offset=0x0008

Bit	Name	Description Binary code	R/W	Reset
31	-	Reserved	R	0
30:24	CENT	00H-63H	RW	-
23	-	Reserved	R	0

22:16	YEAR	00H-63H	RW	-
15:12	-	Reserved	R	0
11:8	MON	01H-0CH	RW	-
7:5	-	Reserved	R	0
4:0	DATE	01H-1FH	RW	-

Note: It can detect the leap year and month.

This register is reset by RST bit in RTC_Con Register.

3.3.4 RTC_DHMSALM

RTC Day Hour Minute and Second Alarm Register

Offset=0x000C

Bit	Name	Description Binary code	R/W	Reset
31:21	-	Reserved	R	0
20:16	HOURAL	00H-17H	RW	-
15:14	-	Reserved	R	0
13:8	MINAL	00H-3BH	RW	-
7:6	-	Reserved	R	0
5:0	SECAL	00H-3BH	RW	-

3.3.5 RTC_YMDALM

RTC Year Month Date Alarm Register

Offset=0x0010

Bit	Name	Description Binary code	R/W	Reset
31:23	-	Reserved	R	0
22:16	YEARAL	00H-63H	RW	-
15:12	-	Reserved	R	0
11:8	MONAL	01H-0CH	RW	-
7:5	-	Reserved	R	0
4:0	DATEAL	01H-1FH	RW	-

3.3.6 RTC_WDCTL

RTC Watch Dog Control Register

Offset=0x0014

Bit	Name	Description	R/W	Reset
31:7	-	Reserved	R	0
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select. 0: Irq, 1: Reset-. 1: Send Reset signal when watchdog overflow. 0: Send IRQ signal when watchdog overflow.	RW	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot.	RW	0
3:1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length 000 1 KHz 176 ms 001 512 Hz 352 ms 010 128 Hz 1.4 s 011 32 Hz 5.6 s 100 8 Hz 22.2 s 101 4 Hz 45 s 110 2 Hz 90 s 111 1 Hz 180 s	RW	0
0	CLR	Clear bit, writing 1 to clear WD timer; it is cleared automatically.	RW	0

3.3.7 RTC_T0CTL

RTC Timer0 Control Register

Offset=0x0018

Bit	Name	Description	R/W	Reset
31:6	-	Reserved	R	0
5	EN	Timer 0 Enable 0: Disable, 1:Enable	RW	0
4:3	-	Reserved	R	0

2	RELO	Timer 0 Reload. 0: Not reload,1:Reload	RW	0
1	ZIEN	Timer0 Zero IRQ Enable When this bit is enabled, TIMER0_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The Count only can count down. When the count is zero, IRQ will be sent.

3.3.8 RTC_T0

RTC Timer0 value Register

Offset=0x001C

Bit	Name	Description	R/W	Reset
31:24	–	Reserved	R	0
23:0	T0	Read or write current Timer0 value	RW	-

3.3.9 RTC_T1CTL

RTC Timer1 Control Register

Offset=0x0020

Bit	Name	Description	RW	Reset
31:6	-	Reserved	R	0
5	En	Timer0 Enable 0: Disable,1:Enable	RW	0
4:3	-	Reserved	R	0
2	RELO	Timer1 Reload 0: Not reload,1:Reload	RW	0
1	ZIEN	Timer1 Zero IRQ Enable When this bit is enabled, TIMER1_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The Count can only count down. When count becomes zero, IRQ will be sent.

3.3.10 RTC_T1

RTC Timer1 Value

Offset=0x0024

Bit	Name	Description	R/W	Reset
31:24		Reserved		
23:0	T1	Read or write current Timer1 value	RW	0

4 Interrupt Controller

4.1 Interrupt Controller Description

Interrupt controller supports 32 interrupt sources. It can generate five outputs as interrupt requests 0, 1, 2, 3 and 4. Each of these outputs is connected to CPU core; the following table shows the interrupt controller's connections to CPU.

Table 1: Interrupt Controller Connects to CPU

Interrupt Controller Requests	CPU Interface	CPU Interrupt Request
Request 0	SI_INT[0]	IP2
Request 1	SI_INT[1]	IP3
Request 2	SI_INT[2]	IP4
Request 3	SI_INT[3]	IP5
Request 4	SI_INT[4]	IP6

Table 2: Interrupt Sources

Interrupt Number	Sources	Type
0	Reserved	High Level
1	Reserved	High Level
2	SD/MMC	High Level
3	MHA	High Level
4	USB	High Level
5	DSP	High Level
6	BT656	High Level
7	PC (Performance Counter)	High Level
8	2Hz/WatchDog	High Level
9	TIMER1	High Level
10	TIMER0	High Level
11	RTC	High Level
12	DMA	High Level
13	Key	High Level
14	External	High Level
15	Reserved	High Level

16	SPI	High Level
17	IIC2	High Level
18	IIC1	High Level
19	UART2	High Level
20	UART1	High Level
21	ADC	High Level
22	DAC	High Level
23	SPDIF	High Level
24	NAND	High Level
25	Reserved	High Level
26	YUV2RGB	High Level
27	Reserved	High Level
28	Reserved	High Level
29	Reserved	High Level
30	Reserved	High Level
31	Reserved	High Level

4.2 Interrupt Controller Register List

Table 3: INTC Base Address

Name	Physical Base Address	KSEG1 Base Address
INTC	0x10020000	0xB0020000

Table 4: INTC Register Address

Register Name	Offset	Description
INTC_PD	0x0000	Interrupt Pending register
INTC_MSK	0x0004	Interrupt Mask register
INTC_CFG0	0x0008	Interrupt Config register 0
INTC_CFG1	0x000C	Interrupt Config register 1
INTC_CFG2	0x0010	Interrupt Config register 2
INTC_EXTCTL	0x0014	External Interrupt control and status register

4.2.1 INTC_PD

Interrupt Pending Register.

CPU can access to the status of interrupt sources by read this register.

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:0	INTC_PD[n]	Interrupt Pending bit. Interrupt name “n” is in accordance with the Interrupt **Sources Table.** 0: Interrupt source n request is not active; 1: Interrupt source n request is active.	R	0

4.2.2 INTC_MSK

Interrupt MASK Register. CPU can enable or disable by writing this register.

Offset=0x0004

Interrupt Mask.

0: Interrupt is disabled.

1: Interrupt is enabled.

Bit	Name	Description	R/W	Reset
31:27	-	Reserved	R	0
26	YUV	YUV2RGB Interrupt Mask Bit	RW	0
25	–	Reserved	RW	0
24	NAND	NAND Interface Interrupt Mask Bit	RW	0
23	SPDF	SPDIF Interface Interrupt Mask Bit	RW	0
22	DAC	DAC Interrupt Mask Bit	RW	0
21	ADC	ADC Interrupt Mask Bit	RW	0
20	URT1	URT1 Interrupt Mask Bit	RW	0
19	URT2	URT2 Interrupt Mask Bit	RW	0
18	IIC1	IIC1 Interrupt Mask Bit	RW	0
17	IIC2	IIC2 Interrupt Mask Bit	RW	0
16	SPI	SPI Interrupt Mask Bit	RW	0
15	–	Reserved	RW	0
14	EXT	External IRQ Interface Interrupt Mask Bit	RW	0
13	KEY	KEY Interrupt Mask Bit	RW	0
12	DMA	DMA Interrupt Mask Bit	RW	0
11	RTC	RTC Interrupt Mask Bit	RW	0
10	T0	T0 Interrupt Mask Bit	RW	0
9	T1	T1 Interrupt Mask Bit	RW	0
8	WD	Watchdog Interrupt Mask Bit/2Hz	RW	0
7	PCNT	Performance Count Interrupt Mask Bit	RW	0
6	BT	BT Interrupt Mask Bit	RW	0
5	DSP	DSP Interrupt Mask Bit	RW	0

4	USB	USB Interrupt Mask Bit	RW	0
3	MHA	MHA Interrupt Mask Bit	RW	0
2	SD	SD Interface Interrupt Mask Bit	RW	0
1	–	Reserved	RW	0
0	-	Reserved	RW	0

4.2.3 INTC_CFGx

Interrupt Config Registers. CPU can assign any interrupt source to one of the five interrupt requests.

INTC_CFG0: Offset=0x0008 INTC_CFG1: Offset=0x000C

INTC_CFG2: Offset=0x0010

INTC_CFGx List

INTC_CFG2[n]	0	0	0	0	1
INTC_CFG1[n]	0	0	1	1	x
INTC_CFG0[n]	0	1	0	1	x
The interrupt request assigned	0	1	2	3	4

Bit	Name	Description	R/W	Reset
31:27	-	Reserved	R	0
26	YUV	YUV2RGB Interrupt CFGx Bit	RW	0
25	–	Reserved	RW	0
24	NAND	NAND Interface Interrupt CFGx Bit	RW	0
23	SPDF	SPDIF Interface Interrupt CFGx Bit	RW	0
22	DAC	DAC Interrupt CFGx Bit	RW	0
21	ADC	ADC Interrupt CFGx Bit	RW	0
20	URT1	URT1 Interrupt CFGx Bit	RW	0
19	URT2	URT2 Interrupt CFGx Bit	RW	0
18	IIC1	IIC1 Interrupt CFGx Bit	RW	0
17	IIC2	IIC2 Interrupt CFGx Bit	RW	0
16	SPI	SPI Interrupt CFGx Bit	RW	0
15	–	Reserved	RW	0
14	EXT	External IRQ Interface Interrupt CFGx Bit	RW	0
13	KEY	KEY Interrupt CFGx Bit	RW	0
12	DMA	DMA Interrupt CFGx Bit	RW	0

11	RTC	RTC Interrupt CFGx Bit	RW	0
10	T0	T0 Interrupt CFGx Bit	RW	0
9	T1	T1 Interrupt CFGx Bit	RW	0
8	WD	WatchDog Interrupt CFGx Bit/2Hz	RW	0
7	PCNT	Performance Count Interrupt CFGx Bit	RW	0
6	BT	BT Interrupt CFGx Bit	RW	0
5	DSP	DSP Interrupt CFGx Bit	RW	0
4	USB	USB Interrupt CFGx Bit	RW	0
3	MHA	MHA Interrupt CFGx Bit	RW	0
2	SD	SD Interface Interrupt CFGx Bit	RW	0
1	–	Reserved	RW	0
0	-	Reserved	RW	0

4.2.4 INTC_EXTCTL

External Interrupt Control and Status Register.

Offset=0x0014

Bits	Name	Description	Read/Write	Reset
31:27	-	Reserved	R	0
26:25	E1TYPE	External Interrupt 1 Type 00 High level active. 01 Low level active. 10 rising edge-triggered. 11 Falling edge-triggered.	RW	00
24	E1EN	Enable External interrupt 1 0 Disable 1 Enable	RW	0
23:17	-	Reserved	R	0
16	E1PD	External Interrupt 1 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 1 is edge-triggered, this bit must be cleared by software after detected.	R/W	-

15:11	E0TYPE	External interrupt 0 type 00 High level active. 01 Low level active. 10 rising edge-triggered. 11 Falling edge-triggered.	R/W	0
10:8	E0EN	Enable external interrupt 0 0 Disable 1 Enable	R/W	0
7:1	-	Reserved.	R	0
0	E0PD	External Interrupt 0 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 0 is edge-triggered, this bit must be cleared by software after detected.	R/W	0

5 PMU/DC-DC Converter

5.1 Description

The PMU includes:

- ATJ2256 & ATJ2257B have only one DC/DC converter working in buck & boost mode. Their output voltage is 1.6V, which can be programmed. For ATJ2257, it has two DC/DC converters; both can work in buck mode, and the output voltages are 3.1V and 1.6V, and programmable.
- Two regulators, whose output voltages are 3.1V and 1.6V, can be programmed.
- A bias current generator.
- An Oscillator, outputs a 600KHz for DC-DC converters and a 32KHz for RTC.
- 6bits low speed ADC, whose input range is from 0V to 3.1V，monitors remote control signal.
- Battery charger, all support Li+ battery
- VCC voltage detector, VDD voltage detector, Power OK signal (PWROK) generator.

PIN in PMU

- DC-DC1 PIN: LX_VCC, IO_VCC. (for ATJ2257 only)
- DC-DC2 PIN: LX_VDD, IO_VDD.
- High voltage regulator input and output PIN: respectively DC5V and VCC.
- Low voltage regulator output PIN: VDD
- Battery input/output PIN: BAT
- DC-DC NMOS ground: PGND
- Remote controller ADC Input: REM_CON
- ECL PFM DC/DC PIN: BL_NDR
- External power PIN: VCCOUT

PMU Working Mode

- Li+ Battery, 2 Inductor (for ATJ2257 only)
- Li+ Battery, 1 Inductor for VDD
- Li+ Battery, No Inductor
- External power

5.2 Register List

CMU Block Base Address

Module name	Physical Bass Address	KSEG1 Base Address
PMU	0x10000000	0xB0000000

Configuration Registers Offset

Offset	Register Name	Description
0x00	PMU_CTL	PMU Control Register
0x04	PMU_LRADC	PMU Low Resolution ADC Register
0x08	PMU_CHG	PMU Charge Control Register
0x40	PMU_USBPDR	USB Power Detect Register

5.3 Register Description

5.3.1 PMU_CTL

DC/DC Converter and Regulator's register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31	LBRM	Low Battery Reset Mask bit LB_ mask, "1",OPEN	R/W	1
30:28	VCVS	VCC Voltage Set Register 3.3V* 111 3.2V 110 3.1V 101 3.0V 100 2.9V 011 2.8V 010 2.7V 001 2.6V 000	R/W	0x7
27	LBNM	Low Battery Non-masked Interrupt Mask bit LBNMI_ mask, "1", OPEN	R/W	1
26:24	VDVS[3:1]	VDD Voltage Set Register 2.0V 111 1.9V 110	R/W	0x5

		1.8V* 101 1.7V 100 1.6V 011 1.5V 010 1.4V 001 1.3V 000		
23	VCDE	VCC Detect Enable “1”, enable	R/W	0
22:20	VCVD	VCC Voltage Detect Register 111 2.9V 110 2.8V 101 2.7V 100 2.6V 011 2.5V 010 2.4V 001 2.3V 000 2.2V	R/W	0x5
19	VDDE	VDD Detect Enable “1”, enable	R/W	0
18:16	VDVD	VDD voltage Detect Register 1.8V 111 1.7V 110 1.6V 101 1.5V 100 1.4V 011 1.3V 010 1.2V 001 1.1V 000	R/W	0x3
15	-	Reserved	R/W	0
14	VCOE	VCCOUT Enable 1: Enable 0: Disable	R/W	0
13	BATADC	BATADC Enable 1: Enable 0: Disable	R/W	0
12	REMADC	REMADC Enable 1: Enable 0: Disable	R/W	0
11:10	IBIAS	Current bias control	R/W	0x2

		00: 0.92uA 01: 0.96uA 10: 1.0uA 11: 1.04uA		
9:8	OSCFREQ	PMU Oscillator Frequency Set Freq. Current 00 470KHz 1.5uA 01 600kHz 2.0uA 10 750kHz 2.5uA 11 880kHz 3.0uA	R/W	0x1
7	DC1M	DCDC1 Mode 1:PWM 0:PFM	R/W	1
6	DC2M	DCDC Mode 1: PWM 0: PFM	R/W	1
5-3	BLCS	Back Light Current Set BLCS[3..0] BL_FB 0000 0.4V 0001 0.39 0010 0.38 0011 0.37 0100 0.36 0101 0.35 0110 0.34 0111 0.33 1000 0.32 1001 0.31 1010 * 0.30 1011 0.29 1100 0.28 1101 0.27 1110 0.26 1111 0.25 BLCS[3..1] is mapped PMU_CTL [5..3] BLCS[0] is mapped PMU_CHG[6]	R/W	0x101
2	VDV0	VDD Voltage Set bit0 1: +50mV for VDD	R/W	0
1:0	PWRM	Power Mode	R	0x3

		1*—Li+ Note: bit0 for test		

5.3.2 PMU_LRADC

Low Resolution ADC Data Register

Offset=0x0004

Bits	Name	Descriptions	R/W	Reset
31	DC5V	DC5V available for charge. 1:available 0:unavailable	R	0
30	RemADC_Average	RemADC Average slect 0—— no average 1—— 2 times average	R/W	0
29-28	RemADCSample	Remote ADC sample frequency select 00——64Hz 01——128Hz 10——256Hz 11——512Hz	R/W	00
27-22	REMOADC6	Remote Control 6bit Voltage ADC Range:0-AVCC	R	x
21-16	BATADC6	Battery 6bit Voltage ADC Range: Li+:2.1-4.5V	R	-
15-14	—	Reserved	R	0
13-8	—	Reserved	R	-
7-0	—	Reserved	R	0

5.3.3 PMU_CHG

PMU Charger Control and Status register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31	EN	Enable Charge Circuit 1: Enable charge circuit 0: Disable charge circuit. Charge circuit will not	R/W	0

		work, and consume little power.		
30-28	CURRENT	Charge Current Configure 000:50mA 001:100mA 010:150mA 011:200mA 100:250mA 101*:300mA 110:400mA 111:500mA	R/W	0x5
27	STAT	Charging Status. 0: not charging, 1: charging.	R	0
26-25	CHGPHASE	Charging phase 00 Reserved 01 Pre-charging 10 Constant current 11 Constant voltage The two bits will be available only when bit 31 of this register is set, or will be always read 00.	R	00
24	—	Reserved	R/W	0x1
23:20	–	Reserved	R/W	0
19-16	–	Reserved	R/W	1
15	PBLS	PWM OR BL_NDR select 0: BL_NDR output 1: PWM pulse output	R/W	0
14	PPHS	PWM FHASE SELECT, this bit in effect only when PBLS is 1 0: LOW IS SELECT 1: HIGH IS SELECT	R/W	0
13	-	reserved	R/W	0
12-8	PDUT	PWM Back Light Duty 00000 0/32 00001 1/32 00010 2/32 . 11110 30/32 11111 31/32	R/W	01111
7	-	reserved	R/W	0

6	BLC0	Back Light Current Set bit 0	R/W	0
5-4	TMPSET	Temperature Monitor's Maxim Temperature Setting: 55C 11 50C 10 45C * 01 40C 00	R/W	1
3-2	LBNMIVS	Low Battery Non-mask Interrupt Voltage Setting Li+ 00* 2.9V 01 3.1V 10 3.3V 11 3.5V	R/W	0
1-0	LBRVS	Low Battery Reset Voltage setting Li+ 00 2.7V 01 2.9V 10 3.1V 11 3.3V	R/W	1

5.3.4 PMU_USBPDR

USB Power Detect Register

offset: 0x0040

Bits	Name	Description	R/W	Reset
31:12	-	reserved	R/W	0
11	bvalid	USB bvalid. When vbus is higher than 1.65V, this signal is 1.	R	x
10	vbus	Vbusvalid. The vbus detection threshold is determined by vbusth, when vbus is higher than threshold, vbusvalid will be 1.	R	x
9:8	ls	USB linestate[1:0].	R	x
7:4	-	reserved	R/W	0
3	dmpuen	500Kohm DM pull up resistor enable.	R/W	0
2	dppuen	500Kohm DP pull up resistor enable.	R/W	0
1	dmpddis	DM pull down disable.	R/W	0

0	dppddis	DP pull down disable.	R/W	0

This register used for USB vbus detection threshold setting, and charger/USB Host detection.

According to USB specification, USB host should supply VBUS, the voltage should be 4.75V~5.25V, and USB function should work only if VBUS is higher than 4.4V (for bus powered USB function). However, in this application, some exception may happen. For example, some host cannot supply VBUS voltage between 4.75V~5.25V, or VBUS ripple is over specification; in these cases, adjustable VBUS detection threshold will promote the compliance of USB function.

Another application requirement is that the firmware shall be notified whether it is connecting to a USB host or a USB charger. To achieve this, assuming the firmware enabled vbus wakeup function, then once vbus wakeup interrupt happens, it shows a USB host or a USB charger connecting to us. The firmware disables DP and DM pulldown, and enables DP/DM 500Kohm pullup, then check linestate[1:0] status, if 00, it is connecting to a USB Host, otherwise, to a charger.

6 32-BIT RISC Core

The core follows MIPS 4KEc SPEC. This Chapter describes the features of RISC Core which are not implemented or different from MIPS 4KEc SPEC.

6.1 Coprocessor 0 Description

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostics capability, the operating modes (kernel, user, and debug), and whether interrupts are enabled or disabled.

7 SDRAM Interface

7.1 SDRAM Interface Description

SDRAM interface can support both SDRAM (Synchronous DRAM) and Mobile SDRAM. It has the following features:

- Supports SDRAM and Mobile SDRAM
- Separate I/O power supply supporting 1.8V, 2.5V and 3.3V
- Supports 3.3V SDRAM of clock frequency up to PC100
- Supports 3.3V SDRAM of capacity up to 512Mbits
- Supports 3.3V/2.5V/1.8V Mobile SDRAM of Clock frequency up to PC100
- Supports 3.3V/2.5V/1.8V Mobile SDRAM of capacity up to 512Mbits
- Thirteen address signals and two bank address signal
- Access to SDRAM in Byte, Half or Word are supported
- Supports up to 23 address bits, 13 for row address, and 10 for column address
- Three clock sources to be chosen for different application
- Priority of transferring through special channel or AHB bus is programmable
- Supports random read or write operation

7.2 SDRAM Interface Register List

SDR Base Address

Name	Physical Base Address	KSEG1 Base Address
SDR	0x10070000	0xB0070000

SDRAM Interface Configuration Registers

Register Name	Offset	Description
SDR_CTL	0x0000	SDRAM control
SDR_ADDRCFG	0x0004	SDRAM addresses configure
SDR_EN	0x0008	SDRAM Enable
SDR_CMD	0x000C	SDRAM command
SDR_STAT	0x0010	SDRAM status
SDR_RFSH	0x0014	SDRAM Auto Refresh control register
SDR_MODE	0x0018	Mode register of SDRAM
SDR_MOBILE	0x001C	Extended Mode Register of Mobile SDRAM

7.2.1 SDR_CTL

SDRAM Control Register

Offset=0000

Bit	Name	Description	R/W	Reset
31:21	—	Reserved	R/W	0
20	VPDE	SDRAM VP Voltage Detect enable 0 Detect circuit disable 1 Detect circuit enable	R/W	0x0
19:18	PADDRV	SDRAM Pad Drive Control 0 0 Reserved 0 1 Reserved 1 0 Reserved 1 1 3.3V	R/W	0x0
17:16	VPDET	SDRAM_VP Voltage Detect 0 0 Reserved 0 1 Reserved 1 0 Error 1 1 3.3V	R/W	Depend on SDRAM_VP pin
15	—	Reserved	R/W	0
14:12	PRIO	BUS & Special DMA Priority Bus access can halt Equal or Lower Priority Special DMA, "0" is the highest: 0: BUS>DMA4>DMA5>DMA6>DMA7 1: DMA4>BUS>DMA5>DMA6>DMA7 2: DMA4>DMA5>BUS>DMA6>DMA7 3: DMA4>DMA5>DMA6>BUS>DMA7 4~7:DMA4>DMA5>DMA6>DMA7>BUS		0x0
9:8	BUSW	SDRAM Bus width 0 0 8bit 01 16bit 10 Reserved 11 Reserved		0x1
7	—	Reserved	R/W	0
6:4	CAP	SDRAM Capacity 000 16Mbits 001 32Mbits 010 64Mbits	R/W	0x0

		011 128Mbits 100 256Mbits 101 512Mbits 111 Reserved		
3:2	—	Reserved	R/W	0
1:0	TYPE	SDRAM Type: 0 0 SDRAM 0 1 Mobile SDRAM Others reserved	R/W	0x0

7.2.2 SDR_EN

SDRAM Enable Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:1	—	Reserved	R/W	0
0	EN	SDRAM Enable: Disable Enable	R/W	0x0

7.2.3 SDR_CMD

SDRAM Command Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:16	—	Reserved	R/W	0
15:0	CMD	Writing this register to make the responded command of SDRAM to be issued. CMD ID CMD action 10h self refresh 12h exit self refresh 14h pre-charge all 18h auto refresh 20h OCD decrease by 1 22h OCD increase by 1 40h burst read	RW	0x00

		44h burst write 80h command inhibit 84h power down 88h exit power down A0h power up A2H MRS A4H EMRS Other value reserved.		

7.2.4 SDR_STAT

SDRAM Status Register

Offset=0x0014

Bit	Name	Description	R/W	Reset
31:1	—	Reserved	R	0
0	ICF	Initiation Completed Flag, 0 not completed 1 completed Write 1 to clear it.	R/W	0x0

7.2.5 SDR_AUTORFC

SDRAM Auto Refresh Cycles Register

Offset=0018

Bit	Name	Description	R/W	Reset
31:0	ARFC	Auto Refresh Cycles	R/W	0xaf

7.2.6 SDR_MODE

SDRAM Mode Register

Offset=0x0018

Bit	Name	Description	R/W	Reset
31:16	—	Reserved	R	0
15:13	BA	Bank Address. When setting SDRAM Mode Register, the	R/W	0x0

		three bits must always be 0.		
12:10	-	Reserved	R/W	0
9	WBM	Write Burst Mode 0 burst write 1 Reserved	R/W	0x0
8:7	–	Reserved	R/W	0x0
6:4	CL	CAS Latency A6 A5 A4 Latency 0 1 0 2 0 1 1 3 Others reserved.	R/W	0x2
3	BT	Burst Type A3 Burst Type 0 Sequential 1 Reserved	R/W	0x0
2:0	BL	Burst Length A2 A1 A0 BL 0 0 0 reserved 0 0 1 reserved 0 1 0 4 0 1 1 8 1 1 1 reserved Others reserved	R/W	0x3

7.2.7 SDR_MOBILE

SDRAM Extended Mode Register

Offset=0x001C

Bit	Name	Description	R/W	Reset
31:16	—	Reserved	R/W	0
15:13	BA	Bank Address. When setting SDRAM Extended Mode Register, these three bits must always be 01.	R/W	0x2
12:7	—	Reserved	R/W	0
6 :5	DS	Driver Strength A6 A5 0 0 Full Strength Driver3 0 1 Half Strength Driver	R/W	0x0

		1 0 Quarter Strength Driver 1 1 One-eight Strength Driver		
4:3	TCSR	Temperature Compensated Self Refresh	R/W	0x00
2:0	PASR	Partial Array Self Refresh Coverage A2 A1 A0 0 0 0 Full Array (All Banks)3 0 0 1 Half Array (BA1 = 0) 0 1 0 Quarter Array (BA1 = BA0 = 0) 0 1 1 Reserved 1 0 0 Reserved 1 0 1 One-eighth array (BA1 = BA0 = Row Address MSB = 0) 1 1 0 One-sixteenth array (BA1 = BA0 = Row Address MSB = 0) 1 1 1 Reserved	R/W	0x00

8 DMA/Bus Arbiter

8.1 Description

The chips' DMA controller contains 8 tasks, which are divided into two types, bus DMA and special channel DMA. System bus adopts the subset of AMBA bus protocol.

8.1.1 DMA Architecture

DMA controller in the chips is a special master, for it has 4 independent special channel to high speed AHB slaves, and these 9 special slaves have two access port, so the slave has to decide which port has the higher priority. In the slave there is a reg to set which is higher priority.

Each DMA task can be set the priorities.

DMA0~DMA3 can transfer through bus only, DMA4~DMA7 can only transfer through the special channel.

DRQ Trig Source

Drq source	DRQ_Trig Field(5bit)	DRQ_line connect	Simultaneous Task num	Fifo depth	Fifo Wide	Operation wide	Block/ Demand
Uart0_t	0	DRQ0	1(DST)	8	8	8/16/32	B
Uart0_r	1	DRQ1	1(SRC)	8	8	8/16/32	B
Uart1_t	2	DRQ2	1(DST)	8	8	8/16/32	B
Uart1_r	3	DRQ3	1(SRC)	8	8	8/16/32	B
SPDIF_t	4	DRQ4	1(DST)	8	24	32	B
SPDIF_r	5	DRQ5	1(SRC)	8	24	32	B
DAC/I2S_t	6	DRQ6	1(SRC|DST)	4|16	24	32	D
ADC/I2S_r	7	DRQ7	1(SRC) note	16	24	32	D
SPI_t	8	DRQ8	1(DST)	8	16	16/32	B/D
SPI_r	9	DRQ9	1(SRC)	8	16	16/32	B/D
PCM_t	10	DRQ10	1(DST)	8	16	16/32	B/D
PCM_r	11	DRQ11	1(SRC)	8	16	16/32	B/D
reserved	12~15						

SDRAM	16	DRQ16	>2(SRC&DST)	—	—	8/16/32	—
DSPMEM	17	DRQ17	>2(SRC&DST)	—	—	8/16/32	—
NOR	18	DRQ18	>2(SRC&DST)	—	—	8/16/32	—
Reserved	19						
NAND	20	DRQ20	1(SRC|DST)	8	32	8/16/32	B/D
BT656_R	21	DRQ21	1(SRC)	16	32	8/16/32	B/D
SD	22	DRQ22	1(SRC|DST)	16	32	8/16/32	B/D
USB	23	DRQ23	1(SRC|DST)	2k	32	8/16/32	D
YUV	24	DRQ24,25	2(SRC&DST)	8	32	8/16/32	B/D
BT656_T	26	DRQ26	1(DST)	16	32	8/16/32	B/D
Reserved	25~31						

Note: IIC0,IIC1,SPI,use only IRQ mode.

If selecting the reserved DRQ, DRQ is always valuable.

In normal application, DAC is DRQ DST and ADC is DRQ SRC, which FIFO depth is 16.

For auto test, DAC is DRQ SRC when DAC_Debug FIFO depth is 4, and DMA Burst Length should be single. ADC debug data cannot be accessed by DMA.

8.2 Register List

DMA Base Address

Module name	Physical Bass Address	KSEG1 Base Address
DMA	0x10060000	0xB0060000

Bus Controller and DMA Control Register Address

Control register name	Offset	Description
DMA_CTL	0x0000	DMA Control Register
DMA_IRQEN	0x0004	DMA IRQ Enable
DMA_IRQPD	0x0008	DMA IRQ Pending

General DMA Channel Registers Block Base Address

General DMA Channel	REGS BLOCK Base Address Offset
DMA0	0x0100
DMA1	0x0120
DMA2	0x0140

DMA3	0x0160
DMA4	0x0180
DMA5	0x01A0
DMA6	0x01C0
DMA7	0x01E0

General DMA Channel Configuration Registers

Register Name	Offset From Block Base Address	Description
DMA_MODE	0x0000	Mode register
DMA_SRC	0x0004	Source address
DMA_DST	0x0008	Destination address
DMA_CNT	0x000C	Count byte
DMA_REM	0x0010	Remain count byte
DMA_CMD	0x0014	Start DMA command

8.2.1 DMA_CTL

DMA Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:24	-	Reserved	R	0
23	RST7	Write “1” to reset the relevant DMA task	RW	0
22	RST6	Write “1” to reset the relevant DMA task	RW	0
21	RST5	Write “1” to reset the relevant DMA task	RW	0
20	RST4	Write “1 to reset the relevant DMA task	RW	0
19	RST3	Write “1” to reset the relevant DMA task	RW	0
18	RST2	Write “1” to reset the relevant DMA task	RW	0
17	RST1	Write “1” to reset the relevant DMA task	RW	0
16	RST0	Write “1” to reset the relevant DMA task	RW	0
15:4	-	Reserved	R	0

3:0	CPUPRIO	CPU Priority CPU can halt Equal or Lower Priority DMA, “0” is the highest, it is shown as follows: 0: CPU>DMA0>DMA1>DMA2>DMA3 1: DMA0>CPU>DMA1>DMA2>DMA3 2: DMA0>DMA1>CPU>DMA2>DMA3 3: DMA0>DMA1>DMA2>CPU>DMA3 4~15: DMA0>DMA1 >DMA2>DMA3>CPU	RW	0

8.2.2 DMA_IRQEN

DMA IRQ Enable

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15	D7HE	DMA7 Half-transfer Complete IRQ Enable.	RW	0
14	D7TE	DMA7 Transfer Complete IRQ Enable.	RW	0
13	D6HE	DMA6 Half-transfer Complete IRQ Enable.	RW	0
12	D6TE	DMA6 Transfer Complete IRQ Enable.	RW	0
11	D5HE	DMA5 Half-transfer Complete IRQ Enable.	RW	0
10	D5TE	DMA5 Transfer Complete IRQ Enable.	RW	0
9	D4HE	DMA4 Half-transfer Complete IRQ Enable.	RW	0
8	D4TE	DMA4 Transfer Complete IRQ Enable.	RW	0
7	D3HE	DMA3 Half-transfer Complete IRQ Enable.	RW	0
6	D3TE	DMA3 Transfer Complete IRQ Enable.	RW	0
5	D2HE	DMA2 Half-transfer Complete IRQ Enable.	RW	0

4	D2TE	DMA2 Transfer Complete IRQ Enable.	RW	0
3	D1HE	DMA1 Half-transfer Complete IRQ Enable.	RW	0
2	D1TE	DMA1 Transfer Complete IRQ Enable.	RW	0
1	D0HE	DMA0 Half-transfer Complete IRQ Enable.	RW	0
0	D0TE	DMA0 Transfer Complete IRQ Enable.	RW	0

8.2.3 DMA_IRQPD

DMA IRQ Pending

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15	D7HP	DMA7 Half-transfer Complete IRQ Pending.	RW	0
14	D7TP	DMA7 Transfer Complete IRQ Pending.	RW	0
13	D6HP	DMA6 Half-transfer Complete IRQ Pending.	RW	0
12	D6TP	DMA6 Transfer Complete IRQ Pending.	RW	0
11	D5HP	DMA5 Half-transfer Complete IRQ Pending.	RW	0
10	D5TP	DMA5 Transfer Complete IRQ Pending.	RW	0
9	D4HP	DMA4 Half-transfer Complete IRQ Pending.	RW	0
8	D4TP	DMA4 Transfer Complete IRQ Pending.	RW	0
7	D3HP	DMA3 Half-transfer Complete IRQ Pending.	RW	0
6	D3TP	DMA3 Transfer Complete IRQ Pending.	RW	0

5	D2HP	DMA2 Half-transfer Complete IRQ Pending.	RW	0
4	D2TP	DMA2 Transfer Complete IRQ Pending.	RW	0
3	D1HP	DMA1 Half-transfer Complete IRQ Pending.	RW	0
2	D1TP	DMA1 Transfer Complete IRQ Pending.	RW	0
1	D0HP	DMA0 Half-transfer Complete IRQ Pending.	RW	0
0	D0TP	DMA0 Transfer Complete IRQ Pending.	RW	0

Note: For pending bit, write “1” to clear it.

8.2.4 DMA_MODEx

DMAx Mode Register

Offset=0x0100+x*0x0020

Note: In the register description, the postfix “_x” means each task has the register.

Bit	Name	Description	R/W	Reset
31:29	DBURLEN	Destination Burst Length. *: Burst must not cross a 1kB address boundary. 000: single 001: reserved 010: reserved 011: incr4 100: reserved 101: incr8 110: reserved 111: reserved Mainly for SDRAM. If DST_Burst_Len is burst 4or8, DST_Dir must be 0, DST_Fix must be 0, DST_DSP must be 0, DST_Colloum_Mode must be 0.	RW	0

28	RELO	DMA Reload Bit When DMA transmission finishes, DMA starts again with current setting. 1: Reload, 0: can NOT reload	RW	0
27	DDSP	Destination DSP mode 1: enable DSP mode 0: disable DSP mode Valuable when DST_Collum_Mode =0 and DST_Tran_Wide=0, DST_Burst_Len=0, DST_Fix=0.	RW	0
25	DDIR	Destination address direction; 0: increase, 1: decrease Valuable when DST_Fix=0 . If DST_Burst_Len is burst 4or8, DST_Dir must increase.	RW	0
24	DFXA	Destination Fix Address(IO) or Not; 0: Not fixed, 1: Fix	RW	0
26	DCOL	Destination Column Mode 0: enable row mode 1: Enable column mode Valuable when DST_Burst_Len=0 and DST_Fix=0.	RW	0
23:19	DTRG	Destination DRQ Trig Source	RW	0
18:17	DTRANWID	Destination Transfer wide: 00: 8 01: 16 10: 32 11: reserved	RW	0
16	DFXS	Destination Fix Size bit 0: not fixed, 1: fixed If DST_FixedSize=0, DMA will transfer in 8bit mode when remain counter is less than DST_Tran_Wide. If DST_FixedSize=1, DMA will always transfer in DST_Tran_Wide.	RW	0

15:13	SBURLEN	Source Burst Length. *: Burst must not cross a 1kB address boundary. 000: single 001: reserved 010: reserved 011: incr4 100: reserved 101: incr8 110: reserved 111: reserved Mainly for SDRAM. If SRC_Burst_Len is burst 4or8, SRC_Dir must be 0, SRC_Fix must be 0, SRC_DSP must be 0, SRC_Colloum_Mode must be 0.	RW	0
12	-	Reserved		0
11	SDSP	Source DSP Mode 1: enable DSP mode 0: disable DSP mode Valuable when SRC_Collum_Mode =0 and SRC_Tran_Wide=0, SRC_Burst_Len=0, SRC_Fix=0.	RW	0
10	SCOL	Source Column Mode 0: enable row mode 1: enable column mode Valuable when SRC_Burst_Len=0, SRC_Fix=0.	RW	0
9	SDIR	Source address direction; 0: increase, 1: decrease Valuable when SRC_Fix=0. If SRC_Burst_Len is burst 4or8 SRC_Dir must increase.	RW	0
8	SFXA	Source Fix Address (IO) or not (MEM) 0: not fixed, 1:fixed	RW	0
7:3	STRG	DRQ trig source: can select always trig	RW	0
2:1	STRANWID	Source Transfer Width: 00: 8 01: 16 10: 32 11: reserved	RW	0

0	SFXS	Source Fix Size 0: not fixed, 1: fixed If SRC_FixedSize=0, DMA will transfer in 8bit mode when remain counter is less than DST_Tran_Wide. If SRC_FixedSize=1, DMA will always transfer in SRC_Tran_Wide.	RW	0

8.2.5 DMA_SRCx

DMAx SRC Register

Offset=0x0104+x*0x0020

Bit	Name	Description	R/W	Reset
31:0	SRC	DMA Source Address	RW	0

8.2.6 DMA_DSTx

DMAx DST Register

Offset=0x0108+x*0x0020

Bit	Name	Description	R/W	Reset
31:0	DST	DMA Destination Address	RW	0

8.2.7 DMA_CNTx

DMAx CNT Register

Offset=0x010C+x*0x0020

Bit	Name	Description	R/W	Reset
31:20	-	Reserved	R	0
19:0	CNT	DMA Count byte	RW	0

8.2.8 DMA_REMx

DMAx Remain Register

Offset=0x0110+x*0x0020

Bit	Name	Description	R/W	Reset
31:20	-	Reserved	-	0
19:0	REMAIN	DMA Remain Byte	RW	0

8.2.9 DMA_CMDx

DMAx CMD Register

Offset=0x0114+x*0x0020

Bit	Name	Description	R/W	Reset
31:6	-	Reserved	-	0
7:5	WAIT	Wait state 0~7 Wait bit is valuable only in Block mode.	RW	0
4	BLOC	DMA block mode enable 0: demand mode 1: block mode There is no block mode for special DMA. Special DMA4 and 5 only support burst transmission of one side at most; both sides burst transmission is not supported. Special DMA6 and 7 only support single to single transmission.	RW	0
3:2	-	Reserved		
1	PAUS	Write “1” to Pause the relevant DMA task. When the task pauses, it will not request system and response to the relevant DRQ sources.	RW	0
0	STAR	After DMA Transmission finishes, the bit will be cleared. The low-go-high edge of this bit will load SRC start address, DST start address, byte count into current working counters.	RW	0

Note: SpecDMA cannot work normally in non-single-single mode

9 SD/MMC Interface

9.1 Description

SD/MMC Interface is based on MMC card SPEC 4.1 and is compatible with SD memory card physical layer SPEC version 1.01. Multimedia Card/SD is a serial input/output interface to send command and receive data. Its features are as follows:

1. Supports SD memory card, MMC memory card.
2. Supports 1bit, 4bit, 8bit, bus mode.
3. Clock max rate up to 52MHz.
4. Data transfer FIFO and DMA control.
5. Read /Write CRC Status Hardware checked automatically.

10NAND FLASH/SMC State Machine

10.1 Description

The general purpose Nand Flash Interface controller is a State Machine configurable interface to external Nand Flash. The flash data bus width only support 8bit .
The flash State machine provides automatic timing control for the using data read and write access signal line. The Controller will transfer the data between the Int_RAM Mem and ext_Flash Mem by AHB or DMA.
The Controller module can monitor the relatively interval transitions of the NAND flash device's Ready/Busy signal. This include an interrupt that can monitor the rising edge of the busy signal and that can be set generate a interrupt if the NAND flash device hang up, etc.

The forward error correction module is used to provide Actions GL5006 applications with a reliable interface to various storage media, especially storage media that would otherwise have nacceptable bit error rates. The ECC module comprises two different error correcting code processors:
- 8-BCH correcting encoder/decoder.
- 12-BCH correcting encoder/decoder.

The purpose of the 8-BCH decoder is to process a coded block (data block followed by "parity" check data) to determine if there is an error and, if there are errors, where they are located and how to correct them. The purpose of the BCH encoder is to read a block of 512-symbols from RAM, alculate and append 13-parity symbols to form a 516-symbol BCH-codeword.

The purpose of the 12-BCH decoder is to process a coded block (data block followed by "parity" check data) to determine if there is an error and, if there are errors, where they are located and how to correct them. The purpose of the BCH encoder is to read a block of 512-symbols from RAM, alculate and append 20-parity symbols to form a 516-symbol BCH-codeword.

Six byte address support for new NAND Flash support
SLC & MLC NAND Flash support
8bit/12bit Error Correction support
8 bit wide NAND support
Monitor the NAND flash Ready/Busy signal by HW support

11 BT.656&601 Interface

11.1 Description

The BT.656 & 601 Interface consists of two parts: Video Encoder & Decoder & CMOS Sensor & TS Interface and Internal Video Encoder.

11.2 Video Encoder/Decoder/CMOS Sensor/TS Interface

Video encoder interface connects to digital video encode IC, which can display NTSC or PAL mode on TV. The output format of the video encoder interface can be configured to BT.656 or BT.601 format.

Video decoder & CMOS Sensor interface connects to digital video decoder IC or CMOS sensor, which can record TV or sample picture. The input format of the video decoder & CMOS sensor interface can be configured to BT.656 or BT.601 format.

Video Encoder & CMOS Sensor & Decoder Interface has the following features:

- Supports 8bit digital pixel data bus.
- Supports 16-level by 32bit FIFO.
- Supports BT.656 and BT.601 protocol for NTSC/PAL mode.

11.2.1 Register List

BT Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
VEDCSTI	0x100D0000	0xB00D0000

VEDCSTI: Video Encoder & Decoder & CMOS Sensor & TS Interface

BT Registers list—for output part, including external and internal TV-Encoder

Offset	Register Name	Description
0x0000	BTO_MODESEL	TV-encoder Interface Mode Select Register
0x0004	BT_FIFO_ODAT	TV-encoder Interface FIFO Data Register; 16 level * 32 bit FIFO
0x0008	BT_VEICTL	TV-encoder Interface Control Register
0x000C	BT_VEIALSEOF	TV-encoder Interface active line start and end position(Odd Field) register
0x0010	BT_VEIALSEEF	TV-encoder Interface active line start and end position (Even

		Field)register
0x0014	BT_VEIADLSE	TV-encoder Interface active data in every line start and end position register
0x0018	BT_VEIFTP	TV-encoder Interface Field Transition Position Register
0x001C	BT_VEIFIFOCTL	TV-encoder Interface FIFO Control Register

BT Registers List—for input parts, including External TV-Decoder, External CMOS Sensor and TS.

Offset	Register Name	Description
0x0020	BTI_MODESEL	TV- Decoder/ CMOS Sensor/ TS Interface Mode Select Register
0x0024	BT_FIFO_IDAT	TV_Decoder/ CMOS Sensor /TS Interface FIFO Data Register; 16 level * 32 bit FIFO.
0x0028	BT_VDICTL	TV-decoder Interface Control Register
	BT_CSICTL	CMOS Sensor Interface Control Register
	BT_TSICTL	TS Interface Control Register
0x002C	BT_VDIHSPOS	TV-decoder Interface Hsync Start Position Register and active data in every line
	BT_CSIHSPOS	CMOS Sensor Interface Hsync Start Position Register and active pixel number in every line
0x0030	BT_VDIVSEPOF	TV-decoder Interface VSYNC Start/size(Odd Field) Register
	BT_CSIVSEPOF	CMOS Sensor Interface active lines start position and size Register
0x0034	BT_VDIVSEPEF	TV-decoder Interface VSYNC Start/size (Even Field) Register
0x0038	BT_VDIIRQSTAT	TV-decoder Interface IRQ Status Register
	BT_CSIRQSTAT	CMOS Sensor Interface IRQ Status Register
0x003C	BT_VDIFIFOCTL	Video Decoder Interface FIFO Control Register
	BT_CSIFIFOCTL	CMOS Sensor Interface FIFO Control Register
	BT_TSIFIFOCTL	TS Interface FIFO Control Register

11.2.2 Register Description

11.2.2.1 Output Interface Register (External & Internal TV-Encoder)

11.2.2.1.1 BTO_MODESEL

TV-encoder Interface Mode Select Register
Offset=0x00

Bits	Name	Description	R/W	Default
31:2	-	Reserved	R	0
1	DMS	DMA Mode Select 0: demand mode 1:block mode	RW	0
0	EIEN	Encoder Interface Enable 0:disable, 1:enable	RW	0

11.2.2.1.2 BT_FIFO_ODAT

TV-encoder Interface FIFO Data Register
Offset=0x04

Bits	Name	Description	R/W	Default
31:0	FIFOD	FIFO Data	W	x

11.2.2.1.3 BT_VEI_CTL

TV-encoder Interface Control Register
Offset=0x08

Bits	Name	Description	R/W	Default
31:11	-	Reserved	R	0
10	HPS	Horizontal Pixel Scaler 0: 1: 1 1: 1: 2	Rw	0
9:8	-	Reserved	R	0
7	DFS	Data Format Select. 0: Y3Y2Y1Y0, Cb3Cb2Cb1Cb0, Y7Y6Y5Y4, Cr3Cr2Cr1Cr0... 1: Y1Cr0Y0Cb0, Y3Cr1Y2Cb1 ...	RW	0
6	EIOE	Encoder Interface Output Enable 0: disable, no data or sync signal will output from IC pin. 1: enable	RW	0
5	FVS	Vsync or Field Select — BT601 only 0: Vsync 1: Field	RW	0
4	HAS	Hsync Active Select — BT601 only 0: Hsync active low, 1: Hsync active high	RW	0
3	VFAS	Vsync/Field Active Select. — BT601 only 0: Vsync active low or Odd field active low. 1: Vsync active high or Even field active low	RW	0
2	PAES	Pclk Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	RW	0
1	PNMS	PAL/NTSC Mode Select 0: PAL –625 line, 50 field/s 1: NTSC–525 line, 60 field/s	RW	0
0	VFS	Video Format Select. 0: BT.656 1: BT.601	RW	0

Note: Vsync/Hsync active low means the signal is a negative pulse.

11.2.2.1.4 BT_VEIALSEOF

TV-encoder Interface active line start and end position (Odd Field) register
Offset=0x0C

Bits	Name	Description	R/W	Default
31:17	-	Reserved	R	0
16:8	LEPO	active Line End Position in Odd field	RW	x
7:0	LSPO	active Line Start Position in Odd field	RW	x

Note: Active line start position must be counted from the 1st line.

11.2.2.1.5 BT_VEIALSEEF

TV-encoder Interface active line start and end position (Even Field) register
Offset=0x10

Bits	Name	Description	R/W	Default
31:22	-	Reserved	R	0
21:12	LEPE	Active Line End Position in Even field.	RW	x
11:10		Reserved	R	0
9:0	LSPE	active Line Start Position in Even field	RW	x

Note: Active line start position must be counted from the 1st line.

11.2.2.1.6 BT_VEIADLSE

TV-encoder Interface active data in every line start and end position register
Offset=0x14

Bits	Name	Description	R/W	Reset
31:27	—	Reserved	R	0
26:16	ADEP	Active Data bytes End Position in each line	RW	xxx
15:11	—	Reserved	R	0
10:0	ADSP	Active Data bytes Start Position in each line	RW	xxx

11.2.2.1.7 BT_VEIFTP

TV-encoder Interface of Field Transition Position Register
Offset=0x18

Bits	Name	Description	R/W	Default
31:26	-	Reserved	R	0
25:16	FTPE	Field Transition Position(Even field)	RW	x
15:10		Reserved	R	0
9:0	FTPO	Field Transition Position(Odd field)	RW	x

Note: The register is active only in BT.601 format.

11.2.2.1.8 BT_VEIFIFOCTL

TV-encoder Interface FIFO Control Register
Offset=0x1c

Bits	Name	Description	R/W	Default
31:8	-	Reserved	R	0
7	FFU	FIFO FUll flag. 0: Not Full 1: Full	RW	0
6	ACS	FIFO Access Channel Select. 0: Special Channel 1: AHB Bus	RW	0
5	EIME	FIFO Empty IRQ interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable.	RW	0
4	FDE	FIFO empty DRQ Enable. 0: Disable 1: Enable	RW	0
3	EIE	FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0
2:1	FEC	FIFO Empty Condition. 00: 7/16 Empty, means there is 7 level of data when report empty 01: 8/16 Empty(Half Empty) 10: 9/16 Empty 11: 10/16 Empty	RW	01
0	EIP	FIFO Empty IRQ Pending bit. 0: No IRQ 1: IRQ Write 1 to the bit, clear the bit.	RW	0

Note: The register is active for BT.656 & BT.601 format.

11.2.2.2 Input Interface General Register (External TV-Decoder, External CMOS Sensor and TS)

11.2.2.2.1 BTI_MODESEL

Decoder & CMOS Sensor & TS Interface Mode Select Register
Offset=0x20

Bits	Name	Description	R/W	Default
31:6	-	Reserved	R	0
5	DMS	DMA Mode Select 0: demand mode 1: block mode	RW	0
4	CKOE	CLKOUT Enable. 0: Disable 1: Enable	RW	0

3	-	reserved	R	0
2:1	VFS	Video Format Select. 00: BT.656 01: BT.601 10: Ts 11: Sensor	RW	00
0	IIE	Input Interface Enable 0:disable 1:enable	RW	0

11.2.2.2.2 BT_FIFO_IDAT

TV_Decoder/ CMOS Sensor /TS Interface FIFO Data Register
Offset=0x24

Bits	Name	Description	R/W	Default
31:0	FIFOD	FIFO Data.	R	X

11.2.2.3 TV Decoder Interface Register

11.2.2.3.1 BT_VDICTL

TV-decoder Interface Control Register
Offset=0x28

Bits	Name	Description	R/W	Default
31:13	-	Reserved	R	0
12	HalfF	Receive 1 field or 2 field for 1 frame for TV-decoder 0: 2 field for 1 frame 1: 1 field for 1 frame	RW	0
11:10	VSbuS	TV-decoder input vertical Sub-sample ratio 00: 1:1 01: 2:1 10: 4:1 11: reserved	RW	00
9:8	HSubS	TV-decoder input horizontal sub-sample ratio 00: 1:1 01: 2:1 10: 4:1 11: reserved	RW	00
7	DATF	Data Format Select. 0:Y3Y2Y1Y0, Cb3Cb2Cb1Cb0, Y7Y6Y5Y4, Cr3Cr2Cr1Cr0,... 1:Y1Cr0Y0Cb0, Y3Cr1Y2Cb1...	RW	0
6	—	Reserved	R	0
5	FVS	VSYNC or FIELD select, — BT601 only 0:VSYNC 1:FIELD	RW	0

4	HAS	Hsync Active Select, — BT601 only 0: Hsync active low 1: Hsync active high	RW	0
3	FVAS	Vsync/Field Active Select. —refer to BT_VDICTL_bit5. 0: Vsync active low or Odd field active low. 1: Vsync active high or Even field active low	RW	0
2	PAES	PCLK Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	RW	0
1:0	-	reserved	R	0

11.2.2.3.2 BT_VDIHSPOS

TV decoder Interface Hsync Start Position Register and active data in every line (in PCLK)
Offset=0x2c

Bits	Name	Description	R/W	Default
31:25	-	Reserved	R	0
24:12	ADEL	Active Data in Every Line	RW	x
11	-	Reserved	R	0
10:0	HSP	Hsync Start Position	RW	x

Note: The register is active only for BT.601 format.

11.2.2.3.3 BT_VDIVSEPOF

TV decoder Interface active lines start position and size (Odd Field) Register (in Hsync)
Offset=0x30

Bits	Name	Description	R/W	Default
31:25	-	Reserved	R	0
24:12	ALOF	Active Lines of Odd Field.	RW	x
11		Reserved	R	0
10:0	ALSPO	Active Lines Start Position in Odd field	RW	x

Note: The register is active only for BT.601 format.

11.2.2.3.4 BT_VDIVSEPEF

TV decoder Interface active lines start position and size (Even Field) Register (in Hsync)
Offset=0x34

Bits	Name	Description	R/W	Default
31:25	-	Reserved	R	0
24:12	ALEF	Active Lines of Even Field.	RW	x
11		Reserved	R	0
10:0	ALSPE	Active Lines Start Position in Even field	RW	x

Note:

Hsync start and end position are calculated from its active area position.
Vsync start and end position are calculated from its active area position.
The register is active only for BT.601 format.

11.2.2.3.5 BT_VDIIRQSTAT

TV-decoder Interface IRQ status Register
Offset=0x38

Bits	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8	FSIM	Finish-flag Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	RW	0
7	VSIM	Vsync Edge or SAV IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	RW	0
6	HEIM	Hsync Edge or EAV IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	RW	0
5	FSIE	Finish-flag IRQ Enable. 0: Disable 1: Enable	RW	0
4	VSIE	Vsync Edge or SAV IRQ Enable. 0: Disable 1: Enable	RW	0
3	HEIE	Hsync Edge or EAV IRQ Enable. 0: Disable 1: Enable	RW	0
2	FSIP	Finish-flag IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0
1	VSIP	Vsync Edge or SAV IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0
0	VEIP	Hsync Edge or EAV IRQ pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0

11.2.2.3.6 BT_VDIFIFOCTL

TV decoder Interface FIFO Control Register
Offset=0x3C

Bits	Name	Description	R/W	Default
31:8	-	Reserved	R	0

7	FEF	FIFO Empty Flag. 0: Not Empty 1: Empty	R	0
6	ACS	FIFO Access Channel Select. 0: Special Channel 1: AHB Bus	RW	0
5	FIME	FIFO Full IRQ interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable.	RW	0
4	FDE	FIFO Full DRQ Enable. 0: Disable 1: Enable	RW	0
3	FIE	FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0
2:1	FFC	FIFO Full Condition. 00: 9/16 Full 01: 8/16 Full 10: 7/16 Full 11: 6/16 Full	RW	01
0	FIP	FIFO Full IRQ Pending bit. Write 1 to the bit, clear the bit. 0: No IRQ 1: IRQ	RW	0

11.2.2.4 CMOS Sensor Interface Register

11.2.2.4.1 BT_CSICTL

CMOS Sensor Interface Control Register

Offset=0x28

Bits	Name	Description	R/W	Default
31:12	-	Reserved	R	0
11:10	VSbuS	CMOS Sensor input vertical sub-sample ratio 00: 1:1 01: 2:1 10: 4:1 11: reserved	RW	00
9:8	HSubS	CMOS Sensor input horizontal sub-sample ratio 00: 1:1 01: 2:1 10: 4:1 11: reserved	RW	00
7	DATF	Data Format Select. 0:Y3Y2Y1Y0, Cb3Cb2Cb1Cb0, Y7Y6Y5Y4, Cr3Cr2Cr1Cr0... 1: Y1Cr0Y0Cb0, Y3Cr1Y2Cb1 ...	RW	0
6:5	—	Reserved	R	0
4	HAS	Hsync Active Select — BT601 only 0: Hsync active low 1: Hsync active high	RW	0
3	VAS	Vsync Active Select— BT601 only. 0: Vsync active low 1: Vsync active high	RW	0
2	PAES	PCLK Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	RW	0
1:0	-	Reserved	R	0

11.2.2.4.2 BT_CSIHSPOS

CMOS Sensor Interface Hsync Start Position Register and active data in every line (in PCLK)

Offset=0x2c

Bits	Name	Description	R/W	Default
31:25	-	Reserved	R	0
24:12	ADEK	Active Pixel Number in Every Line	RW	x

11	-	Reserved	R	0
10:0	HSP	Active Pixel Start Position in Every Line	RW	x

11.2.2.4.3 BT_CSIVSEPOF

CMOS Sensor Interface TV decoder Interface active lines start position and size(Odd Field) Register (in Hsync)

BT_CSIVSEPOF

Offset=0x30

Bits	Name	Description	R/W	Default
31:25	-	Reserved	R	0
24:12	ALOF	Active Lines number in Every Frame	RW	x
11		Reserved	R	0
10:0	ALSPO	Active Line Start Position in Every Frame	RW	x

Notes:

The register is active only for BT.601 format.

Hsync start and end position are calculated from its active area position.

Vsync start and end position are calculated from its active area position.

11.2.2.4.4 BT_CSIRQSTAT

CMOS Sensor Interface IRQ status Register

Offset=0x38

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7	VSIM	Vsync Edge or SAV IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	RW	0
6	HEIM	Hsync Edge or EAV IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	RW	0
5	-	Reserved	R	0
4	VSIE	Vsync Edge or SAV IRQ Enable. 0: Disable 1: Enable	RW	0

3	HEIE	Hsync Edge or EAV IRQ Enable. 0: Disable 1: Enable	RW	0
2	-	Reserved	R	0
1	VSIP	Vsync Edge or SAV IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0
0	VEIP	Hsync Edge or EAV IRQ pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0

11.2.2.4.5 BT_CSIFIFOCTL

CMOS Sensor Interface FIFO Control Register

Offset=0x3C

Bits	Name	Description	R/W	Default
31:8	-	Reserved	R	0
7	EMF	FIFO Empty Flag. 0: Not Empty 1: Empty	R	0
6	ACS	FIFO Access Channel Select. 0: Special Channel 1: AHB Bus	RW	0
5	FIME	FIFO Full IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable.	RW	0
4	FDE	FIFO Full DRQ Enable. 0: Disable 1: Enable	RW	0
3	FIE	FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0
2:1	FTH	FIFO Full Condition. 00: 9/16 Full 01: 8/16 Full 10: 7/16 Full	RW	01

		11: 6/16 Full		
0	FIP	FIFO Full IRQ Pending Bit. Write 1 to the bit, clear the bit. 0: No IRQ 1: IRQ	RW	0

11.2.2.5 TS Interface Register

11.2.2.5.1 BT_TSICTL

TS Interface Control Register

Offset=0x28

Bits	Name	Description	R/W	Default
31:8	-	Reserved	R	0
7	DATF	Data Format Select. 0:Y3Y2Y1Y0, Cb3Cb2Cb1Cb0, Y7Y6Y5Y4, Cr3Cr2Cr1Cr0... 1:Y1Cr0Y0Cb0, Y3Cr1Y2Cb1...	RW	0
6:5	-	Reserved	R	0
4	HAS	Hsync Active Select — BT601 only 0: Hsync active low 1: Hsync active high	RW	0
3	VAS	Vsync Active Select— BT601 only. 0: Vsync active low 1: Vsync active high	RW	0
2	PAES	PCLK Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	RW	0
1:0	-	Reserved	R	0

11.2.2.5.2 BT_TSIFIFOCTL

TS Interface FIFO Control Register

Offset=0x40

Bits	Name	Description	R/W	Default
31:8	-	Reserved	R	0
7	EMF	FIFO Empty Flag. 0: Not Empty 1: Empty	R	0

6	ACS	FIFO Access Channel Select. 0: Special Channel 1: AHB Bus	RW	0
5	FIME	FIFO Full IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable.	RW	0
4	FDE	FIFO Full DRQ Enable. 0: Disable 1: Enable	RW	0
3	FIE	FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0
2:1	FTH	FIFO Full Condition. 00: 9/16 Full 01: 8/16 Full 10: 7/16 Full 11: 6/16 Full	RW	01
0	FIP	FIFO Full IRQ Pending Bit. Write 1 to the bit, clear the bit. 0: No IRQ 1: IRQ	RW	0

11.3 Internal Video Encoder

The integrated video encoder can directly connect to TV to display all kinds of modes. The integrated video encoder has the following features:

- Supports NTSC-M, -J and –4.43 modes.
- Supports PAL-B, -D, -G, -H, -I, -M, -N, -Nc modes.
- Supports CVBS (Composite Video Broadcasting Signal) output.
- Supports outputting blue color when no data input.

11.3.1 Registers List

Internal Video Encoder Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address
Internal Video Encoder	0x100D0000	0xB00D0000

VEDCSTI Registers Offset Address

Offset	Register Name	Description
0x0050	BT_IVECTL	Internal Video Encoder Control Register
0x0054	BT_IVEOUTCTL	Internal Video Encoder Output Control Register
0x0058	BT_IVECOTCTL	Internal Video Encoder Contrast Control Register
0x005c	BT_IVEBRGCTL	Internal Video Encoder Brightness Control Register
0x0060	BT_IVECSATCTL	Internal Video Encoder Color Saturation Control Register
0x0064	BT_IVECBURCTL	Internal Video Encoder Color Burst Control Register
0x0068	BT_IVESYNCAMCTL	Internal Video Encoder SYNC Amplitude Control Register

11.3.2 Registers Description

11.3.2.1 BT_IVECTL

Internal Video Encoder Control Register

Offset=0x0050

BT_IVECTL Bit Field Description

Bits	Name	Description	R/W	Reset
31:7	-	Reserved	R	0
8	PCBL	PaInc colorburst length 0: 2.22us 1: 2.51us	RW	0
7	-	Reserved	R	0
6	IVEN	Integrated Video Encoder Enable. 1:Enable 0:Disable	RW	0
5	-	Reserved	-	0
4	CLKS	Clock Mode Select. 0:27MHzPLL+24MHz 1:27MHzPLL	RW	0

3:0	TVFS	TV Format Select. 0000: NTSC-M 0001: NTSC-J 0010: PAL-Nc 0011: PAL-B,G,H 0100: PAL-D 0101: PAL-I 0110: PAL-M 0111: PAL-N Others: PAL-D	RW	0100

Note: When PAL-Nc mode is selected, bit4 of IVECTL must be set to 1.

11.3.2.2 BT_IVEOUTCTL

Internal Video Encoder Output Control Register

Offset=0x0054

BT_IVEOUTCTL Bit Field Description

Bits	Name	Description	R/W	Reset
31:3	-	Reserved	R	0
2:1	CVBSOUT	CVBS Output. 00: Blue color(default) 01: Black color 1x: Color bar signal	RW	0
0	DACT	DAC Close/Open Control. 0: Close 1: Open.	RW	0

NOTE: When encoder is enabled & no pixel data input, CVBS outputs blue color & black color. When color bar outputs, Pixel data path is closed.

11.3.2.3 BT_IVECOTCTL

Internal Video Encoder Contrast Control Register

Offset=0x0058

BT_IVECOTCTL Bit Field Description

Bits	Name	Description	R/W	Reset
31:4	-	Reserved	R	0

3:0	COTCTL	Contrast control. 0000: 75% ... 0111: 100% ... 1110: 125% 1111: Reserve	RW	0111

Note: Contrast Control Register[3:0]=(X-0.75)×28; X is 75% to 125%.

11.3.2.4 BT_IVEBRGCTL

Internal Video Encoder Brightness Control Register

Offset=0x005c

BT_IVEBRGCTL Bit Field Description

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	BRGCTL	Brightness control. 00H:0LSB ... 7FH:127LSB 80H:0LSB 81H:-127LSB ... FFH:-1LSB	RW	0

Note: The MSB of Brightness Control Register[7:0] is sign bit. The unit is LSB of DAC. The value is calculated with 2-complement.

11.3.2.5 BT_IVECSATCTL

Integrated Video Encoder Color Saturation Control Register

Offset=0x0060

Bits	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3:0	CSATCTL	Color Saturation control. 0000:75% ... 0111:100% ... 1110:125% 1111:Reserve	RW	0111

Note:: Color Saturation Control Register[3:0]=(X-0.75)×28; X is 75% to 125%.

11.3.2.6 BT_IVECBURCTL

Integrated Video Encoder Color Burst Control Register

Offset=0x0064

Bits	Name	Description	R/W	Reset
31:12	-	Reserved	R	0
11:0	CBURPH	The Phase of Color Burst Phase Compensate. 00H: 0 degree ... 3FFH: 360 degree	RW	0

Note: The register value of the phase of color burst phase compensate is X×360/4096. X is the wanted phase of color burst phase compensate.

11.3.2.7 BT_IVESYNCAMCTL

Integrated Video Encoder SYNC Amplitude Control Register

Offset=0x0068

Bits	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3:0	SYNCAM	SYNC Pedestal Level Amplitude. 0000: 0LSB ... 1111: 15LSB	RW	0

12 YUV2RGB Interface

12.1 Description

The Module performs image data transfer from frame buffer to LCD panel. It accelerates the frame data display by hardware operation. It is optional and mainly used in movie decoding. The processes include:

1. Up-sampling from YUV 422 to YUV 444
2. Change from YUV / YCbCr to RGB (8, 8, 8) format

YCbCr to RGB:

R = Y + 1.402 *(Cr-128)

G = Y - 0.34414*(Cb-128) - 0.71414*(Cr-128)

B = Y + 1.772 *(Cb-128)

YUV to RGB:

R = Y + 1.14V

G = Y - 0.39U - 0.58V

B = Y + 2.03U

3. Cut down RGB (8, 8, 8) to the RGB format required in LCD Panel.

12.2 Register List

YUV2RGB Registers Block Base Address

Block Name	Physical Base Address	KSEG1 Base Address
YUV2RGB	0x100F0000	0xB00F0000

TYUV2RGB Registers Offset Address

Offset	Register Name	Description
0x0000	YUV2RGB_CTL	YUV2RGB Control Register
0x0004	YUV2RGB_FIFODAT	YUV2RGB FIFO Data Register
0x0008	YUV2RGB_CLKCTL	YUV2RGB Clock Control Register
0x000c	YUV2RGB_FrameCount	YUV2RGB Frame Count Register

12.2.1 YUV2RGB_CTL

YUV2RGB Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:22	-	Reserved	R	0
21	RFBM	Read FIFO Block Mode 0: Normal Mode 1: Block Mode	RW	0
20	WFBM	Write FIFO Block Mode 0: Normal Mode 1: Block Mode	RW	0
19	EN	RGB Decoder Enable. 0: Disable 1: Enable	RW	0
18	FES	FIFO Empty Status 0: Not Empty 1: Empty	R	1
17:16	WDCS	Write Data/Command Select 00:Write Command （Write LCD register address） 01: Write Data (Write LCD register data) 10: RGB(565) Data FrameBuffer Transfer 11: YCbCr/YUV Data FrameBuffer Transfer	RW	0
15	DEST	RGB Decoder Destination. 0: LCD interface 1: Frame buffer	RW	0
14	INS	Input YUV/YCbCr Select. 0: YCbCr 1: YUV	RW	0
13:11	FORMATS	RGB Format Select: 000: 16bit (RGB 565 1transfer) 001:18bit (RGB 666 1transfer) 010:8bit (RGB 565 2transfer) 011:9bit (RGB 666 2transfer) 100: 8bit (RGB 888 3transfer) 101:6bit (RGB 666 3transfer) 110: Reserved 111: Reserved	RW	0
10	SEQ	RGB Sequence. 0: RGB 1: BGR	RW	0

9	FWCS	FIFO Write Channel Select. 0: Special Channel 1: AHB Bus	RW	0
8	FRCS	FIFO Read Channel Select. 0: Special Channel 1: AHB Bus	RW	0
7	EMDE	FIFO Empty (Write) DRQ Enable. 0: Disable 1: Enable	RW	0
6	EMIE	FIFO Empty (Write) IRQ Enable. 0: Disable 1: Enable	RW	0
5	FUDE	FIFO Full (Read) DRQ Enable. 0: Disable 1: Enable	RW	0
4	FUIE	FIFO Full (Read) IRQ Enable. 0: Disable 1: Enable	RW	0
3	EMCO	FIFO Empty (Write) Condition. 0: 4/8 Empty 1: 0/8 Empty	RW	0
2	EMIP	FIFO Empty (Write) IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit to clear it.	RW	1
1	FUIP	FIFO Full (Read) IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit to clear it.	RW	0
0	ERP	FIFO Error Pending Bit. 0: No Error 1: Error Write 1 to the bit to clear it and reset the FIFO.	RW	0

Note: When RGB decoder destination (Bit15) selects LCD interface, LCD color depth can select RGB565, RGB666 and RGB888 format.

When RGB decoder destination selects frame buffer, LCD color depth can only select RGB565 format.

12.2.2 YU2RGB_DAT

YUV2RGB FIFO Data Register

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:0	DAT	FIFO Data	RW	x

12.2.3 YUV2RGB_CLKCTL

YUV2RGB Clock Control Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:15	-	Reserved	R	0
14:8	RWCLKHDIV	R/W Clock High Cycle Division (from AHB Bus). Divide from 1~128	RW	0x7f
7	-	Reserved	R	0
6:0	RWCLKLDIV	R/W Clock Low Cycle Division (from AHB Bus) Divide from 1~128	RW	0x7f

12.2.4 YUV2RGB_FrameCount

YUV2RGB Frame Count Register

Offset=0x000c

Bit	Name	Description	R/W	Reset
31:17	-	Reserved	R	0
16:8	FCOLC	Frame Column Counter.	RW	0
7:0	FROWC	Frame Row Counter.	RW	0

13 USB2.0 SIE (OTG)

13.1 General Description

OTG controller is designed to support all tasks specified in OTG Supplement. AOTG uses hardware implementation of Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). Special Function Registers are provided for the control of HNP and SRP.

AOTG can be used as a dual-role device and can act as a USB host or a USB peripheral device. The ID input pin controls the default role. If the ID=1, it means that the mini-B plug has connected and AOTG becomes a B-device. When the ID=0, it means that a mini-A plug has connected and AOTG becomes an A-device. See On-The-Go Supplement to the USB2.0 SPEC Rev 1.0a for the details.

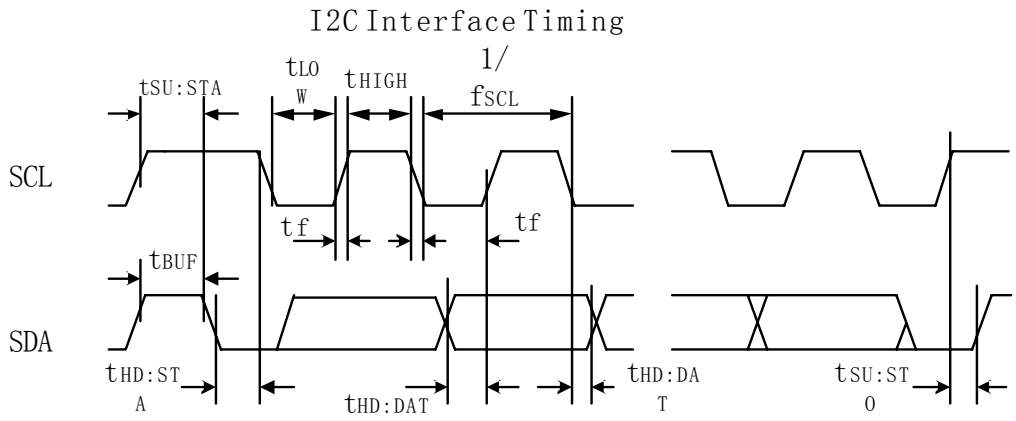
Please refer to OTG specification –AOTG_v04.pdf

14 I2C (2) Interface

14.1 Description

The chips have two I2C Interfaces, which can be configured as either master or slave device. In master mode, it generates the clock (I2C_SCL) and initiates transactions on the data line (I2C_SDA). Data on the I2C bus is byte oriented. Multi-Master mode, 10-bit address and Hi-speed mode are not supported. See I2C_Bus_Specification_1995 for detailed information.

Pull-up resistors are required on both of the I2C lines as all of the I2C drivers are open drain. Typically external 2k-Ohm resisters are used to pull the signals up to VCC.



14.2 Register List

I2C Register Block Base Address

Block Name	Physical Base Address	KSEG1 Base Address
I2C1	0x10180000	0xB0180000
I2C2	0x10180020	0xB0180020

The register block contains the registers.

I2C Registers Offset Address

Offset	Register Name	Description
0x0000	I2Cx_CTL	I2Cx Control Register
0x0004	I2Cx_CLKDIV	I2Cx Clock Divide Register

0x0008	I2Cx_STAT	I2Cx Status Register
0x000c	I2Cx_ADDR	I2Cx Address Register
0x0010	I2Cx_DAT	I2Cx Data Register

14.2.1 I2Cx_CTL

I2Cx Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8	PUEN	Internal Pull-up Resistor (4.7k) Enable. 0: Disable 1: Enable	RW	0
7	EN	Enable. 0: Disable 1: Enable	RW	0
6	SIE	START Condition Generates IRQ Enable (only for slave mode). 0: Disable 1: Enable	RW	0
5	IRQE	IRQ Enable. 0: Disable 1: Enable	RW	0
4	MS	Mode Select. 0: Master mode 1: Slave mode	RW	0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition	RW	0
1	RB	Release Bus. Writing 1 to this bit will release the clock and data line to idle. MCU should write 1 to this bit after transmitting or receiving the last bit of the whole transfer.	RW	0

0	GRAS	Generating/Receiving Acknowledge Signal. In receiving mode: 0: generate the ACK signal to the transmitter at 9th clock of SCL 1: do not generate the ACK signal at 9th clock of SCL In transmitting mode: 0: has not received the ACK signal 1: has received the ACK signal. This bit will be cleared when the 9th clock of next SCL arrives	RW	0

14.2.2 I2Cx_CLKDIV

I2Cx Clock Divide Control Register

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	CLKDIV	Clock Divider Factor (only for master mode). I2Cx clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as follows: SCL=PCLK/(CLKDIV*16)	RW	0

14.2.3 I2Cx_STAT

I2CX Status Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7	TRC	Transmit/Receive Complete Bit. The bit is automatically set when the buffer is empty in transmit mode or when the buffer is full in receive mode. Writing 1 to this bit will clear it. In transmitting mode: 0: Transmitting in progress 1: Transmitting complete In receiving mode: 0: Receiving in progress 1: Receiving complete	RW	0

6	STPD	STOP Detect Bit. The bit will be cleared when the I2C mode disables or when the START condition is detected again. Writing 1 to the bit will clear it. 1: Indicate that the STOP bit is detected 0: STOP bit is not detected	RW	0
5	STAD	START Detect Bit. The bit is cleared when the I2C mode disables or when the STOP condition is detected. Writing 1 to the bit will clear it. 1: Indicate that the START bit is detected 0: START bit is not detected	RW	0
4	RWST	Read/Write Status Bit (only for Slave mode). When in slave mode, this bit reflects the master device read from or writes to the slave device if the last address is matched. This bit is valid before the next start bit, stop bit or NAK bit occurred. 1: Read 0: Write	RW	0
3	LBST	Last Byte Status Bit. 1: Indicate the last byte received or transmitted is data 0: Indicate the last byte received or transmitted is address	RW	0
2	IRQP	IRQ Pending Bit. Writing 1 to this bit will clear it. 1: IRQ 0: No IRQ	RW	0
1	OVST	Overflow Status Bit. Writing 1 to this bit will clear it. 1: A new byte is received whereas the previous byte has not been read 0: No overflow	RW	0
0	WCO	Writing Collision Bit. Writing 1 to this bit will clear it. 1: The I2C data register is written when it is still transmitting the previous byte. 0: No collision	RW	0

Note: Whenever writing collision or overflow is set, NAK will occur automatically.

14.2.4 I2Cx_ADDR

I2Cx Address Register

Offset=0x000C

Bit	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:1	SDAD	Slave Device Address. In master mode, these bits are I2C slave device address. In slave mode, these bits are used to compare with the address that the master device sends out.	RW	0
0	RWCM	Read/Write Control or Match. In master mode, the bit is read/write control bit. 0: Write 1: Read In slave mode, the bit is slave address match bit. 0: Not match, do not send the IRQ 1: Match, I send IRQ to MCU	RW	0

14.2.5 I2Cx_DAT

I2Cx Data Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	TXRXDAT	Transmit/Receive Data.	RW	0

15 SPI Interface

15.1 Description

The SPI can be configured as either a master or slave device. During an SPI transfer, data is shifted out and shifted in (transmitted and received) simultaneously. The SPI_SCK line synchronizes the shifting and sampling of the information. It is an output when the SPI is configured as a master or an input when the SPI is configured as a slave.

The SPI uses a couple parameters called clock polarity (CPOL) and clock phase (CPHA) to determine when data is valid with respect to the clock signal. These must be set on the Master and all the Slaves in order for communication to work. CPOL determines whether the leading edge is defined to be the rising or falling edge of the clock (and vice versa for the trailing edge). CPHA determines whether the leading edge is used for setup or sample (and vice versa for the trailing edge).

15.2 Register List

SPI Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address
SPI	0x10080000	0xB0080000

The register block contains the registers.

SPI Registers Offset Address

Offset	Register Name	Description
0x0000	SPI_CTL	SPI Control Register
0x0004	SPI_CLKDIV	SPI Clock Divide Register
0x0008	SPI_STAT	SPI Status Register
0x000c	SPI_RXDAT	SPI Receive FIFO Data Register
0x0010	SPI_TXDAT	SPI Transmit FIFO Data Register

15.2.1 SPI_CTL

SPI Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset

31:24	-	Reserved	R	0
23:22	RDIC	RX DRQ/IRQ Control. 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	0
21:20	TDIC	TX DRQ/IRQ Control. 00: set when TX FIFO is 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	0
19	TWME	Two wire mode enable bit 0: normal 4 wire mode 1: two wire mode, use two pin, SPI_CLK and SPI_MOSI	RW	0
18	EN	Enable. 0: Disable 1: Enable	RW	0
17:16	RWC	R/W control 00: no effect 01: write only 10: read only 11: write and read	RW	00
15	DTS	DMA transfer start（available only in master read only mode） 0: DMA transfer over.(this bit will be cleared to 0 when transfer over) 1: DMA transfer start(write 1 will start the DMA data transfer)	RW	0
14	SSATEN	SPI_SS active automatically enable when in mode 0 and mode 2 0:disable 1:enable	RW	0
13	RXBL	SPI RX DMA block mode enable 0: demand mode 1: block mode	RW	0

12	TXBL	SPI TX DMA block mode enable 0：demand mode 1：block mode	RW	0
11	CEB	Convert Endian bit 0: not convert Endian 0x3210 ->0x3210 1: convert Endian 16bit mode: 0x3210->0x1032 MSB or LSB first shift in or out	RW	0
10	FMS	SPI fast mode select, only apply to SPI master mode. 0: synchronization design, SPICLK=HCLK/(CLKDIV*2), the least value of CLKDIV is 3, so the least divide is 6. 1: fast mode, SPICLK=HCLK/(CLKDIV*2), but when CLKDIV is set to 0, the divide is 1. so the least divide is 1.	RW	0
9	MS	Master/Slave Select. 0: Master 1: Slave	RW	0
8	DAWS	Data/Address Width. Select 0: 8 bit data and address 1: 16 bit data and address	RW	0
7:6	CPOS	Clock Polarity Select. CPOL CPHA 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3	RW	b11
5	LMFS	LSB/MSB First Select. 0:Transmit and receive MSB first 1:Transmit and receive LSB first	RW	0
4	SSCO	SPI_SS Control Output (only for master mode). 1: output high 0: output low.	RW	1
3	TIEN	TX IRQ Enable. 0: Disable 1: Enable	RW	0
2	RIEN	RX IRQ Enable. 0: Disable 1: Enable	RW	0

1	TDEN	TX DRQ Enable. 0: Disable 1: Enable	RW	0
0	RDEN	RX DRQ Enable. 0: Disable 1: Enable	RW	0

Note:

1. The bit 14 is valuable only operation in the mode 0、mode2.
2. When the TMS=1 & RWC=10, the controller will automatically send the clock.
3. When the TMS=1 & RWC=11, the controller will send the clock depend on the data of register SPI_TXDATA.
4.When the data<4 bytes(8 bit mode)、data<8 bytes(16 bit mode), the DMA mode should not used.
5. The select DMA mode or CPU mode depend on the [TDEN] and [RDEN].

15.2.2 SPI_CLKDIV

SPI Clock Divide Control Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9:0	CLKDIV	Depend on the SPI_CTL bit 10: SPICLK=HCLK/(CLKDIV*2), When not select fast mode, the least value of CLKDIV is 3, so the least divide from HCLK is 6. Supporting SPI clock rate up to 15MHz. When SPI master selects fast mode, the least value of CLKDIV is 0.when CLKDIV is set to 0, the divide is 1. So the least divide is 1. Supporting SPI clock rate up to 60MHz.	RW	0

15.2.3 SPI_STAT

SPI Status Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0

9	TFEM	TX FIFO Empty. 1: Empty 0: Not Empty	R	1
8	RFFU	RX FIFO Full. 1: Full 0: Not Full	R	0
7	TFFU	TX FIFO Full. 1: Full 0: Not Full	R	0
6	RFEM	RX FIFO Empty. 1: Empty 0: Not Empty	R	1
5	TFER	TX FIFO Error. When overflow, the bit is set to 1. Writing 1 to the bit will clear the bit and reset the FIFO.	RW	0
4	RFER	RX FIFO Error. When overflow, the bit is set to 1. Writing 1 to the bit will clear the bit and reset the FIFO.	RW	0
3	-	Reserved	R	0
2	TCOM	Transfer Complete Bit. DMA mode: bit will be set to 1 when all the data sent out CPU mode: will be set to 1 when very byte data sent out Write 1 will clear to zero	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit will clear it.	RW	0
0	PIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to this bit will clear it.	RW	0

Note

1. When the SPI_CTL[RWC]=11 and :

TX: DMA mode, RX: CPU mode

Or TX: CPU mode, RX: DMA mode

Than SPI_STA[TCOM] will be set to 1 when every byte data sent out.

15.2.4 SPI_RXDAT

SPI RX Data Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	RXDAT	Receive Data. The depth of RXFIFO is 16bit×16 levels.	R	x

15.2.5 SPI_TXDAT

SPI TXData Register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	TXDAT	Transmit Data. The depth of RXFIFO is 16bit×16 levels.	W	x

16 UART (2) Interface

16.1 Description

ATJ2256/ATJ2257/ATJ2257B Platform contains two UART interfaces. Each UART has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Interrupts for Receive FIFO Half Full and Not Empty
- Interrupts for Transmit FIFO Empty and Half Empty
- Support RTS/CTS Automatic Hardware Flow Control on UART1 to reduce interrupts to host system
- Capable of speeds up to 1.5Mbs to enable connections with Bluetooth and other peripherals
- UART2 has Infrared Data Association(IrDA) Inputs and Outputs (Optional)

16.2 Register List

Each UART is controlled by a register block.

UART Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address
Uart1	0x10160000	0xB0160000
Uart2	0x10160020	0xB0160020

The register block contains the registers.

UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register
0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register
0x000c	UARTx_STAT	UART Status Register

16.2.1 UART1_CTL

UART1 Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. Both in UART and IR. 0: Disable 1: Enable	RW	0
19	TXIE	UART1 TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART1 RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART1 TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART1 RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART1 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0
14	TRFS	UART1 TX/RX FIFO Select TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART1_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set.	RW	0

12	AFE	Autoflow Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals.	RW	0
11:10	RDIC	UART1 RX DRQ/IRQ Control 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
9:8	TDIC	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is 1 byte leave in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
7	BLOC	Uart1 DMA block mode Enable 0:demand 1:Block	RW	0
6:4	PRS	Parity Select. Bit 4: EPS, Even parity Bit 5: STKP, Stick parity Bit 6: PEN, Parity enable PEN EPS STKP Selected Parity 0 x x None 1 0 0 Odd 1 0 1 Even 1 1 0 logic 1 1 1 1 logic 0	RW	000
3	-	Reserved	R	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	RW	0

1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	00

Note: 1. The UART module should be reset for the next time usage.

16.2.2 UART1_RXDAT

UART1 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
8:0	RXDAT	Received Data. The depth of FIFO is 9bit×16 levels. Bit 8 is error status bit.	R	x

16.2.3 UART1_TXDAT

UART1 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
7:0	TXDAT	Transmit Data. The depth of FIFO is 8bit×16 levels.	R	x

16.2.4 UART1_STAT

UART1 Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:11	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0

10	TFES	TX FIFO empty Status 0: empty 1: no empty	R	0
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	x
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

Note:

1. Software should reset the Uart module when some error information is detected.

16.2.5 UART2_CTL

UART2 Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:24	-	Reserved	R	0
23	PWS	SIR pulse width select 0: 3/16 bit width 1: 1.6us width, (support baudrate from 9600 to 115200 bps)	RW	0
22	IRTR	IR TX Reverse bit, 0: disable; 1: enable	RW	0
21	IRRR	IR RX Reverse bit, 0: disable; 1:enable	RW	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. Both in UART and IR. 0: Disable 1: Enable	RW	0
19	TXIE	UART2/IR TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART2/IR RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART2/IR TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART2/IR RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART2/IR Enable. When this bit is cleared, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0

14	TRFS	TX/RX FIFO Select. TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART2_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13:12	MS	Mode Select. 00: UART2 01: IRDA-SIR 10: IRDA-MIR 11: IRDA-FIR	RW	0
11:10	RDIC	UART2 RX DRQ/IRQ Control 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	0
9:8	TDIC	UART2 TX DRQ/IRQ Control 00: set when TX FIFO is 1 byte leave in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	0
7	BLOC -	Uart2 DMA block mode Enable 0: demand 1: Block	R	0
6:4	PRS	Parity Select. Bit 4: EPS, Even parity Bit 5: STKP, Stick parity Bit 6: PEN, Parity enable PEN EPS STKP Selected Parity 0 x x None 1 0 0 Odd 1 0 1 Even 1 1 0 logic 1 1 1 1 logic 0	RW	0

3	VFIRE	VFIR Function enable 0: disable 1: enable	RW	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. The receiver always checks 1 stop bit only.	RW	0
1:0	DWLS	Data Width Length Select. 00: 5bit 01: 6bit 10: 7bit 11: 8bit	RW	00

Notes

1. The Uart module should be reset when the next time usage.

16.2.6 UART2_RXDAT

UART2 Receive FIFO DATA Register

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9:0	RXDAT	UART2/IR Received Data. The depth of FIFO is 10bit×8 levels. The 9th bit is the error bit, the 8th bit is the end of package bit and the 7:0 bits is the data.	R	x

16.2.7 UART2_TXDAT

UART2 Transmit FIFO DATA Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8:0	TXDAT	UART2/IR Transmit Data. The depth of FIFO is 9bit×8 levels. The 8th bit is the end of package bit and the 7:0 bits is the data.	W	x

16.2.8 UART2_STAT

UART2 Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:11	TRFL	UART2/IR TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0
10	TFES	TX FIFO empty Status 0: empty 1: no empty	R	0
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	IRES	IR EOP Status. Writing the bit to high when next writing IR TX FIFO is the last byte of the packet. Next writing TX FIFO after this bit is set will clear this bit automatically. When read from this bit, the EOP status bit of IR receiver is returned. This bit can be polled by MCU to see if end of package is reached.	RW	0
7	IRCE	IR CRC Error Flag Bit (only in MIR or FIR mode). Write 1 to this bit will clear it.	RW	0
6	TFFU	UART2/IR TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	UART2/IR RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	UART2/IR Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	UART2/IR TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0

2	RXER	UART2/IR RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP	UART2/IR TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	UART2/IR RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

Note:

1. Software should reset the UART module when some error information is detected.

17 IR Interface

17.1 Description

IrDA is a standard defined by IrDA consortium (Infrared Data Association). It specifies the way to transfer data via infrared radiation wireless. The IrDA specifications include standards for both the physical devices and the protocols used to communicate with each other. IrDA devices conform to standards IrDA 1.0 and 1.1.

Speed for IrDA v1.0 ranges from 2400bps to 115200bps. Pulse modulation with 3/16 of the length of the original duration of a bit is used. Data format is the same as a serial port asynchronously transmitted word, with a start bit at the beginning.

IrDA v1.1 defines the speed 0.576 and 1.152 Mbps for MIR mode and 4Mbps for FIR mode with 1/4 mark-to-space ratio.

For MIR mode, the basic unit (packet) is transmitted synchronously, with a starting sequence at the beginning. A packet consists of two start words followed by a target address (IrDA devices are assigned numbers by the means of IrDA protocol, so they are able to unambiguously identify themselves), data, CRC-16 and a stop word.

IR Interface Modes

Mode	Speed	CLK setting	Compliance
SIR	2.4 to 115.2kbps	Depend on the UART2_CTL bit 23: When select pulse width 3/16 bit : BaudRate*16=CORE_CLK/UART2_CLK_DIV When select pulse width 1.6u, (support baudrate from 9600 to 115200 bps) BaudRate*16*16= CORE_CLK/UART2_CLK_DIV	IrDA 1.0
MIR	0.576 and 1.152 Mbps	BaudRate*8=CORE_CLK/UART2_CLK_DIV	IrDA 1.1 with error detection
FIR	4 Mbps	24M=CORE_CLK/UART2_CLK_DIV	IrDA 1.1 with error detection

17.2 Register List

IR Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address
IR	0x10160000	0xB0160000

IR Registers Offset Address

Offset	Register Name	Description
0x0030	IR_PL	IrDA Packet Length Register
0x0034	IR_RBC	IrDA Receive Byte Count Register

17.2.1 IR_PL

IrDA Packet Length Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:13	-	Reserved	R	0
12:0	MAXSPL	Maximum Send Packet Length (only used in MIR or FIR mode).	RW	0

17.2.2 IR_RBC

IrDA Receive Byte Count Register

Offset=0x0014

Bit	Name	Description	R/W	Reset
31:13	-	Reserved	R	0
12:0	CRXBN	Current Received Bytes Number (only used in MIR or FIR mode). Writing the field to reset it.	RW	0

18 SPDIF Interface

18.1 Register List

SPDIF Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address

SPDIF	0x10140000	0xB0140000

SPDIF Registers Offset Address

Offset	Register Name	Description
0x0000	SPDIF_CTL	SPDIF Control Register
0x0004	SPDIF_STAT	SPDIF Status Register
0x0008	SPDIF_TXDAT	SPDIF TX FIFO Data Register
0x000c	SPDIF_RXDAT	SPDIF RX FIFO Data Register
0x0010	SPDIF_TXCSTAT	SPDIF TX Channel Status Register
0x0014	SPDIF_RXCSTAT	SPDIF RX Channel Status Register

18.1.1 SPDIF_CTL

SPDIF Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15	EN	SPDIF Enable. 0: Disable (will reset the RX and TX state machine) 1: Enable	RW	0
14	TRFS	SPDIF TX/RX FIFO Select. TX/RX FIFO Level is reflected in bit 15 to bit 12 of SPDIF_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13:12	-	Reserved	R	0
11:10	TDIC	SPDIF TX DRQ/IRQ Control. X0:set when FIFO is empty X1:set when FIFO is half empty In DMA DRQ mode,this field must be set X1. In DMA mode，TX fifo empty is at least 2 bytes remained.	RW	0
9:8	RDIC	SPDIF RX DRQ/IRQ Control. X0:set when FIFO is half full X1:set when at least one byte is received In DMA DRQ mode,this field must be set X0.	RW	0
7	TXDE	SPDIF TX DRQ Enable. 0: Disable 1: Enable	RW	0

6	RXDE	SPDIF RX DRQ Enable. 0: Disable 1: Enable.	RW	0
5	TXIE	SPDIF TX IRQ Enable. 0: Disable 1: Enable.	RW	0
4	RXIE	SPDIF RX IRQ Enable. 0: Disable 1: Enable.	RW	0
3	BIE	SPDIF Block IRQ Enable. 0: Disable 1: Enable	RW	0
2	TXFR	SPDIF TX FIFO Reset. (also reset the TX state machine). 0: FIFO reset valid 1: FIFO reset invalid.	RW	0
1	RXFR	SPDIF RX FIFO Reset. (also reset the RX state machine). 0: FIFO reset valid 1: FIFO reset invalid	RW	0
0	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0

18.1.2 SPDIF_STAT

SPDIF Status Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:18	-	Reserved	R	0
17	TFES	TX FIFO empty Status 0: empty 1: no empty	R	0
16	RFFS	RX FIFO full Status 0: no full 1: full	R	0
15:12	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0

11:10	-	Reserved	R	0
9:8	SAMRD	Sample Rate Detected. 00:44.1 kHz 01:DC 10:48 kHz 11:32 kHz	R	0
7	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
6	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
5	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
4	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0
3	BIP	SPDIF Block IRQ Pending Bit. (receive the B preamble) 0: No IRQ 1: IRQ Writing 1 to this bit will clear it.	RW	0
2	TFEP	TX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to this bit will clear it or reset FIFO clear it.	RW	0
1	RFEP	RX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to this bit will clear it or reset FIFO clear it.	RW	0
0	RERP	Receive Error Pending Bit. 0: No Error 1: Error Writing 1 to this bit will clear it.	RW	0

18.1.3 SPIDF_TXDAT

SPDIF TX FIFO DATA Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:26	-	Reserved	R	0
25:0	TXDAT	SPDIF TX FIFO DATA. The depth of TX FIFO is 26bit x 8 levels. Note: bit[23:0] is the really send data.	W	x

18.1.4 SPDIF_RXDAT

SPDIF RX FIFO DATA Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:26	-	Reserved	R	0
25:0	RXDAT	SPDIF RX FIFO DATA. The depth of TX FIFO is 26bit x 8 levels. Note: bit[23:0] is the really received data. Bit[25:24] is the data type 00: B 01: W 10: M 11:reserved	R	x

18.1.5 SPDIF_TXCSTAT

SPDIF TX Channel Status Register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:0	TXCSTAT	SPDIF TX Channel Status.	RW	x

Note: For TX:

There is no channel status CRC to transfer. The SPDIF_TXSTAT just mapped to first 32 bit of every 192 frames data and the remained bit will be set to zero by the hardware.

18.1.6 SPDIF_RXCSTAT

SPDIF RX Channel Status Register

Offset=0x14

Bits	Name	Description	R/W	Reset
31:0	RXCSTAT	SPDIF RX Channel Status.	RW	x

Note:

For RX:

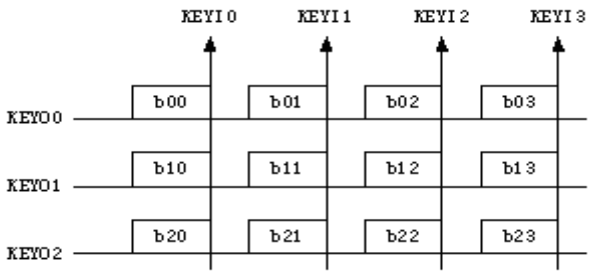
There are 192 bits status data per 192 frames transfer. The SPDIF_RXSTAT register only receive the bit 32 bit data ever 192 frames data of the left channel status.

19 Key Scan

19.1 Description

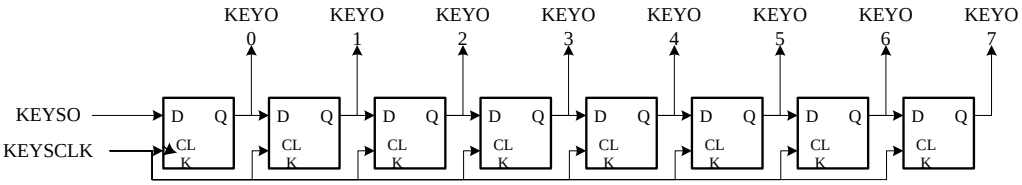
The Key Scan supports parallel mode and serial mode. The max scan matrix in serial mode is 4x16. There are 4 key scan data registers. For each byte (there are 4 bytes for each register), only the low 4 bits are valid.

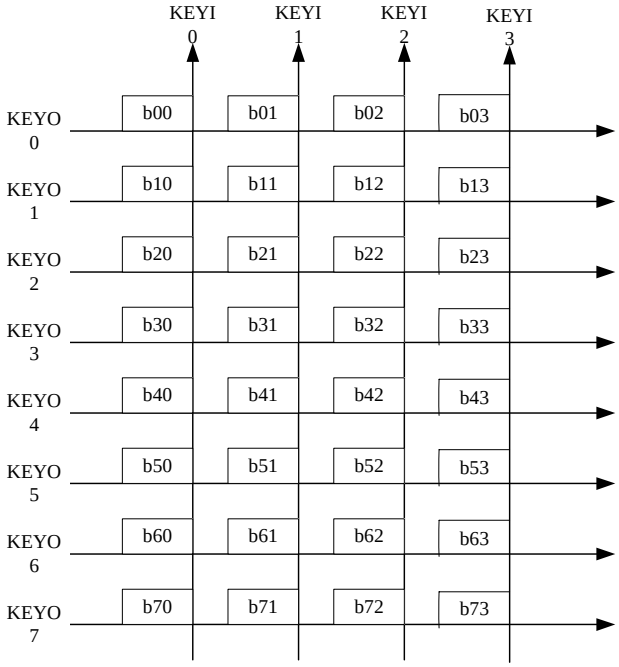
In parallel mode, the max scan matrix is 3x4 and is shown as follows:



Max Key Scan Matrix in Parallel Mode

In the serial mode, one or more external shift register chips should be used. The following is a 4x8 scan matrix example.

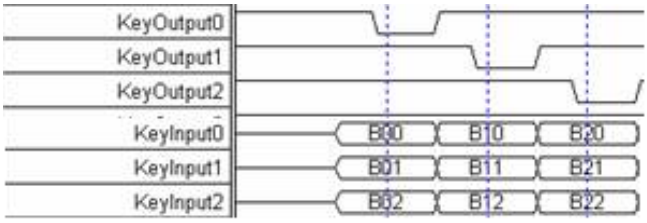




4*8 Key Scan Matrix in Serial Mode

Note: KEYSO is PIN KEYO1, KEYSCLK is PIN KEYO0.

The whole timing is as follows (parallel mode):



The Whole Key Scan Timing

In serial mode, two external 8bit shift registers can be used at least, that is to say, the

maximum scan matrix is 4x16.

The state machine of KEY controller is described as below:

Idle	Debounce	Scan	Wait	Idle

Idle is active when no key is touched. Normally the time of Idle is equal to the time of one line scan. When key touch is not occurred again, the idle state will be extended to the time of scan period in order to save power in serial mode.

19.2 Register List

Key Scan Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address
KEY	0x101A0000	0xB01A0000

Key Scan Registers Offset Address

Offset	Register Name	Description
0x0000	KEY_CTL	Key Scan Control Register
0x0004	KEY_DAT0	Key Scan Data Register0
0x0008	KEY_DAT1	Key Scan Data Register1
0x000c	KEY_DAT2	Key Scan Data Register2
0x0010	KEY_DAT3	Key Scan Data Register3

19.2.1 KEY_CTL

Key Scan Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:27	-	Reserved	R	0
26:24	WTS	Key Scan Wait Time Select. KeyScan Wait Time=WTS*32ms	RW	0
23	–	Reserved		
22:20	KOUTEN	Key Scan output (KEYO[2:0])enable bit 0:Mask Key scan output 1: Enable Key scan output These bits are available for Parallel/Serial Mode	RW	0

19	OTYP	KSOUT pin output type, Only for Parallel Key mode 0: Opendrain output. 1: push pull output	RW	0
18	IRCL	Key Scan IRQ Cleared (only used when shutting down APB Clock).	R	0
17	IRP	Key Scan IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear the bit.	RW	0
16	IREN	Key Scan IRQ Enable. 0: Disable 1: Enable	RW	0
15:12	–	Reserved		
11:8	INMKEN	Key Scan Input (KEYI[3:0]) Mask Enable. 0: Mask Key Input 1: Enable Key Input When any pin of KEYI[3:0] is masked, it can used as GPIO, even if key scan mode is active.	RW	0
7:6	MATS	Key Scan Matrix Select (Only active in serial mode). 00: 8*4. Use Key_DAT0 register. 01: 8*8. Use Key_DAT0 and Key_DAT1 registers. 10: 8*16. Use registers from Key_DAT0 to Key_DAT3 11: Reserved	RW	0
5:4	PRS	Key Scan Period Select. 00: 40ms 01: 80ms 10: 160ms 11: 320ms	RW	0
3:2	DTS	Key Scan Debounce Time Select. 00: 10ms 01: 20ms 10: 40ms 11: No debounce time The decounce time is 24MHz dividing frequency.	RW	0
1	MS	Key Scan Mode Select. 0: Parrel Mode 1: Serial Mode	RW	0
0	EN	Key Scan Enable. 0: Disable 1: Enable	RW	0

19.2.2 KEY_DAT0

Key Scan Data Register0

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data	R	x

19.2.3 KEY_DAT1

Key Scan Data Register1

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data	R	x

19.2.4 KEY_DAT2

Key Scan Data Register2

Offset=0x000c

Bit	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data	R	x

19.2.5 KEY_DAT3

Key Scan Data Register3

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data	R	x

20 GPIO and Multi-function Configuration

20.1 Description

There is 64 bit General purpose IO port in ATJ2256/ATJ2257/ATJ2257B. Each GPIO is controlled by corresponding bit in GPIOx_Out_En reg and GPIOx_In_En reg.

20.1.1 Multi-function

There many multi function pin in ATJ2256/ATJ2257/ATJ2257B. The register Multi_con0 and Multi_con1 can control the pad's function. Some special pads with build-in pull up or pull down resistance.

20.1.2 GPIO/Function pin

There are 64 GPIO in ATJ2256/ATJ2257/ATJ2257B. GPIO share pads with many functional pads. The GPIO function has the highest priority. That is to say, if GPIO enables input or output, the corresponding functional signal is masked.

20.1.3 Pad with Built-in Resistance

1. SD data bus:
SD_D0~D7, SD_CMD, pull up 50k
2. NF
NF_RB 2.2k pull up
3. I2C
SDA, SCL 4.7k pull up
4. Keyin
600K pull up

20.2 Register List

GPIO Registers Block Base Address

Module name	Physical Bass Address	KSEG1 Base Address
GPIO	0x101C0000	0xB01C0000

GPIO Registers Offset Address

Offset	Register Name	Description
0x0000	GPIO_AOUTEN	GPIOA Output Enable Register
0x0004	GPIO_AINEN	GPIOA Input Enable Register
0x0008	GPIO_ADAT	GPIOA Data Register
0x000c	GPIO_BOUTEN	GPIOB Output Enable Register
0x0010	GPIO_BINEN	GPIOB Input Enable Register
0x0014	GPIO_BDAT	GPIOB Data Register
0x0018	GPIO_MFCTL0	Multi-function Control Register0
0x001c	GPIO_MFCTL1	Multi-function Control Register1

20.2.1 GPIO_AOUTEN

GPIOA Output Enable Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:0	OUTEN	GPIOA[31:0] Output Enable. 0: Disable 1: Enable	RW	0

20.2.2 GPIO_AINEN

GPIOA Input Enable Register

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:0	INEN	GPIOA [31:0] Input Enable. 0: Disable 1: Enable	RW	0

20.2.3 GPIO_ADAT

GPIOA Data Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:0	IODAT	GPIOA [31:0] Input/Output Data.	RW	0

20.2.4 GPIO_BOUTEN

GPIOB Output Enable Register

Offset=0x000c

Bit	Name	Description	R/W	Reset
31:0	OUTEN	GPIOB [31:0] Output Enable. 0: Disable 1: Enable	RW	0

20.2.5 GPIO_BINEN

GPIOB Input Enable Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:0	INEN	GPIOB [31:0] Input Enable. 0: Disable 1: Enable	RW	0

20.2.6 GPIO_BDAT

GPIOB Data Register

Offset=0x0014

Bit	Name	Description	R/W	Reset
31:0	IODAT	GPIOB [31:0] Input/Output Data.	RW	0

20.2.7 GPIO_MFCTL0

Multi-function Control Register0

Offset=0x0018

Bit	Name	Description	R/W	Reset
31	-	Reserved	R	0
30:29	OTGDRV	OTG DRVVBUS Multi Function. 00: Reserved 01: OTG_DRVVBUS 10: RGB_RDB 11: Reserved	RW	01
28:27	-	Reserved	RW	01
26:22	-	Reserved	RW	0
21:20	CEB6	CEB6 Multi-function. 00: reserved 01: reserved 10: RGB_CE 11: SDCLK	RW	11
19:18	-	Reserved	RW	11
17:16	CEB4	CEB4 Multi Function. 00: NOR_CEB4 01: RGBS_CE 10: RGB_CE 11: Reserved	RW	11
15:14	CEB3	CEB3 Multi-function. 00: reserved 01: NandFlash_CEB3 10: RGB_CE 11: reserved	RW	10
13:12	CEB2	CEB2 Multi-function. 00: reserved 01: NandFlash_CEB2 10: RGB_CE 11: reserved	RW	01

11:10	CEB1	CEB1 Multi-function. 00: reserved 01: NandFlash_CEB1 10: RGB_CE 11: reserved	RW	01
9:8	CEB0	CEB0 Multi-function. 00: reserved 01: NandFlash_CEB0 10: RGB_CE 11: reserved	RW	0
7:6	WRRD	Write and Read (WR and RD) Multi-function. 00: reserved 01: NandFlash_WR and NandFlash_RD 10: RGB_WRB and RGB_RDB 11: reserved	RW	0
5:3	NAND_D[7:0]	NAND_D[7:0] Multi-function. 001: NandFlash_D[7:0] 010: RGB_WD[17:10] Others: Reserved	RW	0
2:0	NAND_D[15:8]	NAND_D[15:8] Multi-function. 001: NandFlash_D[15:8] 010: RGB_WD[8:1] 100: SD_D[7:0] Others: Reserved	RW	0

20.2.8 GPIO_MFCTL1

Multi-function Control Register1

Offset=0x001c

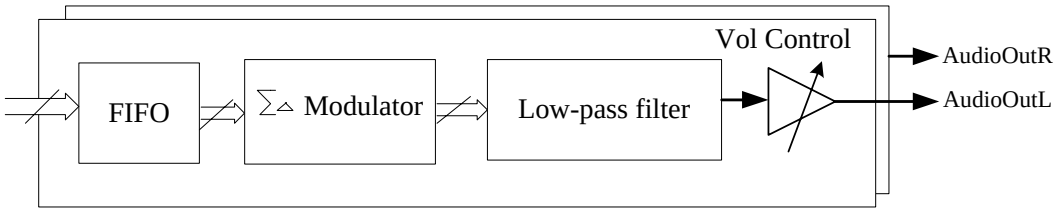
Bit	Name	Description	R/W	Reset
31	MFEN	Multi Function Enable. 0: Disable 1: Enable	RW	0
30:18	-	Reserved	R	0
17	SD2E	Select SD Card Clock Output Enable. 0:Disable 1:Enable	RW	0

16	–	Reserved	RW	0
15:14	–	Reserved	RW	00
13:12	–	Reserved	RW	1
11	SIR0	SIRQ0 Multi Function. 0: SIRQ0 1: Reserved Pad Enables by MFEN.	RW	0
10:9	-	Reserved		0
8	U2TR	UART2 TX and RX Multi Function. 0: UART2_TX and UART2_RX 1: I2C2_SCL and I2C2_SDA Pad Enables by MFEN.	RW	0
7:6	U1TR	UART1_TX and UART1_RX Multi Function. 00: UART1_TX and UART1_RX 01: SPI_SS and SPI_MISO 10: I2C2_SCL and I2C2_SDA 11: SPDIF_Pin1 and SPDIF_Pin2 Pad Enables by MFEN.	RW	0
5:4	I2C1SS	I2C1 SCL and SDA Multi Function. 00: I2C1_SCL and I2C1_SDA 01: UART2_TX and UART2_RX 10: Reserved 11: Reserved Pad Enables by MFEN.	RW	0
3:1	-	Reserved	RW	0
0	BT656	BT656] Multi Function. 0: NOR_A[17:6] 1: BT656_CLKOUT, VSYNC, HSYNC, PCLK, D[7:0] Pad Enables by MFEN or CE0S.	RW	0

21 DAC and Headphone Driver

21.1 Description

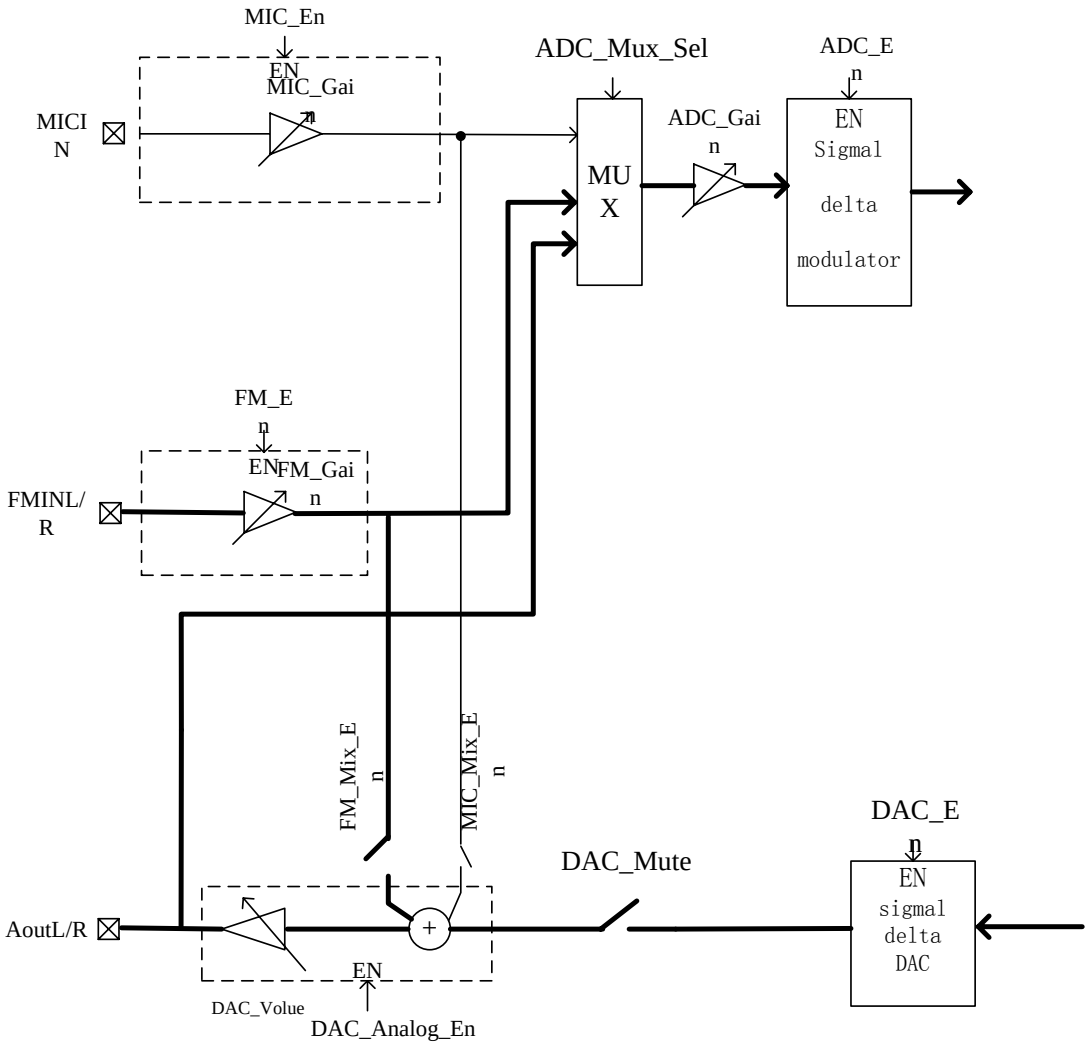
ATJ2256/ATJ2257/ATJ2257B's internal DAC is an on-chip Sigma-Delta Modulator of which an 18-bit high performance DAC is composed. DAC interface supports 8-level play back FIFO (16 X 24bit PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz).



DAC Block Diagram

The following is ADDA Analog diagram:

ADDA Analog diagram



21.2 Register List

DAC Registers Block Base Address

Module Name	Physical Bass Address	KSEG1 Base Address
DAC	0x10100000	0xB0100000

DAC Registers Offset Address

Offset	Register Name	Description
0x0000	DAC_CTL	DAC Control Register

0x0004	DAC_FIFOCTL	DAC FIFO Control Register
0x0008	DAC_DAT	DAC Data Register
0x000c	DAC_Debug	DAC Debug Register
0x0010	DAC_Analog	DAC Analog Register

21.2.1 DAC_CTL

DAC Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:30	-	Reserved	RW	0
29:24	-	Reserved	R	000011
23:20	-	Reserved	RW	0
19:18	DIAM	DAC Dither Amplitude. 00: ×1/8 01: ×1/4 10: ×1/2 11: ×1	RW	00
17	DDEN	DAC Dynamic Dither Enable. 0: Disable 1: Enable	RW	0
16	DIEN	DAC Dither Enable. 0: Disable 1: Enable	RW	0
15:12	QUL	Internal DAC Quantization Levels. Levels=[3*(22+QUL[3:0])]/64, Default levels=3*27/64=1.27	RW	1001
11	QUBS	Internal DAC Quantization Bit Select. 0: 3bit 1: 1bit	RW	1
10	MOEN	DAC Mono Enable. 0: Stereo, 8 levels FIFO 1: mono, 16 levels FIFO When enabled, L & R channel sends same data.	RW	0
9:8	-	Reserved	R	00
7	-	Reserved	RW	0

6:4	-	Reserved	R	000
3	-	Reserved	RW	0
2	SRS	Internal DAC Sample Rate Select. 0: Sample Rate Internal Set 1: Reserved	RW	0
1	OUTS	Internal DAC Output Select. 0: On-chip Sigma-Delta 1: Reserved	RW	0
0	EN	Internal DAC Enable. 0: Disable 1: Enable	RW	0

21.2.2 DAC_FIFOCTL

DAC FIFO Control Register

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:14	-	Reserved	R	0
13	LRCS	DAC FIFO Debug Left/Right Channel Select. 0: Left 1: Right	RW	0
12	DDRF	DAC FIFO Debug Data Ready Flag. 0: Not Ready 1: Ready After DAC_DAT_Debug is read, the bit is automatically cleared.	R	0
11	FUF	DAC PLAYBACK FIFO FULL Flag. The above bits are also mapped into a 24-bit DSP memory mapped EM port 0x3FEEh, low byte of this port. DSP3FEEh.bit0: Reserved DSP3FEEh.bit1: Reserved DSP3FEEh.bit2: Internal DAC FIFO FULL	R	0
10	FEIP	DAC FIFO Empty IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

9	FEIE	DAC FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0
8	FEDE	DAC FIFO Empty DRQ Enable. 0: Disable 1: Enable	RW	0
7	-	Reserved	R	0
6:5	EMCO	DAC Empty Condition. 00: 16/16 Empty (All empty) 01: 15/16 Empty (Mono almost empty) 10: 14/16 Empty (Stereo almost empty) 11: 13/16 Empty	RW	01
4	DSPE	DAC DSP Port Enable. 0: Disable 1: Enable	RW	0
3	-	Reserved	RW	0
2:1	FINS	DAC FIFO Input Select. 00: APB 01: Reserved 10: Reserved 11: ADC	RW	0
0	FIRT	DAC FIFO Reset. 0: Reset FIFO 1: Enable FIFO	RW	0

21.2.3 DAC_DAT

DAC FIFO Data Register

Offset=0x0008

Bit	Name	Description	R/W	Reset
31:8	DAT	DAC FIFO Data	W	x
7:0	-	Reserved	R	0

21.2.4 DAC_Debug

DAC Debug Register

Offset=0x000c

Bit	Name	Description	R/W	Reset
31:8	DATDE	DAC Data Debug. Data is the same as the DAC reads from the FIFO. Speed of refreshing the register is equal to FS*2, whether stereo or mono. When DAC_Fifo_Debug_Flag (DDRF) becomes 1, the data is ready. DAC_Fifo_Debug_LR (LRCS) bit shows whether the data comes from left or right channel.	R	x
7:0	-	Reserved	R	0

21.2.5 DAC_ANALOG

DAC Analog Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:30	-	Reserved	R	0
29:27	PAAPCTL	PA Anti-pop Control. Note: 000 is the worst, 111 is the best.	RW	100
26	DACC	DAC Bias Current Control. Note: 00 is minimum, 11 is maximum.	RW	0
25:24	OPGCTL	OPG Bias Current Control. Note: 00 is minimum, 11 is maximum.	RW	01
23:22	PACCTL	PA Bias Current Control. Note: 00 is minimum, 11 is maximum.	RW	01
21:20	OPFCCTL	OPF Bias Current Control. Note: 00 is minimum, 11 is maximum.	RW	01
19:18	OP3CCTL	OPDA3P Bias Current Control. Note: 00 is minimum, 11 is maximum.	RW	01
17:15	OP12CCTL	OPDA1 & 2 Bias Current Controls. Note: 000 is minimum, 111 is maximum.	RW	011
14:13	OP0CTL	OP0 Output Stage Voltage Control. Note: 00 is minimum, 11 is maximum.	RW	01
12	ZCDE	DAC Zero Cross Detect Enable. 0: Disable 1: Enable	RW	0

11	PBM	Internal DAC Playback Mute. 0: Mute DAC Playback 1: Enable DAC Playback	RW	0
10	FIMM	FM Input to Analog Mixer Mute. 0: Mute 1: Not Mute	RW	0
9	–	Reserved	RW	0
8	MIMM	MIC Input to Analog Mixer Mute. 0: Mute 1: Not mute	RW	0
7:3	HAVC	Master/Headphone Amp Volume Control. Total 32 level, -1.8Db/step	RW	0
2	PAGC	PA Gain Control. 0: 1.2 Vpp 1: 1.6 Vpp	RW	0
1	AMPE	Internal Analog Mixer and PA Enable. 0: Disable 1: Enable	RW	0
0	EN	Internal DAC Analog Circuit Enable. 0: Disable 1: Enable	RW	0

22 ADC

22.1 Description

Internal microphone amplifier has gain for recording. VMIC pin is the power supply (2.57V) for microphone.

Audio ADC is a 21-bit Sigma-delta Analog-to-digital converter. Its input source can be selected from MIC amplifier or external FM, and it has two FIFO.

Fs supports 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz.

22.2 Register List

ADC Registers Block Base Address

Module name	Physical Bass Address	KSEG1 Base Address
ADC	0x10110000	0xB0110000

ADC Registers Offset Address

Offset	Register Name	Description
0x0000	ADC_CTL	ADC Control Register
0x0004	ADC_FIFOCTL	ADC FIFO Control Register
0x0008	ADC_DAT	ADC Data Register
0x000c	ADC_ANALOG	ADC Analog Register
0x0010	ADC_DEBUG	ADC Debug Register

22.2.1 ADC_CTL

ADC Control Register

Offset=0x0000

Bit	Name	Description	R/W	Reset
31:29	-	Reserved	R	1000

28	VMIC_CTL	VMIC Enable. 0: Disable 1: Enable	RW	0
27:26	AVCC_Voltage	AVCC Voltage 00: 0.15V 01: 0.20V 10: 0.25 11: 0.20V	RW	10
25	-	Reserved		1
24:23	ADCINGC	ADC Input Gain Control. 00: -6dB 01: -3dB 10: 00dB 11: +3dB	RW	10
22:21	ADCINS	ADC Input Source Select. 00: MIC 01: FM 10: Reserved 11: Internal Analog Mixer Output(AOUT)	RW	01
20:18	–	Reserved	RW	101
17	LIRE	Linein Right Channel Enable. 0: Disable 1: Enable	RW	0
16	LILE	Linein Left Channel Enable. 0: Disable 1: Enable	RW	0
15:13	FMGC	FM Input Gain Control: 000: -7.5db 001: -6.0db 010: -4.5db 011: -3.0db 100: -1.5db 101: 0db 110: 1.5db 111: 3.0db	RW	101
12	FMRE	FM Right Channel Enable. 0: Disable 1: Enable	RW	0

11	FMLE	FM Left Channel Enable. 0: Disable 1: Enable	RW	0
10:8	MIGC	MIC Gain Control. 000: ×1 001: ×10 010: ×20 011: ×30 100: ×40 101: ×50 110: ×60 111: ×70	RW	101
7	MIRE	MIC Right Channel Enable. 0: Disable 1: Enable	RW	0
6	MILE	MIC Left Channel Enable. 0: Disable 1: Enable	RW	0
5	ADRE	ADC Right Channel Enable. 0: Disable 1: Enable	RW	0
4	ADLE	ADC Left Channel Enable. 0: Disable 1: Enable	RW	0
3:1	-	Reserved ADC Sample Rate Set. (For Debug)	RW	101
0	-	Reserved 0: ADC Clock from CMU 1: ADC Clock from OSC (For Debug)	RW	0

22.2.2 ADC_FIFOCTL

ADC FIFO Control Register

Offset=0x0004

Bit	Name	Description	R/W	Reset
31:11	-	Reserved	R	0
10	-	Reserved	RW	0

9	FEF	ADC PLAYBACK FIFO Empty Flag. The above bits are also mapped into a 24-bit DSP memory mapped EM port 0x3FEEh, low byte of this port. DSP3FEEh. bit0: Reserved DSP3FEEh. bit1: Internal ADC FIFO Empty DSP3FEEh. bit2: Reserved	R	0
8	FFIP	ADC FIFO Full IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0
7	FFIE	ADC FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0
6	FFDE	ADC FIFO Full DRQ Enable. 0: Disable 1: Enable	RW	0
5:4	FIFU	Internal ADC FIFO Full Condition: 00: 16/16 Full (all full) 01: 15/16 Full (almost full) 10: 14/16 Full 11: 13/16 Full	RW	01
3	DSPE	ADC DSP Port Enable. 0: Disable 1: Enable	RW	0
2	APBE	ADC APB Port Enable. 0: Disable 1: Enable	RW	0
1	FINS	ADC FIFO Input Select. 0: ADC 1: Reserved	RW	0
0	FIRT	ADC FIFO Reset. 0: Reset FIFO 1: Enable FIFO	RW	0

22.2.3 ADC_DAT

ADC FIFO Data Register
Offset=0x0008

Bit	Name	Description	R/W	Reset
31:8	DAT	ADC FIFO Data. Simultaneously mapped into a 24-bit DSP memory mapped EM port 0x3FECh.	R	x
7:0	-	Reserved	R	0

22.2.4 ADC_Analog

ADC Analog Register

Offset=0x000c

Bit	Name	Description	R/W	Default
31:15	-	Reserved	R	0
14:12	OPAD3CS	OPAD3 in ADC Bias Current Select. 000: 0 level 001: 1 level 010: 2 level 011: 3 level 100: 4 level 101: 5 level 110: 6 level 111: 7 level	RW	101
11:9	OPAD2CS	OPAD2 in ADC Bias Current Select. 000: 0 level 001: 1 level 010: 2 level 011: 3 level 100: 4 level 101: 5 level 110: 6 level 111: 7 level	RW	101

8:6	OPAD1CS	OPAD1 in ADC Bias Current Select. 000: 0 level 001: 1 level 010: 2 level 011: 3 level 100: 4 level 101: 5 level 110: 6 level 111: 7 level	RW	011
5:3	LPFCS	Audio ADC LPF Bias Current Select. 000: 0 level 001: 1 level 010: 2 level 011: 3 level 100: 4 level 101: 5 level 110: 6 level 111: 7 level	RW	100
2:0	OPCS	OP in Audio ADC Pre-amplifies Bias Current Select: 000: 0 level 001: 1 level 010: 2 level 011: 3 level 100: 4 level 101: 5 level 110: 6 level 111: 7 level	RW	010

22.2.5 ADC_Debug

ADC Debug Register

Offset=0x0010

Bit	Name	Description	R/W	Reset
31:23	-	Reserved	R	0
22	DEDF	ADC Debug Data Channel Flag.	R	0

21	DERF	ADC Debug Ready Flag. 0: Not Ready 1: Ready Writing 1 to the bit will clear it.	RW	0
20:0	DEDAT	ADC Debug Data.	R	x

23 Electrical Characteristics

23.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	-0.3	2.4	V
	RTCVDD	-0.3	2.4	V
	VCC	-0.3	3.8	V
Input voltage	DC5V	-0.3	6	V
	BAT	-0.3	4.6	V
	IOVCC	-0.3	4.6	V
	IOVDD	-0.3	4.6	V
	LXVCC	-0.3	4.6	V
	LXVDD	-0.3	4.6	V
Junction Temperature	T_j		150	℃
Lead Temperature	(Soldering, 10 sec)		260	℃
Storage temperature	T_{stg}	-65	150	℃

Note:

1. TO = 25℃（Operating Temperature）， VDD = 1.8 V, VCC = 3.1 V.
2. Do not short-circuit two or more output pins simultaneously.
3. Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in the DC and AC characteristics are the ranges for normal operation and the quality assurance of the product.

23.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		20	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		20	pF

Note: T_O = 25℃, VCC = 0 V.

23.3 DC Characteristics

DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -2 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
High-level input voltage	V_{IH}		0.9VCC		VCC+0.3	V
Low-level input voltage	V_{IL}		-0.3		0.1VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V			±10	uA
Output leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V			±5	uA

Notes:

1. TA = 0 to +70℃, VDD = 1.8 V, VCC = 3.1 V
2. IVDD is a total power supply current for the 2.5 V power supply. IVDD is applied to the LOGIC and PLL and OSC block.
3. IVCC is a total power supply current for the 3.0 V power supply. IVCC is applied to the USB, IO, TP, and AD block.

Recommended Operating Condition

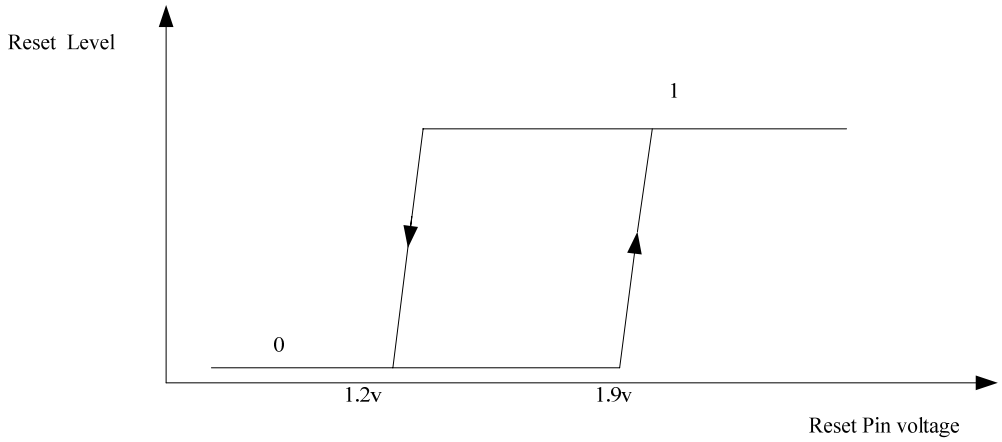
PINS	MIN	TYPE	MAX
DC5V	2.9 V	4.5V	5.5V
BAT	2.9V	3.9V	4.2V
VCC,GPIO	2.6V	3.1V	3.6V
VDD, RTCVDD（Note 1）	1.3V（Note 2）	1.8V	2.2V
IOVCC , IOVDD	2.9V	—	4.2V
LXVCC, LXVDD	-0.3V	—	4.2V

VMIC	2.4V	2.6V	2.8V

Note: 1: the recommended voltage differential between RTCVDD & VDD is <0.2V for normal working.

Note 2：VDD shall be no less than 1.6V when USB functions normally.

23.4 Reset Characteristics



Reset Hysteresis

Note: Reset Pin input has the characteristics of hysteresis. The relationship between reset level and reset pin is shown in Figure 17: upper threshold V_{T+}=1.9V, lower threshold V_{T-}=1.2V.

23.5 PMU

DC/DC Operating Voltages: When Li-ion mode: DC/DC operates with battery as low as 2.8V.

System Standby Dissipation

Parameter	MIN (uA)	Typical (uA)	MAX (uA)
IVCC+IAVCC		100	112.6
IVDD		40	55
IAVDD		3.5	4.5
RTCVDD		1.0[1]	

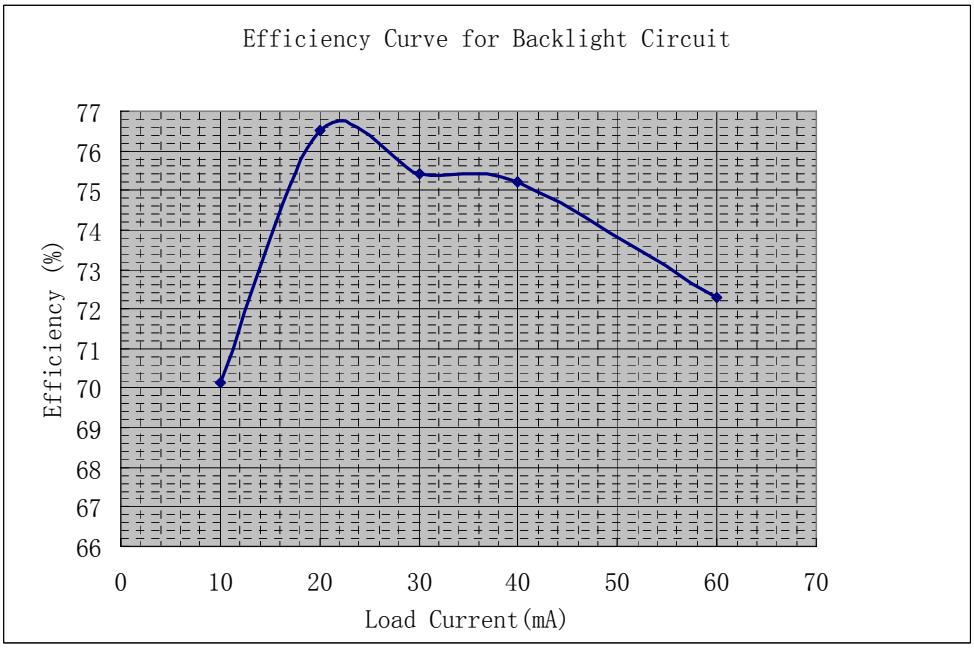
		0.3[2]	
IUVCC		150	175

Note1: When ex osc is enabled.

Note2: When ex osc is disabled.

LRADC Precision

ERROR / Parameter	MIN	TYPICAL	MAX	Unit
REMO_ADC	-	-	20	mV
BAT_ADC Li-ION	-	-	50	mV



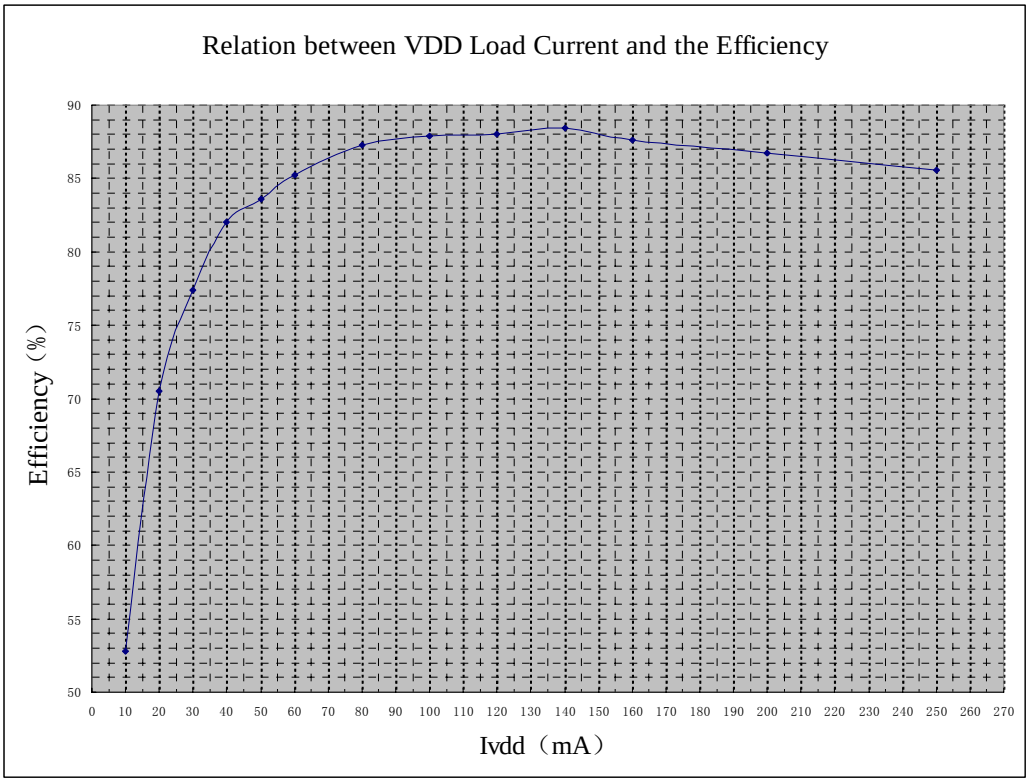
Efficiency Curve for Backlight Step Up Circuit

It is the ordinary TDK47uH inductor that has been applied in backlight circuit, and the diode is RB491D Schottky.

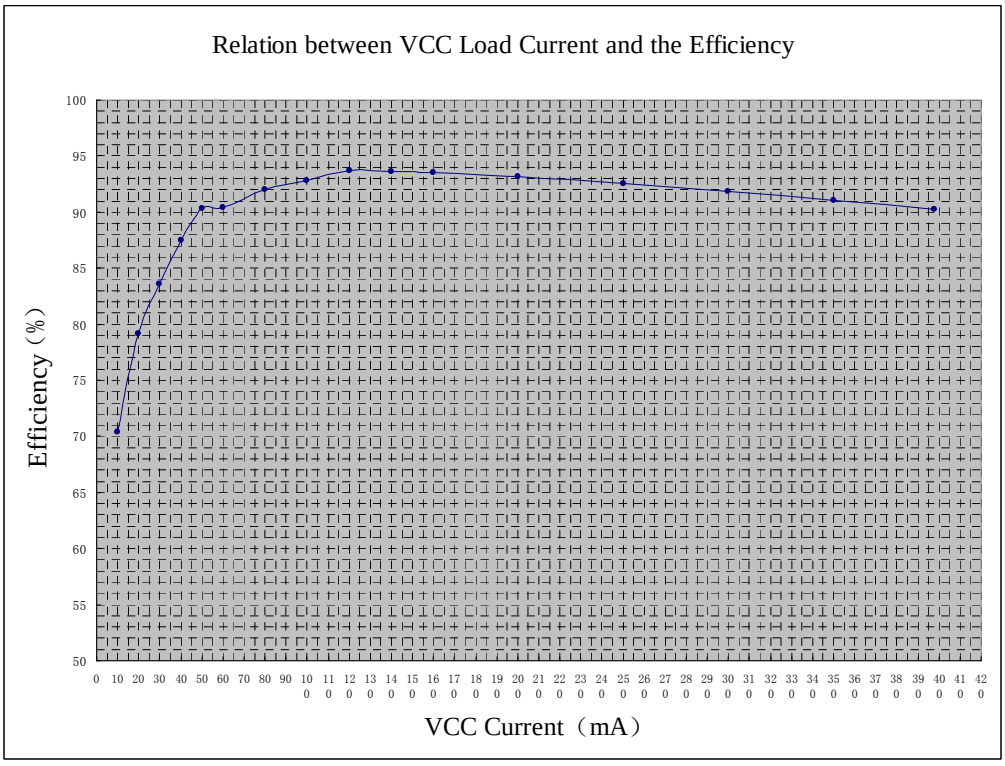
When Vin=3.6V, Vout=12V

(Please refer to the corresponding schematic diagram of reference circuit for DC/DC circuit components)

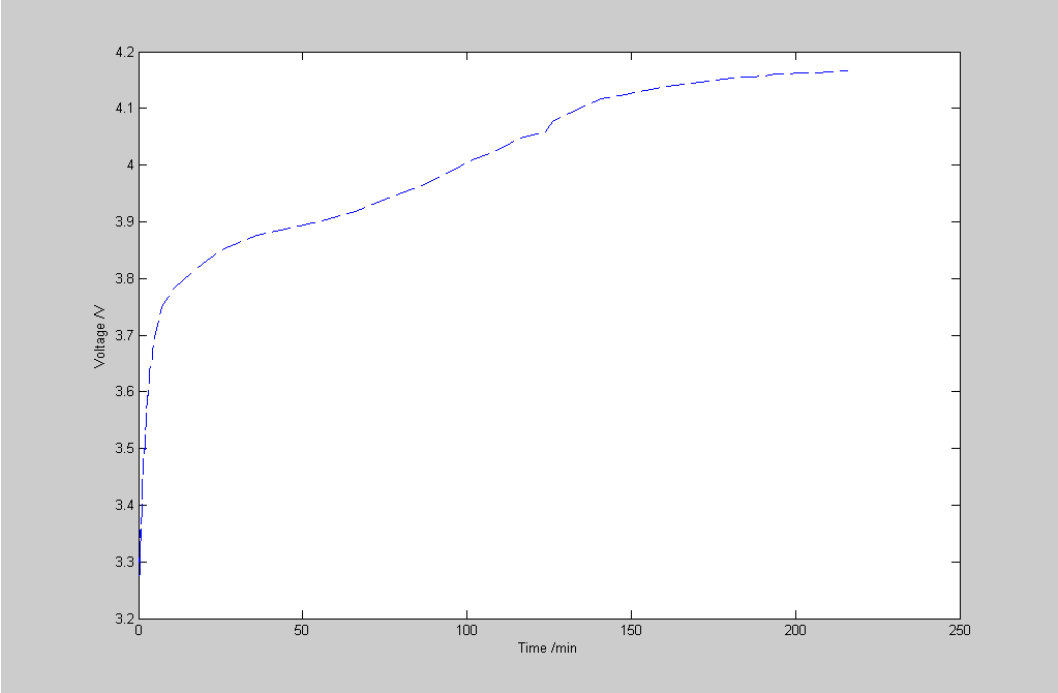
Li-ION mode: VBAT=3.6V



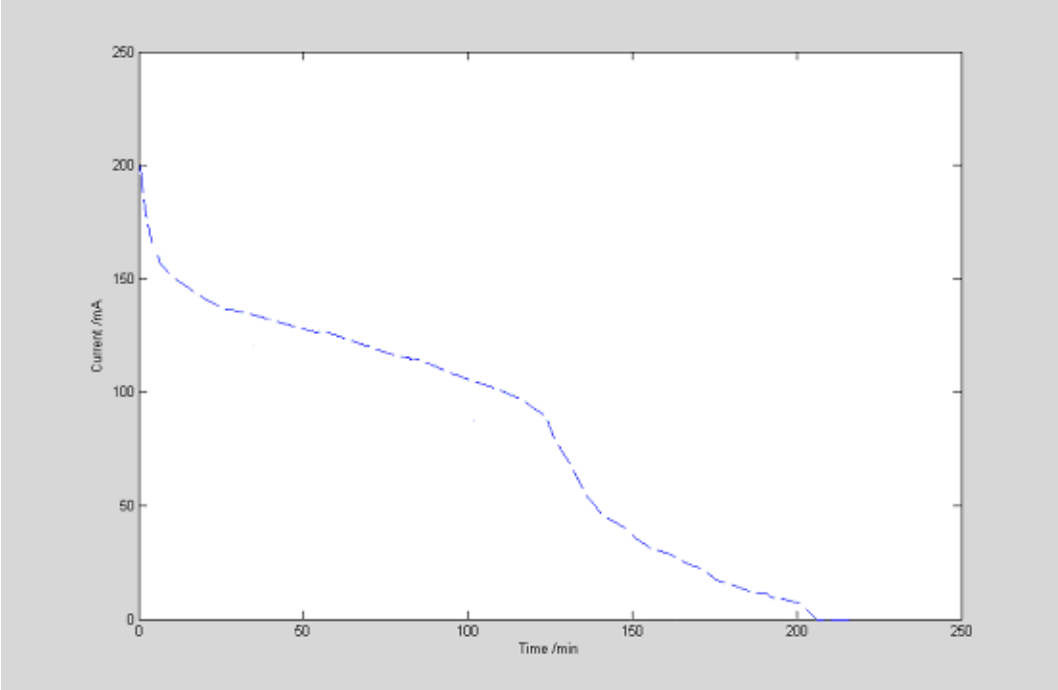
DC/DC Efficiency Curve 1



DC/DC Efficiency Curve 2



Charging Curve—Voltage Characteristics Curve



Charging Curve—Current Characteristics Curve

Note: the above results are measured when charging 270mAh Li-ion battery at the charging current of 200mA.

LDO Load Capacity

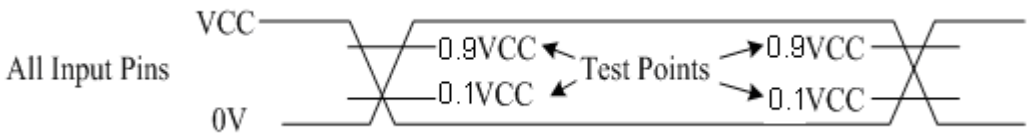
LDO Input	IVCC（vcc=3.1v）			IVDD (vcc=1.6v)		
	MIN (mA)	Typical (mA)	MAX (mA)	MIN (mA)	Typical (mA)	MAX (mA)
3.6V	320	350		350	400	
4.5V	350	380				
5.0V	420	480				

Note: the parameter is tested when VOUT is 95%VIN.

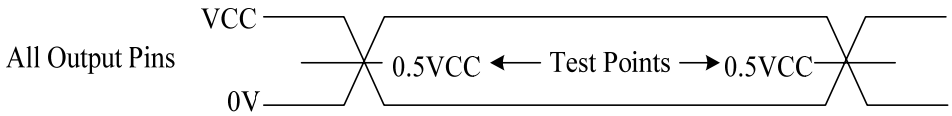
23.6 AC Characteristics

(To = 0 to +70℃, VDD = 2 to 3 V, VCC = 2.7 to 3.6 V)

23.6.1 AC Test Input Waveform



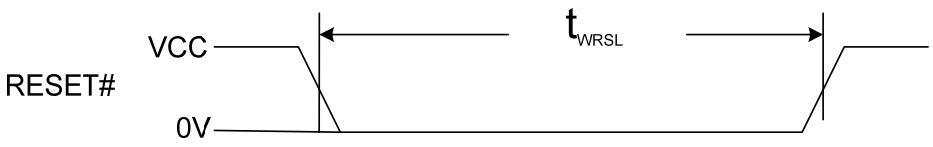
23.6.2 Output Measuring Points



23.7 Reset Parameter

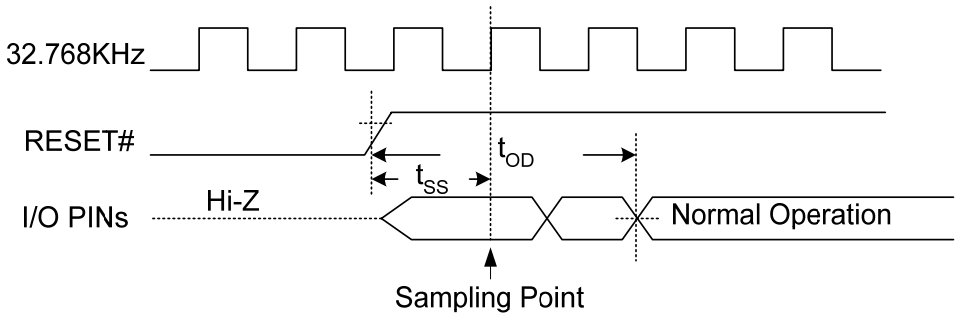
Parameter	Symbol	Condition	MIN.	MAX.	Unit

Reset input low-level width	t_{WRSL}	RESET# pin	230		us



23.8 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}			120	us
Output delay time (from RESET#)	t_{OD}			120	us



23.9 GPIO Interface Parameter

Table 5: GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	TYPE	MAX.	Unit
GPIO output rise time	t_{GPRISE}		3		40	ns
GPIO output fall time	t_{GPFALL}		3		40	ns

GPIO Interface – Output time

Table 6: GPIO Drive

GPIOX (Name)	Rh (ohm)	Ioh (mA)	Rl (ohm)	Iol (mA)	Power on status (CEOS=1)
GPIOA0(A0)	330.0	9.000	297.0	10.000	ale-0
GPIOA1(A1)	297.0	10.000	330.0	9.000	rb-1
GPIOA2 (A2)	330.0	9.000	297.0	10.000	cle-0
GPIOA6 (I2C1SCL)	330.0	9.000	330.0	9.000	z
GPIOA7 (I2C1SDA)	330.0	9.000	330.0	9.000	z
GPIOA8 (KSIN0)	990.0	3.000	742.5	4.000	1
GPIOA9 (KSIN1)	990.0	3.000	742.5	4.000	1
GPIOA10 (KSIN2)	1485.0	2.000	742.5	4.000	1
GPIOA11 (KSIN3)	990.0	3.000	742.5	4.000	z
GPIOA12 (KSOUT0)	1485.0	2.000	742.5	4.000	z
GPIOA13 (KSOUT1)	1485.0	2.000	742.5	4.000	0
GPIOA14 (WRB)	330.0	9.000	297.0	10.000	0
GPIOA15 (DRVVBUS)	330.0	9.000	330.0	9.000	0
GPIOA16 (CEB0)	330.0	9.000	297.0	10.000	1
GPIOA17 (CEB2)	330.0	9.000	297.0	10.000	1
GPIOA18 (SDRRASB)	198.0	15.000	135.0	22.000	0
GPIOA19 (SDRCASB)	371.3	8.000	297.0	10.000	uncertain
GPIOA20 (SDRWEB)	371.3	8.000	297.0	10.000	1
GPIOA21 (SDRA7)	371.3	8.000	297.0	10.000	1
GPIOA22 (SDRA8)	371.3	8.000	297.0	10.000	1
GPIOA23 (SDRA9)	371.3	8.000	297.0	10.000	1
GPIOA24 (SDRA10)	371.3	8.000	330.0	9.000	1
GPIOA25 (SDRA11)	371.3	8.000	330.0	9.000	0
GPIOA26 (SDRA12)	371.3	8.000	297.0	10.000	0
GPIOB28 (CEB5)	330.0	9.000	330.0	9.000	
GPIOA31 (SIRQ0)	990.0	3.000	742.5	4.000	0

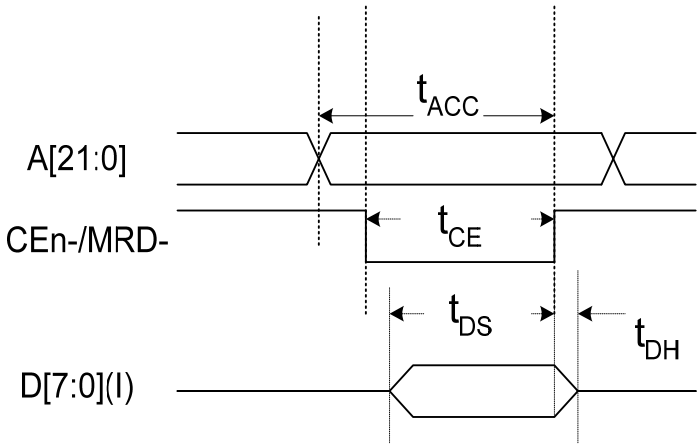
GPIOB0 (GPIOB0)	330.0	9.000	297.0	10.000	z
GPIOB1 (GPIOB1)	330.0	9.000	330.0	9.000	z
GPIOB2 (GPIOB2)	330.0	9.000	297.0	10.000	z
GPIOB3 (GPIOB3)	330.0	9.000	330.0	9.000	z
GPIOB4 (A10)	330.0	9.000	330.0	9.000	z
GPIOB5 (GPIOB5)	330.0	9.000	330.0	9.000	z
GPIOB6 (GPIOB6)	330.0	9.000	297.0	10.000	z
GPIOB7 (GPIOB7)	330.0	9.000	330.0	9.000	z
GPIOB8 (GPIOB8)	371.3	8.000	330.0	9.000	z
GPIOB9 (GPIOB9)	330.0	9.000	330.0	9.000	z
GPIOB10 (GPIOB10)	330.0	9.000	330.0	9.000	z
GPIOB11 (GPIOB11)	330.0	9.000	297.0	10.000	z
GPIOB12 (UART2TX)	330.0	9.000	330.0	9.000	z
GPIOB13 (UART2RX)	330.0	9.000	330.0	9.000	z
GPIOB14 (UART1TX)	330.0	9.000	330.0	9.000	z
GPIOB15 (UART1RX)	330.0	9.000	330.0	9.000	z
GPIOB17 (CEB3)	330.0	9.000	297.0	10.000	z
GPIOB22 (KSOUT2)	990.0	3.000	990.0	3.000	1
GPIOB27 (CEB4)	330.0	9.000	297.0	10.000	1
GPIOB29 (CEB6)	212.1	14.000	165.0	18.000	1
GPIOB31 (SIRQ1)	1485.0	2.000	990.0	3.000	0

Notes:

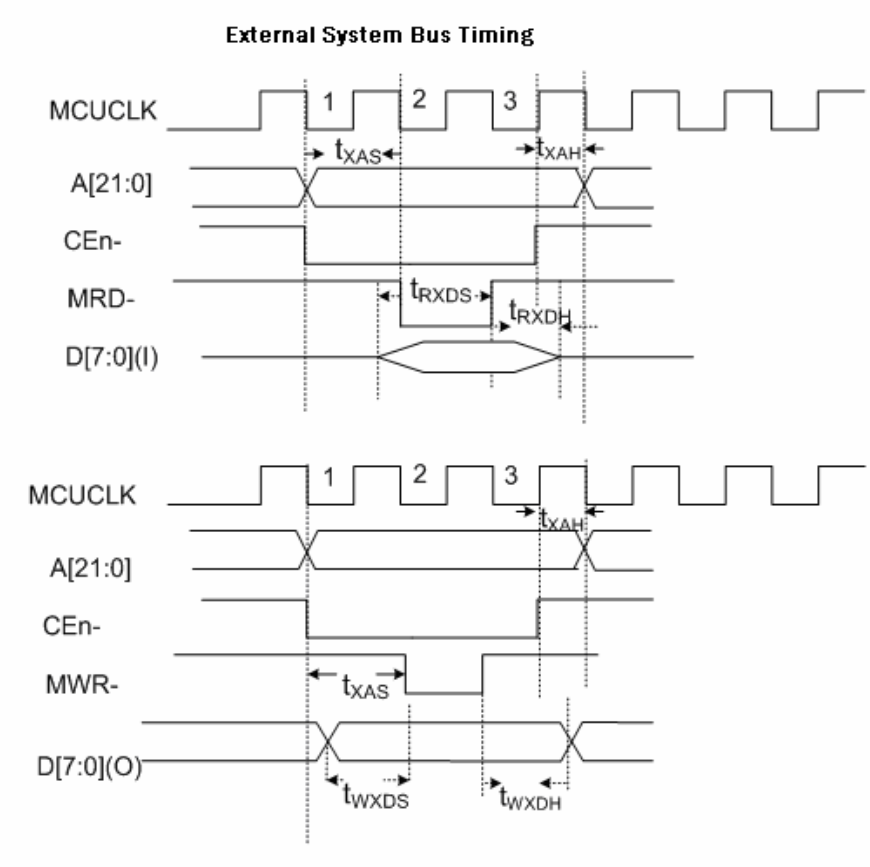
1. Rh is internal pull up resistance, and IoH is drive ability of output H;
2. RL is internal pull down resistance, and IoL is drive ability of output L;
3. Power up status means the status start from BROM;
4. For those GPIO reused with SDRAM (A18-A26), there is HOLD circuit. Its pull up/down resistance status is decided by the previous pad level status in Input Enable status. HOLD circuit is meaningless in output status.

23.10 Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)	t_{ACC}	HOSC=24MHz	102		ns
Data access time (from CEx#)	t_{CE}	HOSC=24MHz	82		ns
Data input setup time	t_{DS}	HOSC=24MHz	0		ns
Data input hold time	t_{DH}	HOSC=24MHz	0		ns



23.11 External System Bus Parameter



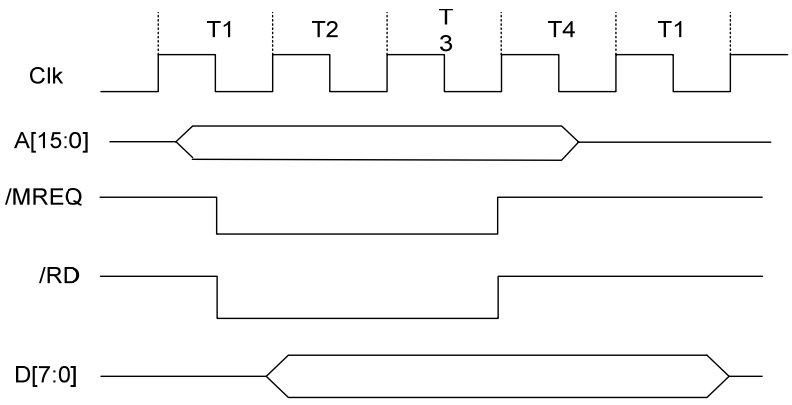
External System Bus Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	25		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

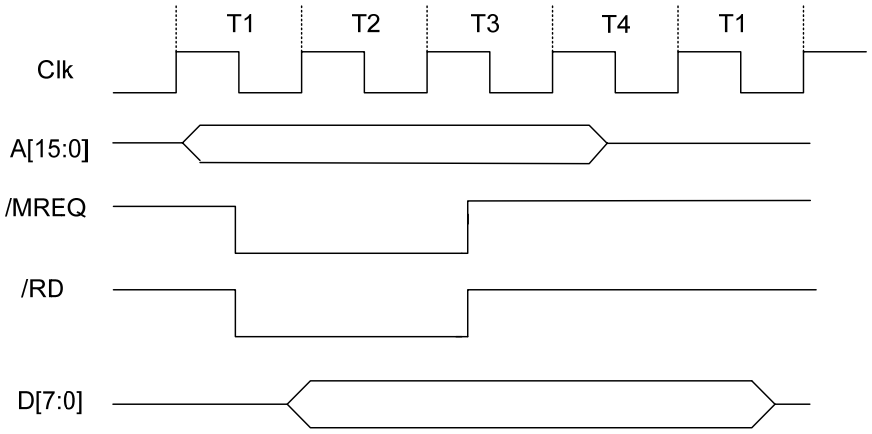
Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

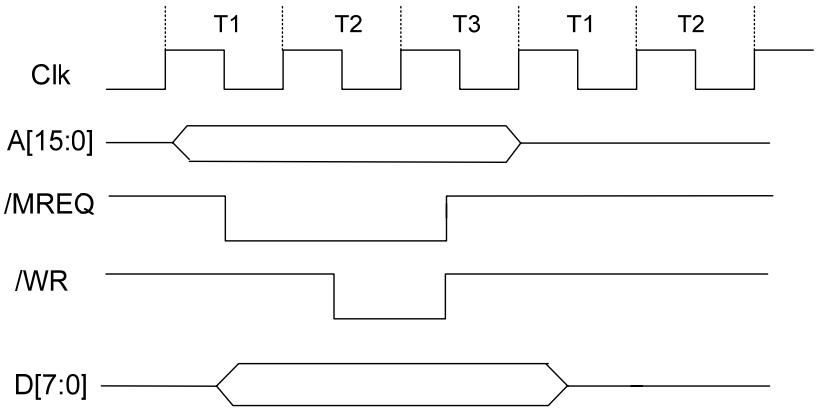
23.12 Bus Operation



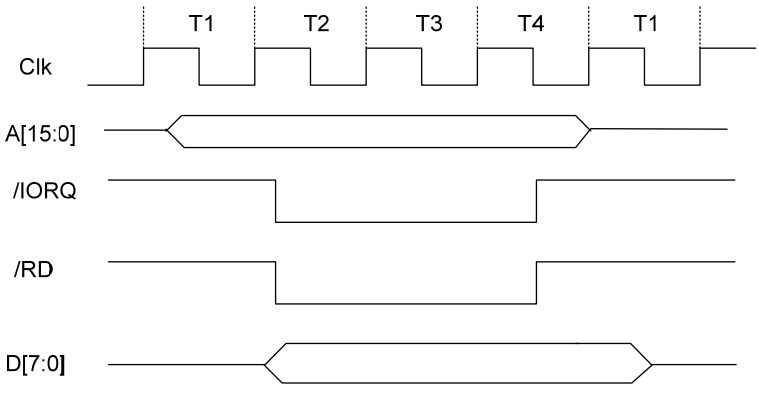
Instruction Fetch Timing



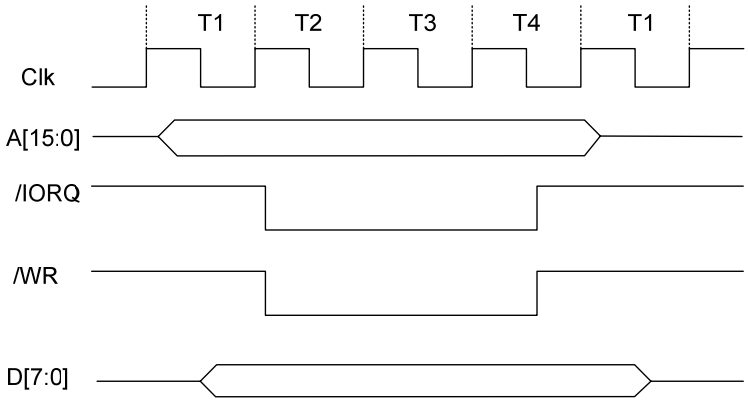
Memory Read Timing



Memory Write Timing

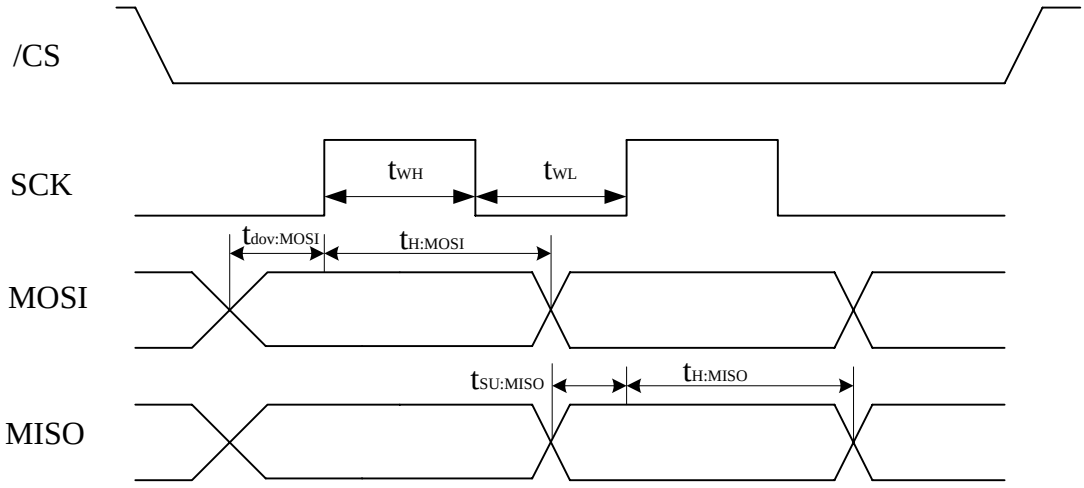


IO Read Timing



IO Write Timing

23.13 SPI Parameter



SPI timing

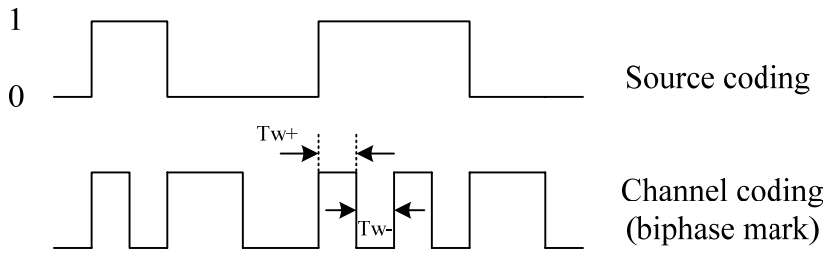
coreCLK=180M, Sclk=90M, PCLK=45M, CLKDIV=3, SPICLK=7.5M, double the drive ability at PAD_DRV.

SPI Parameter

Parameter	Symbol	Min	Max	Unit
SCK Clock	fclk		7.5	MHz
SCK High time	t_{WH}	66		ns

SCK Low time	t_{WL}	68		ns
SCK rise time	t_r		11.6	ns
SCK fall time	t_f		12.8	ns
Data output valid	$t_{DOV:MOSI}$	14		ns
Data output hold	$t_{H:MOSI}$	100		ns
Data in setup time	$t_{SU:MISO}$	14		ns
Data in hold time	$t_{H:MISO}$	100		ns

23.14 SPDIF Interface Parameter



SPDIF Channel coding

SPDIF Interface Parameter

Sampling Rate	Channel Bit Theoretical Value	Channel Bit Tw+	Channel Bit Tw-
32K	244nS	242nS	246
44.1K	177nS	176nS	178
48K	163nS	161nS	163

23.15 I2C Interface Parameter

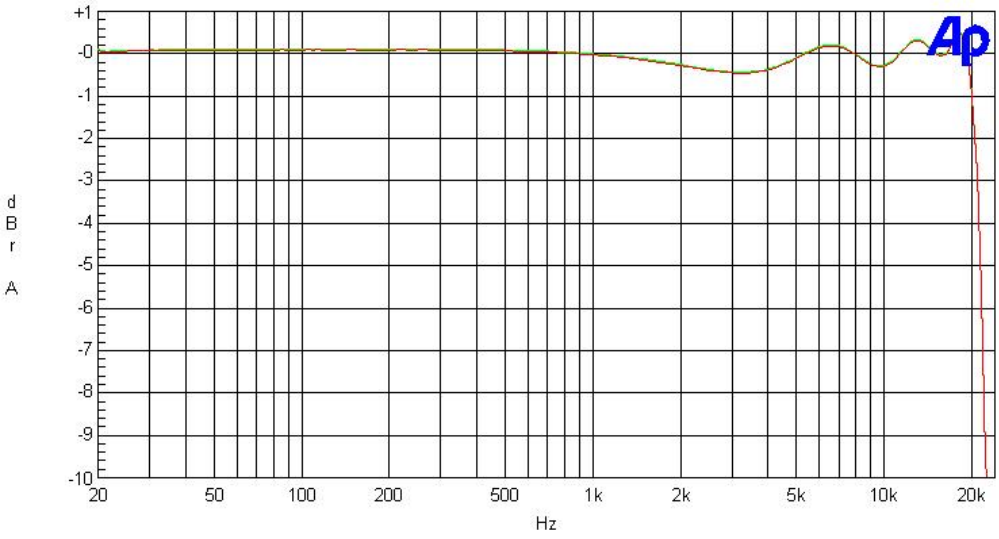
Parameter	Symbol	Typical		Unit
SCL period	f_{SCL}	100	400	kHz
Clock low time	T_{LOW}	5.0	1.26	us
Clock high time	T_{HIGH}	4.96	1.22	us
Clock rise time	t_r	90	90	ns
Clock fall time	t_f	7.5	8	ns
Data setup time	$t_{SU:DAT}$	3.7	0.68	us

Data hold time	$t_{HD:DAT}$	1.24	0.74	us
Start hold time	$t_{HD:STA}$	9.2	2.45	us
Start setup time	$t_{SU:STA}$	5.3	1.3	us
Stop setup time	$t_{SU:STO}$	5.3	1.3	us

23.16 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 1.8 V, VCC = 3.1V, Sample Rate=48KHz)

Characteristics	Min.	Typ.	Max.	Unit
Dynamic Range –40 dBFS Input		89		dB
Total Harmonic Distortion+Noise		-81		dB
Frequency Response 20-18KHz			0.5	dB
Reference Voltage		1.510		V
Full Scale Input Voltage		2.58		Vpp

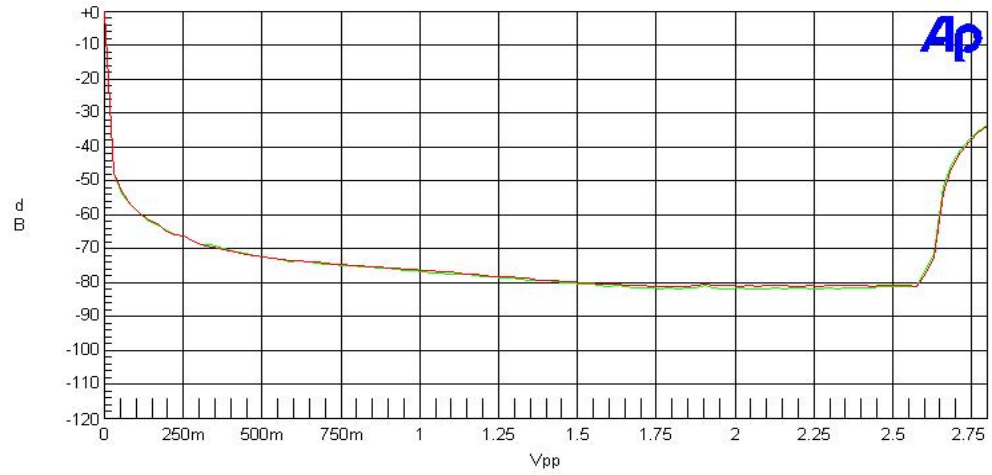


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Anlr.Level A	Left	
1	2	Red	Solid	1	Anlr.Level B	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

A/D Converter – Frequency Response Characteristics

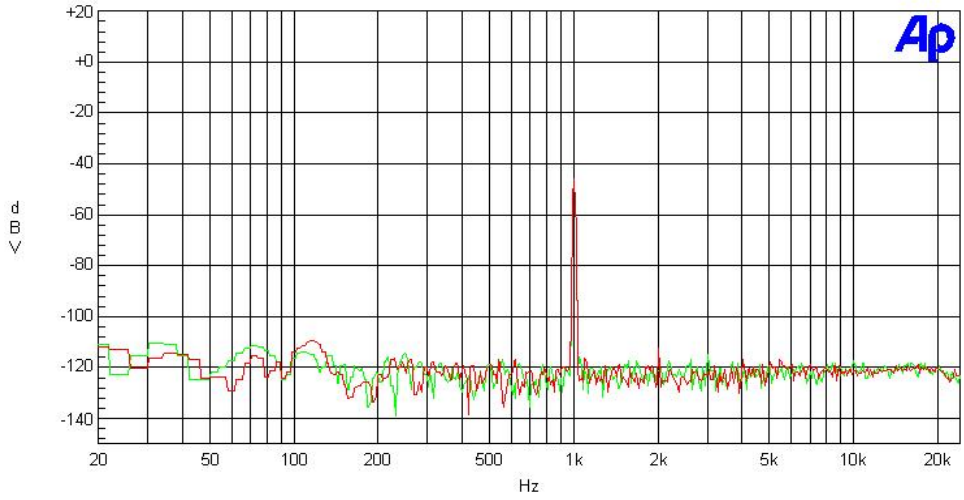


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Anlr.THD+N Ratio	Left	
1	2	Red	Solid	1	Anlr.THD+N Ratio	Left	

DSP required. Simultaneous THD+N measurement can be made by using both the Analog Analyzer and the DSP Audio Analyzer in THD+N mode (see pg 1). Filters choice is limited in the DSP Analyzer. Set bandwidth for similar range. At low distortion amplitudes the DSP analyzer is limited by the A-D quantization noise and distortion as can be seen here.

A-A THD+N VS FREQ 2-CH.at27

A/D Converter – THD+N vs AMP

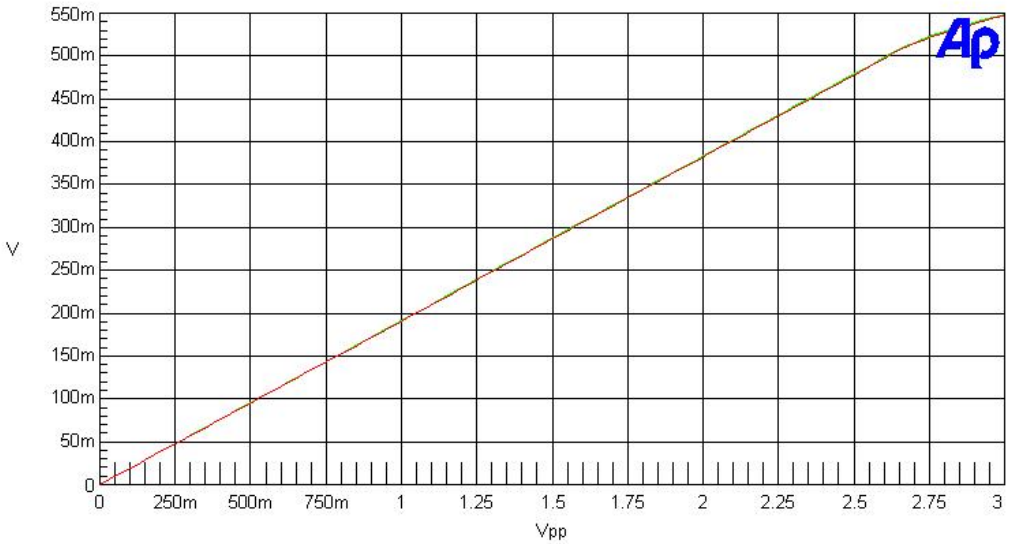


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Red	Solid	1	Fft.Ch.2 Ampl	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

A/D Converter –Small Signal Power Spectrum

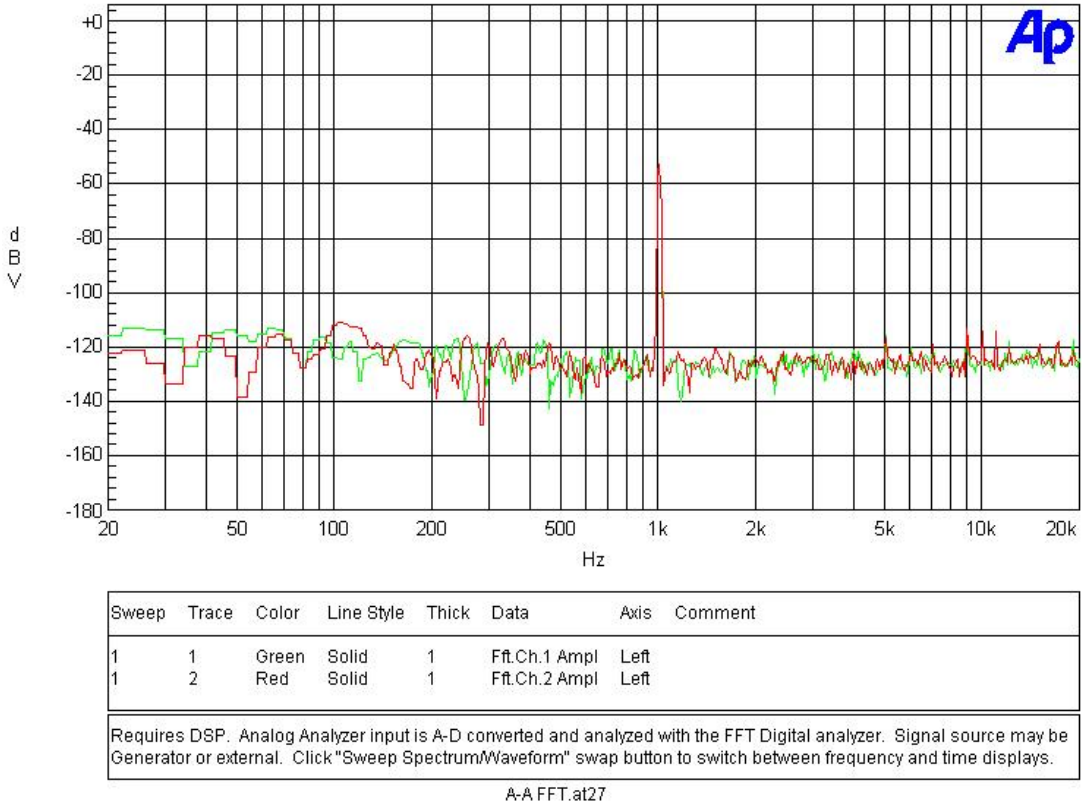


A/D Converter – Linearity

23.17 DAC Characteristics

DAC Characteristics

Characteristics	MIN.	Typ.	MAX.	UNIT
Dynamic Range –48 dBFS Input		91.5		dB
Total Harmonic Distortion + Noise		-85.5		dB
Full Scale Output Voltage	0.48	0.58	0.72	Vrms
Interchannel Isolation (1k)		-99/-81		dB

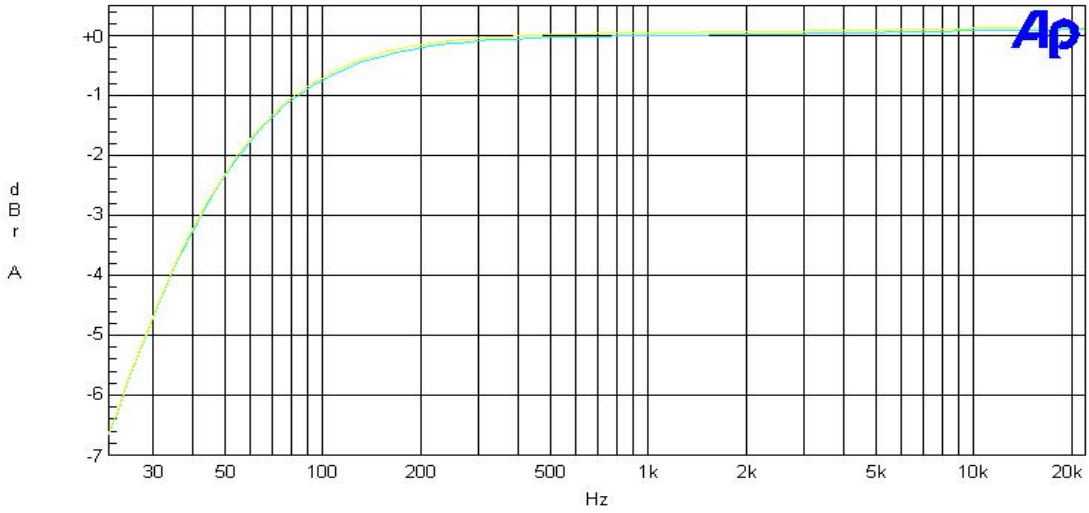


DAC –Small Signal Power Spectrum

23.18 Headphone Driver Characteristics

(T_A =-10 - +70℃, VDD = 2.0 V, VCC = 3.0 V, Sample Rate=48KHz, Volume Level=0x1F)

Characteristics	MIN.	Typ.	MAX.	UNIT
Dynamic Range		94		dB
Total Harmonic Distortion+Noise		-90		dB
Output Common Mode Voltage		1.516		Vrms
Full Scale Output Voltage@-70dB thd+n		1.77		Vpp
Output Power @16ohm		24		mW

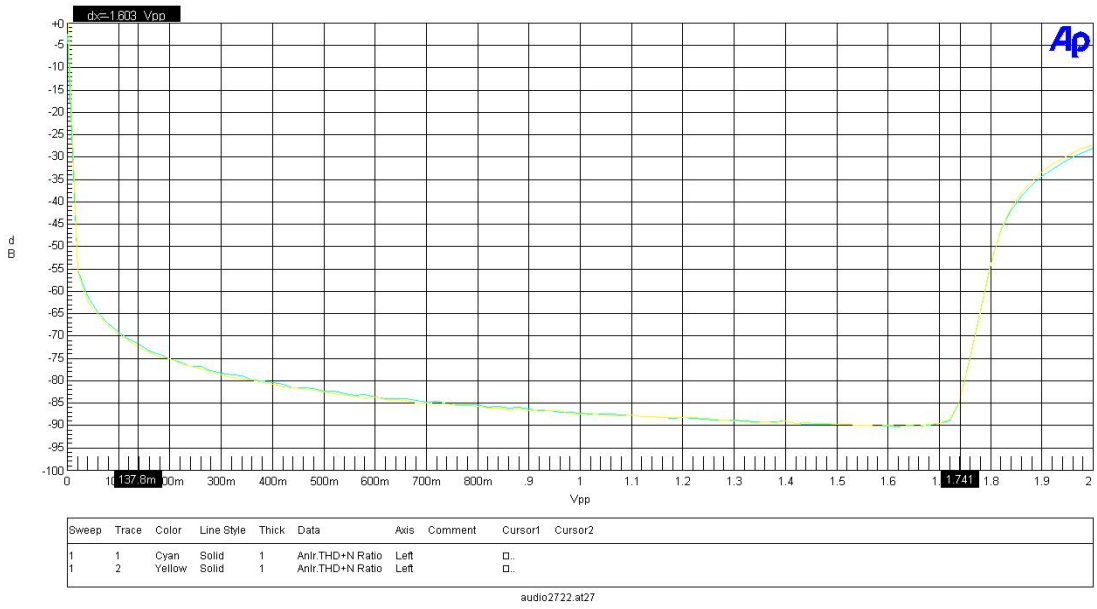


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.Level A	Left	
1	2	Yellow	Solid	1	Anlr.Level B	Left	

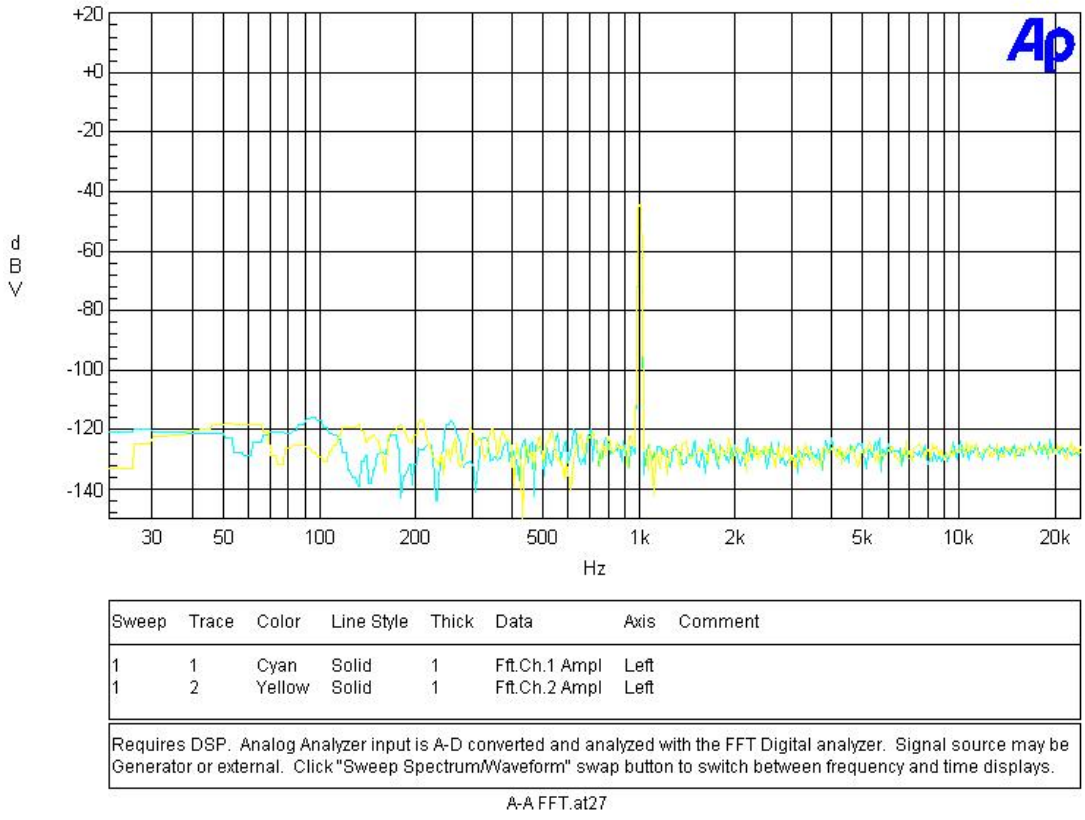
Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

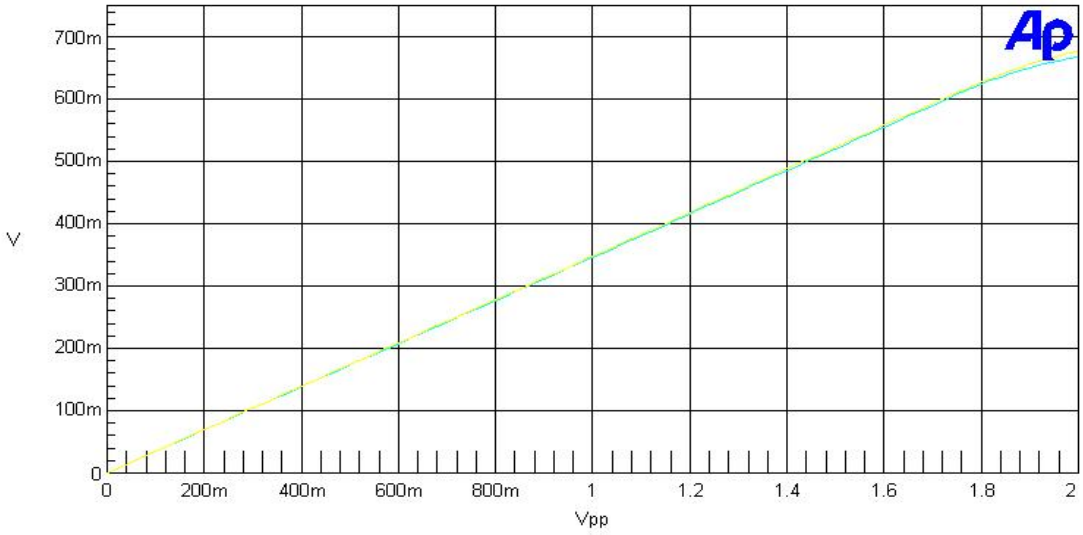
Headphone Driver–Frequency Response



Headphone Driver–THD + N Amplitude Diagram of Headphone Driver



Headphone Driver—Linearity



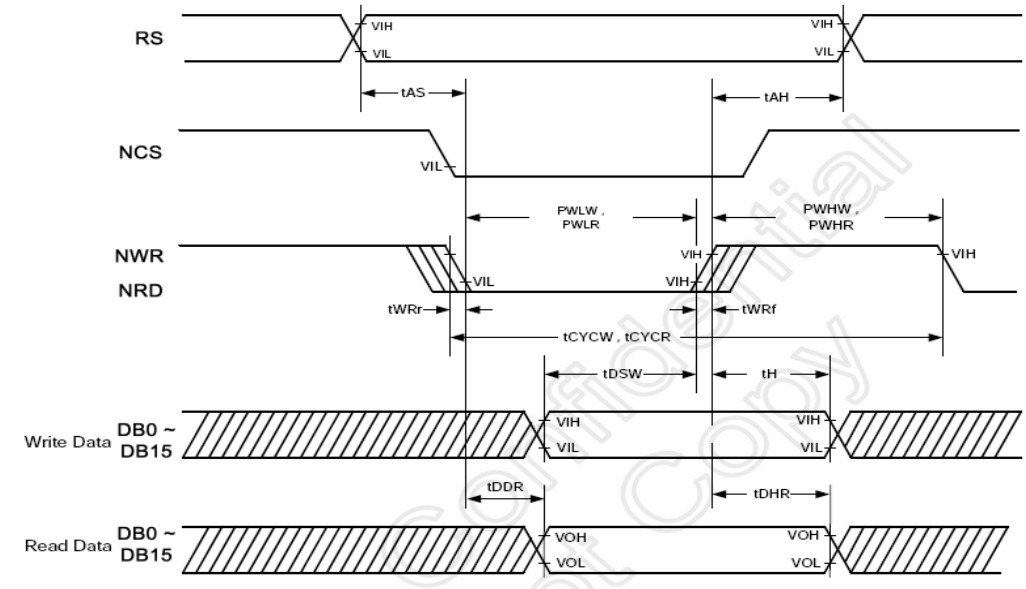
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.Level A	Left	
1	2	Yellow	Solid	1	Anlr.Level B	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

A-A FFT.at27

Headphone Driver–Small Signal Power Spectrum

23.19 LCM Driver Parameter

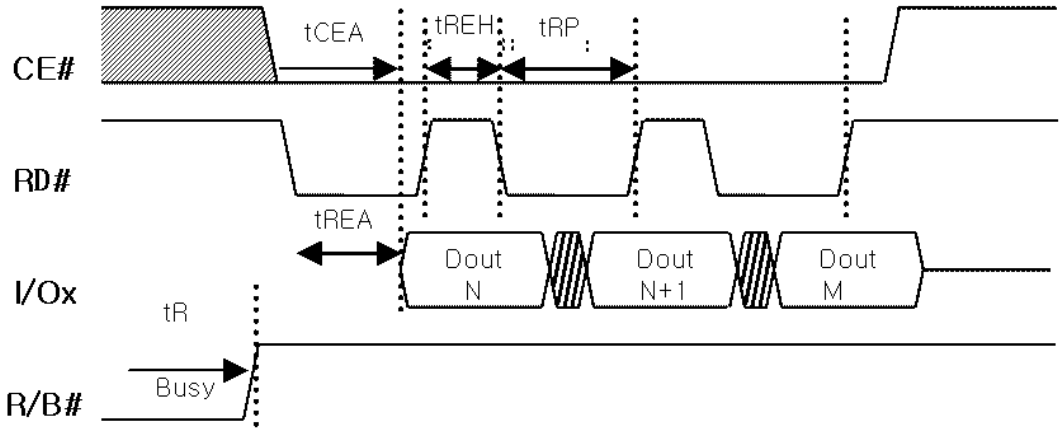


LCM Timing

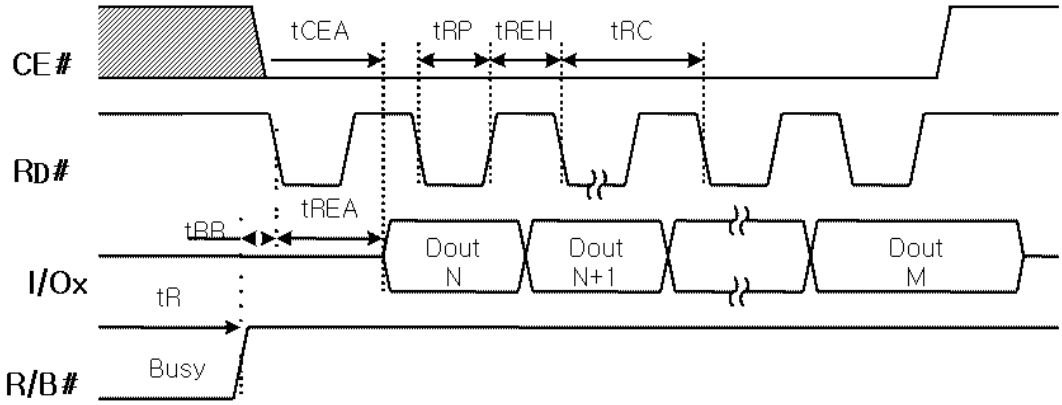
LCM Driver Parameter

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	tCYCW	ns	34	200	-	AHB clk.=60MHz
	Read	tCYCR	ns	34	134	-	AHB clk.=60MHz
Write low-level pulse width		PWLW	ns	17	100	-	AHB clk.=60MHz
Read low-level pulse width		PWLR	ns	17	67	-	AHB clk.=60MHz
Write high-level pulse width		PWHW	ns	17	100	-	AHB clk.=60MHz
Read high-level pulse width		PWHR	ns	17	67	-	AHB clk.=60MHz
Write / Read rise / fall time		tWRr , tWRf	ns	-	11	-	AHB clk.=60MHz
Write data set up time		tDSW	ns	27	110	-	AHB clk.=60MHz
Write data hold time		tH	ns	23	28	-	AHB clk.=60MHz
Read data delay time		tDDR	ns	-	45	-	AHB clk.=60MHz
Read data hold time		tDHR	ns	-	105	-	AHB clk.=60MHz

23.20 NAND Flash IF

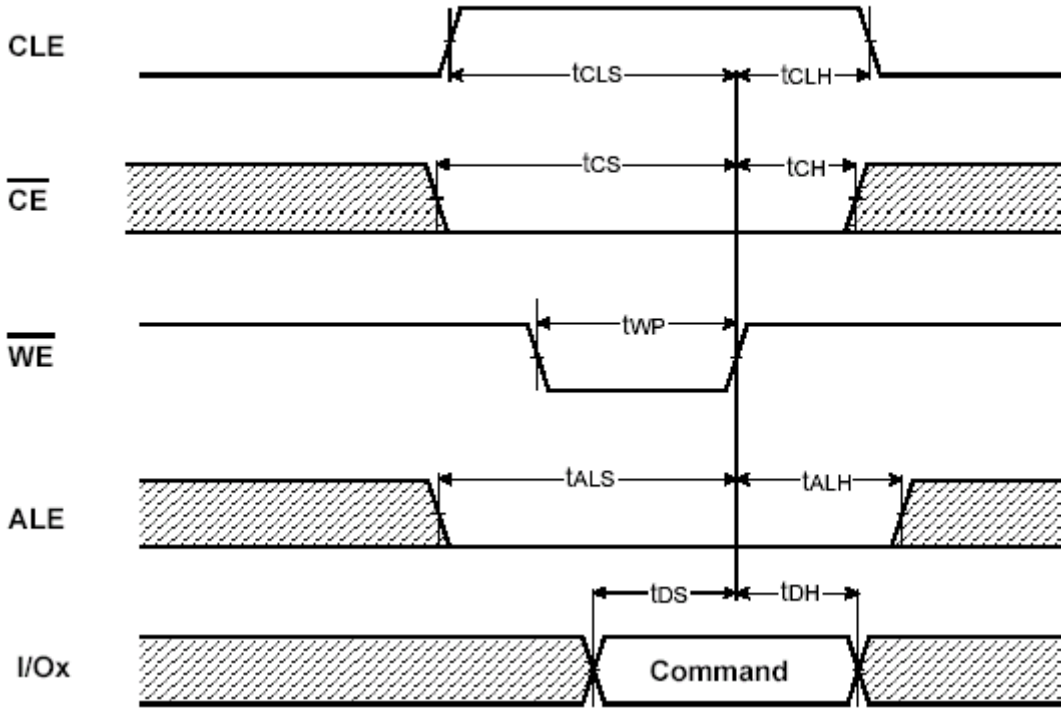


Data Fetch at RD# Rising Edge
Conventional Serial Access Mode



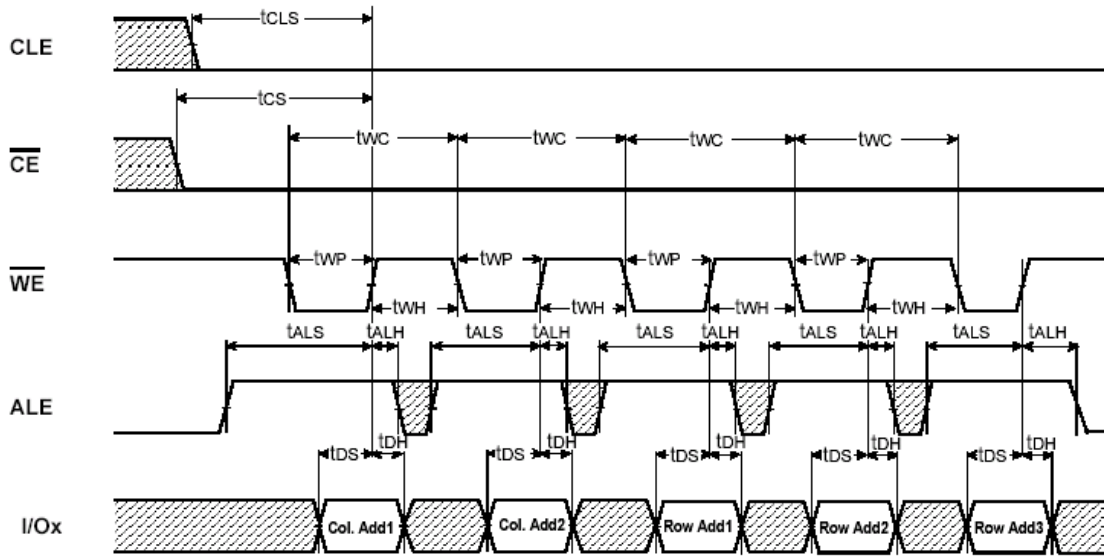
Data Fetch at RD# Falling Edge
EDO Type Serial Access Mode

Command Latch Cycle



IO[15:8] must be set to zero
Command Latch Cycle

Address Latch Cycle



IO[15:8] must be set to zero

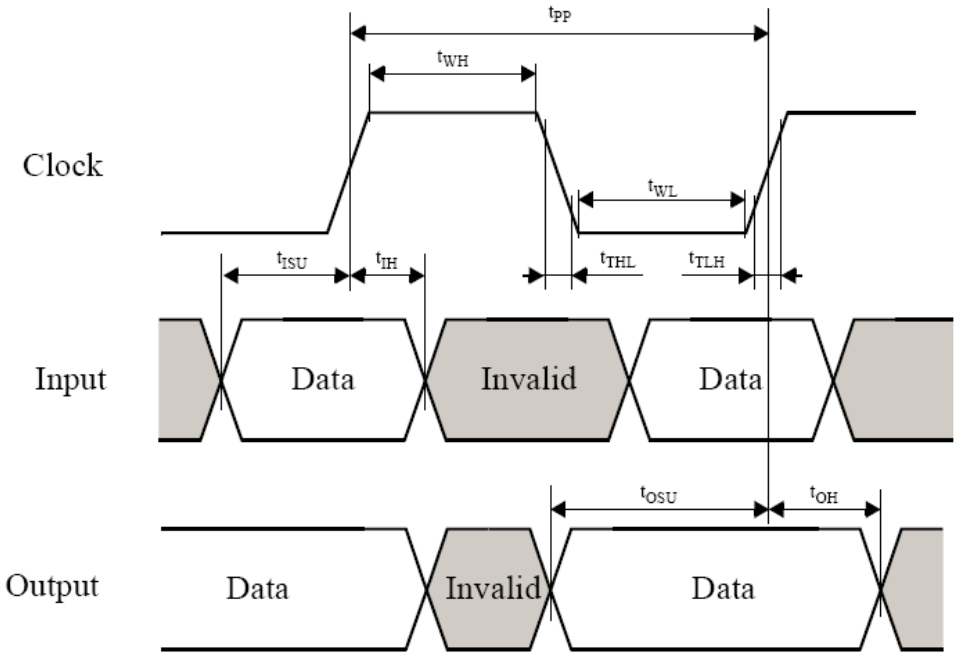
Address Latch Cycle

Nand Flash Timing Request

Item	Conventional Serial Access	EDO Type Serial Access	Remark
tCEA	23nS (min)	23nS (min)	
tREA	30nS (max)	18nS (max)	
tREH	15nS (min)	12.5nS (min)	
tRP	25nS (min)	12.5nS (min)	
tRC	30nS (min)	25nS (min)	Conventional: duty≠50% EDO type: duty=50%
Data Fetch	At RD# Rising Edge	At next RD# Falling Edge	
tFALLING	5nS	5nS	
tRISINFG	5nS	5nS	
tCLS	25nS (min)	12nS (min)	
tCLH	10nS (min)	5nS (min)	
tCS	35nS (min)	20nS (min)	
tCH	10nS (min)	5nS (min)	
tALS	25nS (min)	12nS (min)	

tALH	10nS (min)	5nS (min)	
tDS	20nS (min)	12nS (min)	
tDH	10nS (min)	5nS (min)	
tWC	30nS (min)	25nS (min)	
DMA clk	30MHz	40MHz	

23.21 SD Card



Timing Diagram Data Input/Output Referenced to Clock

Card Interface Timings

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	26/52	MHz	CL<=30pF(tolerance +100KHz)
Clock frequency identification Mode(Open Drain)	fOD	0	400	KHz	Tolerance:+20KHz
Clock low time	tWL	6.5		ns	CL<=30pF
Clock rise time	tTLH		3	ns	CL<=30pF

Clock fall time			3	ns	CL<=30pF
Inputs CMD DAT (reference to CLK)					
Input setup time	tISU	3		ns	CL<=30pF
Input hold time	tIH	3		ns	CL<=30pF
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	5		ns	CL<=30pF
Output hold time	tOH	5		ns	CL<=30pF
Signal rise time	trise		3	ns	CL<=30pF
Signal fall time	tfall		3	ns	CL<=30pF

Bus Signal Line Load

Parameter	Symbol	Min	Recommend	Max	Unit	Remark
Pull up resistance for CMD	Rcmd	4.7	10	100	KOhm	To prevent bus floating
Pull up resistance for dat0-7	Rdat	50	50	100	KOhm	To prevent bus floating
Bus signal line capacitance	CL			30	pF	Single card
Signal card capacitance	Ccard			7	pF	
Maximum signal line inductance				16	nH	Fpp<=52MHz

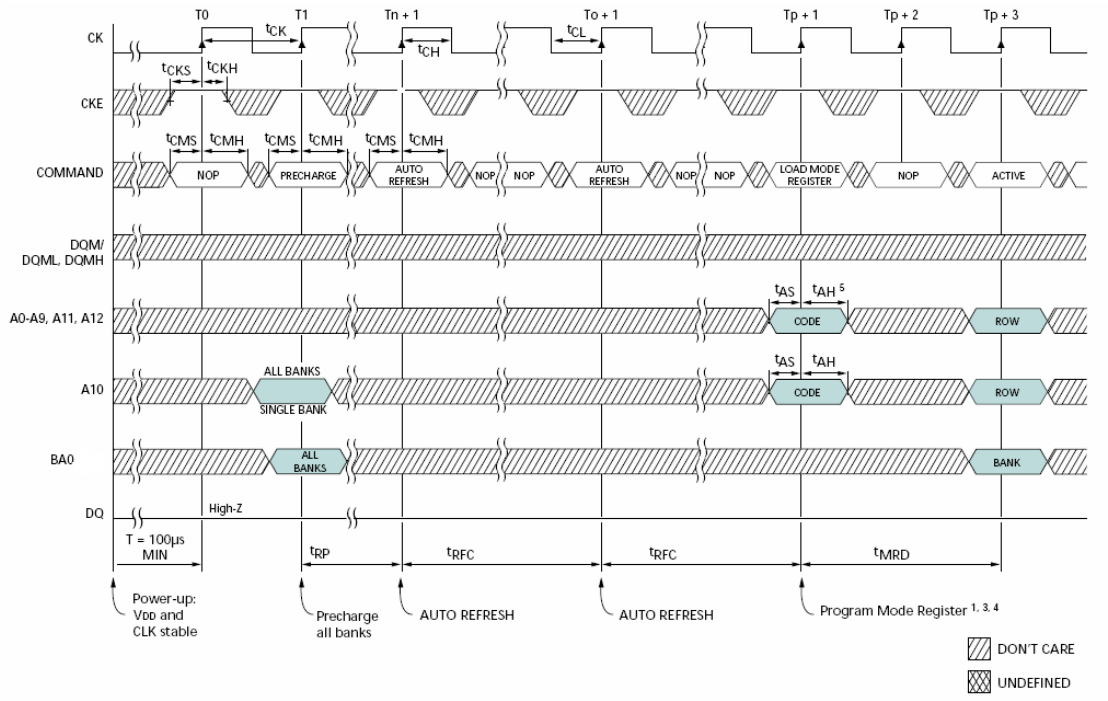
CL=CHost+Cbus+Ccard

SD Spec. ver1.0 Timing

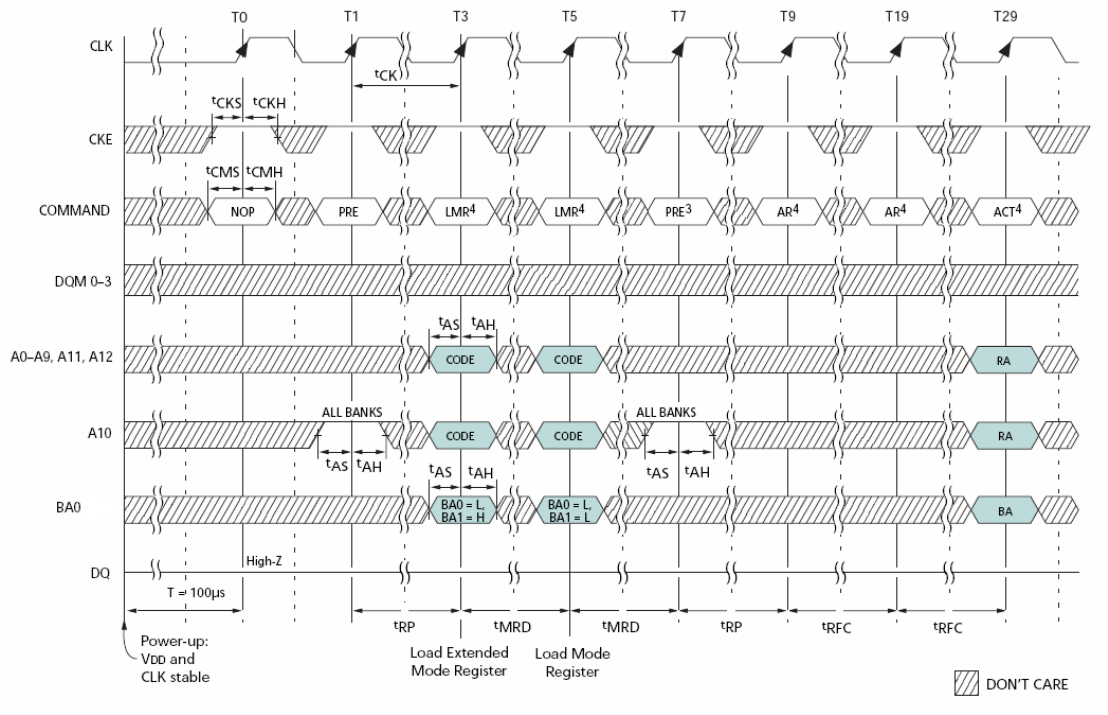
Parameter	Symbol	Min	Max	Unit	Remark
Clock Frequency Data transfer mode	fpp	0	25	MHz	CL<=100Pf
Clock Frequency identification mode	fOD	0~100	400	KHz	CL<=250pF
Clock Low Time	tWL	10		Ns	CL<=100pF
Clock High Time	TWH	10		Ns	CL<=100pF
Clock Rise Time	tTLH		10	Ns	CL<=100pF
Clock Fall Time	tTHL		10	Ns	CL<=100pF
Clock Low Time	tWL	50		Ns	CL<=100pF
Clock High Time	TWH	50		Ns	CL<=100pF
Clock Rise Time	tTLH		50	Ns	CL<=100pF
Clock Fall Time	tTHL		50	Ns	CL<=100pF
Input Set-up Time	tISU	5		Ns	CL<=25pF
Input Hold Time	tIH	5		Ns	CL<=25pF
Output Delay Time under Data Transfer	tODLY		14	Ns	CL<=25pF

Mode					
Output Delay time under identification transfer mode	tODLY		50	Ns	CL<=25pF

23.22 SDRAM IF



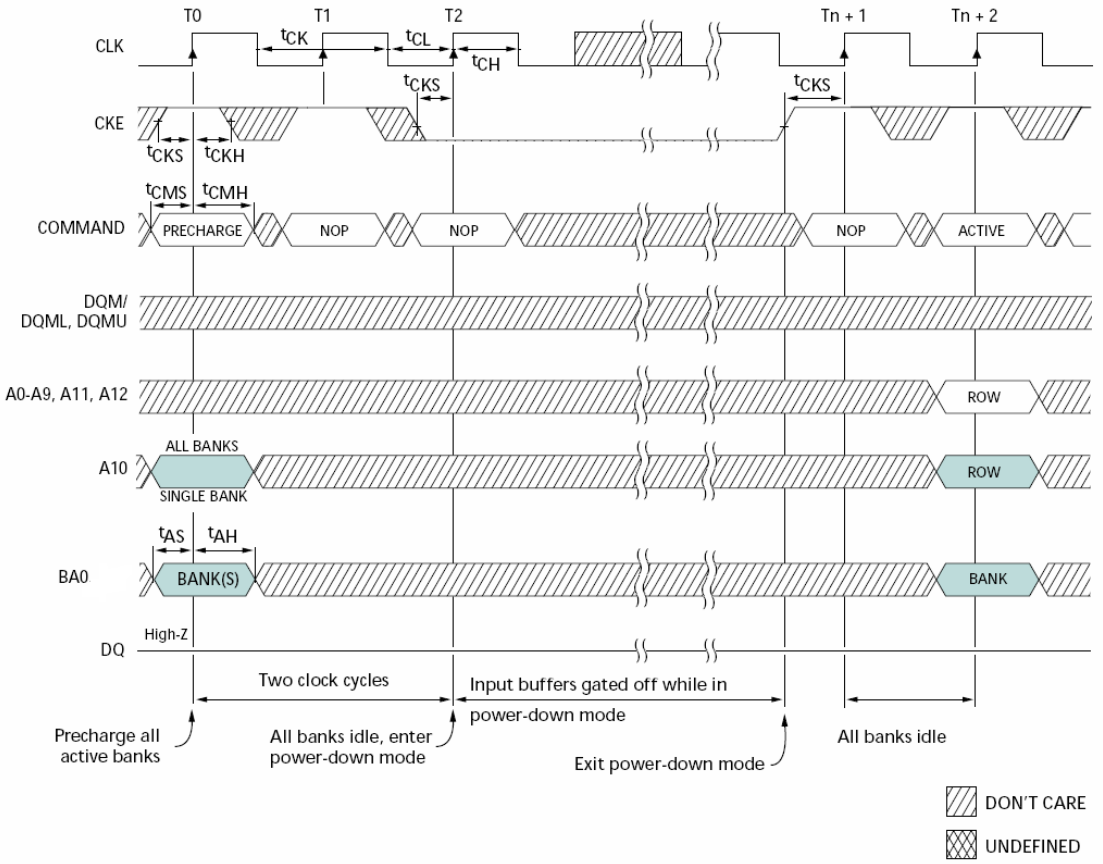
Standard SDRAM Power Up



Mobile SDRAM Power Up

NOTE:

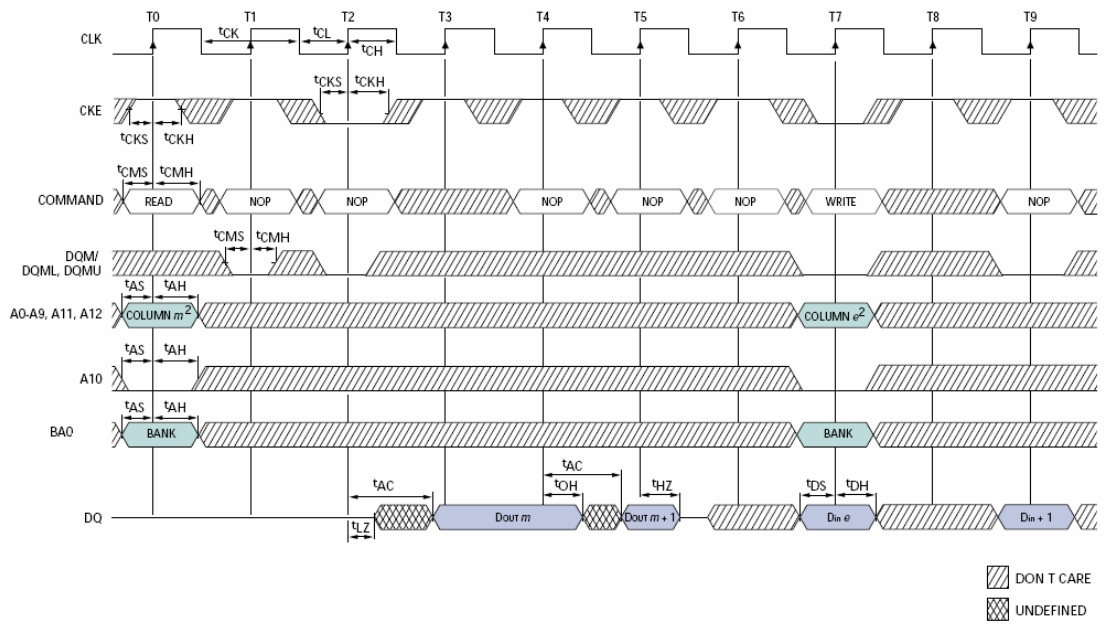
1. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
2. If CS is HIGH at clock high time, all commands applied are NOP.
3. Outputs are guaranteed High-Z after command is issued.
4. A12 should be a LOW at tP + 1.



SDRAM IF– Power Down

NOTE:

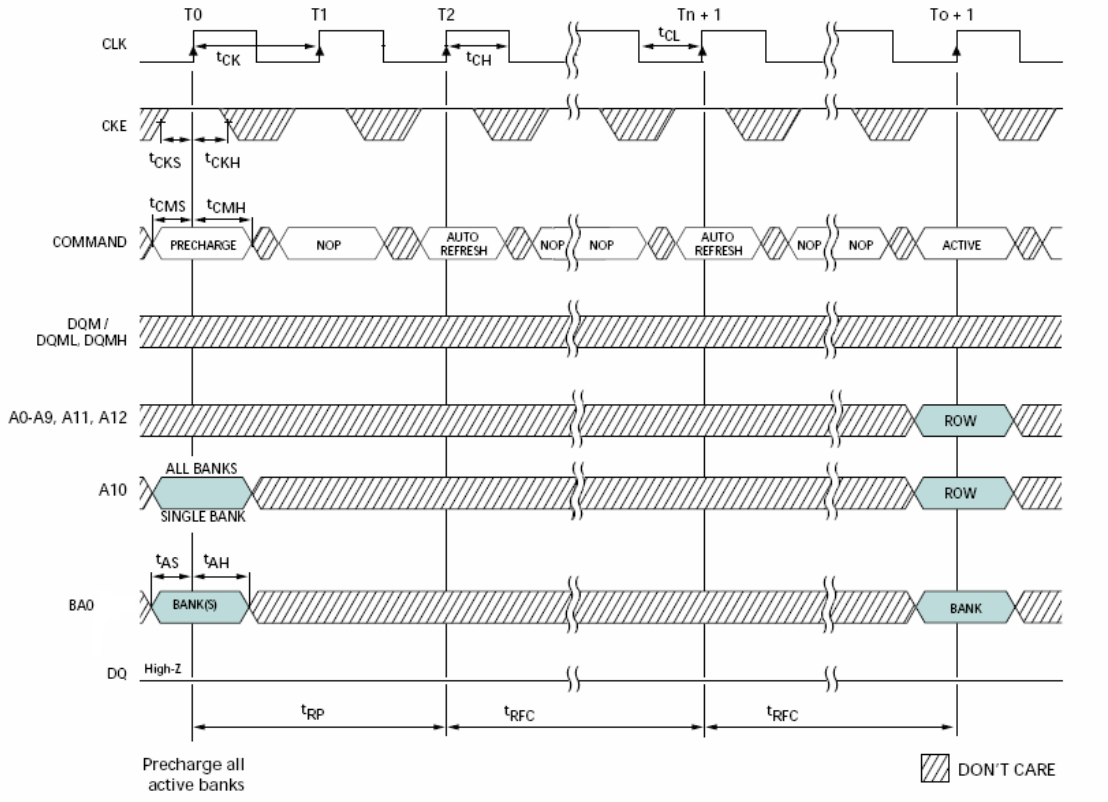
1. Violating refresh requirements during power-down may result in a loss of data.
2. CAS latency indicated in parentheses



SDRAM IF– Clock Suspend

NOTE:

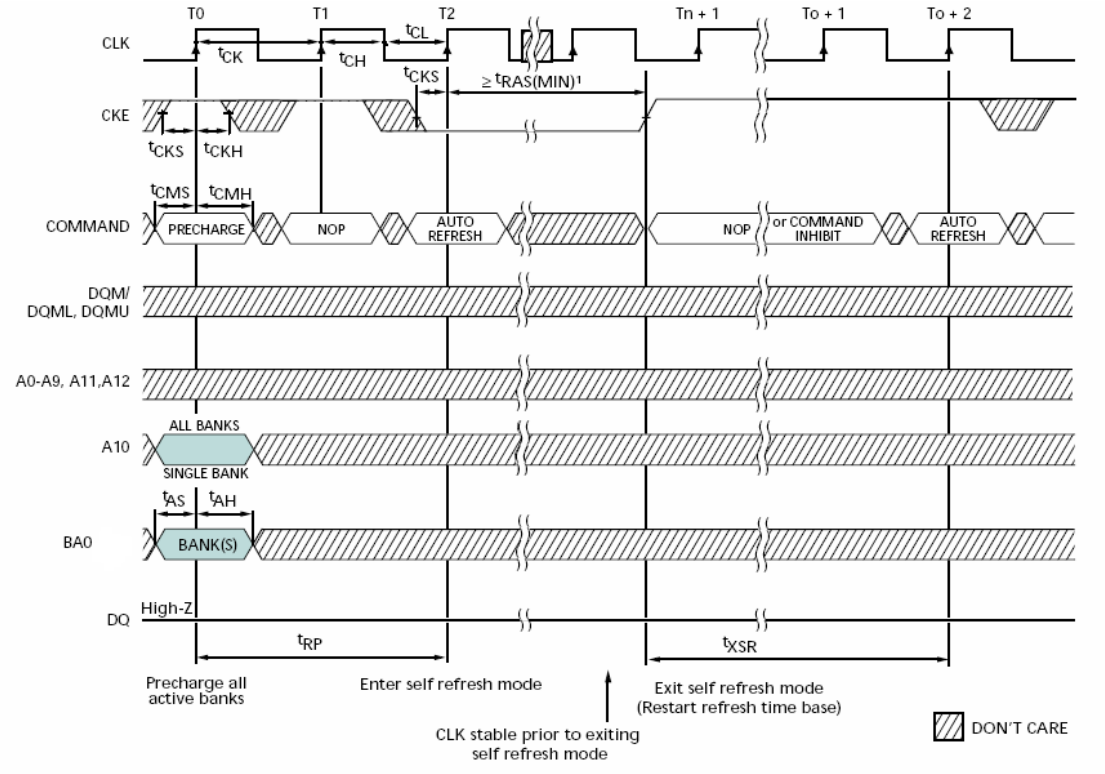
1. For this example, the burst length = 2, the CAS latency = 3, and AUTO PRECHARGE is disabled.
2. CAS latency indicated in parentheses



SDRAM IF– Auto Refresh

NOTE:

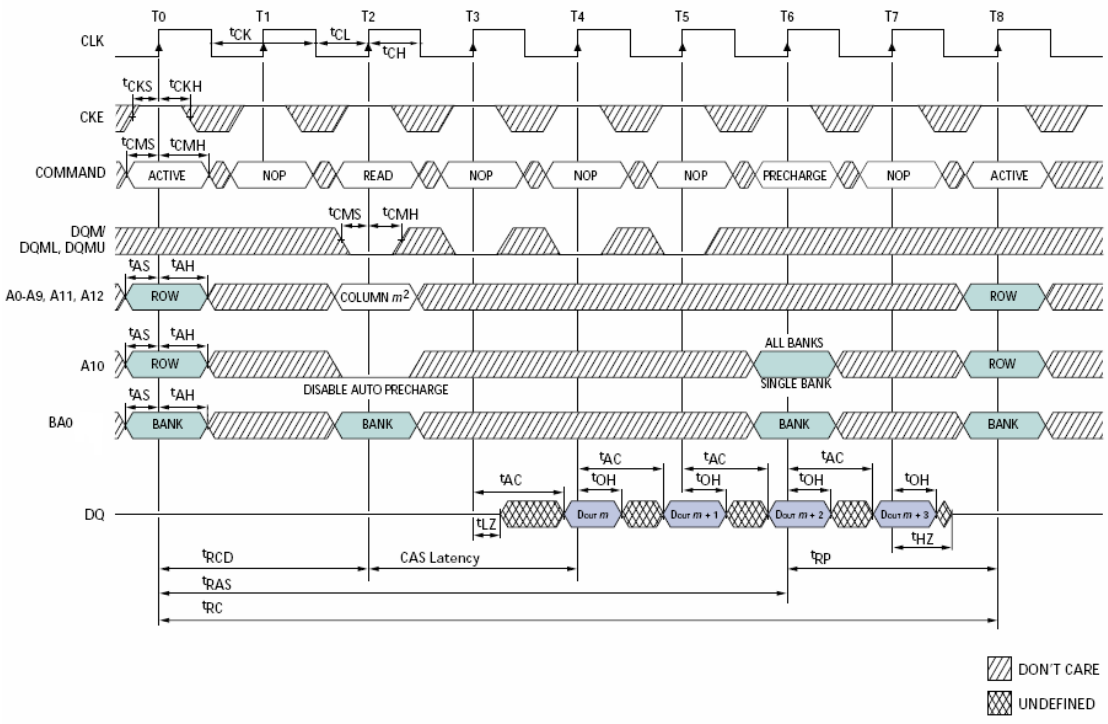
1. CAS latency indicated in parentheses



SDRAM IF – Self Refresh

NOTE:

1. No maximum time limit for Self Refresh. tRAS(MIN) applies to non-Self Refresh mode.
2. tXSR requires minimum of two clocks regardless of frequency or timing.
3. CAS latency indicated in parentheses

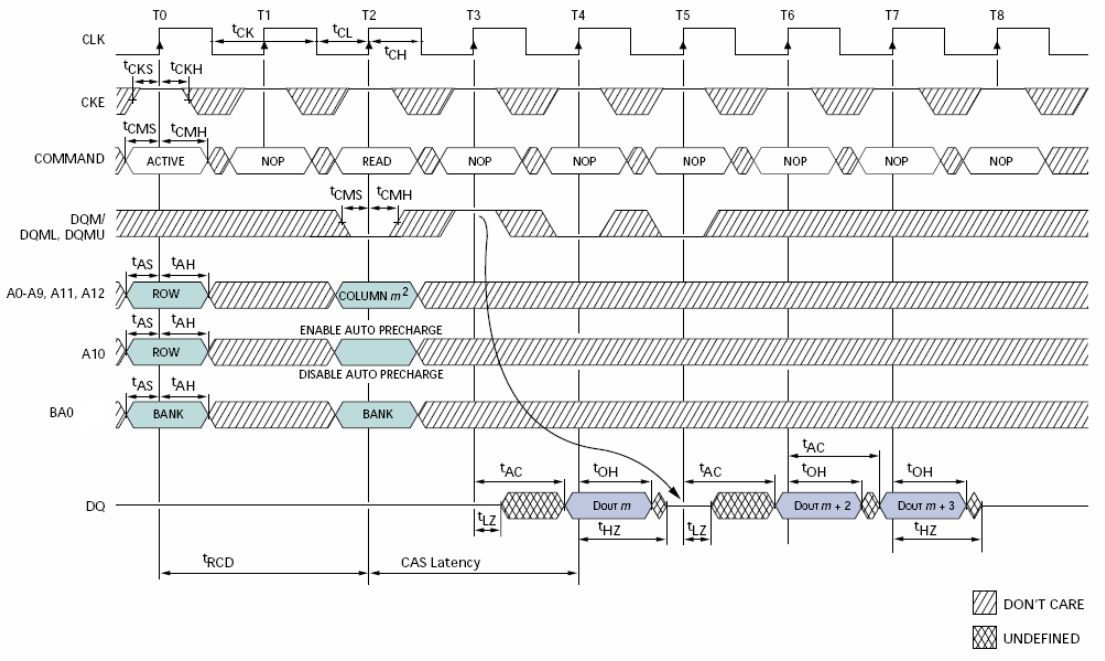


SDRAM IF– Read

NOTE:

1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a "manual" PRECHARGE.

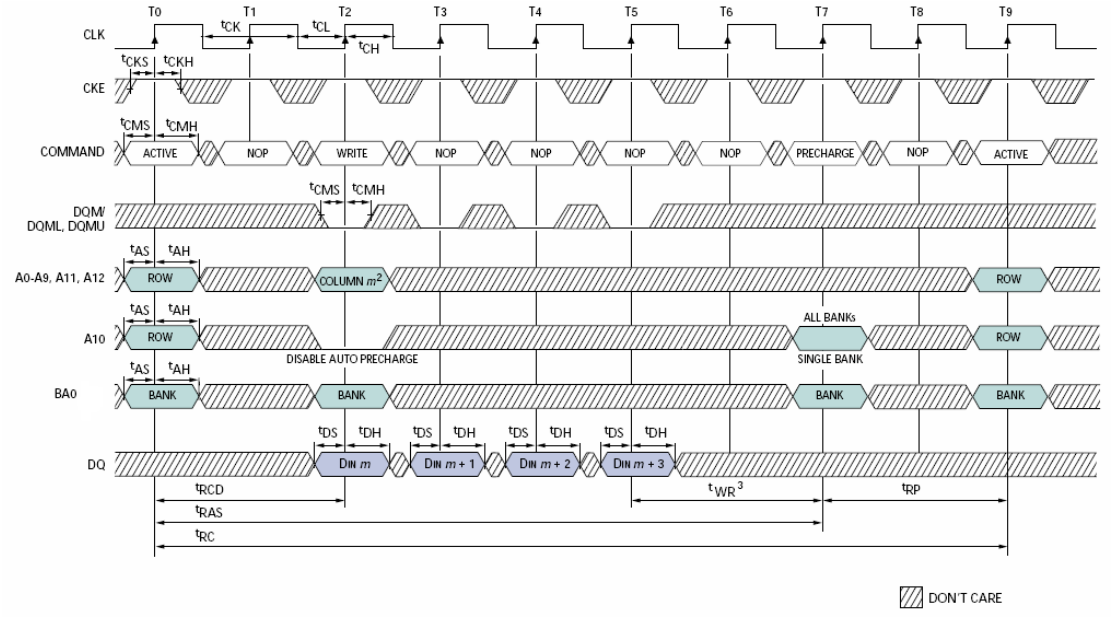
2. CAS latency indicated in parentheses



SDRAM IF – Read DQM Operation

NOTE:

1. For this example, the burst length = 4, and the CAS latency = 2.
2. CAS latency indicated in parentheses.



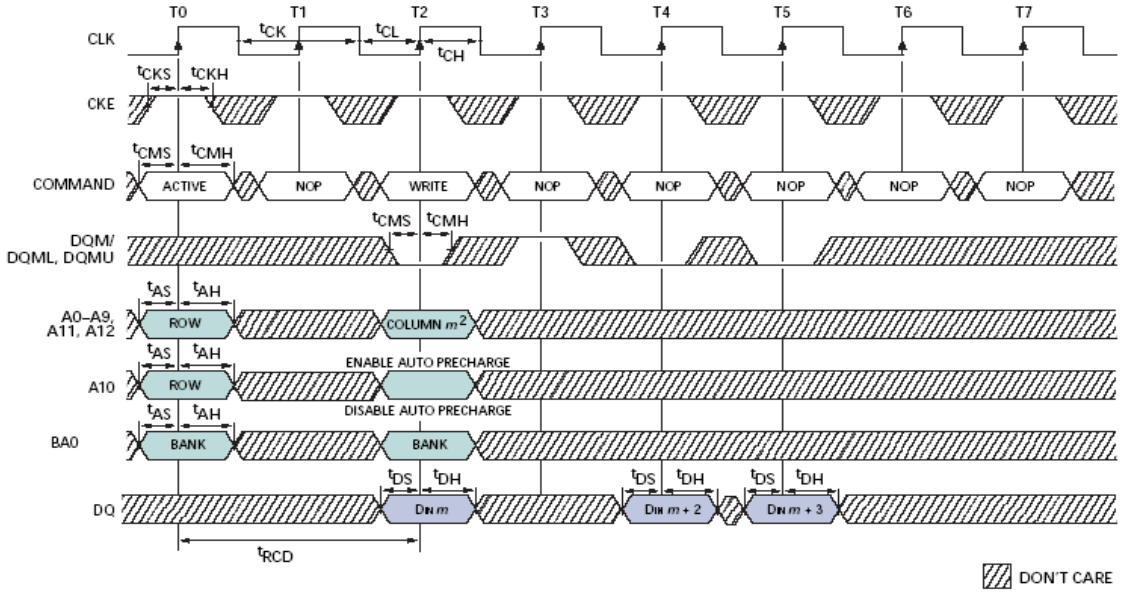
SDRAM IF– Write

NOTE:

1. For this example, the burst length = 4, and the WRITE burst is followed by a “manual” PRECHARGE.

2. 14ns to 15ns is required between <DIN m> and the PRECHARGE command, regardless of frequency.

3. CAS latency indicated in parentheses.



SDRAM IF– Write-DQM Operation

NOTE:

1. For this example, the burst length = 4.
2. CAS latency indicated in parentheses.

SDRAM IF – Parameter

AC Characteristics		Symbol	PC-100		Units
Parameter			Min	Max	
Access time from CLK (positive edge)	CL = 3	tAC (3)		7	ns
	CL = 2	tAC (2)		8	ns
Address hold time		tAH	1		ns
Address setup time		tAS	2.5		ns
CLK high-level width		tCH	3		ns
CLK low-level width		tCL	3		ns
Clock cycle time	CL = 3	tCK (3)	10		ns
	CL = 2	tCK (2)	12		ns
CKE hold time		tCKH	1		ns
CKE setup time		tCKS	2.5		ns
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	1		ns
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	2.5		ns
Data-in hold time		tDH	1		ns
Data-in setup time		tDS	2.5		ns
Data-out High-Z time	CL = 3	tHZ (3)		7	ns
	CL = 2	tHZ (2)		8	ns
Data-out Low-Z time		tLZ	1		ns
Data-out hold time (load)		tOH	2.5		ns
Data-out hold time (no load)		tOHN	1.8		ns
ACTIVE-to-PRECHARGE command		tRAS	50	120,000	ns
ACTIVE-to-ACTIVE command period		tRC	100		ns
ACTIVE-to-READ or WRITE delay		tRCD	20		ns
Refresh period		tREF		64	ms
AUTO REFRESH command period		tRFC	100		ns
PRECHARGE command period		tRP	20		ns
ACTIVE bank a to ACTIVE bank b		tRRD	2		tCK

command				
Transition time	tT	0.5	1.2	ns
WRITE recovery time Auto precharge mode (a)	tWR (a)	1 CLK +5ns		–
Manual precharge mode (m)	tWR (m)	15		ns
Exit SELF REFRESH to ACTIVE command	tXSR	100		ns

24 Ordering Information

24.1 Recommended Soldering Conditions

Soldering Conditions for Surface-mount Devices

Soldering Process	Soldering Conditions
Infrared Ray Reflow	Peak package's surface temperature: 235℃ (Lead) or 260℃ (Lead Free)
	Reflow time: 30 seconds or less (210℃or more)—(Lead) or 60 seconds or less (217℃or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note:

The maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution:

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

24.2 Precaution against ESD for Semiconductors

When the strong electric field is exposed to a MOS device, the destruction of the gate oxide may occur and then it can ultimately degrade the device operation. Measures must be taken to stop the generation of static electricity as many as possible, and it is a must to quickly

dissipate the static electricity when it occurs. Environmental control must be adequate enough. Humidifier should be used when it is dry. Recommend to avoid using insulators, which may easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container or a static shielding bag or objects made from conductive material. All test and measurement tools including work bench and floor should be grounded. The operator shall be grounded by using wrist strap. Semiconductor devices shall not be touched with bare hands. Similar precautions shall be taken for PW boards with semiconductor devices on it.

24.3 Handling of Unused Input Pins for CMOS

The cause for no connection to CMOS device inputs can be the malfunction. If no connection is provided for the input pins, the possible cause is that an internal input level may be generated due to noise, etc., which results in malfunction. CMOS devices behave differently from Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin shall be connected to the corresponding power SDRVP/VCC etc. or GND with a resistor, if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device and follows the related specifications governing the devices.

24.4 Status before Initialization of MOS Devices

Power-on does not necessarily define the initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned on, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after the power-on.

25 Pin Description

25.1 ATJ 2256

25.1.1 Pin Definition

Pin No.	Pin Name	Function Name	I/O Type	Reset Default	Description
1	LOSCI	LOSCI	AI		Low Oscillator Input
2	LOSCO	LOSCO	AO		Low Oscillator Output
3	CEB5	ATA_CS1B/ NOR_CEB5/ RGB_CE	O		Ata Interface CS1 Nor Flash CE5 RGB Interface CE
		GPIOB28	BI		GPIOB Port 28
4	CEB2	NF_CEB2 /RGB_CE	O	1	NAND FLASH Interface CE2 RGB Interface CE
		GPIOA17	BI		GPIOA Port 17
5	CEB1	NF_CEB1 /RGB_CE	O		NAND FLASH Interface CE1 RGB Interface CE
6	SIRQ1	SIRQ1	I	z	External IRQ 1
		GPIOB31	BI		GPIOB Port 31
7	WRB	NF_WR /RGB_WRB	O		NAND FLASH Interface WR RGB Interface WR
8	RDB	NF_RD /RGB_RDB	O		NAND FLASH Interface RD RGB Interface RD
9	VDD	VDD	PWRI		VDD
10	VCC	VCC	PWRI		VCC
11	GND	GND	PWR		GND

12	SDRBA0	SDRAM_BA0	O		SDRAM Interface Bank Address0
13	SDRDQ0	SDRAM_DQ0	BI		SDRAM Interface Data 0
14	SDRA0	SDRAM_A0	O		SDRAM Interface Address 0
15	SDRA1	SDRAM_A1	O		SDRAM Interface Address 1
16	SDRDQ1	SDRAM_DQ1	BI		SDRAM Interface Data 1
17	SDRA2	SDRAM_A2	O		SDRAM Interface Address2
18	SDRBA1	SDRAM_BA1	O		SDRAM Interface Bank Address 1
19	SDRA3	SDRAM_A3	O		SDRAM Interface Address 3
20	SDRDQ2	SDRAM_DQ2	BI		SDRAM Interface Data 2
21	SDRA4	SDRAM_A4	O		SDRAM Interface Address 4
22	SDRA5	SDRAM_A5	O		SDRAM Interface Address 5
23	SDRDQ3	SDRAM_DQ3	BI		SDRAM Interface Data 3
24	SDRA6	SDRAM_A6	O		SDRAM Interface Address 6
25	SDRVP	SDRAM_VP	PWRI		SDRAM Interface Power
26	SDRDQ4	SDRAM_DQ4	BI		SDRAM Interface Data 4
27	SDRA7	SDRAM_A7	O		SDRAM Interface Address 7
28	SDRA8	SDRAM_A8	O		SDRAM Interface Address 8
29	SDRDQ5	SDRAM_DQ5	BI		SDRAM Interface Data 5
30	SDRA9	SDRAM_A9	O		SDRAM Interface Address 9
31	SDRA10	SDRAM_A10	O		SDRAM Address 10
32	SDRDQ6	SDRAM_DQ6	BI		SDRAM Interface Data 6
33	SDRA11	SDRAM_A11	O		SDRAM Interface Address11
		GPIOA25	BI		GPIOA Port 25
34	SDRDQ7	SDRAM_DQ7	BI		SDRAM Interface Data7
35	SDRWEB	SDRAM_WEB	O		SDRAM Interface Write Enable
36	SDRDQ8	SDRAM_DQ8	BI		SDRAM Interface Data 8
37	SDRA12	SDRAM_A12	O		SDRAM Interface Address12
		GPIOA26	BI		GPIOA Port 26
38	SDRDQ9	SDRAM_DQ9	BI		SDRAM Interface Data 9

39	SDRDQ10	SDRAM_DQ10	BI		SDRAM Interface Data10
40	SDRDQ11	SDRAM_DQ11	BI		SDRAM Interface Data11
41	SDRDQ12	SDRAM_DQ12	BI		SDRAM Interface Data 12
42	SDRRASB	SDRAM_RASB	O		SDRAM Interface RAS
43	SDRCASB	SDRAM_CASB	O		SDRAM Interface CAS
44	SDRDQ13	SDRAM_DQ13	BI		SDRAM Interface Data13
45	SDRCSB	SDRAM_CSB	O		SDRAM Interface CS
46	SDRGND	SDRAM_GND	PWR		SDRAM Interface GND
47	SDRVP	SDRAM_VP	PWRI		SDRAM Interface Power
48	SDRCK	SDRAM_CK	O		SDRAM Interface Clock
49	SDRCKE	SDRAM_CKE	O		SDRAM Interface Clock Enable
50	SDRDQM0	SDRAM_LDQM	O		SDRAM Interface LDQM (for 16bits SDRAM)
51	SDRDQ14	SDRAM_DQ14	BI		SDRAM Data14
52	SDRDQM1	SDRAM_DQM/UDQM	O		SDRAM Interface DQM (for 8bits SDRAM) SDRAM Interface UDQM (for 16bits SDRAM)
53	SDRDQ15	SDRAM_DQ15	BI		SDRAM Interface Data15
54	NC				
55	VBUS	VBUS	I		VBUS
56	ID	ID	BI		OTG Interface ID
57	UVCC	UVCC	PWR		UVCC
58	DP	DP	BI		Data Plus
59	DM	DM	BI		Data Minus
60	UGND	UGND	PWR		UGND
61	RREF	RREF	AO		Reference Resistance

62	UART1RX	UART1_RX /SPI_MISO /I2C2_SDA /SPDIF_RX	BI	z	Uart1 Interface RX SPI Interface MISO I2C2 Interface SDA SPDIF Interface RX
		GPIOB15	BI		GPIOB Port 15
63	UART1TX	UART1_TX /SPI_SS /I2C2_SCL /SPDIF_TX	BI	1	Uart1 Interface Tx SPI Interface Slave Selection I2C2 Interface SCL SPDIF Interface TX
		GPIOB14	BI		GPIOB Port 14
64	MICIN	MICIN	AI		Microphone In Left Channel
65	VMIC	VMIC	AI		Microphone Power Supply
66	FMINR	FMINR	AI		FM In Right Channel
67	FMINL	FMINL	AI		FM in Left Channel
68	AGND	AGND	PWR		Audio Analog GND
69	AVCC	AVCC	PWRO		Audio Analog VCC
70	VRDA	VRDA	AO		Audio DAC Voltage Reference
71	VREFI	VREFI	AI		Voltage Reference Input
72	PAGND	PAGND	PWR		Audio PA GND
73	AOUTR	AOUTR	AO		Audio output Right Channel
74	PAVCC	PAVCC	PWRO		Audio PA VCC
75	AOUTL	AOUTL	AO		Audio output Left Channel
76	TVCVBS	TVCVBS	AO		Video CVBS signal Output
77	TVREF	TVREF	AO		TV reference Resistance
78	AVDD	AVDD	PWRO		Audio VDD
79	HOSCO	HOSCO	AO		High Oscillator Output
80	HOSCI	HOSCI	AI		High Oscillator Input
81	VCC	VCC	PWRI		VCC
82	KSIN2	KSIN[2]	BI	1	Key Scan Input2
		GPIOA10	BI		GPIOA Port 10

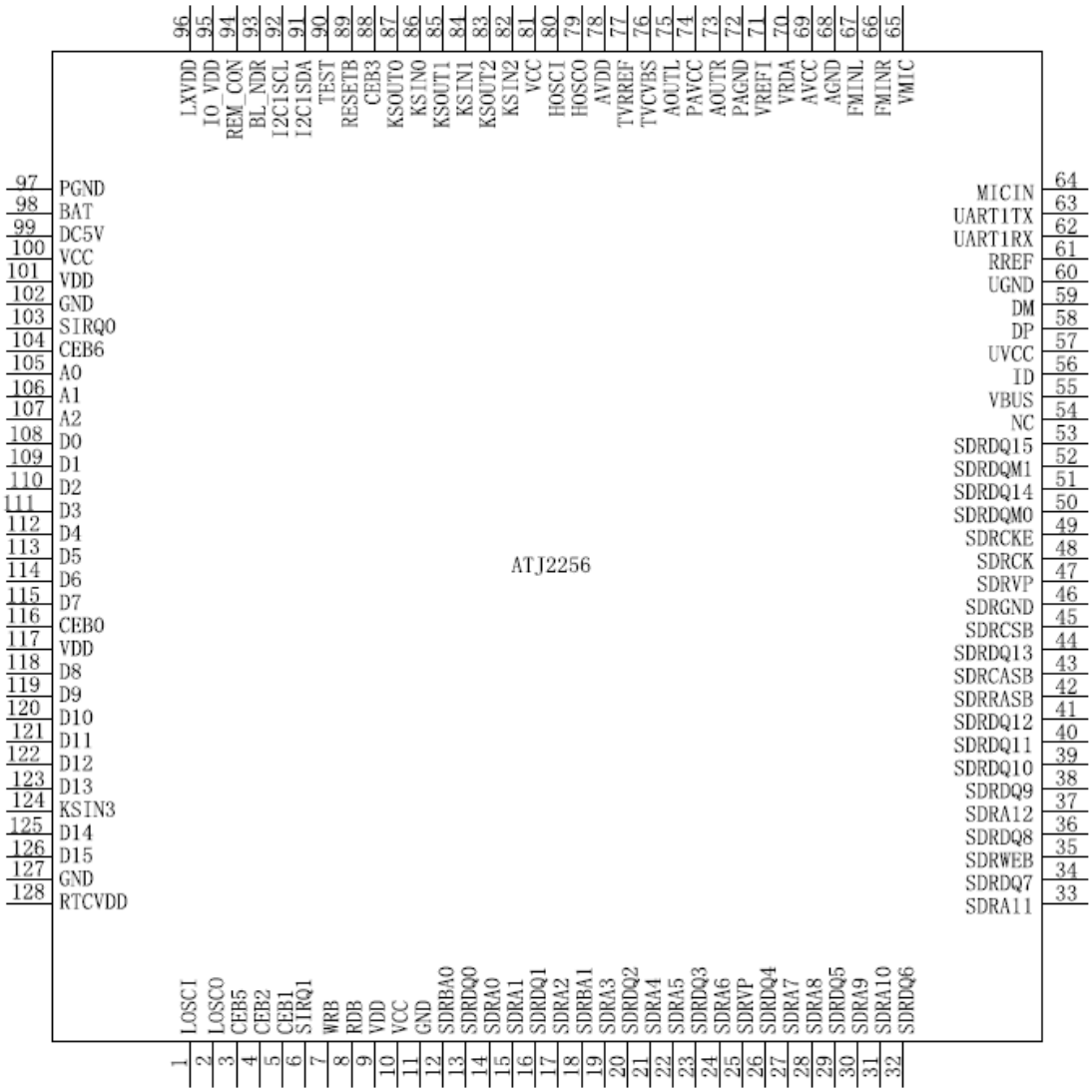
83	KSOUT2	KS_OUT[2]	BI	1	Key Scan output 2
		GPIOB22	BI		GPIOB Port 22
84	KSIN1	KS_IN[1]	BI	1	Key Scan Input 1
		GPIOA9	BI		GPIOA Port 9
85	KSOUT1	KS_OUT[1]	BI	z	Key Scan Output 1
		GPIOA13	BI		GPIOA Port 13
86	KSIN0	KS_IN[0]	BI	1	KEY Scan in 0
		GPIOA8	BI		GPIOA Port 8
87	KSOUT0	KS_OUT[0]	BI	z	Key Scan Output 0
		GPIOA12	BI		GPIOA Port12
88	CEB3	NF_CEB3	O		NAND FLASH Interface CE3
89	RESETB	RESETB	I		System RESET
90	TEST /CLKOUT	TEST	I		TEST FM Module Clock out
91	I2C1SDA	I2C1_SDA /UART2IR_RX /UART1_CTSB /SPI_MOSI	BI	z	I2C1 Interface SDA UART2 or IrDA Interface RX Uart1 Interface CTS SPI Interface Master Output Slave in
		GPIOA7	BI		GPIOA Port 7
92	I2C1SCL	I2C1_SCL /UART2IR_TX /UART1_RTSB /SPI_SCK	BI	z	I2C1 Interface SCL UART2 or IrDA Interface TX Uart1 Interface RTS SPI Interface Clock
		GPIOA6	BI		GPIOA Port 6
93	BL_NDR	BL_NDR	AO		Back Light NDR
94	REM_CON	REM_CON	AI		Remote Control ADC input
95	IO_VDD	IO_VDD	PWR		POWER Pin IOVDD
96	LXVDD	LXVDD	PWR		POWER Pin LXVDD
97	PGND	PGND	PWR		POWER MOS GND
98	BAT	BAT	PWRI		Battery input

99	DC5V	DC5V	PWRI		DC5V input
100	VCC	VCC	PWRIO		VCC
101	VDD	VDD	PWRIO		VDD
102	GND	GND	PWR		GND
103	SIRQ0	External IRQ 0	I		External IRQ 0
		GPIOA Port 31	BI		GPIOA Port 31
104	CEB6	SD_CLK /CE6	O	1	SD CARD Interface CLOCK LCD Interface CE6
		GPIOB29	BI		GPIOB Port 29
105	A0	NF_ALE /RGB_WD[0]	O	0	NAND FLASH ALE RGB Interface Data0
		GPIOA0	BI		GPIOA Port 0
106	A1	NF_RB /RGB_WD[9]	O	0	NAND FLASH Interface Ready/Busy RGB Interface Data 9
		GPIOA1	BI		GPIOA Port 1
107	A2	NF_CLE /RGB_RS /SD_CMD	O	0	NAND FLASH Interface CLE RGB Interface RS SD card Interface CMD
		GPIOA2	BI		GPIOA Port 2
108	D0	NF_D[8] /RGB_WD[1] /SD_DAT[0]	BI		NAND FLASH Data 8 RGB Interface Data 1 SD Card Interface Data 0
109	D1	NF_D[9] /RGB_WD[2] /SD_DAT[1]	BI		NAND FLASH Interface Data 9 RGB Interface Data 2 SD Card Interface Data 1
110	D2	NF_D[10] /RGB_WD[3] /SD_DAT[2]	BI		NAND FLASH Interface Data 10 RGB Interface Data 3 SD Card Interface Data 2

111	D3	NF_D[11] /RGB_WD[4] /SD_DAT[3]	BI		NAND FLASH Interface Data 11 RGB Interface Data 4 SD Card Interface Data 3
112	D4	NF_D[12] /RGB_WD[5] /SD_DAT[4]	BI		NAND FLASH Interface Data 12 RGB Interface Data 5 SD Card Interface Data 4
113	D5	NF_D[13] /RGB_WD[6] /SD_DAT[5]	BI		NAND FLASH Interface Data 13 RGB Interface Data 6 SD card Interface Data 5
114	D6	NF_D[14] /RGB_WD[7] /SD_DAT[6]	BI		NAND FLASH Interface Data 14 RGB Interface Data 7 SD card Interface Data 6
115	D7	NF_D[15] /RGB_WD[8] /SD_DAT[7]	BI		NAND FLASH Interface Data 15 RGB Interface Data 8 SD card Interface Data 7
116	CEB0	NF_CEB0	O		NAND FLASH Interface CE0
		GPIOA16	BI		GPIOA Port 16
117	VDD	VDD	PWRI		VDD
118	D8	NF_D[0] /RGB_WD[10]	BI		NAND FLASH Data 0 RGB Interface Data 10
119	D9	NF_D[1] /RGB_WD[11]	BI		NAND FLASH Interface Data 1 RGB Interface Data 11
120	D10	NF_D[2] /RGB_WD[12]	BI		NAND FLASH Interface Data 2 RGB Interface Data 12
121	D11	NF_D[3] /RGB_WD[13]	BI		NAND FLASH Interface 3 RGB Interface Data 13
122	D12	NF_D[4] /RGB_WD[14]	BI		NAND FLASH Data 4 RGB Interface Data 14
123	D13	NF_D[5] /RGB_WD[15]	BI		NAND FLASH Interface Data 5 RGB Interface WD 15

127	KSIN3	KS_IN[3] / GPIOA11	BI		Key scan input 3 GPIOA port 11
125	D14	NF_D[6] /RGB_WD[16]	BI		NAND FLASH Data 6 RGB Interface Data 16
126	D15	NF_D[7] /RGB_WD[17]	BI		NAND FLASH Interface Data 7 RGB Interface Data 17
127	GND	GND	PWR		GND
128	RTCVDD	RTCVDD	PWRI		RTC Power VDD

25.1.2 Pin Assignment



25.2 ATJ 2257

25.2.1 Pin Definition

Pin No.	Pin Name	Function Name	I/O Type	Reset Default	Short Description
1	LOSCI	LOSCI	AI		Low Oscillator Input

2	LOSCO	LOSCO	AO		Low Oscillator Output
3	CEB2	NF_CEB2	O	1	NAND FLASH Interface CE2
		RGB_CE			RGB Interface CE
		GPIOA17	BI		GPIOA Port 17
4	CEB1	NF_CEB1	O		NAND FLASH Interface CE1
		RGB_CE			RGB Interface CE
5	GPIOB6	BT656_D[6]	BI	0	BT656 Interface Data 6
		GPIOB6	BI		GPIOB Port 6
6	SIRQ1	SIRQ1	I	z	External IRQ 1
		GPIOB31	BI		GPIOB Port 31
7	DRVVBUS	DRV_VBUS	O	0	OTG Interface VBUS
		RGB_RDB	BI		RGB Interface RD
		GPIOA15			GPIOA Port 15
8	WRB	NF_WR	O		NAND FLASH Interface WR
		RGB_WRB			RGB Interface WR
9	GPIOB7	BT656_D[7]	BI	0	BT656 Interface Data 7
		GPIOB7	BI		GPIOB Port 7
10	RDB	NF_RD	O		NAND FLASH Interface RD
		RGB_RDB			RGB Interface RD
11	GPIOB8	BT656_PCLK	BI	0	BT656 Interface PCLK
		GPIOB8	BI		GPIOB Port 8
12	GPIOB11	BT656_CLKOUT	BI	0	BT656 Interface CLKOUT
		GPIOB11	BI		GPIOB Port 11
13	VDD	VDD	PWRI		VDD
14	VCC	VCC	PWRI		VCC
15	GND	GND	PWR		GND
16	SDRBA0	SDRAM_BA0	O		SDRAM Interface Bank Address0
17	SDRDQ0	SDRAM_DQ0	BI		SDRAM Interface Data 0
18	SDRA0	SDRAM_A0	O		SDRAM Interface Address 0

19	SDRA1	SDRAM_A1	O		SDRAM Interface Address 1
20	SDRDQ1	SDRAM_DQ1	BI		SDRAM Interface Data 1
21	SDRA2	SDRAM_A2	O		SDRAM Interface Address2
22	SDRBA1	SDRAM_BA1	O		SDRAM Interface Bank Address 1
23	SDRA3	SDRAM_A3	O		SDRAM Interface Address 3
24	SDRDQ2	SDRAM_DQ2	BI		SDRAM Interface Data 2
25	SDRA4	SDRAM_A4	O		SDRAM Interface Address 4
26	SDRA5	SDRAM_A5	O		SDRAM Interface Address 5
27	SDRDQ3	SDRAM_DQ3	BI		SDRAM Interface Data 3
28	SDRA6	SDRAM_A6	O		SDRAM Interface Address 6
29	SDRVP	SDRAM_VP	PWRI		SDRAM Interface Power
30	SDRGND	SDRAM_GND	PWR		SDRAM Interface GND
31	SDRDQ4	SDRAM_DQ4	BI		SDRAM Interface Data 4
32	SDRA7	SDRAM_A7	O		SDRAM Interface Address 7
33	SDRA8	SDRAM_A8	O		SDRAM Interface Address 8
34	SDRDQ5	SDRAM_DQ5	BI		SDRAM Interface Data 5
35	SDRA9	SDRAM_A9	O		SDRAM Interface Address 9
36	SDRA10	SDRAM_A10	O		SDRAM Address 10
37	SDRDQ6	SDRAM_DQ6	BI		SDRAM Interface Data 6
38	SDRA11	SDRAM_A11	O		SDRAM Interface Address11
		GPIOA25	BI		GPIOA Port 25
39	SDRDQ7	SDRAM_DQ7	BI		SDRAM Interface Data7
40	SDRWEB	SDRAM_WEB	O		SDRAM Interface Write Enable
41	SDRDQ8	SDRAM_DQ8	BI		SDRAM Interface Data 8
42	SDRA12	SDRAM_A12	O		SDRAM Interface Address12
		GPIOA26	BI		GPIOA Port 26
43	SDRDQ9	SDRAM_DQ9	BI		SDRAM Interface Data 9
44	SDRDQ10	SDRAM_DQ10	BI		SDRAM Interface Data10
45	SDRDQ11	SDRAM_DQ11	BI		SDRAM Interface Data11
46	SDRDQ12	SDRAM_DQ12	BI		SDRAM Interface Data 12

47	SDRRASB	SDRAM_RASB	O		SDRAM Interface RAS
48	SDRCASB	SDRAM_CASB	O		SDRAM Interface CAS
49	SDRDQ13	SDRAM_DQ13	BI		SDRAM Interface Data13
50	SDRCSB	SDRAM_CSB	O		SDRAM Interface CS
51	SDRGND	SDRAM_GND	PWR		SDRAM Interface GND
52	SDRVP	SDRAM_VP	PWRI		SDRAM Interface Power
53	SDRCK	SDRAM_CK	O		SDRAM Interface Clock
54	SDRCKE	SDRAM_CKE	O		SDRAM Interface Clock Enable
55	SDRDQM0	SDRAM_LDQM	O		SDRAM Interface LDQM(for 16bits SDRAM)
56	SDRDQ14	SDRAM_DQ14	BI		SDRAM Data14
57	SDRDQM1	SDRAM_DQM	O		SDRAM Interface DQM (for 8bits SDRAM)
		UDQM			SDRAM Interface UDQM (for 16bits SDRAM)
58	SDRDQ15	SDRAM_DQ15	BI		SDRAM Interface Data15
59	VBUS	VBUS	I		OTG Interface VBUS
60	ID	ID	BI		OTG Interface ID
61	UVCC	UVCC	PWR		OTG Interface UVCC
62	DP	DP	BI		OTG Interface Data Plus
63	DM	DM	BI		OTG Interface Data Minus
64	UGND	UGND	PWR		OTG Interface UGND
65	UREF	RREF	AO		OTG Interface Reference Resistance
66	UGNDS	UGNDS	PWR		OTG Interface UGND
67	UVCCS	UVCCS	PWR		OTG Interface UVCC
68	UART1RX	UART1_RX	BI	z	Uart1 Interface RX
		SPI_MISO			SPI Interface MISO
		I2C2_SDA			I2C2 Interface SDA
		SPDIF_RX			SPDIF Interface RX
		GPIOB15			GPIOB Port 15

69	UART1TX	UART1_TX	BI	1	Uart1 Interface Tx
		SPI_SS			SPI Interface Slave Selection
		I2C2_SCL			I2C2 Interface SCL
		SPDIF_TX			SPDIF Interface TX
		GPIOB14			GPIOB Port 14
70	MICIN	MICIN	AI		Microphone Input
71	VMIC	VMIC	AI		Microphone Power Supply
72	FMINR	FMINR	AI		FM Input Right Channel
73	FMINL	FMINL	AI		FM input Left Channel
74	AGND	AGND	PWR		Audio Analog GND
75	AVCC	AVCC	PWRO		Audio Analog VCC
76	VRDA	VRDA	AO		Audio DAC Voltage Reference
77	VREFI	VREFI	AI		Voltage Reference Input
78	PAGND	PAGND	PWR		Audio PA GND
79	AOUTR	AOUTR	AO		Audio output Right Channel
80	PAVCC	PAVCC	PWRO		Audio PA VCC
81	AOUTL	AOUTL	AO		Audio output Left Channel
82	TVOUT	TVCVBS	AO		Video CVBS signal Output
83	TVREF	TVREF	AO		TV reference Resistance
84	AVDD	AVDD	PWRO		Audio VDD
85	HOSCO	HOSCO	AO		High Oscillator Output
86	HOSCI	HOSCI	AI		High Oscillator Input
87	VCC	VCC	PWRI		VCC
88	KSIN2	KSIN[2]	BI	1	Key Scan Input2
		GPIOA10	BI		GPIOA Port 10
89	KSOUT2	KS_OUT[2]	BI	1	Key Scan output 2
		GPIOB22	BI		GPIOB Port 22
90	KSIN1	KS_IN[1]	BI	1	Key Scan Input 1
		GPIOA9	BI		GPIOA Port 9
91	KSOUT1	KS_OUT[1]	BI	z	Key Scan Output 1

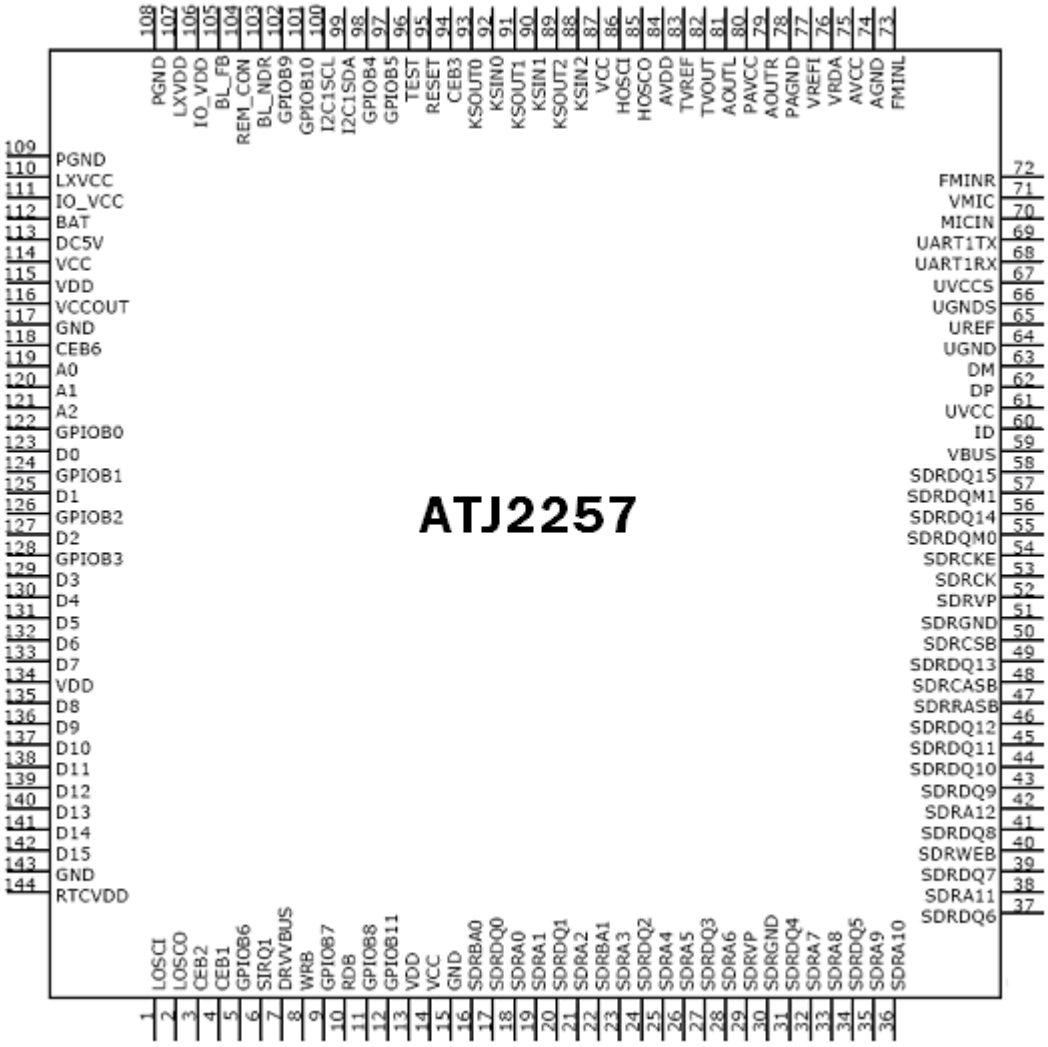
		GPIOA13	BI		GPIOA Port 13
92	KSIN0	KS_IN[0]	BI	1	KEY Scan in 0
		GPIOA8	BI		GPIOA Port 8
93	KSOUT0	KS_OUT[0]	BI	z	Key Scan Output 0
		GPIOA12	BI		GPIOA Port12
94	CEB3	NF_CEB3	O		NAND FLASH Interface CE3
95	RESET	RESETB	I		System RESET
96	TEST	TEST	I		TEST
		CLKOUT			FM Module Clock out
97	GPIOB5	BT656_D[5]	BI	0	BT656 Interface Data 5
		GPIOB5	BI		GPIOB Port 5
98	GPIOB4	BT656_D[4]	BI	0	BT656 Interface Data 4
		GPIOB4	BI		GPIOB Port 4
99	I2C1SDA	I2C1_SDA	BI	z	I2C1 Interface SDA
		UART2IR_RX	BI		Uart2 or IrDA Interface Rx
		UART1_CTSB			Uart1 Interface CTS
		SPI_MOSI			SPI Interface Master Output Slave in
		GPIOA7			GPIOA Port 7
100	I2C1SCL	I2C1_SCL	BI	z	I2C1 Interface SCL
		UART2IR_TX			Uart2 or IrDA Interface Tx
		UART1_RTSB			Uart1 Interface RTS
		SPI_SCK			SPI Interface Clock
		GPIOA6	BI		GPIOA Port 6
101	GPIOB10	BT656_VSYNC	BI	0	BT656 Interface VSYNC
		GPIOB10	BI		GPIOB Port 10
102	GPIOB9	BT656_HSYNC	BI	0	BT656 Interface HSYNC
		GPIOB9	BI		GPIOB Port 9
103	BL_NDR	BL_NDR （PFM/PWM）	AO		Back Light NDR

104	REM_CON	REM_CON	AI		Remote Control ADC input
105	BL_FB	BL_FB	O		Back Light Feed Back
106	IO_VDD	IO_VDD	PWR		POWER Pin IOVDD
107	LXVDD	LXVDD	PWR		POWER Pin LXVDD
108	PGND	PGND	PWR		POWER MOS GND
109	PGND	PGND	PWR		POWER MOS GND
110	LXVCC	LXVCC	PWR		POWER Pin LXVCC
111	IO_VCC	IO_VCC	PWR		POWER Pin IOVCC
112	BAT	BAT	PWRI		Battery input
113	DC5V	DC5V	PWRI		DC5V input
114	VCC	VCC	PWRIO		VCC
115	VDD	VDD	PWRIO		VDD
116	VCCOUT	VCCOUT	PWRO		Programmed VCC output
117	GND	GND	PWR		GND
118	CEB6	SD_CLK	O	1	SD CARD Interface CLOCK
		GPIOB29	BI		GPIOB Port 29
119	A0	NF_ALE	O	0	NAND FLASH ALE
		RGB_WD[0]			RGB Interface Data0
		GPIOA0	BI		GPIOA Port 0
120	A1	NF_RB	O	0	NAND FLASH Interface Ready/Busy
		RGB_WD[9]			RGB Interface Data 9
		GPIOA1	BI		GPIOA Port 1
121	A2	NF_CLE	O	0	NAND FLASH Interface CLE
		RGB_RS			RGB Interface RS
		SD_CMD			SD card Interface CMD
		GPIOA2	BI		GPIOA Port 2
122	GPIOB0	BT656_D[0]	BI	0	BT656 Interface Data 0
		GPIOB0	BI		GPIOB Port 0
123	D0	NF_D[8]	BI		NAND FLASH Data 8
		RGB_WD[1]			RGB Interface Data 1

		SD_DAT[0]			SD Card Interface Data 0
124	GPIOB1	BT656_D[1]	BI	0	Bt656 Interface Data 1
		GPIOB1	BI		GPIOB Port 1
125	D1	NF_D[9]	BI		NAND FLASH Interface Data 9
		RGB_WD[2]			RGB Interface Data 2
		SD_DAT[1]			SD Card Interface Data 1
126	GPIOB2	BT656_D[2]	BI	0	BT656 Interface Data 2
		GPIOB2	BI		GPIOB Port 2
127	D2	NF_D[10]	BI		NAND FLASH Interface Data 10
		RGB_WD[3]			RGB Interface Data 3
		SD_DAT[2]			SD Card Interface Data 2
128	GPIOB3	BT656_D[3]	BI	0	BT656 Interface Data 3
		GPIOB3	BI		GPIOB Port 3
129	D3	NF_D[11]	BI		NAND FLASH Interface Data 11
		RGB_WD[4]			RGB Interface Data 4
		SD_DAT[3]			SD Card Interface Data 3
130	D4	NF_D[12]	BI		NAND FLASH Interface Data 12
		RGB_WD[5]			RGB Interface Data 5
		SD_DAT[4]			SD Card Interface Data 4
131	D5	NF_D[13]	BI		NAND FLASH Interface Data 13
		RGB_WD[6]			RGB Interface Data 6
		SD_DAT[5]			SD card Interface Data 5
132	D6	NF_D[14]	BI		NAND FLASH Interface Data 14
		RGB_WD[7]			RGB Interface Data 7
		SD_DAT[6]			SD card Interface Data 6
133	D7	NF_D[15]	BI		NAND FLASH Interface Data 15
		RGB_WD[8]			RGB Interface Data 8
		SD_DAT[7]			SD card Interface Data 7
134	VDD	VDD	PWRI		VDD

135	D8	NF_D[0]	BI		NAND FLASH Data 0
		RGB_WD[10]			RGB Interface Data 10
136	D9	NF_D[1]	BI		NAND FLASH Interface Data 1
		RGB_WD[11]			RGB Interface Data 11
137	D10	NF_D[2]	BI		NAND FLASH Interface Data 2
		RGB_WD[12]			RGB Interface Data 12
138	D11	NF_D[3]	BI		NAND FLASH Interface 3
		RGB_WD[13]			RGB Interface Data 13
139	D12	NF_D[4]	BI		NAND FLASH Data 4
		RGB_WD[14]			RGB Interface Data 14
140	D13	NF_D[5]	BI		NAND FLASH Interface Data 5
		RGB_WD[15]			RGB Interface WD 15
141	D14	NF_D[6]	BI		NAND FLASH Data 6
		RGB_WD[16]			RGB Interface Data 16
142	D15	NF_D[7]	BI		NAND FLASH Interface Data 7
		RGB_WD[17]			RGB Interface Data 17
143	GND	GND	PWR		GND
144	RTCVDD	RTCVDD	PWRI		RTC Power VDD

25.2.2 Pin Assignment



25.3 ATJ2257B

25.3.1 Pin Definition

No.	Pin No	Pin Name	Function Name	I/O Type	Driver	Reset Default	Description
1	A1	LXVDD	LXVDD	PWR	/		POW Pin LXVDD
2	A2	IOVDD	IO_VDD	PWR	/		POW Pin IOVDD

3	A3	HOSCI	HOSCI	AI	/		High Oscillator Input
4	A4	PGND	PGND	PWR	/		POWER MOS GND
5	A5	TVRREF	TVRREF	AO	/		TV reference Resistance
6	A6	PAVCC	PAVCC	PWRO	/		Audio PA VCC
7	A7	AGND	AGND	PWR	/		Audio Analog GND
8	A8	AVCC	AVCC	PWRO	/		Audio Analog VCC
9	A9	VMIC	VMIC	AI	/		Microphone Power Supply
10	A10	DP	DP	BI	/		OTG Interface Data Plus
11	A11	VBUS	VBUS	I	/		OTG Interface VBUS
12	A12	PAGND	PAGND	PWR	/		Audio PA GND
13	B1	VDD	VDD	PWRI	/		VDD
14	B2	BAT	BAT	PWRI	/		Battery Input
15	B3	HOSCO	HOSCO	AO	/		High Oscillator Output
16	B4	AVDD	AVDD2	PWRO	/		Audio VDD
17	B5	TVCVBS	TVCVBS	AO	/		Video CVBS signal Output
18	B6	VRDA	VRDA	AO	/		Audio DAC Voltage Reference
19	B7	VREFI	VREFI	AI	/		Voltage Reference Input
20	B8	MICIN	MICIN	AI	/		Microphone Input
21	B9	UREF	RREF	AO	/		OTG Interface Reference Resistance
22	B10	ID	ID	BI	/		OTG Interface ID
23	B11	DM	DM	BI	/		OTG Interface Data Minus
24	B12	UVCC	UVCC	PWR	/		OTG Interface UVCC

25	C1	VCC	VCC	PWRI	/		VCC
26	C2	DC5V	DC5V	PWRI	/		DC5V Input
27	C3	I2C1SDA	I2C1_SDA /UART2IR_RX /UART1_CTSB /SPI_MOSI	BI	2mA		I2C1 Interface SDA Uart2 or IrDA Interface Rx Uart1 Interface CTS SPI Interface Master Output Slave in
			GPIOA7	BI			GPIOA Port 7
28	C4	RESETB	RESETB	I	/		System RESET
29	C5	KSOUT1	KS_OUT[1] /EJ_DINT	BI	2mA		Key Scan Output 1 EJTAG Port DINT
			GPIOA13	BI			GPIOA Port 13
30	C6	KSIN1	KS_IN[1] /EJ_TMS	BI	2mA		Key Scan Input 1 EJTAG Port TMS
			GPIOA9	BI			GPIOA Port 9
31	C7	AOUTL	AOUTL	AO	/		Audio Output Left Channel
32	C8	FMINL	FMINL	AI	/		FM in Left Channel
33	C9	UART1TX	UART1_TX /SPI_SS /I2C2_SCL /SPDIF_TX	BI	2mA		Uart1 Interface TX SPI Interface Slave Selection I2C2 Interface SCL SPDIF Interface TX
			GPIOB14	BI			GPIOB Port 14
34	C10	UART1RX	UART1_RX /SPI_MISO /I2C2_SDA /SPDIF_RX	BI	2mA		Uart1 Interface RX SPI Interface MISO I2C2 Interface SDA SPDIF Interface RX
			GPIOB15	BI			GPIOB Port 15

35	C11	SDRDQ0	SDRAM_DQ0	BI	8mA		SDRAM Interface Data 0
36	C12	SDRDQ1	SDRAM_DQ1	BI	8mA		SDRAM Interface Data 1
37	D1	GND	GND	PWR	/		GND
38	D2	VCCOUT	VCCOUT	PWRO	/		Programmed VCC Output
39	D3	I2C1SCL	I2C1_SCL /UART2IR_TX /UART1_RTSB /SPI_SCK	BI	2mA		I2C1 Interface SCL Uart2 or IrDA Interface Tx Uart1 Interface RTS SPI Interface Clock
			GPIOA6	BI			GPIOA Port 6
40	D4	KSOUT0	KS_OUT[0] /EJ_TDO	BI	2mA		Key Scan Output 0 EJTAG Port TDO
			GPIOA12	BI			GPIOA Port12
41	D5	KSOUT2	KS_OUT[2] /EJ_TRST-	BI	2mA		Key Scan Output 2 EJTAG Port TRST
			GPIOB22	BI			GPIOB Port 22
42	D6	KSIN2	KSIN[2] /EJ_TDI	BI	2mA		Key Scan Input2 EJTAG Port TDI
43	D7	AOUTR	AOUTR	AO	/		Audio Output Right Channel
44	D8	FMINR	FMINR	AI	/		FM In Right Channel
45	D9	SDRDQ15	SDRAM_DQ15	BI	8mA		SDRAM Interface Data15
46	D10	SDRDQ14	SDRAM_DQ14	BI	8mA		SDRAM Data14
47	D11	SDRDQ2	SDRAM_DQ2	BI	8mA		SDRAM Interface Data2
48	D12	SDRDQ3	SDRAM_DQ3	BI	8mA		SDRAM Interface

							Data3
49	E1	A15	BT656_HSYNC /NOR_A[15]	BI	2mA		BT656 Interface HSYNC Nor Flash Address 15
			GPIOB9	BI			GPIOB Port 9
50	E2	A16	BT656_VSYNC /NOR_A[16]	BI	2mA		BT656 Interface VSYNC NOR Flash address16
			GPIOB10	BI			GPIOB Port 10
51	E3	A10	BT656_D[4] /NOR_A[10]	BI	4mA		BT656 Interface Data 4 Nor Flash Interface Address 10
			GPIOB4	BI			GPIOB Port 4
52	E4	A14	BT656_PCLK /NOR_A[14]	BI	4mA		BT656 Interface PCLK Nor Flash Address 14
			GPIOB8	BI			GPIOB Port 8
53	E5	KSIN0	KS_IN[0] /EJ_TCK	BI	2mA		KEY Scan in 0 EJTAG Port TCK
			GPIOA8	BI			GPIOA Port 8
54	E6	REMCON	REM_CON	AI	/		Remote Control ADC Input
55	E7	TEST	TEST /CLKOUT	I	/		TEST FM Module Clock out
56	E8	SDRA12	SDRAM_A12	O	8mA		SDRAM Interface Address12
			GPIOA26	BI			GPIOA Port 26
57	E9	SDRDQ13	SDRAM_DQ13	BI	8mA		SDRAM Interface Data13
58	E10	SDRDQ12	SDRAM_DQ12	BI	8mA		SDRAM Interface Data

							12
59	E11	SDRDQ4	SDRAM_DQ4	BI	8mA		SDRAM Interface Data 4
60	E12	SDRDQ5	SDRAM_DQ5	BI	8mA		SDRAM Interface Data 5
61	F1	A13	BT656_D[7] /NOR_A[13]	BI	4mA		BT656 Interface Data 7 Nor Flash Address13
			GPIOB7	BI			GPIOB Port 7
62	F2	A17	BT656_CLKOUT /NOR_A[17]	BI	8mA		BT656 Interface CLKOUT Nor Flash Interface Address 17
			GPIOB11	BI			GPIOB Port 11
63	F3	A6	BT656_D[0] /NOR_A[6]	BI	4mA		BT656 Interface Data 0 Nor Flash Address 6
			GPIOB0	BI			GPIOB Port 0
64	F4	A9	BT656_D[3] /NOR_A[9]	BI	4mA		BT656 Interface Data 3 Nor Flash Interface Address 9
			GPIOB3	BI			GPIOB Port 3
65	F5	BL_NDR	BL_NDR	AO	/		Back Light NDR
66	F6	VCC	VCC	PWRI	/		VCC
67	F7	VCC	VCC	PWRI	/		VCC
68	F8	SD_VP	SDRAM_VP	PWRI	/		SDRAM Interface Power
69	F9	SDRDQ11	SDRAM_DQ11	BI	8mA		SDRAM Interface Data11

70	F10	SDRDQ10	SDRAM_DQ10	BI	8mA		SDRAM Interface Data10
71	F11	SDRDQ6	SDRAM_DQ6	BI	8mA		SDRAM Interface Data 6
72	F12	SDRDQ7	SDRAM_DQ7	BI	8mA		SDRAM Interface Data7
73	G1	A12	BT656_D[6] /NOR_A[12]	BI	4mA		BT656 Interface Data 6 Nor Flash Interface Address 12
			GPIOB6	BI			GPIOB Port 6
74	G2	A11	BT656_D[5] /NOR_A[11]	BI	4mA		BT656 Interface Data 5 Nor Flash A 11
			GPIOB5	BI			GPIOB Port 5
75	G3	A7	BT656_D[1] /NOR_A[7]	BI	4mA		Bt656 Interface Data 1 Nor Flash Interface Address 7
			GPIOB1	BI			GPIOB Port 1
76	G4	A8	BT656_D[2] /NOR_A[8]	BI	4mA		BT656 Interface Data 2 Nor Flash Interface Address 8
			GPIOB2	BI			GPIOB Port 2
77	G5	SIRQ0	SIRQ0 /ATA_IRQ	I	2mA		External IRQ 0 ATA Interface IRQ
			GPIOA31	BI			GPIOA Port 31
78	G6	GND	GND	PWR	/		GND
79	G7	GND	GND	PWR	/		GND

80	G8	GND	GND	PWR	/		GND
81	G9	SDRDQ8	SDRAM_DQ8	BI	8mA		SDRAM Interface Data 8
82	G10	SDRDQ9	SDRAM_DQ9	BI	8mA		SDRAM Interface Data 9
83	G11	SDRWEB	SDRAM_WEB	O	8mA		SDRAM Interface Write Enable
			GPIOA20	BI			GPIOA Port 20
84	G12	SDRDQM0	SDRAM_LDQM /SDRAM_DQM[0]	O	8mA		SDRAM Interface LDQM(for 16bits SDRAM) SDRAM Interface DQM0
85	H1	D0	NF_D[8] /NOR_D[0] /RGB_WD[1] /ATA_D[0] /SD_DAT[0]	BI	4mA		NAND Flash Data 8 Nor Flash Data 0 RGB Interface Data 1 ATA Interface Data 0 SD Card Interface Data 0
86	H2	D1	NF_D[9] /NOR_D[1] /RGB_WD[2] /ATA_D[1] /SD_DAT[1]	BI	4mA		NAND Flash Interface Data 9 Nor Flash Interface Data 1 RGB Interface Data 2 ATA Interface Data 1 SD Card Interface Data 1
87	H3	D4	NF_D[12] /NOR_D[4] /RGB_WD[5] /ATA_D[4]	BI	4mA		NAND Flash Interface Data 12 Nor Flash Interface Data 4

			/SD_DAT[4]				RGB Interface Data 5 ATA Interface Data 4 SD Card Interface Data 4
88	H4	D5	NF_D[13] /NOR_D[5] /RGB_WD[6] /ATA_D[5] /SD_DAT[5]	BI	4mA		NAND Flash Interface Data 13 Nor Flash Interface Data 5 RGB Interface Data 6 ATA Interface Data 5 SD card Interface Data 5
89	H5	KSIN3	KS_IN[3]	BI	2mA		Key scan Input 3
			GPIOA11	BI			GPIOA Port 11
90	H6	CEB4	ATA_CS0B/ NOR_CEB4/ RGB_CE	O	4mA		ATA Interface CS0 NOR Flash CE4 RGB Interface CE
			GPIOB27	BI			GPIOB Port 27
91	H7	CEB0	NOR_CEB0 /NF_CEB0	O	4mA		Nor Flash Interface CE0 NAND Flash Interface CE0
92	H8	DRVVBUS	DRV_VBUS /NOR_RDB /RGB_RDB /ATA_RDB	O	2mA		OTG Interface VBUS Nor Flash Interface RD RGB Interface RD ATA Interface RD
			GPIOA15	BI			GPIOA Port 15
93	H9	SDRCK	SDRAM_CK	O	16mA		SDRAM Interface Clock
94	H10	SDRDQM1	SDRAM_DQM/UDQM /SDRAM_DQM[1]	O	8mA		SDRAM Interface DQM(for 8bits SDRAM)

							SDRAM Interface UDQM(for 16bits SDRAM) SDRAM Interface DQM1(for 32bits SDRAM)
95	H11	SDRRASB	SDRAM_RASB	O	8mA		SDRAM Interface RAS
			GPIOA18	BI			GPIOA Port 18
96	H12	SDRCASB	SDRAM_CASB	O	8mA		SDRAM Interface CAS
			GPIOA19	BI			GPIOA Port 19
97	J1	D2	NF_D[10] /NOR_D[2] /RGB_WD[3] /ATA_D[2] /SD_DAT[2]	BI	4mA		NAND Flash Interface Data 10 Nor Flash Interface Data 2 RGB Interface Data 3 ATA Interface Data 2 SD Card Interface Data 2
98	J2	D3	NF_D[11] /NOR_D[3] /RGB_WD[4] /ATA_D[3] /SD_DAT[3]	BI	4mA		NAND Flash Interface Data 11 Nor Flash Interface Data 3 RGB Interface Data 4 ATA Interface Data 3 SD Card Interface Data 3
99	J3	D6	NF_D[14] /NOR_D[6] /RGB_WD[7] /ATA_D[6]	BI	4mA		NAND Flash Interface Data 14 Nor Flash Interface Data 6

			/SD_DAT[6]				RGB Interface Data 7 ATA Interface Data 6 SD card Interface Data 6
100	J4	D7	NF_D[15] /NOR_D[7] /RGB_WD[8] /ATA_D[7] /SD_DAT[7]	BI	4mA		NAND Flash Interface Data 15 Nor Flash Interface Data 7 RGB Interface Data 8 ATA Interface Data 7 SD card Interface Data 7
101	J5	CEB6	SD_CLK /CE6	O	16mA		SD CARD Interface CLOCK Nor Flash Interface CE6
			GPIOB29	BI			GPIOB Port 29
102	J6	CEB1	NF_CEB1 /NOR_CEB1/RGB_CE /ATA_CS0B	O	4mA		NAND Flash Interface CE1 Nor Flash Interface CE1 RGB Interface CE ATA Interface CS0
103	J7	SIRQ1	SIRQ1	I	2mA		External IRQ 1
			GPIOB31	BI			GPIOB Port 31
104	J8	UART2TX	UART2IR_TX / I2C2_SCL	BI	2mA		Uart2 or IrDA Port Tx I2C2 Interface SCL
			GPIOB12	BI			GPIOB Port 12
105	J9	SDRA11	SDRAM_A11	O	8mA		SDRAM Interface Address11
			GPIOA25	BI			GPIOA Port 25

106	J10	SDRCKE	SDRAM_CKE	O	16mA		SDRAM Interface Clock Enable
			GPIOA16	BI			GPIOA Port 16
107	J11	SDRBA0	SDRAM_BA0	O	8mA		SDRAM Interface bank address0
108	J12	SDRCSB	SDRAM_CSB	O	8mA		SDRAM Interface CS
			GPIOA17	BI			GPIOA Port 17
109	K1	VDD	VDD	PWRI	/		VDD
110	K2	A2	NF_CLE /ATA_A2 /NOR_A[2] /RGB_RS /SD_CMD	O	4mA		NAND Flash Interface CLE ATA Interface Address 2 Nor Flash Interface address 2 RGB Interface RS SD card Interface CMD
			GPIOA2	BI			GPIOA Port 2
111	K3	A1	NF_RB /ATA_A1 /NOR_A[1] /RGB_WD[9]	O	4mA		NAND Flash Interface Ready/Busy ATA Interface Address 1 Nor Flash Interface Address 1 RGB Interface Data 9
			GPIOA1	BI			GPIOA Port 1
112	K4	A0	NF_ALE /ATA_A0 /NOR_A[0] /RGB_WD[0]	O	4mA		NAND Flash ALE ATA Interface Address 0 Nor Flash Interface Address 0 RGB Interface Data0

			GPIOA0	BI			GPIOA Port 0
113	K5	CEB3	NOR_CEB3 /NF_CEB3	O	4mA		NOR Flash Interface CE3 NAND Flash Interface CE3
			GPIOB17	BI			GPIOB Port 17
114	K6	CEB2	NF_CEB2 /NOR_CEB2 /RGB_CE /ATA_CS1B	O	4mA		NAND Flash Interface CE2 Nor Flash Interface CE2 RGB Interface CE ATA Interface CS1
115	K7	RDB	DRV_VBUS /NOR_RDB /RGB_RDB /ATA_RDB	O	2mA		OTG Interface VBUS Nor Flash Interface RD RGB Interface RD ATA Interface RD
			GPIOA15	BI			GPIOA Port 15
116	K8	UART2RX	UART2IR_RX /I2C2_SDA	BI	2mA		Uart2 or IrDA Port Rx I2C2 Interface SDA
			GPIOB13	BI			GPIOB PORT13
117	K9	SDRA8	SDRAM_A8	O	8mA		SDRAM Interface Address 8
			GPIOA22	BI			GPIOA Port A 22
118	K10	SDRA9	SDRAM_A9	O	8mA		SDRAM Interface Address 9
			GPIOA23	BI			GPIOA Port 23
119	K11	SDRA10	SDRAM_A10	O	8mA		SDRAM Address 10
			GPIOA24	BI			GPIOA Port 24
120	K12	SDRBA1	SDRAM_BA1	O	8mA		SDRAM Interface Bank Address 1

121	L1	LOSCO	LOSCO	AO	/		Low Oscillator Output
122	L2	RTCVDD	RTCVDD	PWRI	/		RTC Power VDD
123	L3	D8	NF_D[0] /NOR_D[8] /RGB_WD[10] /ATA_D[8]	BI	4mA		NAND Flash Data 0 Nor Flash Data 8 RGB Interface Data 10 ATA Interface Data 8
124	L4	D10	NF_D[2] /NOR_D[10] /RGB_WD[12] /ATA_D[10]	BI	4mA		NAND Flash Interface Data 2 Nor Flash Interface Data 10 RGB Interface Data 12 ATA Interface Data 10
125	L5	D12	NF_D[4] /NOR_D[12] /RGB_WD[14] /ATA_D[12] /ICE_CK	BI	4mA		NAND Flash Data 4 Nor Flash Data 12 RGB Interface Data 14 ATA Interface Data 12 ICE Port clock
126	L6	D14	NF_D[6] /NOR_D[14] /RGB_WD[16] /ATA_D[14] /ICE_DI	BI	4mA		NAND Flash Data 6 Nor Flash Interface Data 14 RGB Interface Data 16 ATA Interface Data 14 ICE Port DI
127	L7	WRB	DISCHG /NOR_WRB /RGB_WRB /ATA_WRB	O	2mA		OTG charge pump Discharge Nor Flash Interface WR RGB Interface WR ATA Interface WR
			GPIOA14	BI			GPIOA Port 14
128	L8	SD_VP	SDRAM_VP	PWRI	/		SDRAM Interface

							Power
129	L9	SDRA6	SDRAM_A6	O	8mA		SDRAM Interface Address 6
130	L10	SDRA7	SDRAM_A7	O	8mA		SDRAM Interface Address 7
			GPIOA21	BI			GPIOA Port 21
131	L11	SDRA1	SDRAM_A1	O	8mA		SDRAM Interface Address 1
132	L12	SDRA0	SDRAM_A0	O	8mA		SDRAM Interface address 0
133	M1	LOSCI	LOSCI	AI	/		Low Oscillator Input
134	M2	GND	GND	PWR	/		GND
135	M3	D9	NF_D[1] /NOR_D[9] /RGB_WD[11] /ATA_D[9]	BI	4mA		NAND Flash Interface Data 1 Nor Flash Interface Data 9 RGB Interface Data 11 ATA Interface Data 9
136	M4	D11	NF_D[3] /NOR_D[11] /RGB_WD[13] /ATA_D[11] /ICE_EN	BI	4mA		NAND Flash Interface 3 Nor Flash Data 11 RGB Interface Data 13 ATA Interface Data 11 ICE Port EN
137	M5	D13	NF_D[5] /NOR_D[13] /RGB_WD[15] /ATA_D[13] /ICE_RSTB	BI	4mA		NAND Flash Interface Data 5 Nor Flash Interface Data 13 RGB Interface WD 15 ATA Interface Data 13

							ICE Port RST
138	M6	D15	NF_D[7] /NOR_D[15] /RGB_WD[17] /ATA_D[15] /ICE_DO	BI	4mA		NAND Flash Interface Data 7 Nor Flash Port Data 15 RGB Interface Data 17 ATA Interface Data 15 ICE Port DO
139	M7	VDD	VDD	PWRI	/		VDD
140	M8	GND	GND	PWR	/		GND
141	M9	SDRA4	SDRAM_A4	O	8mA		SDRAM Interface Address4
142	M10	SDRA5	SDRAM_A5	O	8mA		SDRAM Interface Address 5
143	M11	SDRA3	SDRAM_A3	O	8mA		SDRAM Interface Address3
144	M12	SDRA2	SDRAM_A2	O	8mA		SDRAM Interface Address2

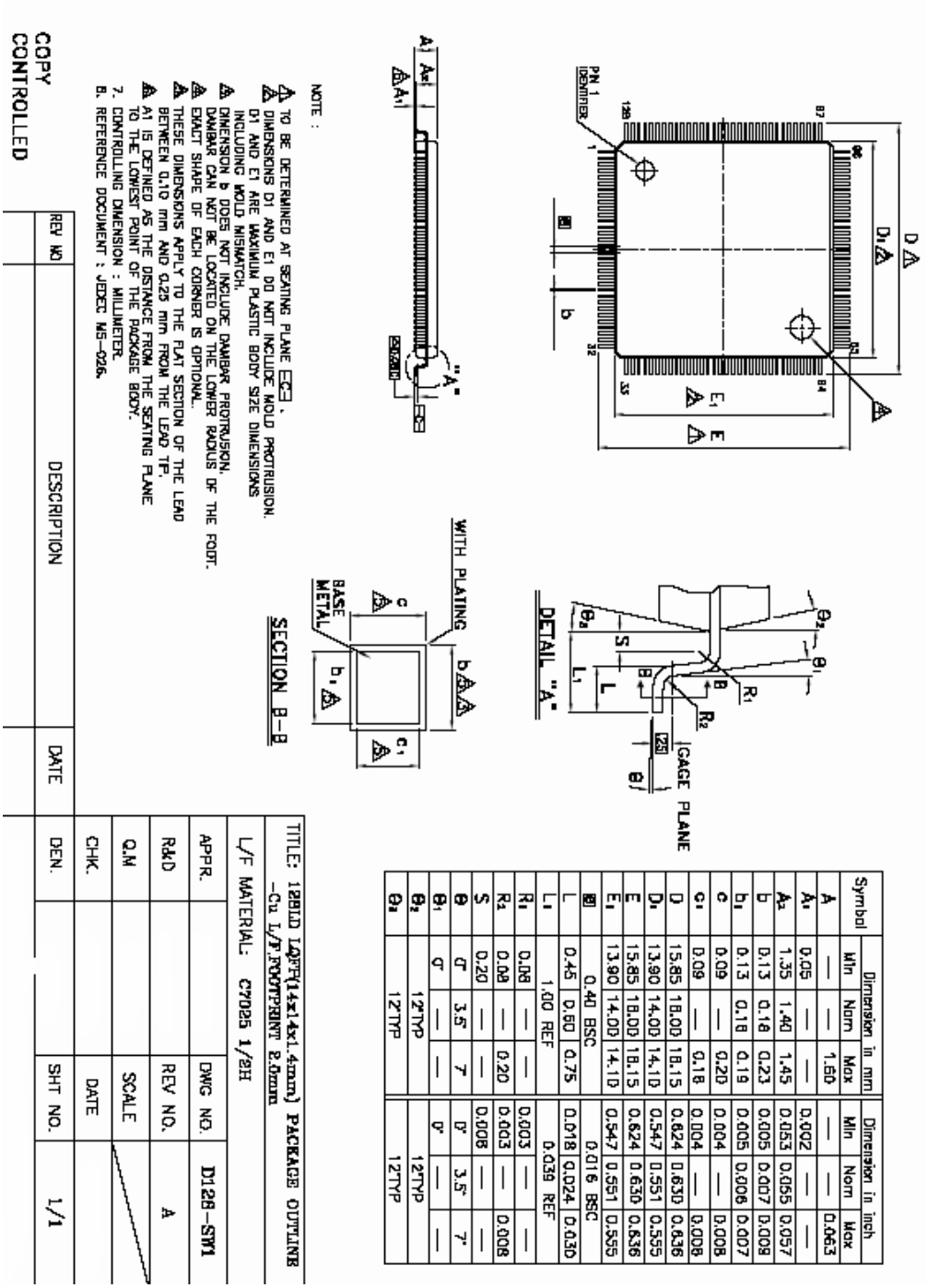
25.3.2 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12
A	LXVDD	IOVDD	HOSCI	PGND	TVRREF	PAVCC	AGND	AVCC	VMIC	DP	VBUS	PAGND
B	VDD	BAT	HOSCO	AVDD	TVCVBS	VRDA	VREFI	MICIN	UREF	IDPIN	DM	UVCC
C	VCC	DC5V	I2C1SDA	RESETB	KSOUT1	KSIN1	AOUTL	FMINL	UART1TX	UART1RX	SDRDQ0	SDRDQ1
D	GND	VCCOUT	I2C1SCL	KSOUT0	KSOUT2	KSIN2	AOUTR	FMINR	SDRDQ15	SDRDQ14	SDRDQ2	SDRDQ3
E	A15	A16	A10	A14	KSIN0	REMCON	TEST	SDRA12	SDRDQ13	SDRDQ12	SDRDQ4	SDRDQ5

F	A13	A17	A6	A9	BL_NDR	VCC	VCC	SD_VP	SDRDQ11	SDRDQ10	SDRDQ6	SDRDQ7
G	A12	A11	A7	A8	SIRQ0	GND	GND	GND	SDRDQ8	SDRDQ9	SDRWEB	SDRDQM0
H	D0	D1	D4	D5	KSIN3	CEB4	CEB0	DRVVBUS	SDRCK	SDRDQM1	SDRRASB	SDRCASB
J	D2	D3	D6	D7	CEB6	CEB1	SIRQ1	UART2TX	SDRA11	SDRCKE	SDRBA0	SDRCSB
K	VDD	A2	A1	A0	CEB3	CEB2	RDB	UART2RX	SDRA8	SDRA9	SDRA10	SDRBA1
L	LOSCO	RTCVDD	D8	D10	D12	D14	WRB	SD_VP	SDRA6	SDRA7	SDRA1	SDRA0
M	LOSCI	GND	D9	D11	D13	D15	VDD	GND	SDRA4	SDRA5	SDRA3	SDRA2

26 Package Drawing

26.1 ATJ2256



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.18	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.18	0.004	—	0.008
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 REF			0.039 REF	
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2		12°TYP			12°TYP	
θ_3		12°TYP			12°TYP	

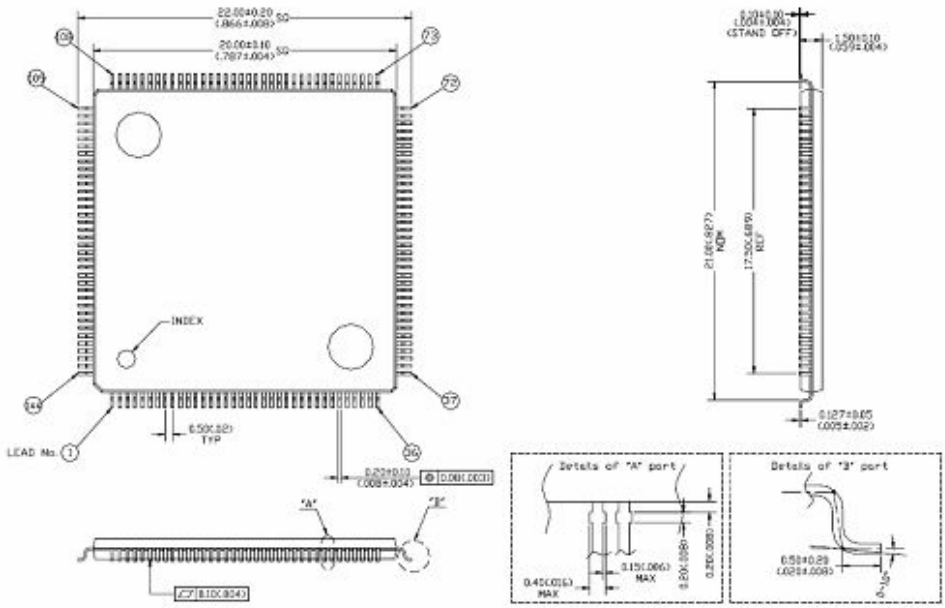
REV NO	DESCRIPTION	DATE

COPY CONTROLLED

TITLE: 128LD LQFP(14x14x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm		DWG NO.	D128-SW1
L/F MATERIAL: C7025 1/2H	APPR.		
	R&D	REV NO.	A
	Q.M	SCALE	
	CHK.	DATE	
	DEN.	SHT NO.	1/1

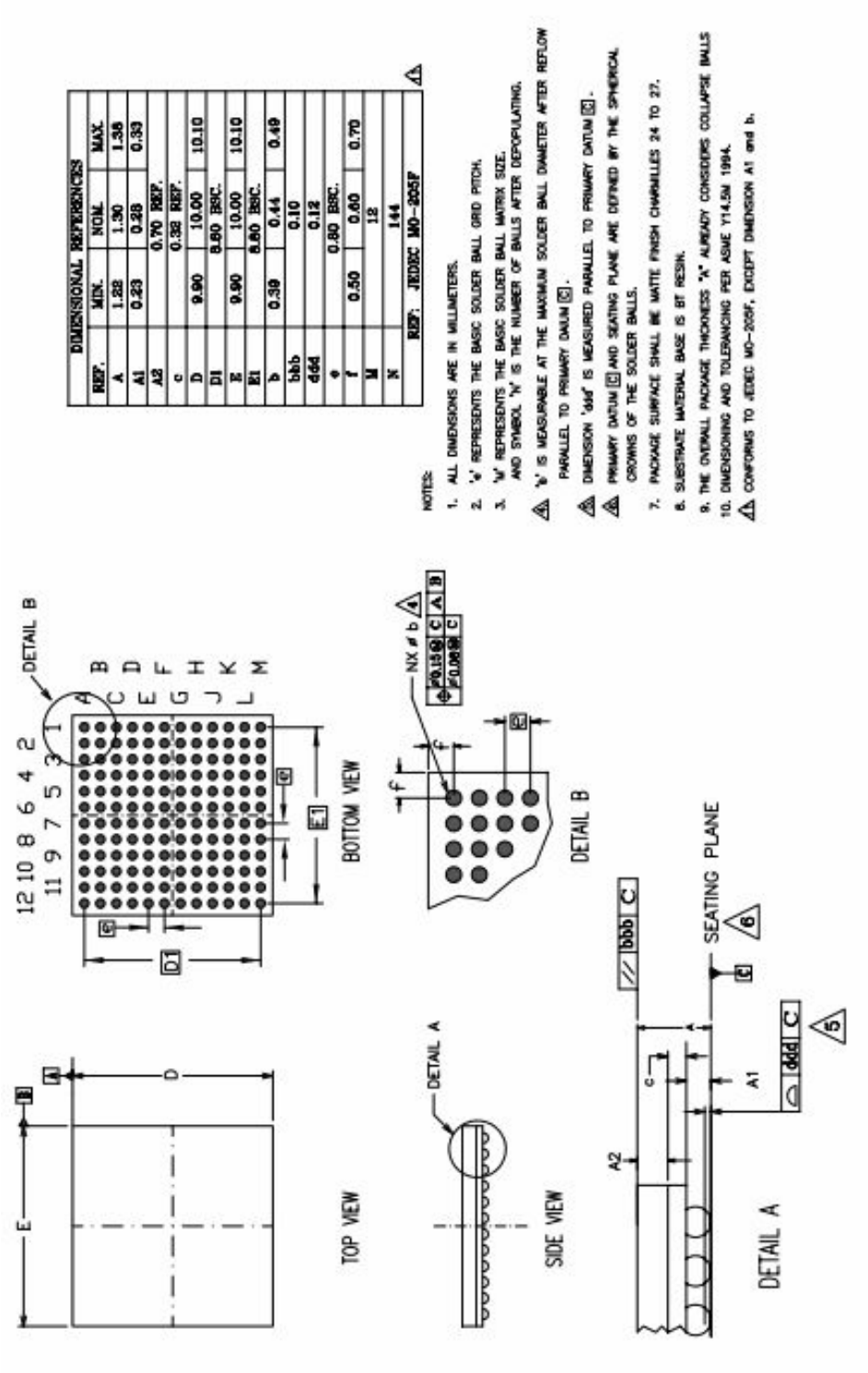
26.2 ATJ2257

Plastic LQFP-144pin



NTG.052. LQFP-144P UNIT:mm(inches)

26.3 ATJ2257B



27 Appendix

27.1 Acronym and Abbreviations

ADC: Analog-to-Digital Converter
AHB: Advanced High-Performance Bus
ALE: Address-Locked Enable
APB: Advanced Peripheral Bus
BIST: Built-in Self-Test
CLE: Command-Locked Enable
CMU: Clock Management Unit
CP0: System Control Coprocessor
CRC: Cyclic redundancy Check
CVBS: Composite Video Broadcasting Signal
DAC: Digital-to-Analog Converter
dB: Decibel
DC: Direct Current
DSP: Digital Signal Processing
DVB: Digital Video Broadcasting
EAV: End of Active Video
ECC: Error Correct Code
FIR: Fast Infrared
GPIO: General-Purpose Input/Output
I2C: Inter-Integrated Circuit
IR: Infrared
IrDA: Infrared Data Association
IRQ: Interrupt Request
JPEG: Joint Photographic Experts Group
Li-Ion: Lithium Ion (battery type)
LRADC: Low Resolution ADC
MAC: Multiplier Accumulator Control
MCA: Motion Compensation Accelerator
MIPS: Million Instructions Per Second
MIR: Mid Infrared
MJPEG: Motion JPEG
MMC: Multimedia Card
MMU: Memory Management Unit
MLC: Multi-Level Cell

MPEG: Motion Picture Expert Group
NTSC: National Television Standards Committee
OLED: Polymer Light-Emitting Diode
PA: Power Amplifier
PAL: Phase Alteration Line
PCM: Pulse Code Modulation
PFM: Pulse Frequency Modulation
PLL: Phase-Locked Loop
PMU: Power Management Unit
PWM: Pulse Width Modulation
RISC: Reduced Instruction Set Computing
RTC: Real-Time Clock
SAV: Start of Active Video
SD: Secure Digital memory card
SIR: Slow Infrared
SMC: State Machine Controller
SLC: Single-Level Cell
SOC: System on a Chip
SPEC: Specification
SPDIF: SONY-Philips Digital Interface Format
SPI: Serial Peripheral Interface
SPRAM: Scratch Pad RAM
SW: Software
THD: Total Harmonic Distortion
TLB: Translation Look-aside Buffer
TS: Transport Stream
UART: Universal Asynchronous Receiver Transmitter
WMA: Windows Media Audio
WMV: Windows Media Video

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