ATJ227X Datasheet

Latest Version: 1.0

2010-11-26

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Revision History

Date	Revision	Description
2010-11-26	1.0	New Release

1 Introduction

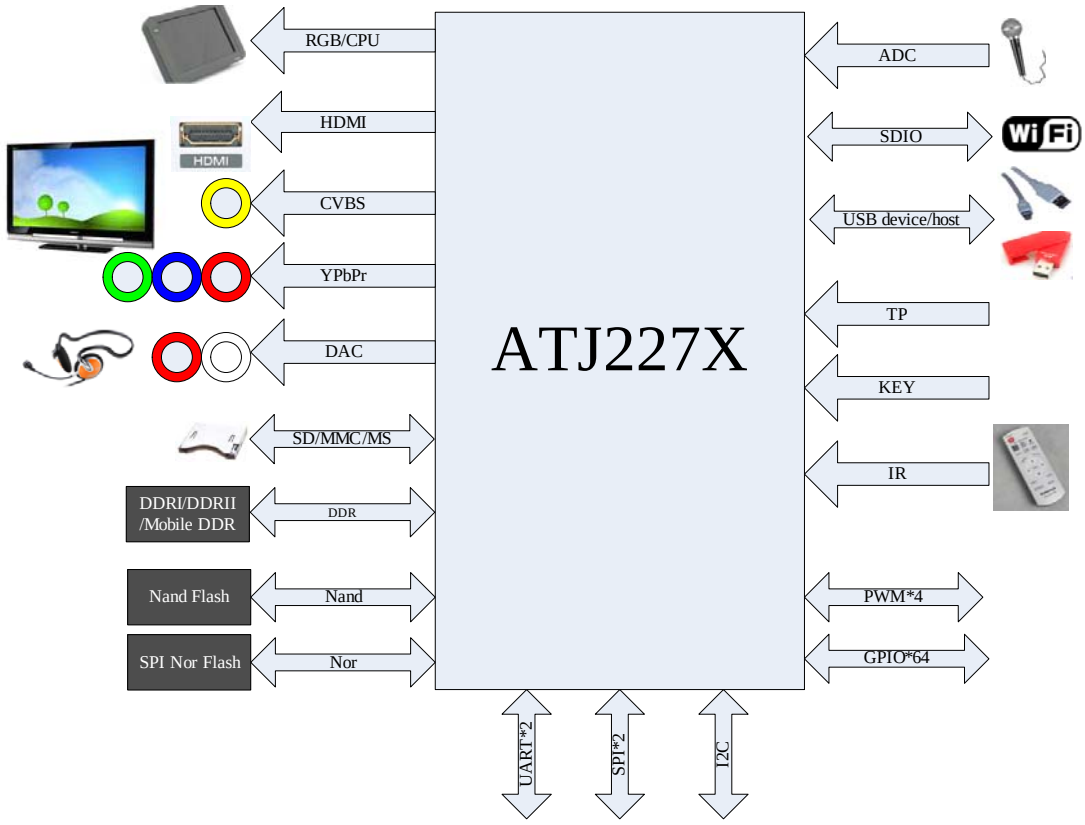
1.1 Overview

ATJ227X is a highly integrated SOC for high density media solution with multiprocessor. The architecture of one 32-bit RISC up to 450 MHz, cooperated with a powerful Video Engine, a build in Graphics Processing Unit (GPU) and a Display Engine, high efficiency buses, high-speed DDR/DDRII/Mobile DDR memory controller. It can achieve high performance and low power dissipation.

ATJ227X is capable of dealing with all formats of video decoder, up to HD resolution, as well as all audio formats with a build in audio codec. And its video recorder can support up to 720p resolution. Audio/Video file can be played through HDMI, CVBS, YPbPr, 5.1 channel, SPDIF, IIS. ATJ227X also has RGB and CPU LCD interfaces with touch panel build-in. The integrated USB V2.0 (HS) SIE with OTG function enables the platform to act as a host or slave mass storage device at the speed up to 480Mbps. Nand Flash Controller, with build in 8bit/12bit/24bit/40bit ECC, randomizer for TLC nand support. 2-bit SPI Nor (SNor) Flash Controller, SD/MMC/MS card Controller and versatile peripheral serial interfaces (IIC, SPI*2, UART*2, IR, SPDIF, I2S), is able to support various memories, and such functions as Wi-Fi, LAN, Bluetooth, IRC is supported. Moreover, the build in Power Management Unit provides necessary system power and manage internal and external power dissipation to realize lower system cost.

ATJ227X therefore can provide a true 'ALL-IN-ONE' solution that is ideally suited for high density media devices.

1.2 System Applications



1.3 HW Feature

High Speed 32bit RISC

- Up to 450 MHz
- 8-stage pipeline
- MIPS32™ instruction set
- Programmable Memory Management Unit
- 16KB I-Cache and 16KB D-cache
- 24kB DSPRAM
- 8kB ISPRAM

Video Engine

- All format of 720p video supported, 30fps, up to 20Mbps averagely;
- Support MPEG-4 encoding, up to 720p resolution
- Support digital room from x1~x4, and with configurable step.

JPEG Codec

- Decoding/Encoding up to 4096*4096
- Decoding Format: YCbCr4:2:2, YCbCr4:2:0

- Encoding Format: YCbCr4:2:2, YCbCr4:2:0

Graphics Processing Unit

- Completely compatible with Openvg 1.0
- Hardware accelerated Pattern Tiling
- Hardware accelerated FastFill
- Hardware accelerated Affine Transform
- Hardware accelerated Device Font

Display Engine

- Four moveable layers
- Alpha blending and color space converting
- Scalar
- Dither function for 16 bit/18 bit interface LCD
- Gamma correction
- Video brightness, contrast and saturation adjustable

Memory Interface

- DDR/DDRII/M-DDR memory controller, x16 data bus, supporting up to 256MB, 200MHz max
- Nand Flash controller with 8bit/12bit/24bit/40bit ECC, x8 data bus, 3.1V, supporting 2RB and 4CE, and hardware randomizer supported.
- SPI Nor Boot Supported

Audio Engine

- All format of Audio decoding supported
- Support MPEG-I decoding, 8~ 448kbps
- Support WMA decoding, 5~383kbps
- Support AAC/OGG/APE decoding
- Several format of Audio encoding supported

LCD Controller

- Support CPU interface LCD
- Support up to 24bit RGB interface
- Programmable timing control for various panels
- Support LCD resolution up to 1024*1024

HDMI

- HDMI 1.1, up to 720p resolution
- Supports RGB, YCbCr format
- Supports IEC60958 audio format up to 24bits

TV Out:

- Support NTSC-M, -J and –4.43 modes.
- Support PAL-B, -D, -G, -H, -I, -M, -N, -Nc mode
- Support CVBS output
- Support YPbPr/YCbCr output up to 720p resolution
- Support outputting blue/black color and ColorBar when no data input

CMOS Sensor interface

- Support BT656&BT601 Interface
- Support CMOS Sensor with YUV422 or RGB565 data format
- With the CLKOUT for CMOS Sensor

USB

- Complies with OTG 2.0
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
- Supports point-to-point communication with

Audio In/Out

- Build in stereo Sigma-Delta DAC, SNR>96dB
- Build in stereo Sigma-Delta ADC, SNR>89dB

one low-speed, full-speed or high-speed device in Host mode
- Supports full-speed or high-speed in peripheral mode, up to 480Mbps

SDIO
- Two 4-wire bus supported
- Up to 8-wire for one bus
- Support SD/HCSD/microSD/miniSD/MS memory card, MMC/RSMMC/MMC PLUS card
- Support SDIO function

UART
- 5-8 Data Bits and LSB first in Transmitting and receiving
- 1-2 Stop Bits
- Even, Odd, or No Parity

SPI
- 2 seperated SPI controller
- Each support master mode and slave mode. The speed of master mode up to 80Mbps, and slave up to 20Mbps.
- Support dual I/O write and read mode as master
- Support single data rate mode and double data rate(DDR mode) as master
- Support two wire mode, only use SCLK and MOSI signal

Timer/Clock
- 2 Timers
- Alarm supported
- Calendar supported
- Two oscillator needed: 24MHz and 32.768KHz

- 18mW*2 Headphone Power Amplify, THD<-90dB
- Support Microphone/FM (Linein) to ADC

I2C
- 1-ch multi-master I2C bus, support both master and slave functions
- Support standard mode (100kbps) and fast-speed mode (400kpbs)

User Interface
- 1 remote control
- 2*4 key matrix
- Build in Touch Panel controller
- IRC build in

I2S&SPDIF
- Support 5.1-Channel through I2S Transmitter module with Ext. 6-Channel DAC, include 3-Wire-DOUT Mode and TDM (time-division multiplexed) Mode
- Support 5.1-Channel digital out through SPDIF

Chip ID
- Programmable for customer

PMU

- Programmable DC/DC converters and regulator
- Battery charger, support Li+ battery.
- Voltage detector for over current protection and temperature surveillance
- Low Power Mode
- Deep Sleep Mode

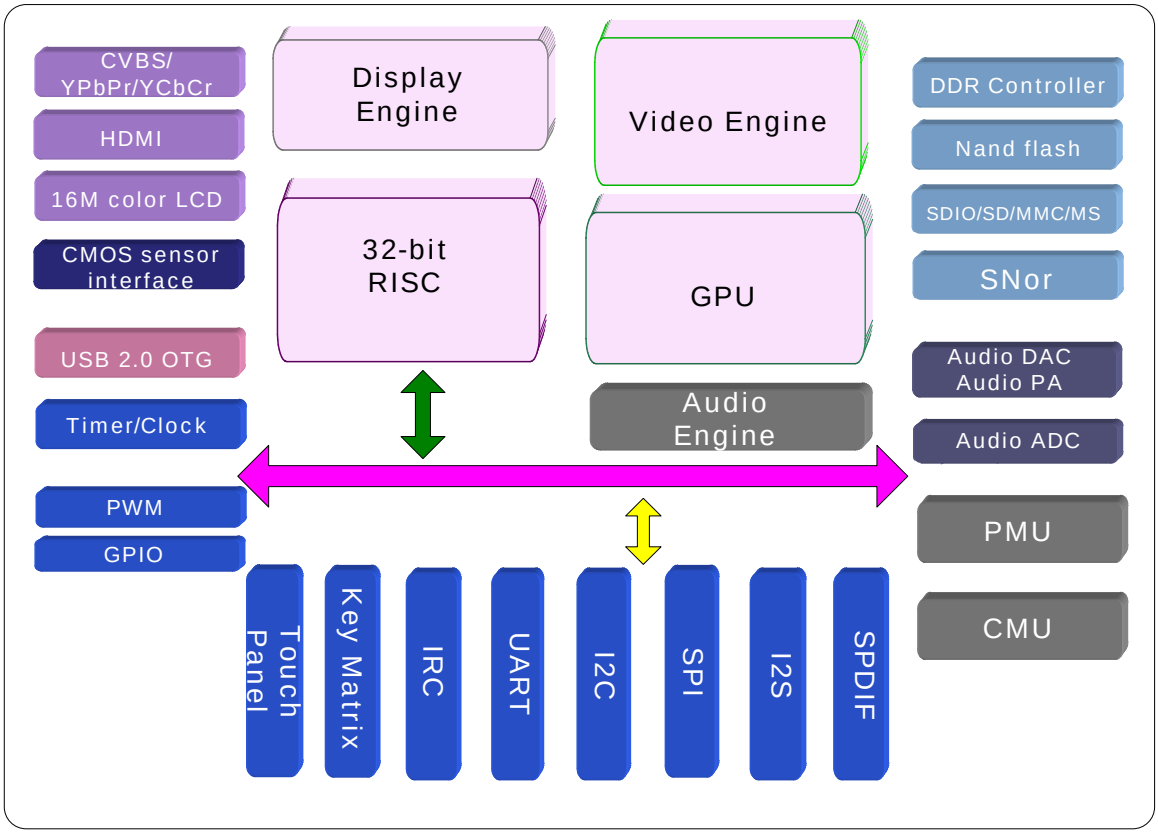
Package

- LQFP216, LQFP176 E-PAD and LQFP128 E-PAD for different usage.

Low SOC power

- Low standby current. Less than 50uA with RTC.
- Low power consumption. Less than 0.5mW/MHz of the CPU.
- Dynamic system clock adjustment

1.4 Block Diagram



1.5 Ordering information

Part Number	Package
ATJ2279	LQFP216 (24*24)
ATJ2279B	LQFP176 E-PAD (20*20)
ATJ2275B	LQFP176 E-PAD (20*20)
ATJ2273B	LQFP128 E-PAD (14*14)

1.6 Functions Contrastive list

ATJ227 series IC: ATJ2279 (216Pin）, ATJ2279B（176Pin-EPAD）， ATJ2275B（176Pin-EPAD） ATJ2273B（128Pin-EPAD）。Here are the differences of functions among them.

Features	ATJ2279	ATJ2279B	ATJ2275B	ATJ2273B
Package	LQFP216	LQFP176-EPAD	LQFP176-EPAD	LQFP128-EPAD
MCU/System	√	√	√	√
PMU	√	√	√	√
DDR1	√	√	√	√
DDR2	√	√	√	√
Nand/SNor Flash	√	√	√	√
CPU LCD screen	√/ 16bit / 18bit	√/ 16bit / 18bit	√/ 16bit / 18bit	√/ 16bit
RGB LCD screen	√/ RGB888	√/ RGB 666	√/ RGB 666	√/ RGB 565
Camera sensor	√/ BT656	√/ BT656	×	×
SD/MMC/MS Card	√ / 8 line	√ / 4line	√ / 4line	√ / 4line
USB Host /Slave	√	√	√	×
Touch Panel	√	√	√	×
Key scan	√	√	√	√
HDMI Output	√	√	√	×
CVBS Output	√	√	√	√
YPbPr Output	√	√	√	√
5.1 CH Output	√	×	×	×

Earphone Output	√	√	√	√
MIC Input	√	√	√	√
FM Module	√	√	√	√
IR Receiver	√	√	√	×

Notes: Here we use ATJ227X when introducing function modules, please refer to the corresponding module for IC of different packages.

2 System Control

2.1 Power Supply

It is very important to provide the adequate power and ground for high-speed digital and sensitive analog circuit. To achieve good and stable quality, the power and ground pins are sepatated into several groups.

Recommended Operating Condition

Supply Voltage		Min	Typ	Max	Unit
BAT		3.4	3.8	4.2	V
DC5V/VBUS		4.5	5	5.2	V
VCC/SVCC/AVCC/PAVCC/ HAVCC/HDVCC/		2.8	3.1	3.4	V
VDDR	DDR1	2.2	2.4	2.6	V
	DDR2	1.6	1.8	2.0	V
VDD/SVDD/AVDD		1.0	1.2	1.5	V

Note 1: According to different application, the VDD voltage can configure differently. For optimum CPU perfomance, the VDD should be higher than 1.2V. For reducing the power consumption, the VDD can supply with 1.0V.

2.2 Power Management Unit

ATJ227X only supports LI-ION battery mode. Power Management Unit consists of DC-DC converters, linear regulators, LI-ION charger, two low resolution A/D converters and power saving control unit.

PIN of PMU:

- VDD DC-DC PIN: LX_VDD, PGND, VDD
- VDDR DC-DC PIN: LX_VDDR,PGND,VDDR
- High voltage regulator input and output PIN: DC5V, VCC
- Battery input/output PIN: BAT
- Line-in controller input PIN: REM_CON
- Light photo sensor input PIN:LPS_IN
- External power PIN: VCCOUT
- Analog power PIN: AVCC， AVDD

- SVCC, SVDD
- ON/OFF PIN

ATJ227X has four power modes, active mode, low-power mode, sleep mode, shut-down mode. In low power mode, all PLLs should be shut down via software programming. In sleep mode, the power supply except VDDR will be shut off.

The loading capacity of DC/DC converters and Regulators as follow:

Block Name	Loading
VDD	1.2V, 450mA @ BAT=3.6V, 5% Drop
VDDR	1.8V/2.5V, 300mA @ BAT=3.6V, 5% Drop
VCCOUT	3.1V, 200mA @ BAT=3.6V, 5% Drop
AVCC	2.95V, 70mA @ AVCC 5% Drop
AVDD	1.2V, 20mA @ AVDD 5% Drop
VCC	3.1V, 350mA @ VCC 5% Drop

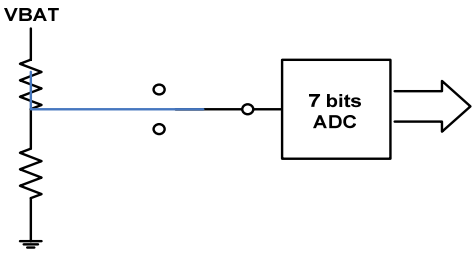
There is a low speed 7bit ADC in ATJ227X for battery monitor.

The relationship between the battery type and the ADC input range is:

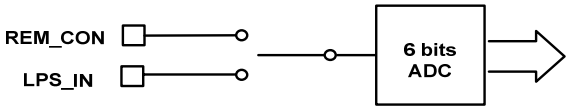
Battery Type	Internal Voltage Divider For Battery	AD Input Range
1 Li+	1/2	0.7-2.2

There is a low speed 6 bits ADC in ATJ227X for remote control and light photo sensor output voltage. The input range is from 0 to SVCC.

Bat ADC



Line-in controller
ADC



2.2.1 Register Description

PMU Register Block Base Address

Name	Physical Base Address	KSEG1 Base Address
INTC	0x10000000	0xB0000000

2.2.1.1 Standby_ONOFF_INT_CTL

OFFSET=0x0008

Bits	Name	Description	Access	Reset
31:3	–	Reserved	R	0
2	OFIEN	Enable ON/OFF press interrupt 0: Disable 1: Enable	R/W	1
1	OFPDS	ON/OFF key short press interrupt pending bit Writing 1 to this bit will clear it.	R/W	0
0	OFPDL	ON/OFF key long press interrupt pending bit Writing 1 to this bit will clear it.	R/W	0

2.2.1.2 Standby_ONOFF_CTL_WK

OFFSET=0x000c

Bits	Name	Description	Access	Reset
31:3	-	Reserved	R	0
2:0	TSET	ON/OFF key long press time limit 000: 1 second 001: 2 seconds 010: 3 seconds 011: 4 seconds 100: 5 seconds 101: 6 seconds 110: 7 seconds 111: 8 seconds	R/W	010

2.2.1.3 PMU_CTL1

OFFSET=0x0018

Bits	Name	Description	Access	Reset
31-21	-	Reserved		
20	REMOTEADCEN	Wire control ADC and LPS ADC Enable 1: Enable 0: Disable	R/W	1
19	REMOTEADC_FS	Wire control ADC frequency select 0: 64Hz 1: 128Hz	R/W	0
18-0	-	Reserved		

2.2.1.4 PMU_BDG_CTL

OFFSET=0x0020

Bits	Name	Description	Access	Reset
31-24	-	Reserved		
23-18	REMOTEADC6	Wire control ADC output	R	xx
17-0	-	Reserved		

2.2.1.5 PMU_CHARGER

OFFSET=0x0028

Bits	Name	Description	Access	Reset
31	ENCH	Enable Charge Circuit 1: Enable charge circuit 0: Disable charge circuit.	R/W	0
30	CHGTIME	Charger timer set enable bit: 0: disable 1: enable If enable Charger timer, the charger will stop when the time set by bit 28-29 has arrived. (Will not stop charging; will set CHGEND to 1).	R/W	0
29:28	TIMER	00 2h 01 4h 10 6h 11 8h	R/W	11
27	CHGEND	Charging end Status. 0: not charging over, 1: charging over. If battery is not full, this bit is 0; If battery is full, this bit is 1.	R	x
26	-	Reserved		
25:24	PHASE	Charging phase 00 Reserved 01 Pre-charging 10 Constant current 11 Constant voltage This two bit will be available Only when bit 31 of this register is set, or will be always read 00	R	xx
23-10	-	Reserved		
9	STOPI	0: 30%, when the charging current is decreased to the 30% of the constant current, battery voltage check starts; 1: 50%, when the charging current is decreased to the 50% of the constant current, battery voltage check starts;	R/W	0

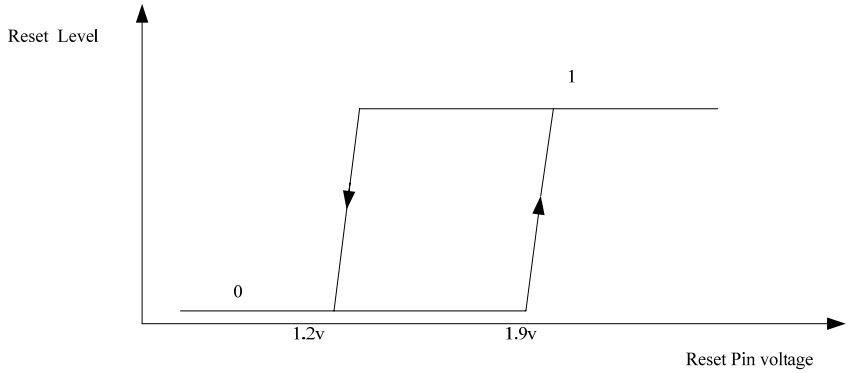
8	STOPV	Charger stop voltage (OCV). 0: 4.18V 1: 4.16V When the charging current is decreased to the set value (set by STOPI) of constant current charging, for every certain period (set by DTSEL), the hardware will stop charging and delay for 1s for re-check the battery voltage. If the voltage > the set value of STOPV, then set CHGEND to 1.	R/W	0
7	-	Reserved		
6-4	CHGIS	Charge Current Configure 000 50mA 001 100mA 010 150mA 011 200mA 100 250mA 101* 300mA 110 400mA 111 500mA	R/W	000
3-0	-	Reserved		

2.3 Reset

There is an external reset signal, active low, and is pulled-up weakly internal.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset Input Low-Level Width	t_{WRSL}	$\overline{RESET}$	230	-	us

Reset Timing



Efficiency Curve for Backlight Step-up Circuit

Note: Reset Pin input has the characteristics of hysteresis. The relationship between reset level and reset pin is shown in the above Figure: upper threshold VT+=1.9V, lower threshold VT-=1.2V.

A Watch dog reset can be used through software configuration, for the details please refer to the chapter of RTC.

2.4 Clock and PLL

Pin Name	IO	Description
LOSCO	AO	32.768KHz Crystal Output
LOSCI	AI	32.768KHz Crystal input
HOSCO	AO	24MHz Crystal Output
HOSCI	AI	24MHz Crystal input

Two external crystals are required, and the embedded PLLs will generate the necessary clock signals under control of the software. The crystal accuracy should under 30ppm to ensure the best quality.

2.5 Interrupt Controller

The interrupt controller supports 32 interrupt sources. It can generate five outputs as interrupt requests 0, 1, 2, 3 and 4. Each of these outputs are connected to the CPU core; the below shows the interrupt controller connections to the CPU.

Interrupt Controller Connects to CPU

Interrupt Controller Requests	CPU Interface	CPU Interrupt Request
Request 0	SI_INT[0]	IP2 (hardware interrupt0)
Request 1	SI_INT[1]	IP3 (hardware interrupt1)

Request 2	SI_INT[2]	IP4 (hardware interrupt2)
Request 3	SI_INT[3]	IP5 (hardware interrupt3)
Request 4	SI_INT[4]	IP6 (hardware interrupt4)

- Can assign anyone of the 32 Interrupt Sources to MIPS hardware interrupt n(n=0,1,2,3,4)
- Have two external interrupts: external interrupt0 and external interrupt1
- External interrupt0 can be used as normal interrupt input, especially it can also be used to awake PMU in status2 and status3.

Interrupt Sources

Interrupt Number	Sources	Type
0	Hantro	High Level
1	AE (Audio Engine)	High Level
2	VE (Video Encoder)	High Level
3	DE (Display Engine)	High Level
4	GPU (Graphics Processing Unit)	High Level
5	VIN(Video Input)	High Level
6	PC(Performance Counter)	High Level
7	2Hz/WatchDog	High Level
8	TIMER1	High Level
9	TIMER0	High Level
10	RTC	High Level
11	DMA	High Level
12	Key	High Level
13	External	High Level
14	TP	High Level
15	SPI0	High Level
16	SPI1	High Level
17	Reserved	-
18	IIC	High Level
19	UART0	High Level
20	UART1	High Level
21	Reserved	-
22	USB	High Level
23	DAC/SPDIF/IIS	High Level
24	ADC	High Level

25	NAND	High Level
26	SD1	High Level
27	SD0/MMC	High Level
28	MS	High Level
29	ON/OFF	High Level
30	HDMI	High Level
31	Reserved	-

2.5.1 Register Description

Interrupt Controller Block Base Address

Name	Physical Base Address	KSEG1 Base Address
INTC	0x10020000	0xB0020000

Interrupt Controller Block Configuration Registers List

Offset	Register Name	Description
0x00	INTC_PD	Interrupt Pending register
0x04	INTC_MSK	Interrupt Mask register
0x08	INTC_CFG0	Interrupt Config register 0
0x0C	INTC_CFG1	Interrupt Config register 1
0x10	INTC_CFG2	Interrupt Config register 2
0x14	INTC_EXTCTL	External Interrupt control and status register
0x18	INTC0_EXTTYPE_CTL	External Interrupt 0 awake type control register

2.5.1.1 INTC_PD

CPU can access the status of interrupt sources by reading this register. The Interrupt Pending bit can not be cleared by writing 1; it is not cleared until device pending is cleared.

offset = 0x00

Bit	Name	Description	R/W	Reset
31:0	INTC_PD[n]	Interrupt Pending bit.Interrupt nume “n” accords to **Interrupt Sources Table.** 0: Interrupt source n request is not active 1: Interrupt source n request is active.	R	INTC_PD[n]

2.5.1.2 INTC_MSK

CPU can be enabled or disabled by writing this register. 0: Interrupt is disabled. 1: Interrupt is enabled.

offset = 0x04

Bits	Name	Description	R/W	Reset
0	Hantro	Hantro Interrupt Mask Bit	R/W	0
1	AE	AE Interrupt Mask Bit	R/W	0
2	VE	VE Interrupt Mask Bit	R/W	0
3	DE	DE Interrupt Mask Bit	RW	0
4	GPU	GPU Interrupt Mask Bit	RW	0
5	VI	Video Input Interrupt Mask Bit	RW	0
6	PC	Performance Count Interrupt Mask Bit	RW	0
7	2Hz/WatchDog	2Hz/WatchDog Interrupt Mask Bit	RW	0
8	TIMER1	TIMER1 Interrupt Mask Bit	RW	0
9	TIMER0	TIMER0 Interrupt Mask Bit	RW	0
10	RTC	RTC Interrupt Mask Bit	RW	0
11	DMA	DMA Interrupt Mask Bit	RW	0
12	Key	KEY Interrupt Mask Bit	RW	0
13	External	External IRQ Interface Interrupt Mask Bit	RW	0
14	TP	Touch Pannel Interrupt Mask Bit	RW	0
15	SPI0	SPI0 Interrupt Mask Bit	RW	0
16	SPI1	SPI1 Interrupt Mask Bit	RW	0
17	Reserved	-	RW	0
18	IIC	IIC Interrupt Mask Bit	RW	0
19	UART0	URT0 Interrupt Mask Bit	RW	0
20	UART1	URT1 Interrupt Mask Bit	RW	0
21	Reserved	-	RW	0
22	USB	USB Interrupt Mask Bit	RW	0
23	DAC/SPDIF/IIS	DAC/SPDIF/IIS Interrupt Mask Bit	RW	0
24	ADC	ADC Interrupt Mask Bit	RW	0
25	NAND	NAND Interface Interrupt Mask Bit	RW	0
26	SD1	SD1 Interface Interrupt Mask Bit	R/W	0
27	SD0/MMC	SD0/MMC Interface Interrupt Mask Bit	RW	0
28	MS	MS Interrupt Mask Bit	RW	0
29	ON/OFF	ON/OFF Interrupt Mask Bit	RW	0
30	HDMI	HDMI Interrupt Mask Bit	RW	0

31	Reserved	-	RW	0

2.5.1.3 INTC_CFGx

Interrupt Config Registers. CPU can assign anyone interrupt source to one of the five interrupt requests.

INTC_CFG2[n]	0	0	0	0	1
INTC_CFG1[n]	0	0	1	1	x
INTC_CFG0[n]	0	1	0	1	x
The interrupt request be assigned	**0**	**1**	**2**	**3**	**4**

INTC_CFG0: Offset=0x0008
INTC_CFG1: Offset=0x000C
INTC_CFG2: Offset=0x0010

Bits	Name	Description	R/W	Reset
0	Hantro	Hantro Interrupt CFGx Bit	R/W	0
1	AE	AE Interrupt CFGx Bit	R/W	0
2	VE	VE Interrupt CFGx Bit	R/W	0
3	DE	DE Interrupt CFGx Bit	RW	0
4	GPU	GPU Interrupt CFGx Bit	RW	0
5	VI	Video Input Interrupt CFGx Bit	RW	0
6	PC	Performance Count Interrupt CFGx Bit	RW	0
7	2Hz/WatchDog	2Hz/WatchDog Interrupt CFGx Bit	RW	0
8	TIMER1	TIMER1 Interrupt CFGx Bit	RW	0
9	TIMER0	TIMER0 Interrupt CFGx Bit	RW	0
10	RTC	RTC Interrupt CFGx Bit	RW	0
11	DMA	DMA Interrupt CFGx Bit	RW	0
12	Key	KEY Interrupt CFGx Bit	RW	0
13	External	External IRQ Interface Interrupt CFGx Bit	RW	0
14	TP	Touch Pannel Interrupt CFGx Bit	RW	0
15	SPI0	SPI0 Interrupt CFGx Bit	RW	0
16	SPI1	SPI1 Interrupt CFGx Bit	RW	0
17	Reserved	-	RW	0
18	IIC	IIC Interrupt CFGx Bit	RW	0
19	UART0	URT0 Interrupt CFGx Bit	RW	0
20	UART1	URT1 Interrupt CFGx Bit	RW	0

21	Reserved	-	RW	0
22	USB	USB Interrupt CFGx Bit	RW	0
23	DAC/SPDIF/IIS	DAC/SPDIF/IIS Interrupt CFGx Bit	RW	0
24	ADC	ADC Interrupt CFGx Bit	RW	0
25	NAND	NAND Interface Interrupt CFGx Bit	RW	0
26	SD1	SD1 Interface Interrupt CFGx Bit	R/W	0
27	SD0/MMC	SD0/MMC Interface Interrupt CFGx Bit	RW	0
28	MS	MS Interrupt CFGx Bit	RW	0
29	ON/OFF	ON/OFF Interrupt CFGx Bit	RW	0
30	HDMI	HDMI Interrupt CFGx Bit	RW	0
31	Reserved	-	RW	0

2.5.1.4 INTC_EXTCTL

External Interrupt Control and Status register. When one of the external interrupt arises, the corresponding pending bit of INTC_PD will be set.

Offset=0x0014

Bits	Name	Description	Read/Write	Reset
31:27	-	Reserved.	R	0
26:25	EXTYPE1	External Interrupt 1 Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	00
24	E1EN	Enable External interrupt 1(irq) 0 Disable 1 Enable	RW	0
23:17	-	Reserved.	R	0
16	E1PD	External Interrupt 1 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 1 is edge-triggered, this bit must be cleared by software after detected.	R/W	-
15:11	-	Reserved.	R	0
10:9	-	Reserved.	R	0
8	E0EN	Enable external interrupt 0(irq)	R/W	0

		0 Disable 1 Enable		
7:1	-	Reserve.	R	0
0	E0PD	External Interrupt 0 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 0 is edge-triggered, this bit must be cleared by software after detected.	R/W	0

2.5.1.5 INTC _EXTTYPE_CTL

External Interrupt 0 awake type control register

Offset=0x0018

Bits	Name	Description	Access	Reset
31:7	–	Reserved	R	0
6:5	ExtIrq0_PIN_TYPE	The pin which configure external interrupt 0 is of different function 00: release EN_PMU single 01: GPIO 10: ExtIrq0 11: not defined	R/W	00
4	ExtIrq0_GPIO_Output_en	The pin which configures external interrupt output enabled 1: Enable 0: Disable	R/W	0
3	ExtIrq0_GPIO_Input_en	The pin which configures external interrupt output enabled 1: Enable 0: Disable	R/W	0
2	EXtIrq0_GPIO_DATA	GPIO DATA	R/W	0
1:0	EXTYPE0	External interrupt 0 type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	R/W	00

2.6 Driver Capacity Configuration of IO Signals

2.6.1 Register Description

Block Name	Physical Bass Address	KSEG1 Base Adress
GPIO/MFP/PWM	0x101C0000	0xB01C0000

0x0088	PAD_DRV0	PAD Drive Capacity0 Select
0x008C	PAD_DRV1	PAD Drive Capacity1 Select
0x0090	PAD_DRV2	PAD Drive Capacity2 Select

2.6.1.1 PAD_DRV0

Pad Driving Capacity 0

Offset=0x0088

Bits	Name	Description	R/W	Default
31:30	SD1CMD_DRV	PAD SD1_CMD Drive Capacity 00: Level 1 01: Level 2 10: Level 3 11: Reserved	RW	00
29:28	SD1CLKA_DRV	PAD SD1_CLKA Drive Capacity 00: Level 1 01: Level 2 10: Level 4 11: Reserved	RW	00
27:26	SD0DH_DRV	PAD SD0_D[7:4] Drive Capacity 00: Level 1 01: Level 2 10: Level 3 11: Reserved	RW	00
25:24	SD0DL_DRV	PAD SD0_D[3:0] Drive Capacity 00: Level 1 01: Level 2 10: Level 3 11: Reserved	RW	00

23:22	SD0CMD_DRV	PAD SD0_CMD Drive Capacity 00: Level 1 01: Level 2 10: Level 3 11: Reserved	RW	00
21:20	SD0CLKA_DRV	PAD SD0_CLKA Drive Capacity 00: Level 1 01: Level 2 10: Level 4 11: Reserved	RW	00
19:18	NFDM_DRV	PAD NAND_D[5:2] Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
17:16	NFDLH_DRV	PAD NAND_D[7:6] and NAND_D[1:0] Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
15:14	NFRB1_DRV	PAD NAND_RB1 Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
13:12	NFRB0_DRV	PAD NAND_RB0 Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
11:10	NFWR_DRV	PAD NAND_WEB and NAND_RDB Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Level 5 (MU1=1&MU2=1&MU3=1)	RW	00
9:8	NFCA_DRV	PAD NAND_ALE and NAND_CLE Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1)	RW	00

		11: Reserved		
7:6	NFCEB3_DRV	PAD NAND _CEB3 Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
5:4	NFCEB2_DRV	PAD NAND _CEB2 Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
3:2	NFCEB1_DRV	PAD NAND _CEB1 Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00
1:0	NFCEB0_DRV	PAD NAND _CEB0 Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 4 (MU1=1&MU2=1) 11: Reserved	RW	00

2.6.1.2 PAD_DRV1

Pad Driving Capacity 1

Offset=0x008C

Bits	Name	Description	R/W	Default
31	BTDH_DRV	PAD BT_D[7:2] Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
30	BTD1_DRV	PAD BT_D1 Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
29	BTD0_DRV	PAD BT_D0 Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
28:27	BTCLKOUT_DRV	PAD BT_CLKOUT Drive Capacity	RW	00

		00: Level 1 01: Level 2 (MU1=1) 10: Level 3 (MU1=1&MU2=1) 11: Reserved		
26	BTCTL_DRV	PAD BT_PCLK, BT_HSYNC and BT_VSYNC Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
25	LCDDM1_DRV	PAD LCD_D[17:10] Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
24	LCDDHL_DRV	PAD LCD_D[23:18] and LCD_D[7:0]Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
23	LCDCTL1DM0_DRV	PAD LCD_LDE/DE and LCD_D[9:8]Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
22	LCDCTL0_DRV	PAD LCD_HSYNC/DE, LCD_VSYNC/RS and LCD_DCLK/WR Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
21	KSIN3_DRV	PAD KS_IN3 Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
20	KSIN2_DRV	PAD KS_IN2 Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
19	KSINOUT_DRV	PAD KS_IN[1:0] and KS_OUT[1:0] Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
18	I2SD2_DRV	PAD I2SD2 Drive Capacity 0: Level 2 1: Level 3 (MU=1)	RW	0
17	I2SD1_DRV	PAD I2SD1 Drive Capacity 0: Level 2 1: Level 3 (MU=1)	RW	0
16	I2SCLKD0_DRV	PAD I2S_MCLK、I2S_BCLK、I2S_LRCLK and I2S_DO0 Drive Capacity 0: Level 2	RW	0

		1: Level 3 (MU=1)		
15	I2C_DRV	PAD I2C_SCLK and I2C_SDATA Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
14	-	Reserved	RW	0
13	SIRQ1_DRV	PAD SIRQ1 Drive Capacity 0: Level 1 1: Level 2 (MU=1)	RW	0
12:11	UART0TXRX_DRV	PAD UART0_TX and UART0_RX Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 3 (MU1=1&MU2=1) 11: Reserved	RW	00
10:9	SPI1MISO_DRV	PAD SPI1_MISO Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 3 (MU1=1&MU2=1) 11: Reserved	RW	01
8:7	SPI1SS_DRV	PAD SPI1_SS Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10:Level 3 (MU1=1&MU2=1) 11: Reserved	RW	01
6:5	SPI1CKDO_DRV	PAD SPI1_SCLK and SPI1_MOSI Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 3 (MU1=1&MU2=1) 11: Reserved	RW	01
4	TEST_DRV	PAD TEST_DRV (FM_CLK) Drive Capacity 0: Level 1 1: Level 2 (MU1=1)	RW	0
3:2	SPI0SSDI_DRV	PAD SPI0_SS and SPI0_MISO Drive Capacity 00: Level 1 01: Level 2 (MU1=1) 10: Level 3 (MU1=1&MU2=1) 11: Reserved	RW	01
1:0	SPI0CKDO_DRV	PAD SPI0_SCLK and SPI0_MOSI Drive Capacity 00: Level 1	RW	01

		01: Level 2 (MU1=1) 10: Level 3 (MU1=1&MU2=1) 11: Reserved		

2.6.1.3 PAD_DRV2

Pad Driving Capacity 2

Offset=0x0090

Bits	Name	Description	R/W	Default
31:8	-	Reserved	RW	0
7:6	EDGEADJ1	CK, CK# and DQMx signal falling edge speed adjust; 00: lowest falling edge 01: normal falling edge 10: fast falling edge 11: fastest falling edge	RW	01
4:5	EDGEADJ2	DQx and DQSx signal falling edge speed adjust; 00: lowest falling edge 01: normal falling edge 10: fast falling edge 11: fastest falling edge	RW	01
3	PADSEL	DDR pad driver selection 0: 2.5V 1: 1.8V	RW	0
2	PADDRV2	1: increase the DQx and DQSx PAD drive strength 0: normal strength	RW	0
1	PADDRV1	1: increase the Address and Command (CAS#/RAS#/WE#/CKE#/CS#/DMx/CK/CK#) PAD drive strength 0: normal strength	RW	0
0	HALF_DRV	When this bit is set to 1, the DDR output driver reduce to half strength: 0: full strength 1: half strength	R/W	0

2.6.2 Recommended Values for Modules' PAD Driver Capacity

The configuration of pads driver capacity follows the order, Level4>Level3>Level2>Level1.

DDR: The current setting for DDR's PAD driver capacity is PAD_DRV2=0X57, which is relatively weak. The weaker configuration is 0x51, and the DDR's highest speed supported by the weakest configure cannot be more than 120MHz. The specific condition is related to the board, recommend not to readily modify the board.

SD/MS:

① initialize, low frequency clock (<400K)
CMD, DAT and CLK all can adopt the first level.

② If SD 4-wire mode adopted, the following is recommended:
SDCLK: for low speed (25MHz CLK), the 2nd level;
SDCMD & SDDATA: for low speed (25MHz CLK) 1st level can be adopted; for high speed, at (25MHz~50MHz CLK), 2nd level.

③ If MMCplus 8-wire mode adopted, the following is recommended:
SDCLK: 4th level;
SDCMD & SDDATA: for low speed (below 25MHz CLK) 2nd level can be adopted; for high speed, (25MHz~50MHz CLK), 3rd level.

HDMI: HDMI Pad driver is adjusted via the registers TMDS_SCR1 and TMDS_SCR2, which can be respetively set as:
TMDS_SCR1 = 0xCEC000F0, TMDS_SCR2 = 0x6068。

Nand Flash: For signle and double CE –Flash, use the lowest level at 20MHz, the middle level for no more than 36MHz and the highest level for more than 36MHz.
4 CE –Flash, middle level for 32MHz and the highest level for more than 32MHz.

LCD: LCD (including CPU screen and RGB screen), defaulted as LEVEL1 for the solution.

Sensor: When SENSOR's CLKOUTis used as output:
Output 24MHz, defauted as LEVEL1
Output 54MHz, use LEVEL2
Output 72MHz, use LEVEL3

2.7 BROM

There is a built-in ROM for system boot in ATJ227X, boot from Nand Flash, SD card, Serials nor and some other storage device are supported.

2.8 ChipID

Some bits of ID number can be programmed and fused by users of ATJ227X with the PC tool we

provided if it is necessary.

2.9 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	-10	+70	℃
Storage Temperature	Tstg	-55	+150	℃
Supply Voltage	DC5V/VBUS/ BAT	-0.3	5.5	V
	VCC/SVCC/AVCC/PAVCC/ HAVCC/HDVCC/VCCOUT	-0.3	3.6	V
	VDDR/LXVDDR/DDR_VP	-0.3	2.8	V
	VDD/SVDD/AVDD/LXVDD	-0.3	1.6	V
Input Voltage	+3.1V IO	-0.3	3.6	V
	+2.5V IO	-0.3	2.8	V
	+1.2V IO	-0.3	1.6	V

Note:

1) Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
2) All voltage values are with respect to GND
3) +3.1V IO/+2.5V IO/+1.2V IO are defined in the Pin list.

DC Characteristics

VCC = 3.1V TA = 0 to 70 °C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0.8	V
High-level input voltage	V_{IH}	2.0			V
Low-level output voltage	V_{OL}			0.4	V

High-level output voltage	V_{OH}	2.4			V

DC Parameters for DDR

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
DDR Reference Voltage	DDR_VREF	0.48xVDDR		0.52 x VDDR	V
Input High Voltage	Vih	DDR_VREF + 0.15		VDDR+0.2	V
Input Low Voltage	Vil	-0.2		DDR_VREF—0.15	V

The DDR interface voltage levels and timing as specified by JEDEC standard.

3 Memory Controller

3.1 DDR Memory Controller

The external DDR memory controller supports 16bit data width DDR/Mobile DDR and DDR2 device. The controller uses the multi-bank pipeline operation feature to archive the high performance bandwidth. In the low bandwidth application, the DDR controller could use the aggressive power saving strategy to save power.

The DDR SDRAM Controller supports Double Data Rate (DDR) synchronous dynamic random access memory. The features of the controller are listed bellow:

- Compatible with the JEDEC Standards about Standard DDR1/ Mobile DDR1 and DDR2 device.
- Bidirectional Data Strobe (DQS) is transmitted or received with data.
- Differential clock output (CK and CK#).
- Commands active at the positive CK edge
- Data mask (DQM) for write data.
- Burst type: Sequential burst operation in the DDR interface.
- CAS latency: 2/3 in DDR and Mobile DDR Application, CAS latency: 2\3\4\5 in DDR2 application.
- Auto refresh and self refresh modes function.
- Aggressive power saving function which put the DDR device in precharge power down state when DDR interface is idle.
- Hardware bank manages to archive the least latency.
- 2.5V (SSTL_2 compatible) I/O for standard DDR1 device. 1.8V (LVCMOS) I/O for lower power DDR1 (or Mobile DDR1) device. 1.8V SSTL I/O for Standard DDR2 SDRAM.
- Support x16 DDR1/Mobile DDR/DDR2 SDRAM device.
- The capacity of the DDR1/Mobile DDR1/DDR2 device range from 64Mbit to 2Gbit is supported.
- Support DDR266\DDR333
- The address assignment are list below:

DDR Device Organization Table

Capacity	Org	Bank	Row Addr	Col Addr	Page（Row）Size (Byte)	Note
64Mb	4M * 16	4	A0~A11	A0~A7	512	DDR/DDR2
128Mb	8M * 16	4	A0~A11	A0~A8	1024	
*128Mb	8M*8bit*2	4	A0~A11	A0~A8	1024	
256Mb	16M * 16	4	A0~A12	A0~A8	1024	
*256Mb	16M*8bit*2	4	A0~A11	A0~A9	2048	

512Mb	32M * 16	4	A0~A12	A0~A9	2048	
*512Mb	32M*8bit*2	4	A0~A12	A0~A9	2048	
1Gb	64M * 16	4	A0~A13	A0~A9	2048	DDR specify
*1Gb	64M*8bit*2	4	A0~A12	A0~A9，A11	4096	
*2Gb	128M*8bit*2	4	A0~A13	A0~A9,A11	4096	
1Gb	64M * 16	8	A0~A12	A0~A9	2048	DDR2 specify
*1Gb	64M*8bit*2	4	A0~A13	A0~A9	2048	
2Gb	128M*16	8	A0~A13	A0~A9	1024	
*2Gb	128M*2	8	A0~A13	A0~A9	4096	

Note:

1. The capacity catalog mark "*" in front of the data means that type is to combine two pcs 8bit width DDR to 16bit width data bus.
2. When 2Gb DDR2 is supported, CKE signal can not work at the same time.

3.2 Nand Flash Controller

The general purpose Nand Flash Interface controller is a configurable interface to external Nand Flash. The highly configurable and flexible interface can attach to using most of readily available Nand Flash device. The Flash data bus can be configured to be 8bit access.
This controller provides automatic timing control for the using data read and write access signal line. The interface automatically maintains proper CLE, ALE and CE setup and hold up as well as proper read/write DMA practical.

The Controller module can monitor the relatively interval transitions of the NAND Flash device's Ready/Busy signal. This include an interrupt that can monitor the rising edge of the busy signal and that can be set to generate a timeout interrupt if the NAND Flash device hang up, etc.

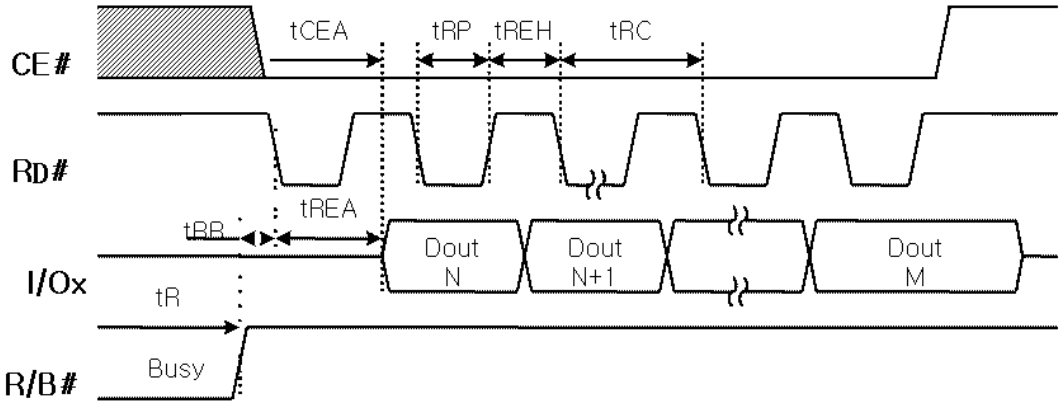
The forward error correction module is used to provide Actions ATJ227X applications with a reliable interface to various storage media, especially storage media that would otherwise have unacceptable bit error rates. The ECC module comprises three different error correcting code processors:

- 1-HM correcting encoder/decoder.
- 8-BCH correcting encoder/decoder.
- 12-BCH correcting encoder/decoder.
- 24-BCH correcting encoder/decoder.
- 40-BCH correcting encoder/decoder

Nand Flash Controller's features are as follows:

- 1bit/8bit/12bit/24bit/40bit Error Correction support
- Data error Corrected by HW automatically
- Seven byte address support for new NAND Flash support
- HW supported Randomizer
- SLC, MLC & TLC NAND Flash support
- 8 bit wide NAND support
- Monitor the NAND Flash Ready/Busy signal by HW support

3.2.1 EDO Mode Timing



3.3 SD/MMC Controller

The chapter describes the SD/MMC card Host Controller and how data is transferred to SD card device and discusses how to configure and program the SD Host Controller (SDC) module. This section is based on MMC card specification 4.3, and is compatible with SD memory card physical layer specification version 2.00. Multimedia Card/SD card is serial/parallel I/output interface to send command and receive data. It has 10 pin, such as CMD, CLK, Data7~0.

SD/MMC Controller's features are as follows:

- Support SD/HCSD/microSD/miniSD memory card, MMC/RSMMC/MMCPLUS card, INAND, MOVINAND, eMMC, CE-ATA Micro Drive and SDIO card etc.
- Support 1 bit, 4bit, 8bit, bus mode.
- Clock max rate up to 52MHz.
- Contain an integrated 32bit*16 FIFO
- Read /Write CRC Status Hardware auto checked.

- Support Auto multi block read/write mode.
- Support SDIO function.
- Support boot mode based on MMC43. SPEC.
- Hardware timeout function.
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for I Signal.
- Build-in pull up resistance for CMD/DAT lines.

3.4 Memory Stick Controller

This chapter describes the Memory stick/pro/micro card Host Controller and How data is transferred to Memory Stick device and discusses how to configure and program the Memory Stick Host Controller (MSHC) module.

The MSHC module provides the following features:

- Full compatibility with Memory Stick Standard Card Format Specification Ver1.43.
- Full compatibility with Memory Stick Pro Card Format Specification Ver1.03.
- Full compatibility with Memory Stick Micro Card Format Specification Ver1.00.
- Full compatibility with Memory Stick Pro-HG Card Format Specification Ver1.02.
- Support Hardware Auto Detecting BREQ INT signal from MS card Before Writing or Reading Data.
- Support Hardware automatically sending Writing or Reading Pages TPC.(Multiple pages Maximum 256 pages).
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for I Signal, Output Delay Chain for output signal.
- Integrated Watchdog Counter to report Exception happening.
- Integrated Pull down resistance (value 51Komh) for Data Line.
- Contains an integrated 32×16-bit FIFO.
- Integrated CRC circuit.
- Pull down resistance Inside for Data Line.

4 GPIO/PWM and Multiplexing

- 64 GPIOs with independent output and input function
- Several different driving capacity of 64 GPIOs
- Software control for Multiplexing
- 4 independent PWM signal from Hz to MHz
- PWM with 64-level duty adjustment
- PWM with high level or low level active
- Built-in pull-up or pull-down resistance in some functional pads

4.1 IO Description

PIN Name	GPIO	Default Status (Boot from NandFlash after Brom)	Drive Capacity (mA)	PU/PD
NAND_D5	GPIOA 00	X (nf_data)	5/9/16	
SIRQ1	GPIOA 01	1(100k pu)	5/9	SIRQ1: PU 100k/PD 100k
NAND_CEB0	GPIOA 02	1	5/9/16	
NAND_CEB1	GPIOA 03	0	5/9/16	
NAND_CEB2	GPIOA 04	1	5/9/16	
NAND_CEB3	GPIOA 05	1	5/9/16	
I2S_D1	GPIOA 06	Z	8/12	
I2S_D2	GPIOA 07	Z	8/12	
NAND_RB0	GPIOA 08	1（2.2k pu）	5/9/16	PU 2.2k (RB0)
NAND_RB1	GPIOA 09	Z	5/9/16	PU 2.2k (RB1)
NAND_D0	GPIOA 10	X (nf_data)	5/9/16	
NAND_D1	GPIOA 11	X (nf_data)	5/9/16	
SD0_D4	GPIOA 12	0	5/9/12	SD:50K PU MS:50K PD
SD0_D5	GPIOA 13	0	5/9/12	SD:50K PU MS:50K PD
SD0_D6	GPIOA 14	0	5/9/12	SD:50K PU MS:50K PD

SD0_D7	GPIOA 15	0	5/9/12	SD:50K PU MS:50K PD
NAND_D6	GPIOA 16	X (nf_data)	5/9/16	
NAND_D7	GPIOA 17	X (nf_data)	5/9/16	
SD0_CLK	GPIOA 18	1	5/9/16	
SD0_CMD	GPIOA 19	0	5/9/12	SD:50K PU
SD0_D0	GPIOA 20	0	5/9/12	SD:50K PU MS:50K PD
SD0_D1	GPIOA 21	0	5/9/12	SD:50K PU MS:50K PD
SD0_D2	GPIOA 22	0	5/9/12	SD:50K PU MS:50K PD
SD0_D3	GPIOA 23	0	5/9/12	SD:50K PU MS:50K PD
UART0_TX	GPIOA 24	0	5/9/12	
UART0_RX	GPIOA 25	0	5/9/12	
LCD_D14	GPIOA 26	0	5/9	
LCD_D15	GPIOA 27	0	5/9	100k PU
LCD_D16	GPIOA 28	0	5/9	100k PD
LCD_D17	GPIOA 29	0	5/9	100k PU
I2C_SCLK	GPIOA 30	0	5/9	I2C:2.7K PU
I2C_SDATA	GPIOA 31	0	5/9	I2C:2.7K PU
SD1_CLK	GPIOB 00	1	5/9/16	
SD1_CMD	GPIOB 01	Z	5/9/12	SD:50K PU
BT_PCLK	GPIOB 02	0	5/9	
BT_HSYNC	GPIOB 03	0	5/9	
BT_VSYNC	GPIOB 04	0	5/9	
BT_CLKOUT	GPIOB 05	0	5/9/12	
BT_D0	GPIOB 06	Z	5/9	
BT_D1	GPIOB 07	Z	5/9	
BT_D2	GPIOB 08	Z	5/9	
BT_D3	GPIOB 09	Z	5/9	
BT_D4	GPIOB 10	Z	5/9	
BT_D5	GPIOB 11	Z	5/9	
BT_D6	GPIOB 12	Z	5/9	
BT_D7	GPIOB 13	Z	5/9	

SPI0_SCLK	GPIOB 14	0	5/9/12	
SPI0_SS	GPIOB 15	Z	5/9/12	
SPI0_MOSI	GPIOB 16	0	5/9/12	
SPI0_MISO	GPIOB 17	Z	5/9/12	
SPI1_SCLK	GPIOB 18	0	5/9/12	
SPI1_SS	GPIOB 19	Z	5/9/12	
SPI1_MOSI	GPIOB 20	0	5/9/12	
SPI1_MISO	GPIOB 21	Z	5/9/12	
I2S_MCLK	GPIOB 22	Z	8/12A	
I2S_BCLK	GPIOB 23	Z	8/12	
I2S_LRCLK	GPIOB 24	Z	8/12	
I2S_D0	GPIOB 25	Z	8/12	
KS_IN0	GPIOB 26	1 (100k PU)	5/9	KEY:100k PU 100k PU
KS_IN1	GPIOB 27	1 (100k PU)	5/9	KEY:100k PU 100k PU
KS_IN2	GPIOB 28	1 (100k PU)	5/9	KEY:100k PU
KS_IN3	GPIOB 29	Z	5/9	KEY:100k PU 100k PU
KS_OUT0	GPIOB 30	0 (100k PD)	5/9	100k PD
KS_OUT1	GPIOB 31	1 (100k PU)	5/9	100k PU

4.2 Register Description

GPIO/MFP/PWM Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
GPIO/MFP/PWM	0x101C0000	0xB01C0000

GPIO/MFP/PWM Registers Offset Address

Offset	Register Name	Description
0x0000	GPIO_AOUTEN	GPIOA Output Enable
0x0004	GPIO_AINEN	GPIOA Input Enable
0x0008	GPIO_ADAT	GPIOA Data
0x000C	GPIO_BOUTEN	GPIOB Output Enable
0x0010	GPIO_BINEN	GPIOB Input Enable

0x0014	GPIO_BDAT	GPIOB Data
0x0018	MFP_CTL0	Multiplexing Control 0
0x001C	MFP_CTL1	Multiplexing Control 1
0x0040	PWM0_CTL	PWM0 Output Control
0x0044	PWM1_CTL	PWM1 Output Control
0x0048	PWM2_CTL	PWM2 Output Control
0x004C	PWM3_CTL	PWM3 Output Control
0x0088	PAD_DRV0	PAD Drive Capacity0 Select
0x008C	PAD_DRV1	PAD Drive Capacity1 Select
0x0090	PAD_DRV2	PAD Drive Capacity2 Select

4.2.1 GPIO_AOUTEN

GPIOA Output Enable Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:0	GPIOA_OUTEN	GPIOA [31:0] Output Enable. 0: Disable 1: Enable	RW	0

4.2.2 GPIO_AINEN

GPIOA Input Enable Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:0	GPIOA_INEN	GPIOA [31:0] Input Enable. 0: Disable 1: Enable	RW	0

4.2.3 GPIO_ADAT

GPIOA Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:0	GPIOA_DAT	GPIOA [31:0] Input/Output Data.	RW	0

4.2.4 GPIO_BOUTEN

GPIOB Output Enable Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:0	GPIOB_OUTEN	GPIOB [31:0] Output Enable. 0: Disable 1: Enable	RW	0

4.2.5 GPIO_BINEN

GPIOB Input Enable Register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:0	GPIOB_INEN	GPIOB [31:0] Input Enable. 0: Disable 1: Enable	RW	0

4.2.6 GPIO_BDAT

GPIOB Data Register

Offset=0x0014

Bits	Name	Description	R/W	Reset
31:0	GPIOB_DAT	GPIOB [31:0] Input/Output Data.	RW	0

4.2.7 MFP_CTL0

Multiplexing Control Register 0
Offset=0x0018

Bits	Name	Description	R/W	Default
31	LCDDHL	LCD_D[15:8] Multiplexing 0: LCD_D[15:8] 1: LCD_D[7:0]	RW	0
30		LCD_D[17:12] 0: LCD 1:reserved	RW	Reserved
29	BT	BT_D[7:2], BT_CLKOUT, BT_VSYNC, BT_HSYNC and BT_PCLK Multiplexing 0: BT_D[7:2], BT_CLKOUT, BT_VSYNC, BT_HSYNC and BT_PCLK or BT_D[7:6], LCD_ D[0:3], BT_CLKOUT, LCD[14:16] according to MFP_CTL0[19] 1: Nor_D[15:10], Nor_A[5:2]	RW	1
28	SD1_CMD	SD1_CMD Multiplexing 0: SD1_CMD 1: MS_BS	RW	0
27	SD1_CLKA	SD1_CLKA Multiplexing 0: SD1_CLKA 1: MS_CLK	RW	0
26:24	SD0DH	SD0_D[7:4] Multiplexing 000: SD0_D[7:4] 001: SD1_D[3:0] (BROM SD1_D0 detect) 010: MS_D[7:4] 011: Nor_A[17:14] 100: LCD_D[7:4] 101: MS_D[3:0] 110: LCD_D[7:5]&SD0_D[0] 110: LCD_D[7:5]&SD1_D[0]	RW	011
23:22	SD0DL	SD0_D[3:0] Multiplexing 00:SD0_D[3:0] (BROM SD0_D0 detect) 01: MS_D[3:0] 10: Nor_A[11:8] 11: LCD_D[3:0]	RW	10

21:20	SD0_CMD	SD0_CMD Multiplexing 00: SD0_CMD 01: MS_BS 10: Nor_A22 11: Reserved	RW	10
19	BTLCD	BT_PCLK、BT_CLKOUT、BT_HSYNC、BT_VSYNC and BT_D[0:5]Multiplexing with LCD 0: BT_PCLK、BT_HSYNC、BT_VSYNC、BT_D[0:5] 1: LCD_ D[16:14]、LCD[13:12]、LCD[3:0]	RW	0
18	SD0_CLKA	SD0_CLKA Multiplexing 0: SD0_CLKA 1:MS_CLK	RW	0
17:16	NFDM	Nand_D[5:2] Multiplexing 00: Nand_D[5:2] 01: Nor_D[5:2] 10: LCD_D[13:10] 11: SPI1_MISO、SPI1_MOSI、SPI1_SS、SPI1_SCLK (BROM SPI Nor detect)	RW	01
15:14	NFDLH	Nand_D[1:0] and Nand_D[7:6] Multiplexing 00: Nand_D[1:0] and Nand_D[7:6] 01: Nor_D[1:0] and Nor_D[7:6] 10: LCD_D[9:8] and LCD_D[15:14] 11: PWM1、SIRQ1 and Nor_D[7:6]	RW	01
13	NFRB1	Nand_RB1 Multiplexing 0: Nand_RB1 1: Nor_CEB5	RW	0
12	NFRB0	Nand_RB0 Multiplexing 0: Nand_RB0 1: Nor_CEB4	RW	0
11:10	NFWR	Nand_WEB and Nand_RDB Multiplexing 00: Nand_WEB and Nand_RDB 01: Nor_WR and Nor_RD 10: LCD_DCLK(WR) and LCD_VSYNC(RS) 11: SPI0_MOSI and SPI0_MISO	RW	01
9:8	NFCA	Nand_CLE and Nand_ALE Multiplexing 00: Nand_CLE and Nand_ALE 01: Nor_A0 and Nor_A1 10: LCD_D16 and LCD_D17 11: SPI0_SS and SPI0_SCLK	RW	01

7:6	NFCEB3	Nand_CEB3 Multiplexing 00: Nand_CEB3 01: Nor_CEB3 10: UART1_RX 11: MS_DBG_CLK	RW	00
5:4	NFCEB2	Nand_CEB2 Multiplexing 00: Nand_CEB2 01: Nor_CEB2 10: UART1_TX 11: SD_DBG_CLK	RW	00
3:2	NFCEB1	Nand_CEB1 Multiplexing 00: Nand_CEB1 01: Nor_CEB1 10: SD1_CLKB 11: Reserved	RW	00
1:0	NFCEB0	Nand_CEB0 Multiplexing 00: Nand_CEB0 01: Nor_CEB0/7 10: SD0_CLKB 11: Reserved	RW	01

4.2.8 MFP_CTL1

Multiplexing Control Register 1

Offset=0x001C

Bits	Name	Description	R/W	Default
31	MFEN	Multi Function Enable. 0: Disable 1: Enable	RW	0
30:29	UART0TRX	UART0_TX and UART0_RX Multiplexing 00:UART0_TX and UART0_RX 01: SPI0_MOSI and SPI0_SCLK 10: Nor_A20 and Nor_A21 11: Reserved	RW	10
28:27	KSIN3	KS_IN3 Multiplexing 00: KS_IN3 01: EJ_TDO	RW	01

		10: PWM3 11: Reserved		
26:25	KSIN2	KS_IN2 Multiplexing 00: KS_IN2 01: EJ_TDI 10: PWM2 11: Reserved	RW	01
24	KSINOUT	KS_IN[1:0] and KS_OUT[1:0] Multiplexing 0: KS_IN[1:0] and KS_OUT[1:0] 1: EJ_TMS、EJ_TCK、EJ_TRST、EJ_DINT	RW	1
23:22	BTD[1:0]	BT_D[1:0] Multiplexing 00: BT_D[1:0], or LCD_D[12:13] according to MFP_CTL0[19] 01: Nor_D[9:8] 10: PWM1、PWM0 11: UART1_TX、UART1_RX	RW	01
21	SIRQ1	SIRQ1 Multiplexing 0: SIRQ1 1: PWM1	RW	0
20	LCDBT	LCD_LDE and LCD_D[15:8] Multiplexing 0: (LCD_LDE/RD 、 LCD_D[15:8]) Or (LCD_LDE/RD 、 LCD_D[7:0]), according to MFP_CTL[31] 1:BT_PCLK、BT_D[5:0]、BT_VSYNC、BT_HSYNC	RW	0
19:18	I2SD2	I2S_DO2 Multiplexing 00: I2S_DO2 01: SPDIF_TX 10: BT_CLKOUT 11: I2S_DI	RW	00
17:16	I2SD1	I2S_DO1 Multiplexing 00: I2S_DO1 01: I2S_DI 10: PWM0 11: Reserved	RW	00
15	I2SCLKD0	I2S_MCLK, I2S_BCLK, I2S_LRCLK and I2S_DO0 Multiplexing 0: I2S_MCLK, I2S_BCLK, I2S_LRCLK and I2S_DO0 1: SPI1_SCLK, SPI1_SS, SPI1_MOSI and SPI1_MISO	RW	0
14:13	I2C	I2C_SCLK and I2C_SDATA Multiplexing 00: I2C_SCLK and I2C_SDATA 01: UART1_RX and UART1_TX	RW	10

		10: Nor_A7 and Nor_A6 11: SPI0_SS and SPI0_MISO		
12	TEST	TEST and FM_CLK Multiplexing 0: TEST 1: FM_CLK (defined in CMU_FMCLK register)	RW	0
11:10	SPI0SSDI	SPI0_SS and SPI0_MISO Multiplexing 00: SPI0_SS and SPI0_MISO 01: UART1_TX and UART1_RX 10: PWM2 and PWM3 11: PWM2 and SPI0_MISO	RW	00
9:8	SPI0CKDO	SPI0_SCLK and SPI0_MOSI Multiplexing 00: SPI0_SCLK and SPI0_MOSI 01: UART1_RTSB and UART1_CTSB 10: UART0_TX and UART0_RX 11: Nor_A12 and Nor_A13	RW	11
7:6	SPI1MISO	SPI1_MISO Multiplexing 00: SPI1_MISO 01: UART1_RX 10: PWM3 11: DRV_VBUS	RW	00
5:4	SPI1SS	SPI1_SS Multiplexing 00: SPI1_SS 01: UART1_TX 10: PWM2 11: Reserved	RW	00
3:2	SPI1CKDO	SPI1_SCLK and SPI1_MOSI Multiplexing 00: SPI1_SCLK and SPI1_MOSI 01: UART1_RTSB and UART1_CTSB 10: UART0_TX and UART0_RX 11: Nor_A18 and Nor_A19	RW	11
1:0	LCDUART0-	LCD_D[17:16] and UART0 multiplexing 00: LCD_D[17:16] 01: BT_D[7:6] 10: UART0_RX and UART0_TX 11: Reserved	RW	00

4.2.9 PWMx_CTL

PWMx output control (x=0, 1, 2, 3)

Offset=0x0040+4*x

Bits	Name	Description	R/W	Default
31:9	-	Reserved	R	0
8	POL_SEL	Polarity select 0: PWM low voltage level active 1: PWM high voltage level active	RW	0
7:6	-	Reserved	R	0
5:0	DUTY	Duty select T active = (DUTY+1)/64	RW	0

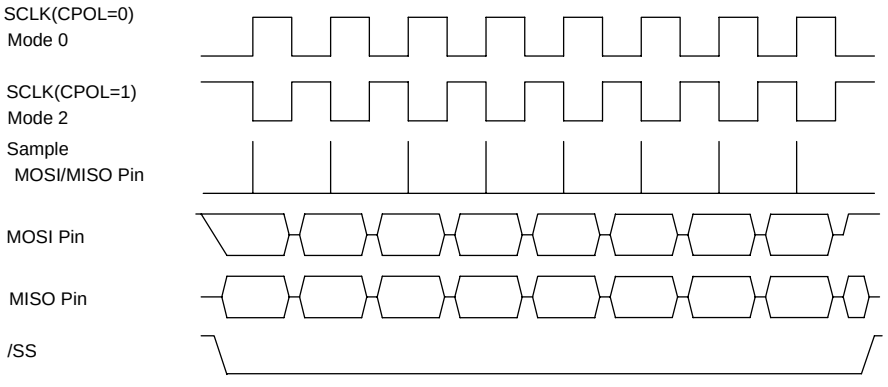
5 Serial Peripheral Interface

5.1 SPI

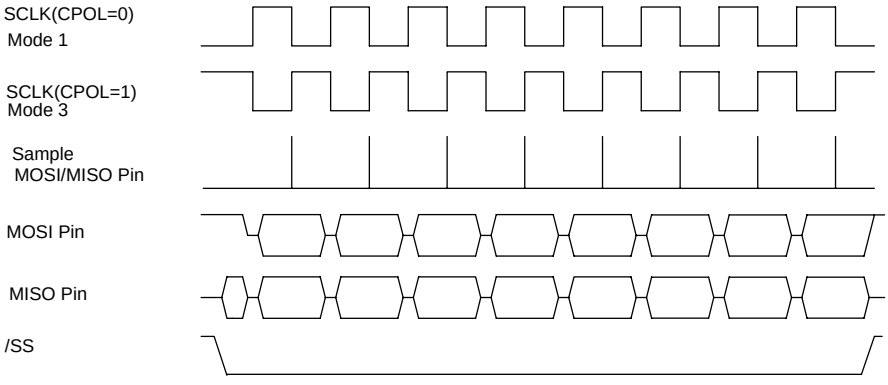
ATJ227X contains two SPI interfaces. Each SPI has the following features:

- Support master mode and slave mode. The speed of master mode up to 80Mbps, and slaver up to 20Mbps.
- Support dual I/O write and read mode while use as master
- Support single data rate mode and double data rate(DDR mode) while use as master
- Support two wire mode, only use SCLK and MOSI signal
- Support IRQ and DMA mode to transmit data

CPOL/CPHA	Leading Edge	Trailing Edge	SPI Mode
0/0	Sample, rising	Setup, falling	0
0/1	Setup, rising	Sample, falling	1
1/0	Sample, falling	Setup, rising	2
1/1	Setup, falling	Sample, rising	3

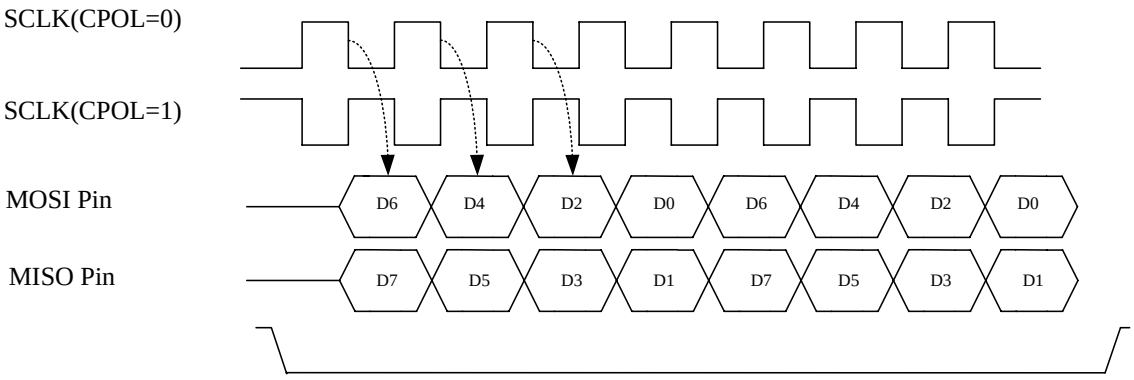


CPHA=0



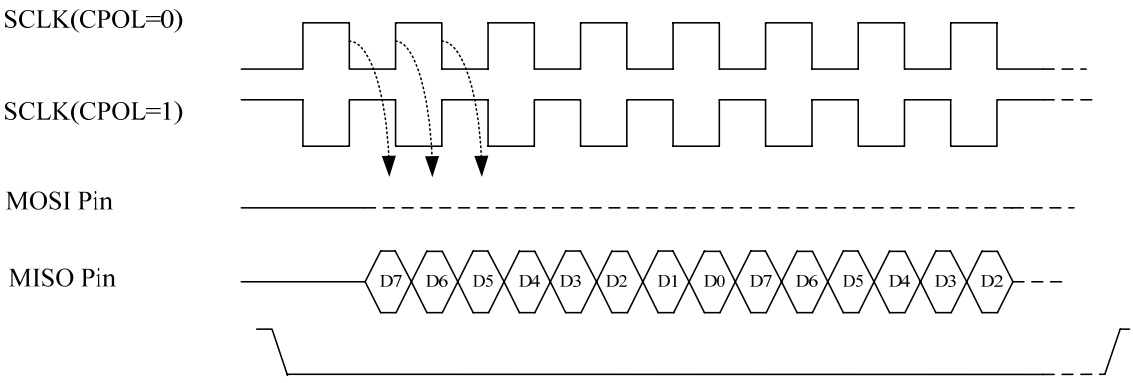
CPHA=1

Normal Operation



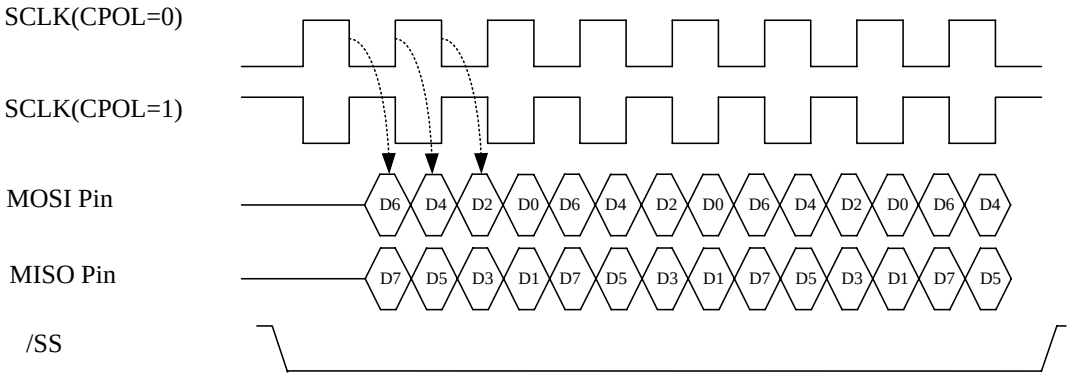
CPHA=0

Dual I/O write&read



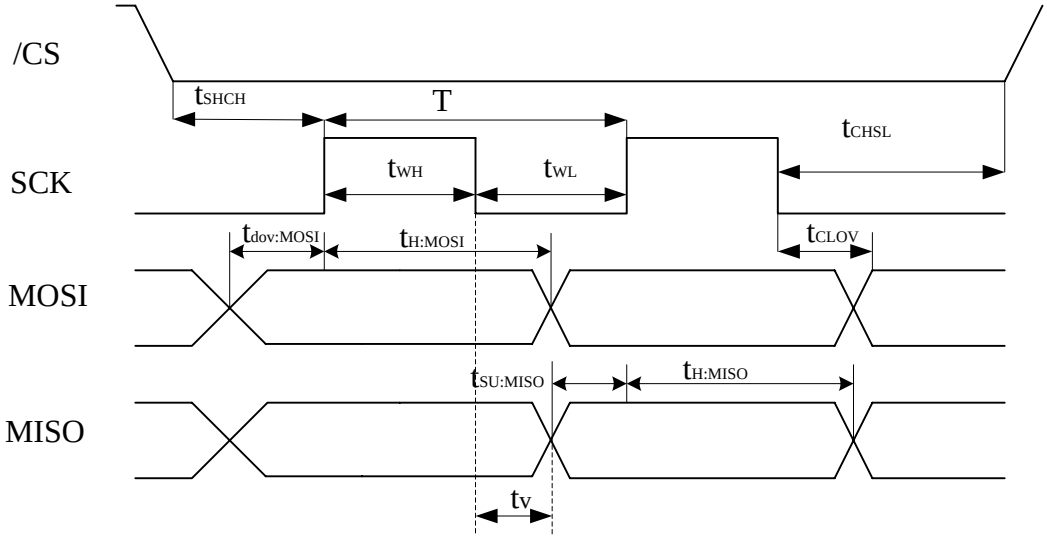
CPHA=0

Single I/O DDR read



CPHA=0

Dual I/O DDR read



SPI timing

SPI max clock is 80MHz and the typical clock is 60MHz act as master.

The parmater s for reading SPI norFlash PMC25LV080 at the speed of 60Mbps are as: (System clock 60M)

Parameter	Symbol	Typical	Unit
SCK Clock	fclk	60	MHz
SCK High time	t_{WH}	8.01	ns
SCK Low time	t_{WL}	8.45	ns
SCK rise time	t_r	7.3	ns
SCK fall time	t_f	9.22	ns
Data output valid	$t_{DOV:MOSI}$	5.5	ns
Data output hold	$t_{H:MOSI}$	9.5	ns
Data in setup time	$t_{SU:MISO}$	3.75	ns
Data in hold time	$t_{H:MISO}$	10.0	ns
Output valid from CLK(MISO)	tv	11.25	ns

Slave:

Speed up to 15MHz if only write, and speed up to 30MHz if only read act as slave.

Parameter	Symbol	typical	Unit
Sck Clock	fclk	10	MHz
SCK High Time	t_{WH}	52	ns

SCK Low Time	t_{WL}	48	ns
SCK Rise Time	t_r	11.5	ns
SCK Fall Time	t_f	12	ns
Data Output Valid	$t_{DOV:MOSI}$	48.0	ns
Data Output Hold	$t_{H:MOSI}$	44.0	ns
Data In Setup Time	$t_{SU:MISO}$	19	ns
Data In Hold Time	$t_{H:MISO}$	75	ns
Output Valid From Clk (Miso)	tv	39	ns

5.1.1 Registers Description

SPI Registers Block Base Address

Block Name	Physical Base Address	KSEG1 Base Adress
SPI0	0x10250000	0xB0250000
SPI1	0x10258000	0xB0258000

SPIx Registers Offset Address

Offset	Register Name	Description
0x0000	SPIx_CTL	SPI Control Register
0x0004	SPIx_CLKDIV	SPI Clock Divide Register
0x0008	SPIx_STAT	SPI Status Register
0x000c	SPIx_RXDAT	SPI Receive FIFO Data Register
0x0010	SPIx_TXDAT	SPI Transmit FIFO Data Register

5.1.1.1 SPIx_CTL

SPIx Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:27	-	Reserved	R	0

26	CEB	Convert Endian bit 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 16bit mode: 0x3210->0x1032 32bit mode: 0x76543210 ->0x10325476 MSB or LSB first shift in or out	RW	0
25:24	SDT	Sample delay time 00: No delay 01: Delay 1 HCLK cycle time 10: 2 HCLK cycle time 11: Reserved	RW	0
23:22	RDIC	RX DRQ/IRQ Control. 00: Set when at least one byte received in IRQ mode. 01: Set when 4 level received in IRQ/DRQ mode 10: Set when 8 level received in IRQ/DRQ mode 11: Set when 12 level received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 level necessary.	RW	0
21:20	TDIC	TX DRQ/IRQ Control. 00: Set when TX FIFO is 1 level empty in IRQ mode. 01: Set when TX FIFO is 4 level empty in IRQ/DRQ mode. 10: Set when TX FIFO is 8 level empty in IRQ/DRQ mode. 11: Set when TX FIFO is 12 level empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 level necessary.	RW	0
19	TWME	Two wire mode enable bit 0: Normal 4 wire mode 1: Two wire mode, use two pin, SPI_CLK and SPI_MOSI	RW	0
18	EN	Enable. 0: Disable 1: Enable	RW	0
17:16	RWC	R/W control 00: Write and read 01: Write only 10: Read only 11: Reserved	RW	00

15	DTS	Read Start Control Write 1 to start Read clock while use DMA to read data, available only in master read only mode. When transfer is finished, this bit will be auto cleared	RW	0
14	SSATEN	SPI_SS active automatically enable when in mode 0 and mode 2 (CPHA=0), only use in standard mode, except dual and DDR mode. 0: Disable 1: Enable	RW	0
13:12	DM	Dual mode and Double data rate Dual mode: Two data wire to read or write Double data rate: DDR 00: Single data wire and single data rate read or write 01: Dual and single data rate mode 10: Single data wire and DDR mode 11: Dual and DDR mode	RW	0
11	LBT	Loopback test 0: Not loopback 1: Loopback	RW	0
10	MS	Master/Slave Select. 0: Master 1: Slave	RW	0
9:8	DAWS	Data/Address Width. Select 00: 8 bit data and address, low 8 bit 01: 16 bit data and address, low 16bit 10: 32 bit data and address 11: Reserved	RW	0
7:6	CPOS	Clock Polarity Select. CPOL CPHA 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3	RW	b11
5	LMFS	LSB/MSB First Select. 0: Transmit and receive MSB first 1: Transmit and receive LSB first	RW	0
4	SSCO	SPI_SS Control Output (only for master mode). 1: Output high 0: Output low.	RW	1

3	TIEN	TX IRQ Enable. 0: Disable 1: Enable	RW	0
2	RIEN	RX IRQ Enable. 0: Disable 1: Enable	RW	0
1	TDEN	TX DRQ Enable. 0: Disable 1: Enable	RW	0
0	RDEN	RX DRQ Enable. 0: Disable 1: Enable	RW	0

5.1.1.2 SPIx_CLKDIV

SPIx Clock Divide Control Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9:0	CLKDIV	In master mode: SPICLK=HCLK/(CLKDIV*2) While CLKDIV is set to 1, the divide is 2. The SPI clock rate up to 80MHz. In slave mode: Need not to set this register. Supporting SPI clock rate up to 20MHz. When use, this register can not be set to 0	RW	0

5.1.1.3 SPIx_STAT

SPIx Status Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9	TFEM	TX FIFO Empty. 1: Empty	R	1

		0: Not Empty		
8	RFFU	RX FIFO Full. 1: Full 0: Not Full	R	0
7	TFFU	TX FIFO Full. 1: Full 0: Not Full	R	0
6	RFEM	RX FIFO Empty. 1: Empty 0: Not Empty	R	1
5	TFER	TX FIFO Error. When overflow, the bit is set to 1. Write 1 to the bit will clear the bit and reset the FIFO.	RW	0
4	RFER	RX FIFO Error. When overflow, the bit is set to 1. Write 1 to the bit will clear the bit and reset the FIFO.	RW	0
3	BEB	Bus error bit. Write 1 to the bit will clear the bit 0: No error 1: Bus error	RW	0
2	TCOM	Transfer Complete Bit. DMA mode: This bit will be set to 1 when all the data sent out or receive over, that the SCK has not clock. CPU mode: This bit will be set to 1 when every byte data sent out or receive over, that the SCK has not clock. Write 1 will clear to zero	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit will clear it.	RW	0
0	PIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to this bit will clear it.	RW	0

5.1.1.4 SPIx_RXDAT

SPIx RXData Register
Offset=0x000c

Bits	Name	Description	R/W	Reset
31:0	RXDAT	Receive Data. The depth of RXFIFO is 32bit×16 levels.	R	x

5.1.1.5 SPIx_TXDAT

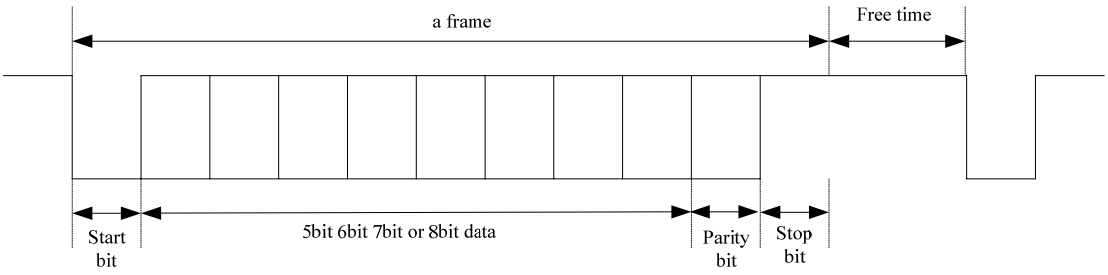
SPIx TXData Register
Offset=0x0010

Bits	Name	Description	R/W	Reset
31:0	TXDAT	Transmit Data. The depth of RXFIFO is 32bit×16 levels.	W	x

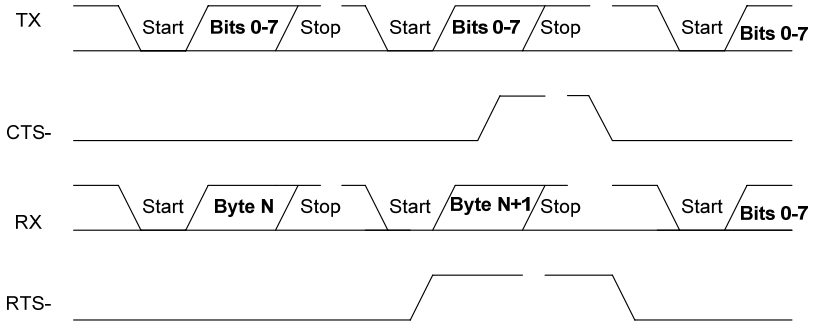
5.2 UART

ATJ227X platform contains two UART interfaces. Each UART has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- Capable of speeds up to 1.5Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Only UART1 support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- Only UART0 support IRC(infrared remote control) Inputs
  Support RC5\9012\NEC (8bit)\AIR protocol, compatible 36kHz, 38kHz, 40kHz carrier.
  Need to connect an IR receiver when use.



UART timing



RTS/CTS Autoflow control timing

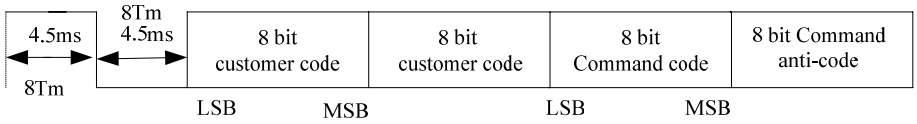
UART: (baudrate*8=clock source/DIV), the clock source can be fixed as 24M or S_CLK, here S_CLK is 120MHz.

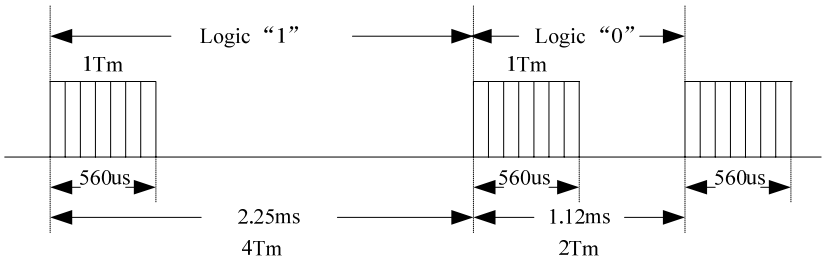
Baud Rate (bps)	Theoretical Bit Width (us)	Real Bit Width (us)	Error Rate (Theoretical)	Remark (Division Frequency)	Remark
2400	416.67	417	0.04%	0x4E2-1	24M clock source
4800	208.33	208.5	0.08%	0x271-1	24M clock source
9600	104.17	105	0.7%	0x13a-1	24M clock source
38400	26.04	26	0.15%	0x4E-1	24M clock source
57600	17.36	17.33	0.17%	0x34-1	24M clock source
115200	8.68	8.7	0.11%	0x1A-1	24M clock source
230400	4.34	4.33	0.11%	0x0D-1	24M clock source

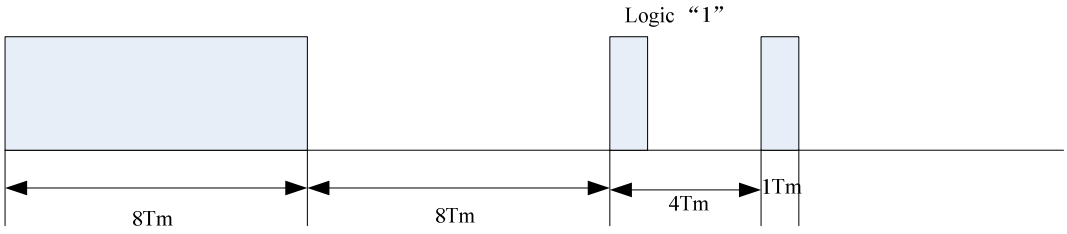
460800	2.17	2.14	1.84%	0x10020-1	S_CLK
750000	1.33	1.33	0.0%	0x10014-1	S_CLK
921600	1.085	1.07	1.75%	0x10010-1	S_CLK
1500000	0.667	0.667	0.0%	0x2-1	24M clock source

The four IRC mode (RC5\9012\NEC (8bit)\AIR protocol), compatible 36kHz, 38kHz, 40kHz carrier timing

IRC 9012 protocol timing:







Repeat code

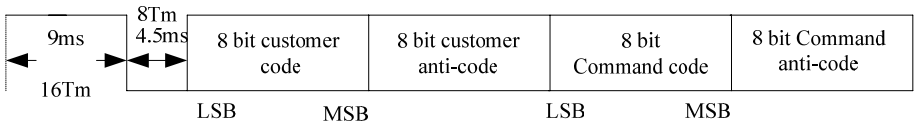
The fault tolerance range for the data from infrared receiving end:

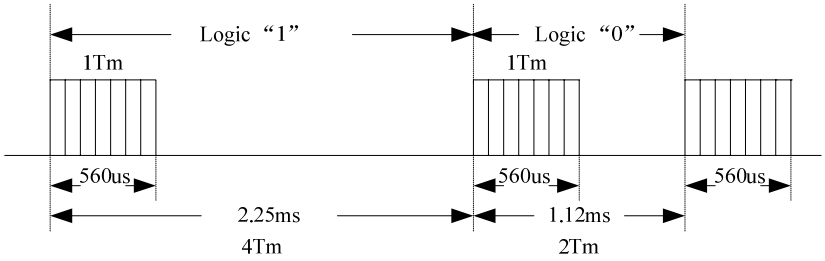
	Max (ms)	Typical (ms)	Min (ms)
Leader Low	5.30	4.5	3.34
Leader High	5.30	4.5	3.34
Bit Low	0.66	0.56	0.42
Bit High	1.99	1.69	1.255

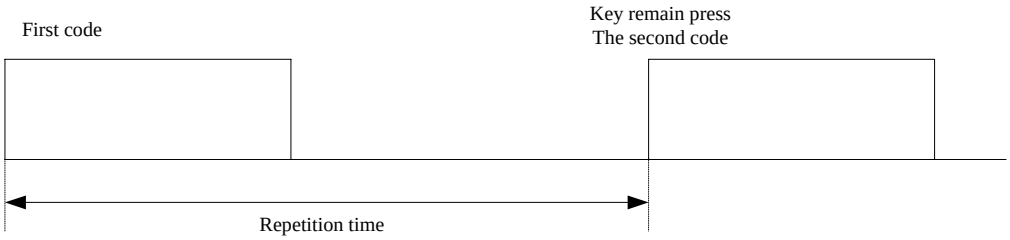
Repeat code:

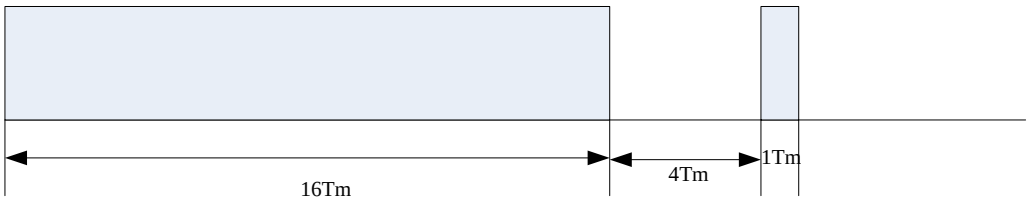
	Max (ms)	Typical (ms)	Min (ms)
Leader Low	5.30	4.5	3.46
Leader High	5.30	4.5	3.46
Bit Low	0.67	0.56	0.44
Bit High	1.99	1.69	1.30

NEC 8bit protocol timing:









Repeat code

The fault tolerance range for the data from infrared receiving end:

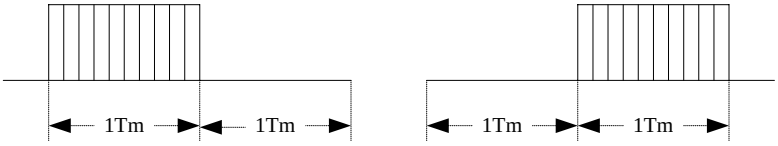
	Max (ms)	Typical (ms)	Min (ms)

Leader Low	10.6	9.0	6.68
Leader High	5.30	4.5	3.34
Bit Low	0.66	0.56	0.42
Bit High	1.99	1.69	1.255

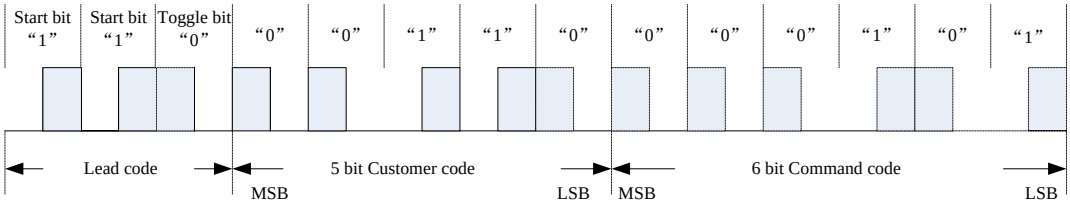
Repeat code:

	Max (ms)	Typical (ms)	Min (ms)
Leader Low	10.6	9.0	7.5
Bit High	2.65	4.5	1.88
Bit Low	0.66		0.47

RC5 protocol timing:



Logic 0 Logic 1



1 bit-time = 3 x 256 /Fosc= 1.688ms (Fosc=455kHz)

Tm= 1 bit-time/2=0.844ms

Repetition time= 4 x 16 x 2Tm=108ms

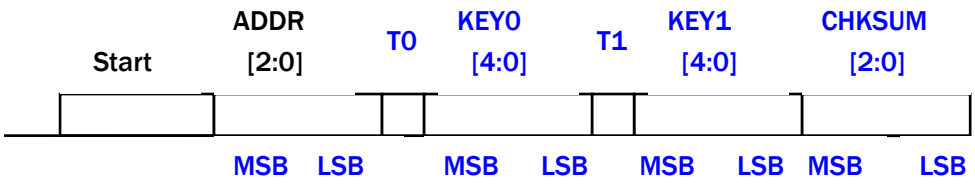
Carrier frequency = Fosc/12

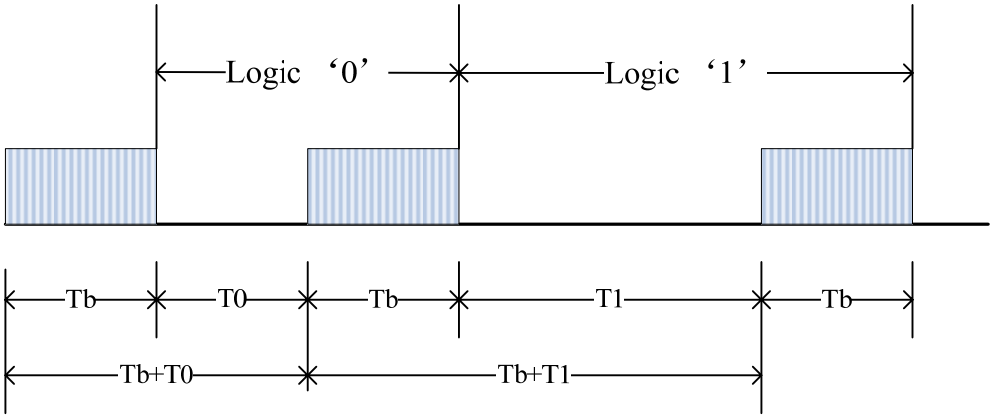
The fault tolerance range for the data from infrared receiving end:

	Max (ms)	Typical (ms)	Min (ms)
Bit Width	1.0	0.844	0.655

AIR protocol timing:

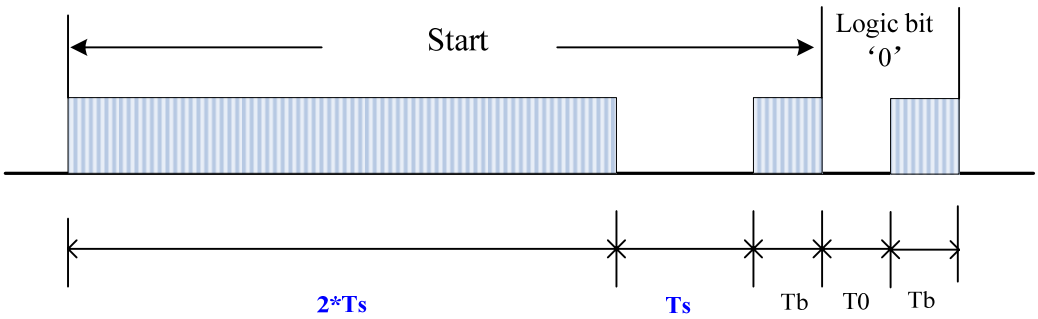
Frame:





Logic Bit

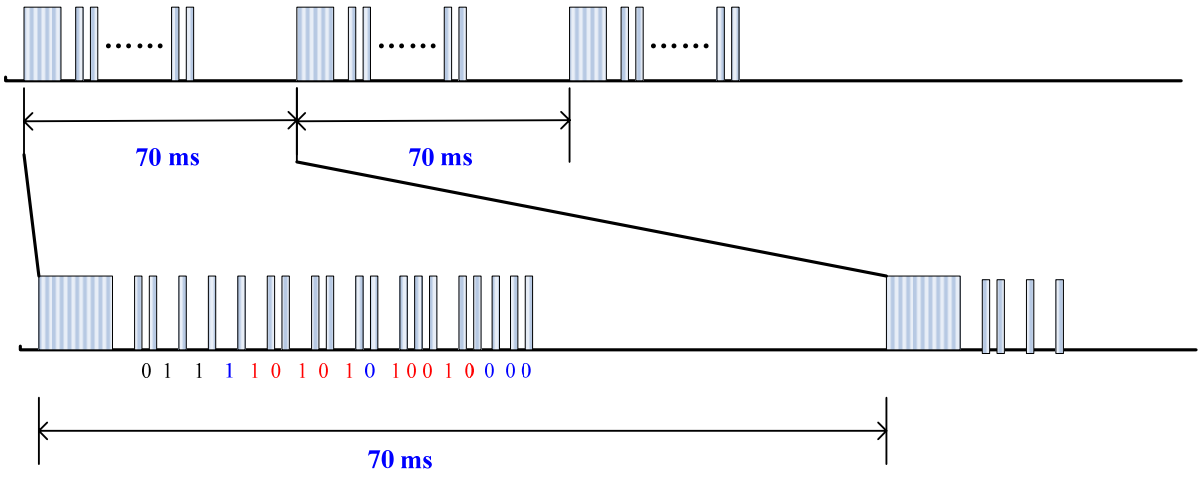
Tb = 160us ≌ 6 D_T; T0 = Tb = 160us; T1 = 360us;



Start Symbol

In which Ts = 500us, so the whole Start Symbol's length is Ts+2*Ts+Tb =1660us.

Checksum[2:0] = { Address[2:0] } + { T0, Key0[4:3] } + { Key0[2:0] }
+ {T1, Key1[4:3]} + { Key1[2:0] };



Repeat Interval

In the above figure, one frame information is: ADDR = b'011, T0 =b'1, KEY0=b'10101, T1=b'0, KEY1 = b'10010.

So, HKSUM = b'011 + b'110 + b'101 + b'010 + b'010 = b'000;

The Fault Tolerance Range for the Data from Infrared Receiving End

	Max (ms)	Typical (ms)	Min (ms)
Leader Low	1.18	1.0	0.836
Leader High	0.59	0.5	0.418
Bit Low	0.19	0.16	0.134
Bit High	0.426	0.36	0.302

5.2.1 Registers Description

Each UART is controlled by a register block.

Uart Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
Uart0	0x10160000	0xB0160000
Uart1	0x10168000	0xB0168000
IRC	0x10160050	0xB0160050

Each register block contains the registers.

UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register
0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register
0x000c	UARTx_STAT	UART Status Register

IRC Registers Offset Address

Offset	Register Name	Description
0x00	IRCCTL	Infrared remote control(IRC) interface control register
0x04	IRCSTAT	IRC status register
0x08	IRCCC	IRC customer code register
0x0C	IRCKDC	IRC key data code register

5.2.1.1 UART0_CTL

UART0 Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0
19	TXIE	UART0 TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART0 RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART0 TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART0 RX DRQ Enable. 0: Disable 1: Enable	RW	0

15	EN	UART0 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0
14	TRFS	UART0 TX/RX FIFO Select TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART0_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13:12	MS	Mode Select. 00: UART0，include TX and RX 01:IRC,infrared remote control, UART0 RX disable	RW	0
11:10	RDIC	UART0 RX DRQ/IRQ Control 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
9:8	TDIC	UART0 TX DRQ/IRQ Control 00: set when TX FIFO is 1 byte leave in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
7	-	Reserved	R	0
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	000
3	-	Reserved	R	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	RW	0

1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	00

5.2.1.2 UART0_RXDAT

UART0 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16 levels.	R	x

5.2.1.3 UART0_TXDAT

UART0 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	TXDAT	Received Data. The depth of FIFO is 8bit×16 levels	R	x

5.2.1.4 UART0_STAT

UART0 Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:17	-	Reserved	R	0
16	UTBB	UART0 TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
15:11	TRFL	TX/RX FIFO Level.	R	0

		The field indicates the current RX and TX FIFO level.		
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8:7	-	Reserved	R	0
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

5.2.1.5 UART1_CTL

UART1 Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0
19	TXIE	UART1 TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART1 RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART1 TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART1 RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART1 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0
14	TRFS	UART1 TX/RX FIFO Select TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART1_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set.	RW	0
12	AFE	Autoflow Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals.	RW	0
11:10	RDIC	UART1 RX DRQ/IRQ Control 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode	RW	00

		11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.		
9:8	TDIC	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is 1 byte leave in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
7	-	Reserved	R	0
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	000
3	-	Reserved	R	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	RW	0
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	00

5.2.1.6 UART1_RXDAT

UART1 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0

7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	x

5.2.1.7 UART1_TXDAT

UART1 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	TXDAT	Received Data. The depth of FIFO is 8bit×16 levels	R	x

5.2.1.8 UART1_STAT

UART1 Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:17	-	Reserved	R	0
16	UTBB	UART1 TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
15:11	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	x
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0

5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

5.2.1.9 IRCCTL

Infrared remote control register

Offset=0x00

Bits	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3	IRE	IRC enable 0: disable 1:enable	RW	0
2	IIE	IRC IRQ enable 0:disable 1:enable	RW	0
1:0	ICMS	IRC coding mode select	RW	0

		00:9012 code 01:8bits NEC code 10:RC5 code 11: AIR code		

5.2.1.10 IRCSTAT

Infrared remote status register

Offset=0x04

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7	IRBB	IRC busy bit. When receiving command, this bit will be set to 1. 0:not busy 1:busy	RW	0
6	UCMP	User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:user code match 1:user code don't match	RW	0
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:key data code match 1:key data code don't match	RW	0
4	RCD	Repeated code detected, Write 1 to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code	RW	0
3	-	Reserved	R	0
2	IIP	IRC IRQ pending bit. write 1 to this bit will clear it 0:no IRQ pending 1: IRQ pending	RW	0
1	IIOF	IRC overflow bit. Write 1 to this bit will clear it. 0: no overflow 1: a new key data code is receiving while the previous one has not been read out.	RW	0
0	IREP	IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing 1 to	RW	0

		this bit will clear this bit, otherwise this bit will be unchanged.		

5.2.1.11 IRCCC

Infrared remote control customer code register.

Offset=0x08

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In AIR mode, Bit2:0 is the address	RW	0

5.2.1.12 IRCKDC

Infrared remote control KEY data code register.

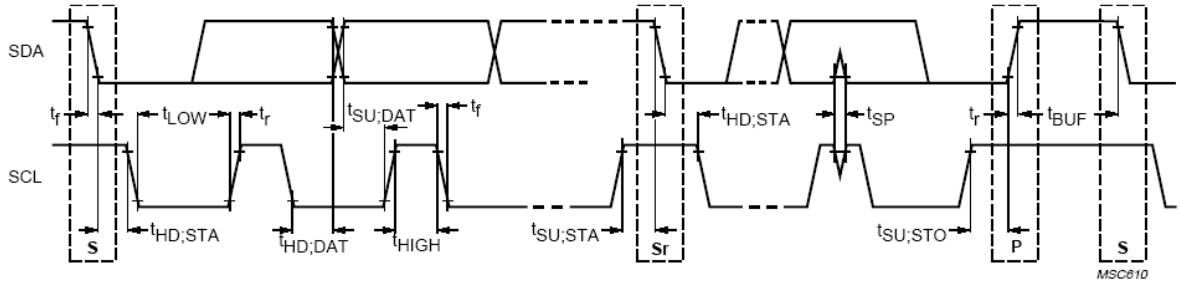
Offset=0x0C

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data In AIR mode, Bit13 is the toggle bit, Bit12:8 is the key1 data Bit5 is the toggle bit, Bit 4:0 is the key0 data,	RW	0

5.3 I2C Controller

- Both master and slave functions support.
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Multi-master capability
- Hi-speed mode and 10bit address mode not support.
- Internal Pull-Up Resistor (2.7k) optional

Pull-up resistors are required on both of the I2C signal lines as the I2C drivers are open drain. Typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal Pull-Up resistor.



I2C: The internal Pull-up resistor is 2.9K ohm

Parameter	Symbol	Typical		Unit
SCL period	f_{SCL}	98.5	375	kHz
Clock low time	T_{LOW}	5.02	1.36	us
Clock high time	T_{HIGH}	5.12	1.31	us
Clock rise time	t_r	115	115	ns
Clock fall time	t_f	3.8	3.8	ns
Data setup time	$t_{SU:DAT}$	3.7	0.92	us
Data hold time	$t_{HD:DAT}$	1.4	0.44	us
Start hold time	$t_{HD:STA}$	9.4	2.32	us
Start setup time	$t_{SU:STA}$	5.8	1.48	us
Stop setup time	$t_{SU:STO}$	5.2	1.42	us

5.3.1 Registers Description

Each I2C is controlled by a register block.

I2C Register Block Base Address

Block Name	Physical Base Address	KSEG1 Base Adress
I2C	0x10180000	0xB0180000

Each register block contains the registers.

I2C Registers Offset Address

Offset	Register Name	Description
0x0000	I2C_CTL	I2C Control Register
0x0004	I2C_CLKDIV	I2C Clock Divide Register
0x0008	I2C_STAT	I2C Status Register
0x000c	I2C_ADDR	I2C Address Register
0x0010	I2C_DAT	I2C Data Register

5.3.1.1 I2C_CTL

I2C Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	RW	0
6	PUEN	Internal Pull-Up resistor (2.7k) enable. 0: Disable 1: Enable	RW	0
5	IRQE	IRQ Enable. When the I2C status change, generate IRQ.I2C can detect four status: start, restart, complete a byte transfer, stop. 0: Disable 1: Enable	RW	0
4	BNB	Bypass NACK bit: 0: data could not be sent out while receive NACK after the slave address sent out. 1: data could be sent out, do not care the NACK after the slave address sent out.	RW	0
3:2	GBCC	Generating Bus Control Condition (only for master mode).	RW	0

		00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the I2C_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus. Auto release the bus when select these command.		
1	RB	Release Bus. Write 1 to this bit will release the bus.	RW	0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0

5.3.1.2 I2C_CLKDIV

I2C Clock Divide Control Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	CLKDIV	Clock Divider Factor (only for master mode). I2C clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=PCLK/(CLKDIV*16) Note: the register can not be set to 0 or 1 when used.	RW	0

5.3.1.3 I2C_STAT

I2C Status Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address	RW	0

		1: Indicate the last byte received or transmitted is data		
7	TCB	Transfer complete bit 0: not finish transfer 1: A byte transfer finish, include transfer the ACK or NACK bit Write "1" to clear this bit	RW	0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0
5	STAD	Start detect bit, include restart. The bit is clear when the I2C module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0
4	STPD	Stop detect bit The bit is clear when the I2C module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	RW	0
3	LAB	Lose arbitration bit 0: not lose 1: lose arbitration	RW	0
2	IRQP	IRQ Pending Bit. Writing 1 to this bit will clear it. 1: IRQ 0: No IRQ	RW	0
1	BEB	Bus error bit 0: No error occur 1: Bus error occur Write "1" to clear this bit The below conditions occur generate error bit: Stop command sent right after start/restart command. Stop ,start，or restart command sent when sending or receiving data.	RW	0
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK	RW	0

		The bit will be clear when the next byte clock arrived		

5.3.1.3 I2C_ADDR

I2C Address Register
Offset=0x000C

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. I2C_Addr contains the own address of the SOC when the device is use in slave mode. Content of the register is irrelevant when the I2C module is functioning as a master.	RW	0
0	-	Reserved. The LSB should be programmed with a “0”.	RW	0

I2C_DAT

I2C Data Register
Offset=0x0010

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	DA	The register of Data or address to be transferred, or received to. I2CDAT contains the byte to be transmitted on the I2C-bus or a byte that has been received from the I2C-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB’s are the slave I2C device address while the LSB is the Read/Write bit.	RW	0

6 Man-Machine Interface

6.1 Key Matrix

Key module in ATJ227X uses a scan matrix mechanism to identify the 4x2 key matrix. Each key has a corresponding key value in the purpose of identifying for software.

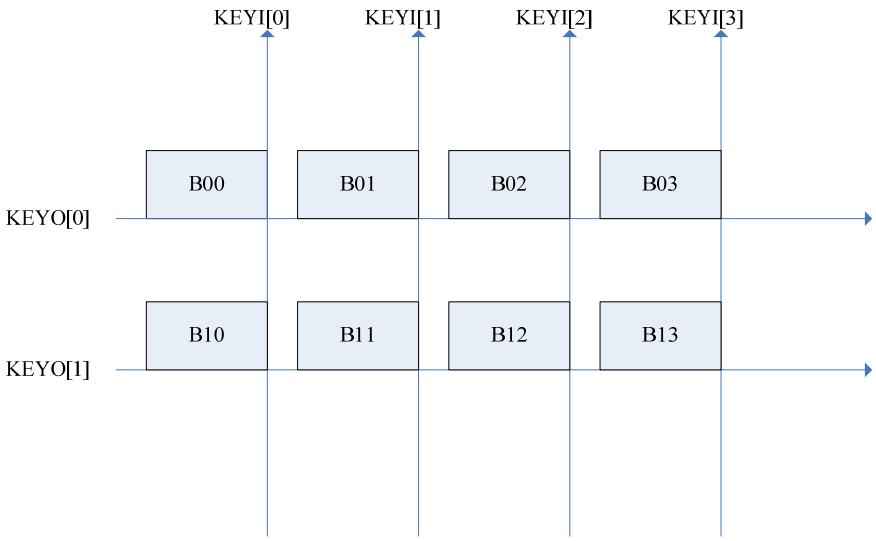
The scan timing can be programmed to control the key sensibility and repeatability for user adjustment.

The key output pad can be set as push-pull or open-drain output type.

- Support 4x2 key scan matrix
- Support programmable scan timing
- Support multi-press

6.1.1 Application Description

6.1.2 KEY Value



Key Value List:

Key	B00	B01	B02	B03	B10	B11	B12	B13
Value	0x00000 0FE	0x00000 0FD	0x00000 0FB	0x00000 0F7	0x00000 0EF	0x00000 0DF	0x00000 0BF	0x00000 07F

6.1.3 Register Description

Key Scan Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
KEY	0x101A0000	0xB01A0000

Key Scan Registers Offset Address

Offset	Register Name	Description
0x0000	KEY_CTL	Key Scan Control Register
0x0004	KEY_DAT	Key Scan Data Register

6.1.4.1 KEY_CTL

Key Scan Control Register
Offset=0x0000

Bits	Name	Description	R/W	Default
31:18	-	Reserved	R	0
17	IRCL	Key Scan IRQ Cleared (only used when shutting down APB Clock).	R	1
16	IRP	Key Scan IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear the bit.	RW	0
15	IREN	Key Scan IRQ Enable. 0: Disable 1: Enable	RW	0
14	OTYP	KSOUT pin output type 0: Opendrain output. 1: push pull output	RW	0
13:10	INMKEN	Key Scan Input(KEYI[3:0]) Mask Enable. 0: Mask Key Input	RW	000

		1: Enable Key Input When any pin of KEYI[3:0] is masked, it can be used as GPIO, even if key scan mode is enable.		
9:8	KOUTEN	Key Scan output (KEYO[1:0])enable bit 0:Mask Key scan output 1: Enable Key scan output When any pin of KEYO[1:0] is masked, it can be used as GPIO, even if key scan mode is enable.	RW	000
7:5	WTS	Key Scan Wait Time Select. KeyScan Wait Time=WTS*32ms 000: 0ms 001: 32ms 010: 64ms 011: 96ms 100: 128ms 101: 160ms 110: 192ms 111: 224ms	RW	000
4:3	PRS	Key Scan Period Select. 00: 20ms 01: 40ms 10: 80ms 11: 160ms	RW	00
2:1	DTS	Key Scan Debounce Time Select. 00: 10ms 01: 20ms 10: 40ms 11: No debounce time	RW	00
0	EN	Key Scan Enable. 0: Disable 1: Enable	RW	0

6.1.4.2 KEY_DAT

Key Scan Data Register

Offset=0x0004

Bits	Name	Description	R/W	Default
31:0	DAT	Key Scan Data.	R	x

6.2 Touch Panel

ATJ227X integrates an 11 bit SAR ADC for Touch panel or 2-channel ADC. When enabled, the ADC will work.

The Touch Panel's features are:

- Support 4-wire resistance touch panel
- 11 bit resolution
- X and Y direction's measurement independently
- Sample Frequency form 1/2K~32K
- Can be used as 2-channel ADC when touch panel's function is not required

6.2.1 Registers Description

Touch Panel Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Address
Touch Panel	0x10120000	0xB0120000

Touch Panel Registers Offset Address

Offset	Register Name	Description
0x0000	TP_CTL	Touch Panel Control Register
0x0004	TP_DAT	Touch Panel Data Register

6.2.1.1 Touch Panel Control Register(TP_CTL)

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:28	-	Reserved	R	0
27:24	-	Reserved for future use	RW	0
23	-	This bit may be fixed to 0 in application.	RW	0
22	REN	Right Channel ADC Enable(X1 acts as R channel input terminal, can not be set when TEN is enabled)	RW	0

21	LEN	Left Channel ADC Enable(Y1 acts as L channel input terminal, can not be set when TEN is enabled)	RW	0
20	RCIP	ADC Right Channel IRQ Pending Bit (not required in touch panel function). 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0
19	LCIP	ADC Left Channel IRQ Pending Bit (not required in touch panel function). 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0
18	RCIE	ADC Right Channel IRQ Enable (not required in touch panel function). 0: Disable 1: Enable	RW	0
17	LCIE	ADC Left Channel IRQ Enable (not required in touch panel function). 0: Disable 1: Enable	RW	0
16	YDR	Touch Panel Y Data Ready Bit (not required in channel ADC function). 0: Not Ready 1: Ready Writing 1 to the bit will clear it.	RW	0
15	XDR	Touch Panel X Data Ready Bit (not required in channel ADC function). 0: Not Ready 1: Ready Writing 1 to the bit will clear it.	RW	0
14	TIP	Touch Panel Touch IRQ Pending Bit (not required in channel ADC function). 0: No IRQ 1: IRQ Writing 1 to the bit will clear it. This bit also indicates a touch occurred when WKE is set.	RW	0
13	TIE	Touch Panel Touch IRQ Enable (not required in channel ADC function). 0: Disable	RW	0

		1: Enable		
12	NOTCH	Indicates the status of touch. 0:No Touch 1:Touch is active	R	0
11	IDLE	Touch Panel Idle Enable(not required in channel ADC function) 0: Enable 1: Disable When enabled, TP goes into idle mode automatically. TP will quit idle state when touched again. When disabled, TP will never go into idle state.	RW	0
10	XYDS	X/Y direction sense control bit(not required in channel ADC function) 0 X direction 1 Y direction	RW	0
9	-	This bit may be fixed to 1 in application.	RW	0
8:6	FSS	Touch Panel Sense Frequency(Fs) Select. 000: 1/2k 001: 1k 010: 2k 011: 4k 100: 8k 101: 16k 110: 21k 111: 32k	RW	101
5	STD	Sampling time duty 0 1/8 1 1/16	RW	1
4:2	ADCBCS	Touch Panel SAR-ADC Bias Current Select. 000: 1uA 001: 3uA 010: 5uA 011: 7uA 100: 9uA 101: 11uA 110: 13uA 111: 15uA	RW	011
1	–	Reserved	RW	0

0	TEN	Touch Panel Enable. 0: Disable 1: Enable (can not be set when LEN or REN is enabled)	RW	0

6.2.1.2 Touch Panel Data Register(TP_DAT)

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:21	YDAT	Touch Panel Y Data.(Signed Data)	R	x
20:16	-	Reserved	R	0
15:5	XDAT	Touch Panel X Data.(Signed Data)	R	x
4:0	-	Reserved	R	0

7 Video IN/OUT

7.1 LCD Controller

The TFT timing controller is expected to drive digital RGB/CPU IF TFT LCD modules. Its main purpose is to convert the pixel stream output from the display engine to the standard TFT LCD display panels. Its features are as follows:

- Support active (TFT) LCD panels with digital RGB/CPU I interface
- Programmable timing control for various panels
- Pixel stream I without strict timing requirements
- Resolutions up to 1024*1024
- Maximum 16777216 simultaneous display color

7.1.1 Pin Mapping

	Serial 8-bit Bus						Parallel 24-bit Bus			
Pin Name	18-bit			24-bit			8-color	16-bit	18-bit	24-bit
	1st	2nd	3rd	1st	2nd	3rd				
LCD_D0				R0	G0	B0			B2	B0
LCD_D1				R1	G1	B1		B3	B3	B1
LCD_D2	R2	G2	B2	R2	G2	B2		B4	B4	B2
LCD_D3	R3	G3	B3	R3	G3	B3		B5	B5	B3
LCD_D4	R4	G4	B4	R4	G4	B4		B6	B6	B4
LCD_D5	R5	G5	B5	R5	G5	B5	Bmsb	B7	B7	B5
LCD_D6	R6	G6	B6	R6	G6	B6		G2	G2	B6
LCD_D7	R7	G7	B7	R7	G7	B7		G3	G3	B7
LCD_D8								G4	G4	G0
LCD_D9								G5	G5	G1
LCD_D10								G6	G6	G2
LCD_D11							Gmsb	G7	G7	G3
LCD_D12									R2	G4
LCD_D13								R3	R3	G5
LCD_D14								R4	R4	G6

LCD_D15		R5	G7
LCD_D16		R6	R0
LCD_D17	Rmsb	R7	R1
LCD_D18			R2
LCD_D19			R3
LCD_D20			R4
LCD_D21			R5
LCD_D22			R6
LCD_D23			R7

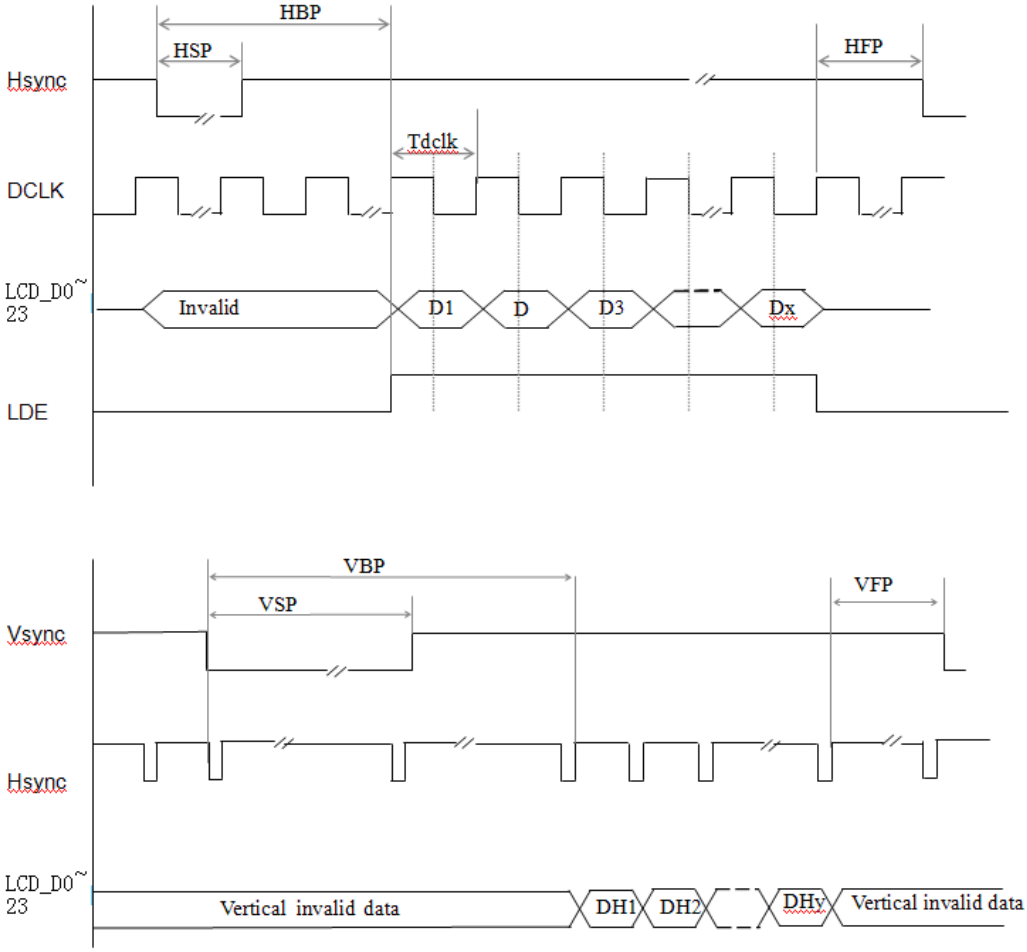
RGB Interface Pin Mapping

Pin Name	1 trans		2 trans				3trans					
	18 bit	16-bit	8bit		9bit		8bit			6bit		
	1st	1st	1st	2nd	1st	2nd	1st	2nd	3rd	1st	2nd	3rd
LCD_D0	B2		G5	B3	G5	B2	R0	G0	B0			
LCD_D1	B3	B3	G6	B4	G6	B3	R1	G1	B1			
LCD_D2	B4	B4	G7	B5	G7	B4	R2	G2	B2	R2	G2	B2
LCD_D3	B5	B5	R3	B6	R2	B5	R3	G3	B3	R3	G3	B3
LCD_D4	B6	B6	R4	B7	R3	B6	R4	G4	B4	R4	G4	B4
LCD_D5	B7	B7	R5	G2	R4	B7	R5	G5	B5	R5	G5	B5
LCD_D6	G2	G2	R6	G3	R5	G2	R6	G6	B6	R6	G6	B6
LCD_D7	G3	G3	R7	G4	R6	G3	R7	G7	B7	R7	G7	B7
LCD_D8	G4	G4			R7	G4						
LCD_D9	G5	G5										
LCD_D10	G6	G6										
LCD_D11	G7	G7										
LCD_D12	R2											
LCD_D13	R3	R3										
LCD_D14	R4	R4										
LCD_D15	R5	R5										
LCD_D16	R6	R6										
LCD_D17	R7	R7										
LCD_D18												
LCD_D19												
LCD_D20												
LCD_D21												

LCD_D22
LCD_D23

CPU Interface Pin Mapping

7.1.2 Interface Timing



Parallel RGB Timing

Serial RGB Timing:

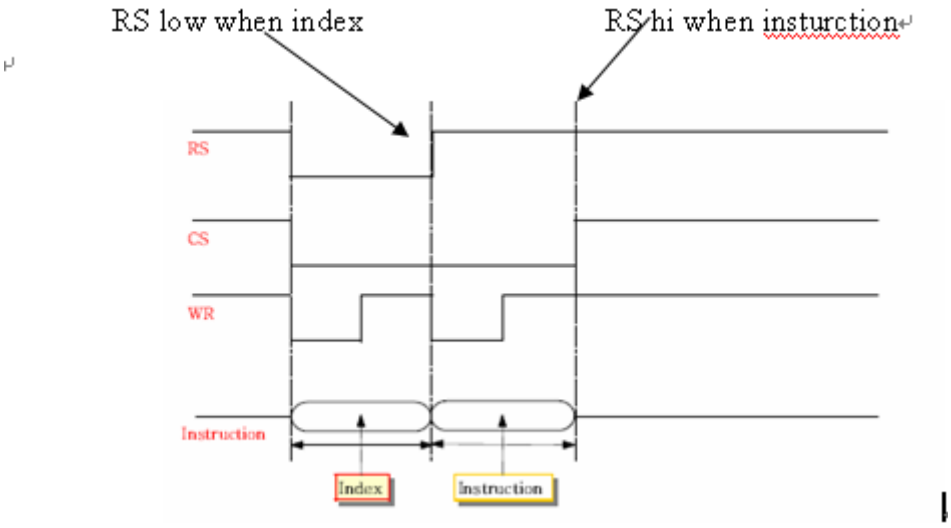
Make a reference to the "Parallel Mode Timing". The only difference between them is: when in serial mode, the RED,GREEN and BLUE ingredients of each pixel should be transmitted in serial (for example, 1st phase R[7..0], 2nd phase G[7..0], 3rd phase B[7..0], so the DCLK frequency will be triple as it is in parallel mode.)

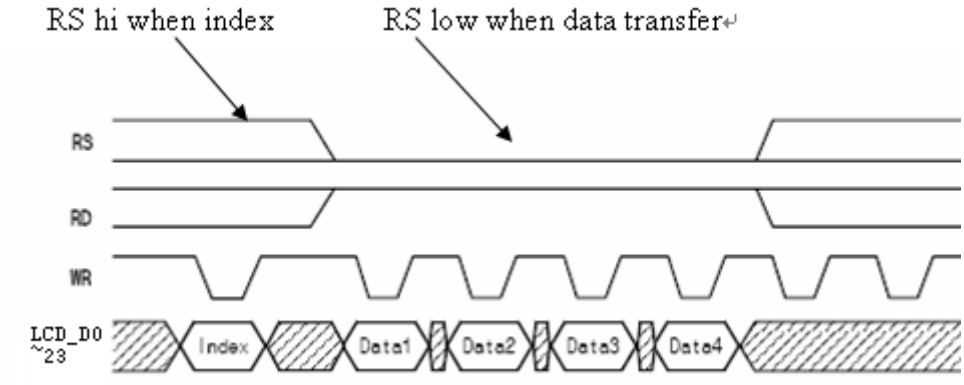
CPU Timing:

Control signal define

RS	R/W	Function
0	0	Sets Index Register
0	1	Read Status
1	0	Writes Instruction
1	1	Reads Instruction

Index/instruction





Framebuffer data

NOTE: the CPU data output timing still has to be embedded in active time, which means even in CPU mode after LCDC received

7.1.3 Registers Description

LCD Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
LCD Control Register	0x102a0000	0xb02a0000

7.1.3.1 LCD_Ctrl0

This register is mainly used to configure the controller to fit the specified RGB IF panel

Lcd_Ctrl0

Offset=0x00

Bits	Name	Description	R/W	Default
31	SEL	LCD interface select 0: RGB interface 1: CPU interface	R/W	0
30:19	Reserved	RESERVED	-	-
18-16	I/F	Panel RGB Interface Type Select 000: 24-bit parallel 001: 18-bit parallel 010: 16-bit(5-6-5 format) parallel 011: 8-color mode parallel 100: 24-bit(8-8-8 format) serial 101: 18-bit(6-6-6 format) serial 110,111: Reserved Note: The unused pins of LD[23..0] should be in stable output state to avoid EMI. For RGB IF only	R/W	0
15:13	CC_ODD	LCD color sequence configuration for odd line 000:RGB 001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other:reserved	R/W	0
12:10	CC_EVEN	LCD color sequence configuration for even line 000: RGB	R/W	0

		001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other:reserved		
09:08	PAD	Color padding to 32 bit/pixel 00: Do not pad 01: Pad X after 10: Pad X before 11: Reserved For example: if CC_ODD=0 and PAD=01, then the serial output should be RGBX. FOR RGB IF ONLY	R/W	0
07:06	VOM	Video Output Mode 00: Reserved 01: Reserved 10: Drive the panel with video from DE 11: Drive the panel with default color	R/W	11
05:02	Reserved	Reserved	-	-
01	RB_SWAP	Swap R,B in input data 0：R,B NO SWAP 1：R,B SWAP	R/W	0
00	EN	LCDC ENABLE RGB IF: When enable, LCDC start RGB IF timing CPU IF: When enable, RD signal become HI	R/W	0

7.1.3.2 LCD_Size

This register is mainly used to configure the size of the LCD.

LCD_Size

Offset=0x04

Bits	Name	Description	R/W	Default
31:26	RESERVED	-	-	-
25:16	Y	Screen Height (in pixels) for RGB IF/ frame size width for CPU IF	R/W	0

		Panel width is Y+1		
15:10	RESERVED	-	-	-
09:00	X	Screen Width (in pixels) for RGB IF/ frame size HEIGHT for CPU IF Panel height is X+1	R/W	0

7.1.3.3 LCD_Status

This register reflects the status of the controller. It also contains the interrupt enable bits

LCD_Status

Offset=0x08

Bits	Name	Description	R/W	Default
31	VBI	Vertical Blanking Interrupt Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period	R/W	0
30	HBI	Horizontal Blanking Interrupt Asserted during horizontal no-display period every scan line. Interrupt triggered at the beginning of blanking period	R/W	0
29	AVSI	Active Video Display Interrupt Asserted during active video display time for each line, Interrupt triggered at the beginning of active period for each line	R/W	0
28:20	-	Reserved	-	-
19:10	CX	Current scan pixel's x axis location (in pixels)	R	0
9:0	CY	Current scan pixel's y axis location (in pixels)	R	0

Note:

The VBI is used for software to reconfigure and start a new DMA transfer when a frame is in its vertical blanking period. When software is interrupted by a VBI, it should reset the DMA , reconfigure and start it. Make sure that the vertical blanking period is long enough for the CPU to process the VBI interrupt routine.

7.1.3.4 LCD_RGBTiming0

This register determines dot clock and output signals' phase. It also can enable/disable the output of the panel driving signals

LCD_Timing0

Offset=0x0C

Bits	Name	Description	R/W	Default
31:8	-	Reserved	-	-
7	Vsync_INV	Vsync Output Polarity Inversion	R/W	0
6	Hsync_INV	Hsync Output Polarity Inversion	R/W	0
5	DCLK_INV	DCLK Output Polarity Inversion	R/W	0
4	LDE_INV	LDE Output Polarity Inversion	R/W	0
3:0	-	Reserved	-	-

Notes:

When we define the timing parameters, it often refers to Tpclk (short for "pixel cycle period"). In parallel output mode, Tpclk = Tdclk; in serial mode, Tpclk = Tdclk * 3.

7.1.3.5 LCD_RGBTiming1

This register specifies timing parameters of the horizontal sync signal

LCD_Timing1

Offset=0x10

Bits	Name	Description	R/W	Default
31:30	-	Reserved	-	-
29:20	HSPW	Horizontal Sync Pulse Width (in pixels) Thspw = (HSPW+1) * Tpclk	R/W	0
19:10	HFP	Horizontal Front Porch (in pixels) Thfp = (HFP +1) * Tpclk	R/W	0
9:0	HBP	Horizontal Back Porch (in pixels) Thbp = (HBP +1) * Tpclk	R/W	0

7.1.3.6 LCD_RGBTiming2

This register specifies timing parameters of the vertical sync signal

LCD_Timing2

Offset=0x14

Bits	Name	Description	R/W	Default
31:29	Reserved	-	-	-
28:20	VSPW	Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Thsync	R/W	0
19:10	VFP	Vertical Front Porch (in lines) Tvfp = (VFP +1) * Thsync	R/W	0
9:0	VBP	Vertical Back Porch (in lines) Tvbp = (VBP +1) * Thsync	R/W	0

7.1.3.7 LCD_Color

This register specifies panel's default color

LCD_Timing2

Offset=0x18

Bits	Name	Description	R/W	Default
31:24	Reserved	-	-	-
23:16	R	Panel's default color R	R/W	0
15:8	G	Panel's default color G	R/W	0
7:0	B	Panel's default color B	R/W	0

7.1.3.8 LCD_CPUCON

CPU LCD INDEX/INSTRUCTION/DATA control resigster

LCD_PWM

Offset=0x20

Bits	Name	Description	R/W	Default
31:11	Reserved	Reserved	-	-
10	RS	RS signal inversed 0: RS low 1: RS high RS is low or high when in index/instruction/data period for different LCD panels.	R/W	0
09:08	WDCS	Write Data/Command Select 00: Index/Instruction command 01: Reserved	R/W	0

		10: RGB Data Transfer 11: Reserved		
07	Reserved	Reserved	-	-
06:04	FORMATS	RGB Format Select: 000: 16bit(RGB 565 1transfer) 001: 18bit(RGB 666 1transfer) 010: 8bit(RGB 565 2transfer) 011: 9bit(RGB 666 2transfer) 100: 8bit(RGB 888 3transfer) 101: 6bit(RGB 666 3transfer) 110: Reserved 111: Reserved	R/W	0
03:01	Reserved	Reserved	-	-
00	ST	Start a index/instruction transmission or a frame's data transmission or disable the circuit 0: Write a 0 to disable the current transmission 1: Write a 1 to start a transmission action	R/W	0

7.1.3.9 LCD_CPUCOM

CPU LCD INDEX/INSTRUCTION command resigster

LCD_PWM

Offset=0x24

Bits	Name	Description	R/W	Default
31:18	Reserved	Reserved	-	-
17:00	COMMAND	Index/instruction command	R/W	0

7.2 HDMI Transmitter

The Whole High Definition Multimedia Interface (HDMI) Module consists of HDMI Video Interface, HDMI Audio Interface, and HDMI Transmitter Core. The HDMI Transmitter Core is a full-function, single-link transmitter with high-bandwidth digital content protection (HDCP), which transmits studio-quality video and/or audio to any HDMI/DVI/HDCP-enabled digital receivers. This module is fully compliant with the HDMI 1.1, DVI 1.0, and HDCP 1.1 specifications.

HDMI's features are:

- Compatible with HDMI 1.1, HDCP1.1 and DVI 1.0

- Support most video formats from 480i to 720p, such as:
  640*480p@59.94/60Hz
  720*480p@59.94/60Hz
  720*576p@50Hz
  1280*720p@59.94/60Hz
  1280*720p@50Hz
  720(1440)*480i@59.94/60Hz
  720(1440)*576i@50Hz
  1440*480p@59.94/60Hz
  1440*576p@50Hz
- Support RGB, YCbCr format
- Support IEC60958 audio format up to 24bits
- Support up to 8-channel Audio sample, supports 32/48/96/44.1/88.2kHz audio sample rate

7.3 TVOUT

The integrated video encoder has the following features:

- Analog CVBS output for SDTV
- Analog YPbPr output for SDTV/EDTV/HDTV
- Support synchronously CVBS,YPbPr and HDMI output for SDTV
- Support synchronously YPbPr and HDMI output for HDTV
- Support 480i/p,576i/p,720p,1080i for YPbPr
- Support NTSC and PAL format for CVBS output

7.4 TVIN

- Support BT656&BT601 Interface

7.4.1 Registers Description

VDI Control Registers Address

Name	Physical Base Address	KSEG1 Base Address
VD/CSI Control Register	0x102b8000	0xb02b8000

VDIController Registers

Offset	Register Name	Description
0x0000	VDCSI_MSR	CSI Mode Select Register
0x0004	VDSCI_FDR	CSI FIFO Data Register
0x0008	CS_CR	CMOS Control Register
0x000C	CS_ADEL_HSP	CMOS Start and Active Data Position
0x0010	CS_ALSPO	CMOS Active Lines Start Position and Size Register, Odd
0x0018	CS_ISR	CMOS IRQ Status Register
0x001C	CS_FCR	CMOS FIFO Control Register

7.4.1.1 VDCSI_MSR

VD/CSI Mode Select Register

Offset = 0x00

Bit(s)	Name	Description	R/W	Reset
31:7	-	Reserved	R	0x0
6:5	DMS	DMA Mode Select 00: Normal mode (4:2:2) 01: YUV 4:2:0 10: YUV 4:2:2 11: Reserved	R/W	0x0
4	CKOE	CLKOUT Enable 0: Disable 1: Enable	R/W	0x0
3		Reserve		
2:1	VFS	Video Source Select 00: Video BT656 01: Video BT601 10: CMOS Sensor 11: Reserve	R/W	0x0
0	IIE	Input Interface Enable 0: Disable 1: Enable	R/W	0x0

Note:

How to set the bit6:5 (DMS) is detailed in chapter 10.4.4.5 and 10.4.4.6

The YUV4:2:2 mode is only used by sensor.

7.4.1.2 VDCSI_FDR

VD/CSI FIFO Data Register

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
31:0	FIFOD	FIFO Data	R	X

7.4.1.3 VDI _CR

VDI/CS Control Register

Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
31:13	-	Reserved	R	0x0
12	RFF	Receive 1 or 2 Field of 1 Frame from external decoder 0: 2 field of 1 frame 1: 1 field of 1 frame (discard the other field)	R/W	0x0
11:10	RDL	Receive the Different Lines according to the following ratio from external decoder 00: 1:1 01: 2:1 (discard the one line from two serial line) 10: 4:1 (discard the one line from four serial line) 11: Reserved	R/W	0x0
9:8	RDD	Receive the Different Data according to the following ratio from external decoder 00: 1:1 01: 2:1 (average the two serial pixels and just reserve the mean value) 10: 4:1 (average the four serial pixels and just reserve the mean value) 11: Reserved	R/W	0x0
7:6	-	Reserved	R	0x0
5	FVS	Vsync or Field select 0: Vsync 1: Field	R/W	0x0

4	HAS	Hsync or Field select 0: Hsync active low 1: Hsync active high	R/W	0x0
3	FVAS	Vsync/Field Active Select 0: Vsync active low or Odd field active low. 1: Vsync active high or Even field active low.	R/W	0x0
2	PAES	PCLK Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	R/W	0x0
1:0		Reserve	R	0x0

7.4.1.4 VDI _ADEL_HSP

VDI/CMOS Start and Active Data Position

Offset = 0x0C

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28:16	ABN	Active Byte Number in Every Line	R/W	X
15:11	-	Reserved	R	0x0
10:0	ABSP	Active Byte Start Position in Every Line	R/W	X

Note:

1. The register is active only for BT.601 format.

2. The ABSP (bit10:0) means the distance between the positive edge of Hsync and the beginning of active data.

3. In YUV 4:2:0 mode, ABN must be set as below.

	RDD=00(1:1)	RDD=01(2:1)	RDD=10(4:1)
ABN	N*64	N*128	N*256

7.4.1.5 VDI _ALSPO

VDI/CMOS Active Line Start Position and Size Register

Offset = 0x10

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved		
28:16	ALOF	Active Lines Number of Odd Field	R/W	X

15:11	-	Reserved		
10:0	ALSPO	Active Line Start Position in Odd field	R/W	X

Note:

1. The register is active only for BT.601 format.
2. The ALSPO (bit10:0) takes count from the active edge of Vsync.

7.4.1.6 VDI_ALSPE

VDI Active Line Start Position and Size (Even Field) Register

Offset = 0x14

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28:16	ALEF	Active Lines Number of Even Field	R/W	X
15:11	-	Reserved	R	0x0
10:0	ALSPE	Active Line Start Position in Even field	R/W	X

Note:

1. The register is active only for BT.601 format.
2. The ALSPE (bit10:0) takes count from the active edge of Vsync.

7.4.1.7 VDI _ISR

VDI/CMOS IRQ Status Register

Offset = 0x18

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FSIM	Finish-flag（every field finish）Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	R/W	0x0
7	SVIM	Vsync Edge or SAV IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	R/W	0x0
6	EVIM	Hsync Edge or EAV IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	R/W	0x0
5	FSIE	Finish-flag IRQ Enable.	R/W	0x0

		0: Disable 1: Enable		
4	SVIE	Vsync Edge or SAV IRQ Enable. 0: Disable 1: Enable	R/W	0x0
3	HEIE	Hsync Edge or EAV IRQ Enable. 0: Disable 1: Enable	R/W	0x0
2	FSIP	Finish-flag IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	R/W	0x0
1	VSIP	Vsync Edge or SAV IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	R/W	0x0
0	HEIP	Hsync Edge or EAV IRQ pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	R/W	0x0

7.4.1.8 VDI/CS_FCR

VDI/CMOS FIFO Control Register

Offset = 0x1C

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FERF	FIFO ERror Flag(if FIFO full and still test the write pointer move, the bit must set to 1) 0: Not error 1: Error Writing 1 to the bit will clear it.	R/W	0x0
7	FEF	FIFO Empty Flag. 0: Not Empty 1: Empty	R	0x1
6	ACS	FIFO Access Channel Select. 0: Special Channel 1: AHB Bus	R/W	0x0

5	FIME	FIFO Full IRQ interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable.	R/W	0x0
4	FDE	FIFO Full DRQ Enable. 0: Disable 1: Enable	R/W	0x0
3	FIE	FIFO Full IRQ Enable. 0: Disable 1: Enable	R/W	0x0
2:1	FFC	FIFO Full Condition. 00: 16/32 Full 01: 20/32 Full 10: 24/32 Full 11: 28/32 Full	R/W	0x1
0	FIP	FIFO Full IRQ Pending bit. Write 1 to the bit, clear the bit. 0: No IRQ 1: IRQ	R/W	0x0

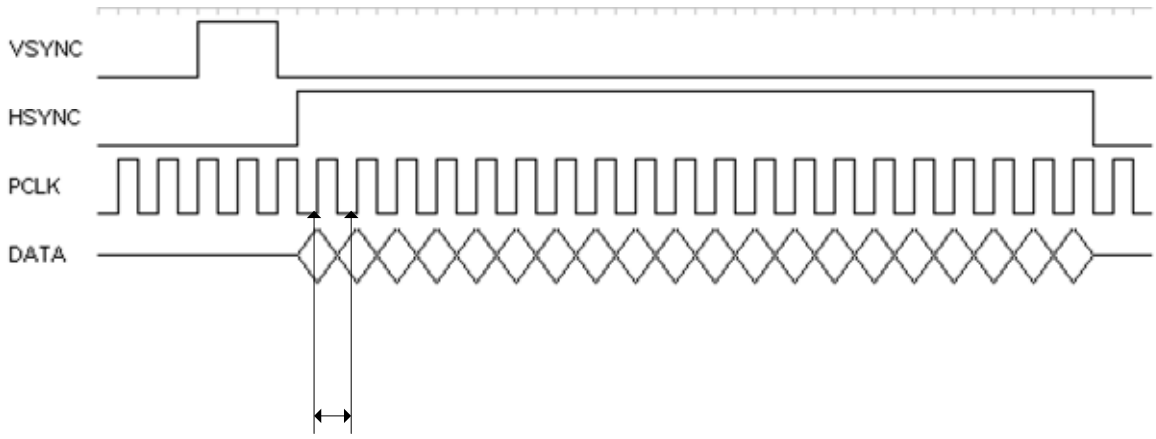
7.5 Sensor

The SENSOR interface support external CMOS sensor which can be used for video recording or photograph. Only the sensor with ISP (Image Signal Processing) is supported.

The sensor's features are

- Support CMOS Sensor which data format is YUV422 or RGB565
- With the CLKOUT for CMOS Sensor(up to 72Mhz)
- Horizontal and vertical subsample is supported
- Maximum resolution is 4096*8192 (in pixels)

Typical timing of CMOS sensor:



T_{min}=13ns

7.5.1 Registers Description

CSI Control Registers Address

Name	Physical Base Address	KSEG1 Base Address
VD/CSI Control Register	0x102b8000	0xb02b8000

VDI Controller Registers

Offset	Register Name	Description
0x0000	VDCSI_MSR	CSI Mode Select Register
0x0004	VDSCI_FDR	CSI FIFO Data Register
0x0008	CS_CR	CMOS Control Register
0x000C	CS_ADEL_HSP	CMOS Start and Active Data Position
0x0010	CS_ALSPO	CMOS Active Lines Start Position and Size Register, Odd
0x0018	CS_ISR	CMOS IRQ Status Register
0x001C	CS_FCR	CMOS FIFO Control Register

7.5.1.1 VDCSI_MSR

VD/CSI Mode Select Register

Offset = 0x00

Bit(s)	Name	Description	R/W	Reset

31:7	-	Reserved	R	0x0
6:5	DMS	DMA Mode Select 00: Normal mode (4:2:2) 01: YUV 4:2:0 10: YUV 4:2:2 11: Reserved	R/W	0x0
4	CKOE	CLKOUT Enable 0: Disable 1: Enable	R/W	0x0
3		Reserve		
2:1	VFS	Video Source Select 00: Video BT656 01: Video BT601 10: CMOS Sensor 11: Reserve	R/W	0x0
0	IIE	Input Interface Enable 0: Disable 1: Enable	R/W	0x0

Note:

1. How to set the bit6:5 (DMS) is detailed in chapter 10.4.4.5 and 10.4.4.6
2. The YUV4:2:2 mode is only used by sensor.

7.5.1.2 VDCSI_FDR

VD/CSI FIFO Data Register

Offset = 0x04

Bit(s)	Name	Description	R/W	Reset
31:0	FIFOD	FIFO Data	R	X

7.5.1.3 CS_CR

CS Control Register

Offset = 0x08

Bit(s)	Name	Description	R/W	Reset
31:12	-	Reserved	R	0x0
11:10	VSbuS	CMOS Sensor input vertical sub-sample ratio	R/W	0x0

		00: 1:1 01: 2:1 10: 4:1 11: Reserved		
9:8	HSubS	CMOS Sensor input horizontal sub-sample ratio 00: 1:1 01: 2:1 10: 4:1 11: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	HAS	Hsync Active Select 0: Hsync active low, Hsync's active pulse is negative 1: Hsync active high, Hsync's active pulse is positive	R/W	0x0
3	VAS	Vsync Active Select 0: Vsync active high, Vsync's active pulse is positive 1: Vsync active low, Vsync's active pulse is negative	R/W	0x0
2	PAES	PCLK Active Edge Select. 0: PCLK positive edge 1: PCLK negative edge.	R/W	0x0
1	PCKO	PCLK output option: 0: PCLK always output 1: No PCLK output when Hsync is active This bit is adapted to CMOS Sensor's setting. Set this bit when all the conditions below are satisfied: a. CMOS Sensor is set to "no PCLK output "(refer to CMOS SENSOR datasheet) b. The end columns are received from CMOS SENSOR.	R/W	0
0	-	Reserve	R	0x0

7.5.1.4 CS_ADEL_HSP

VDI/CMOS Start and Active Data Position

Offset = 0x0C

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28:16	ABN	Active Byte Number in Every Line	R/W	X
15:11	-	Reserved	R	0x0
10:0	ABSP	Active Byte Start Position in Every Line	R/W	X

Note:

1. The ABSP (bit10:0) means the active byte number from the active edge of Hsync. Please reference to the charpter "CMOS Sensor Timming".
2. In YUV 4:2:0 mode, ABN must be set as below.

	HSubS=00(1:1)	HSubS=01(2:1)	HSubS=10(4:1)
ABN	N*64	N*128	N*256

7.5.1.5 CS_ALSPO

VDI/CMOS Active Line Start Position and Size Register

Offset = 0x10

For CMOS Sensor:

Bit(s)	Name	Description	R/W	Reset
31:29	-	Reserved	R	0x0
28:16	ALOF	Active Lines number in Every Frame	R/W	X
15:11	-	Reserved	R	0x0
10:0	ALSPO	Active Line Start Position in Every Frame	R/W	X

Note:

1. The ALSPO (bit10:0) means the active line number from the active edge of Vsync. Please reference to the charpter "CMOS Sensor Timming".

7.5.1.6 CS_ISR

CMOS IRQ Status Register

Offset = 0x18

Bit(s)	Name	Description	R/W	Reset
31:8	-	Reserved	R	0x0
7	VSIM	Vsync Edge IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	R/W	0x0

6	HEIM	Hsync Edge IRQ Interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable	R/W	0x0
5	-	reserved	R	0x0
4	VSIE	Vsync Edge IRQ Enable. 0: Disable 1: Enable	R/W	0x0
3	HEIE	Hsync Edge IRQ Enable. 0: Disable 1: Enable	R/W	0x0
2	-	reserved	R	0x0
1	VSIP	Vsync Edge IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	R/W	0x0
0	HEIP	Hsync Edge IRQ pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	R/W	0x0

7.5.1.7 CS_FCR

CMOS FIFO Control Register

Offset = 0x1C

Bit(s)	Name	Description	R/W	Reset
31:9	-	Reserved	R	0x0
8	FERF	FIFO ERror Flag(if FIFO full and still test the write pointer move, the bit must set to 1) 0: Not error 1: Error Writing 1 to the bit will clear it.	R/W	0x0
7	FEF	FIFO Empty Flag. 0: Not Empty 1: Empty	R	0x1
6	ACS	FIFO Access Channel Select. 0: Special Channel 1: AHB Bus	R/W	0x0

5	FIME	FIFO Full IRQ interrupt Mask Enable. 0: Mask Enable. No Interrupt will occur 1: Mask Disable.	R/W	0x0
4	FDE	FIFO Full DRQ Enable. 0: Disable 1: Enable	R/W	0x0
3	FIE	FIFO Full IRQ Enable. 0: Disable 1: Enable	R/W	0x0
2:1	FFC	FIFO Full Condition. 00: 16/32 Full 01: 20/32 Full 10: 24/32 Full 11: 28/32 Full	R/W	0x1
0	FIP	FIFO Full IRQ Pending bit. Write 1 to the bit, clear the bit. 0: No IRQ 1: IRQ	R/W	0x0

8 Audio In/Out

This unit includes 4 modules: ADC, DAC, I2S and SPDIF.

The DAC module includes a Sigma-Delta DAC and 4 mono 1bit SDM DAC , which can support stereo and 5.1 channel playback. The ADC module supports Microphone/FM input. Both DAC and ADC support 48k/44.1k series sample rate.

It is supported by the DAC on-chip 18mW audio power amplifier with 41 level volume control to drive 16ohm/32ohm earphone.

The I2S module includes Transmitter and Receiver when working in 2.0-Channel Mode, and also supports 5.1-Channel output, just as SPDIF module.

Audio In/Out has the following features:

- Build in 20 bit Sigma-Delta DAC, SNR>93dB, SNR(A-WEIGHTING)>96dB, THD<-85dB
- Build in 21 bit Sigma-Delta ADC, SNR>86dB, SNR(A-WEIGHTING)>89dB, THD<-82dB
- Build in 2*18mW earphone Power Amplify with 41 level volume control
- Support Microphone/FM or Line-in to ADC
- Support 5.1-Channel through I2S Transmitter module with Ext. 6-Channel DAC, include 3-Wire-DOUT Mode and TDM（time-division multiplexed） Mode
- Support 2.0-Channel I2S Transmitter and Receiver
- DAC/ADC/I2S Support sample rate 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/ 8KHz. I2S Transmitter supports sample rate 96k.
- Excluding receiver module, SPDIF only has the transmitter module which supports sample rates 48K/44.1K/32K.

8.1 Module Interface

8.1.1 DAC

The DAC Interface consists of the signals list which is as following:

Signal	Input/Output	Description
AOUTL/R	O	Left/Right Channel Analog Output .
VRO	O	Left/Right Channel 1.5V Voltage Reference Output .

VRO_SENSE	I	Sense of Left/Right Channel 1.5V Voltage Reference Output .

8.1.2 ADC

The ADC Interface consists of the signals list which is as following:

Signal	Input/Output	Description
MICIN	I	Mono Channel Mic Input .
FMINL/R	I	Left/Right Channel FM/Linein Input .

8.1.3 I2S

The I2S Interface consists of the signals list which is as following:

Signal	Input/Output	Description
BCLK	I/O	Continue Serial Clock.
LRCLK	I/O	Left/Right Channel Clock.
MCLK	I/O	Master Clock.
DIN	I	Serial Data in.
DOUT1	O	Serial Data out.
DOUT2/3	O	Serial Data out.

8.2 Characteristics

Test condition:

VCC=3.1V, AVCC=2.9V, VDD=1.3V, AVDD=1.3V, PAVCC=3.09V, Vref=1.5V

When test DAC+PA or PA, test with 16 ohm load.

8.2.1 DAC+PA

DAC+non direct driverPA:

Characteristics	Min	Typical	Max	Unit
Noise		13		uV
SNR		93		dB

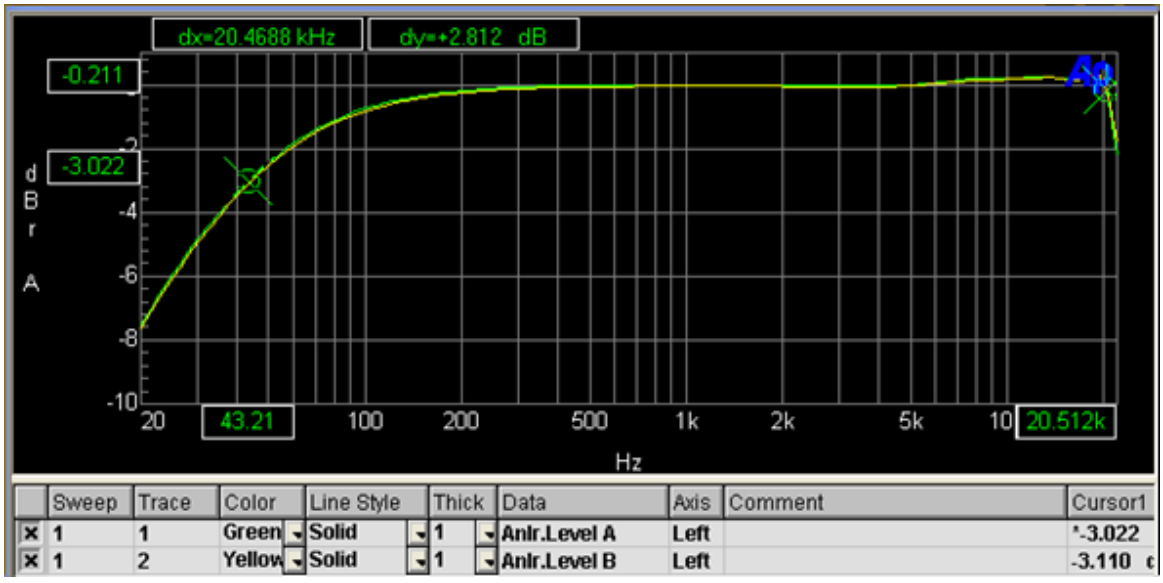
SNR(A-Weighting)		96		dB
Dynamic Range (-48dB Input)		92.5		dB
Dynamic Range (A-Weighting, -48dB Input)		95.5		dB
THD+N (0dB Input)		-85.5		dB
Max Ampl (0dB Input)		562		mV
Max Power		20		mW
Interchannel Isolation (1k,0dB Input)		-88/-78 (L mute/R mute)		dB

DAC+direct driver PA:

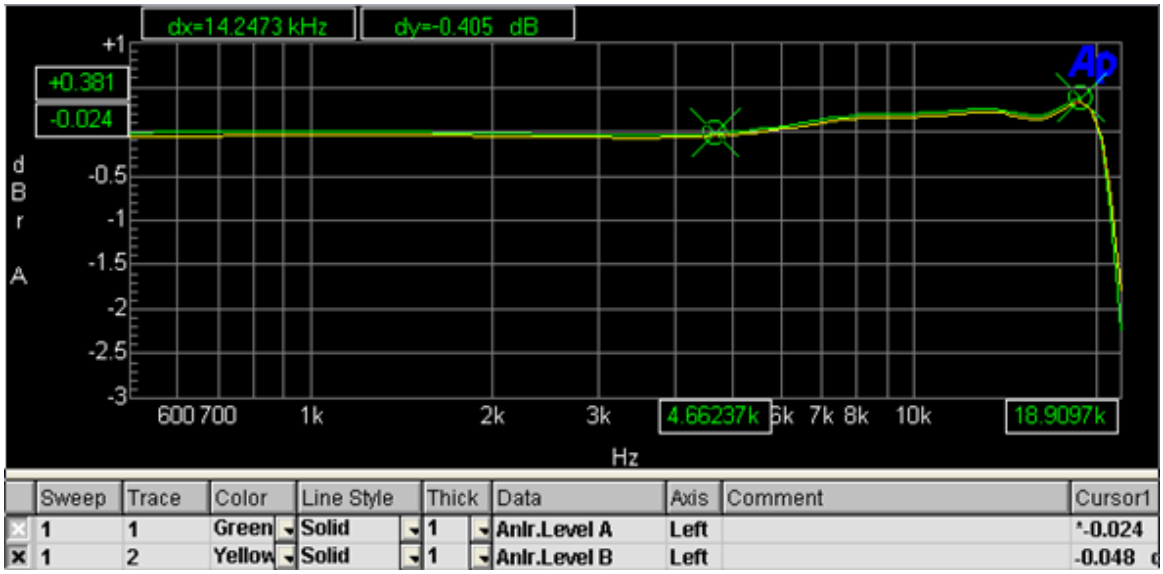
Characteristics	Min	Typical	Max	Unit
Noise		13		uV
SNR		93		dB
SNR(A-Weighting)		95.5		dB
Dynamic Range (-48dB Input)		92.5		dB
Dynamic Range (A-Weighting, -48dB Input)		95		dB
THD+N (0dB Input)		-89		dB
Max Ampl (0dB Input)		580		mV
Max Power		21		mW
Interchannel Isolation (1k,0dB Input)		-61/-61 (L mute/R mute)		dB

Frequency Response:

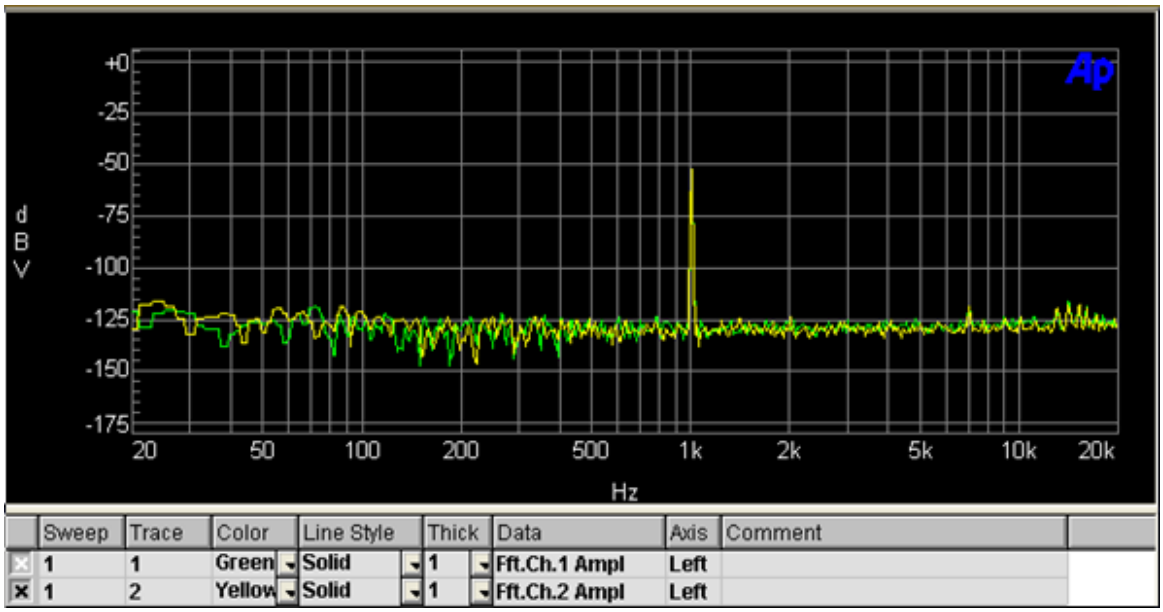
DAC+non direct driver PA:



DAC+ direct driver PA:



FFT:



8.2.2 PA

Non direct driver PA:

Characteristics	Min	Typical	Max	Unit
Noise		9.5		uV
SNR		96		dB

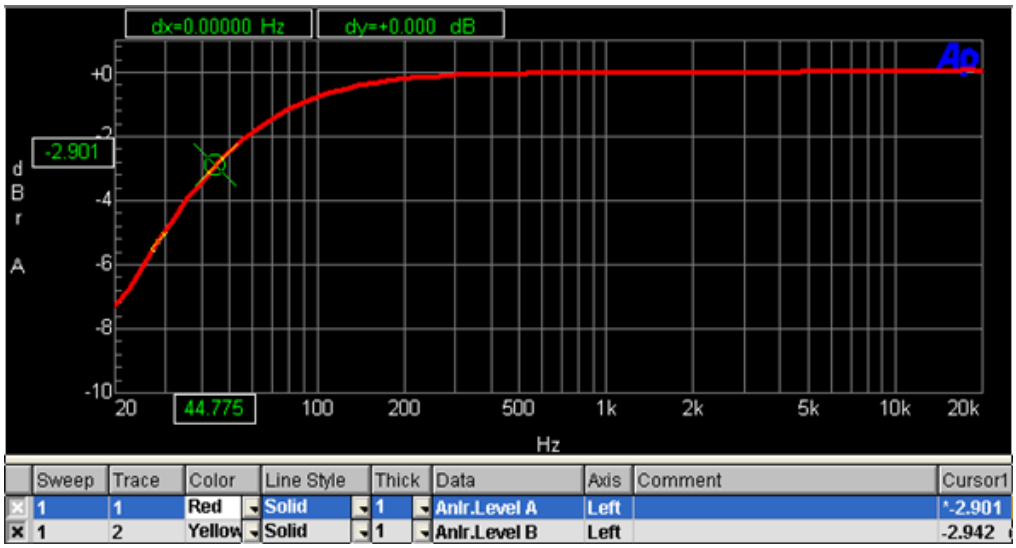
Dynamic Range		96		dB
Total Harmonic Distortion+Noise		-92		dB
Output Common Mode Voltage		1.5		Vrms
Full Scale Output Voltage@-60dB thd+n		0.644Vrms		Vrms
Output Power @16ohm		25.9		mW

Direct driver PA:

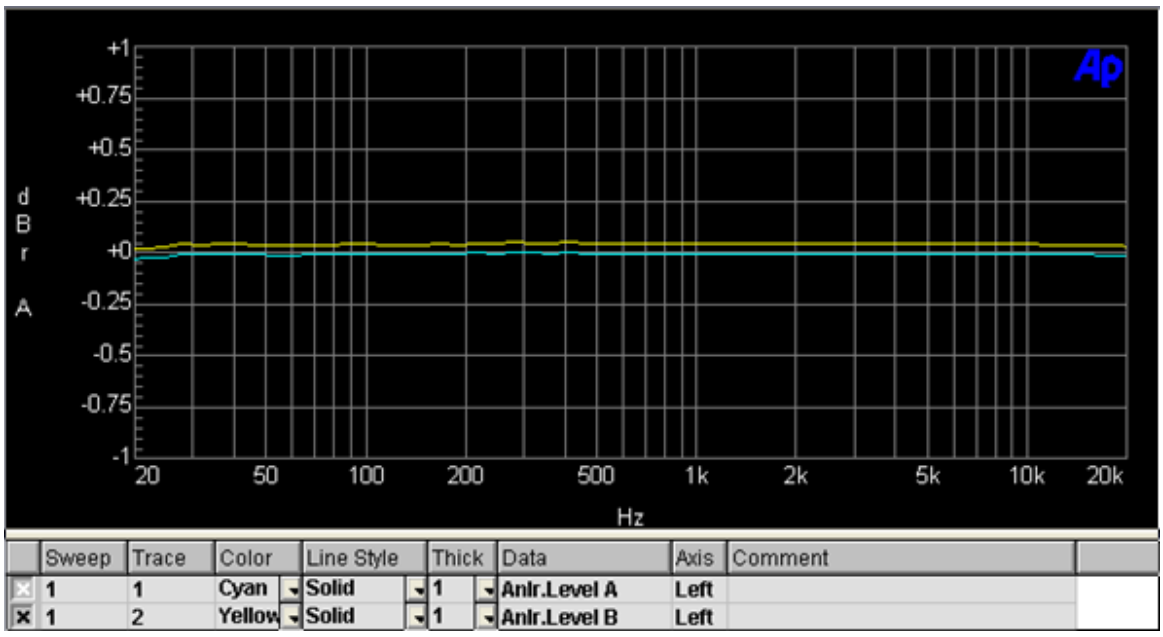
Characteristics	Min	Typical	Max	Unit
Noise		13		uV
SNR		94		dB
Dynamic Range		94		dB
Total Harmonic Distortion+Noise		-91		dB
Output Common Mode Voltage		1.5		Vrms
Full Scale Output Voltage@-60dB thd+n		0.626Vrms		Vrms
Output Power @16ohm		24.5		mW

Frequency Response:

Non direct driver PA:

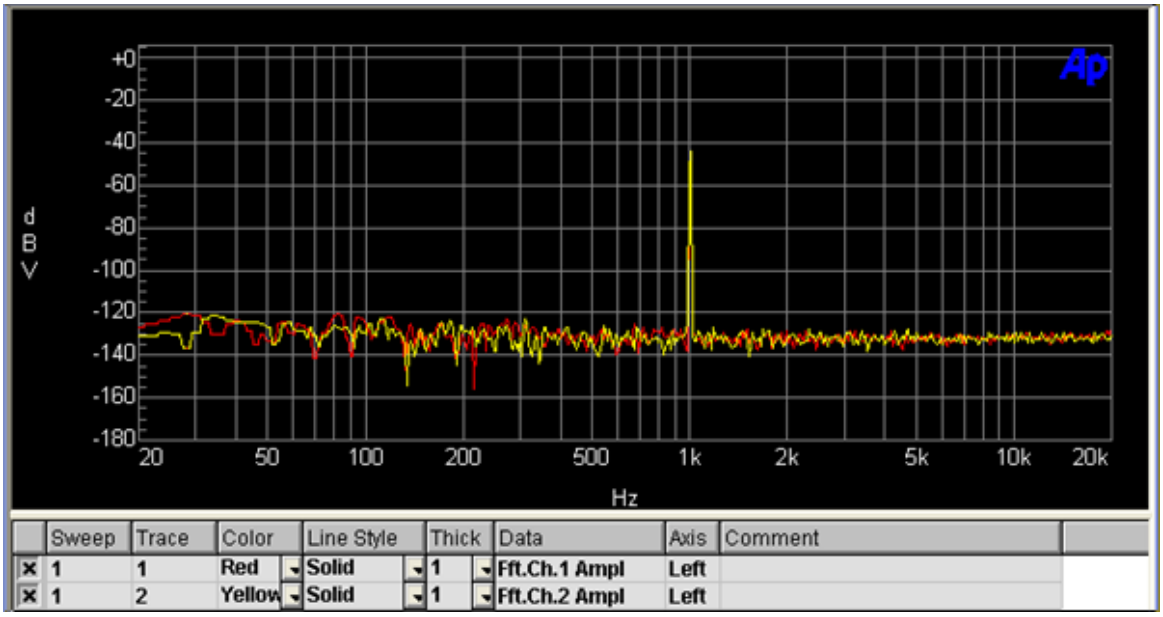


Direct driver PA:

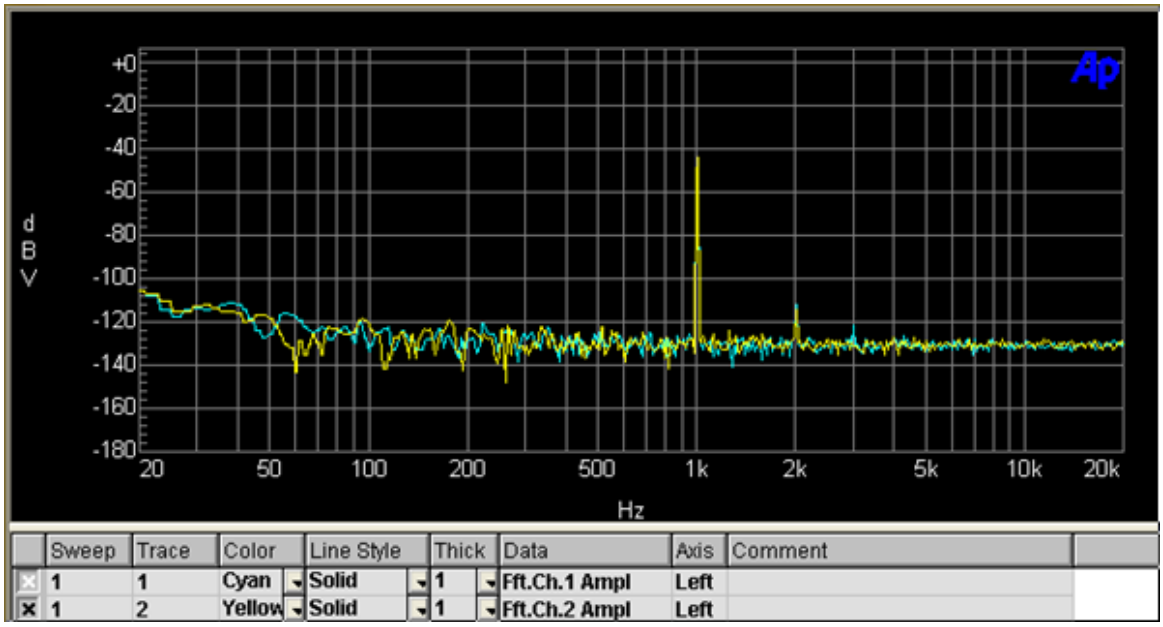


FFT:

Non direct driver PA:

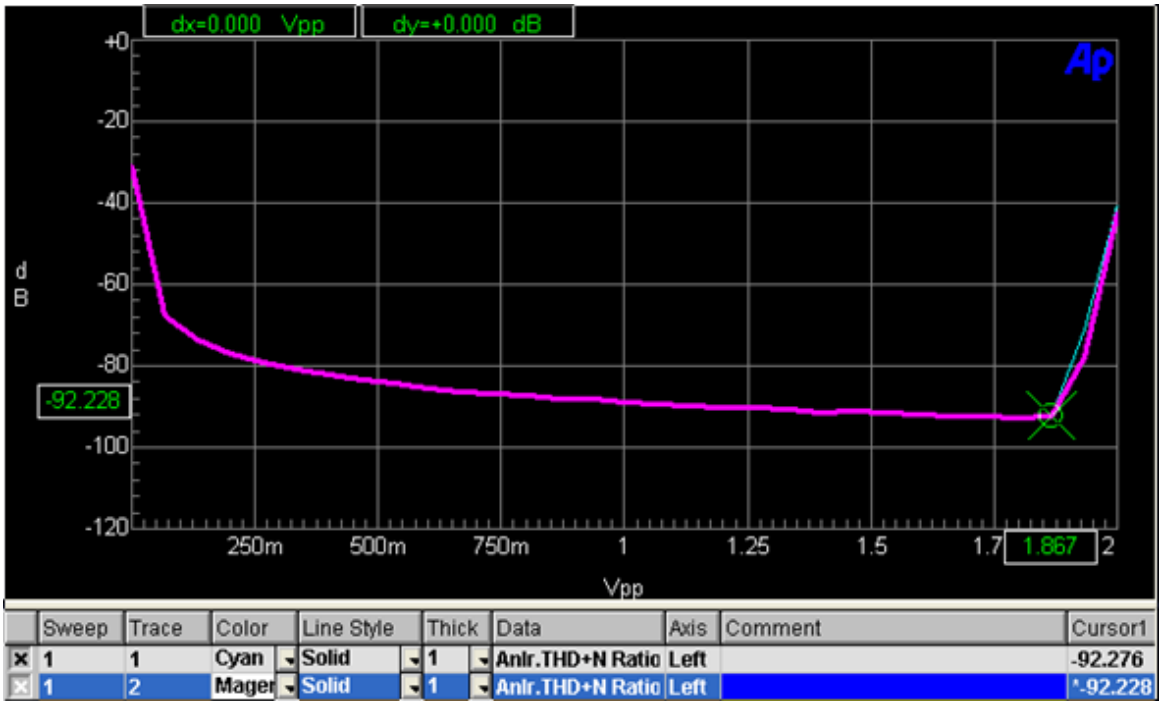


Direct driver PA:

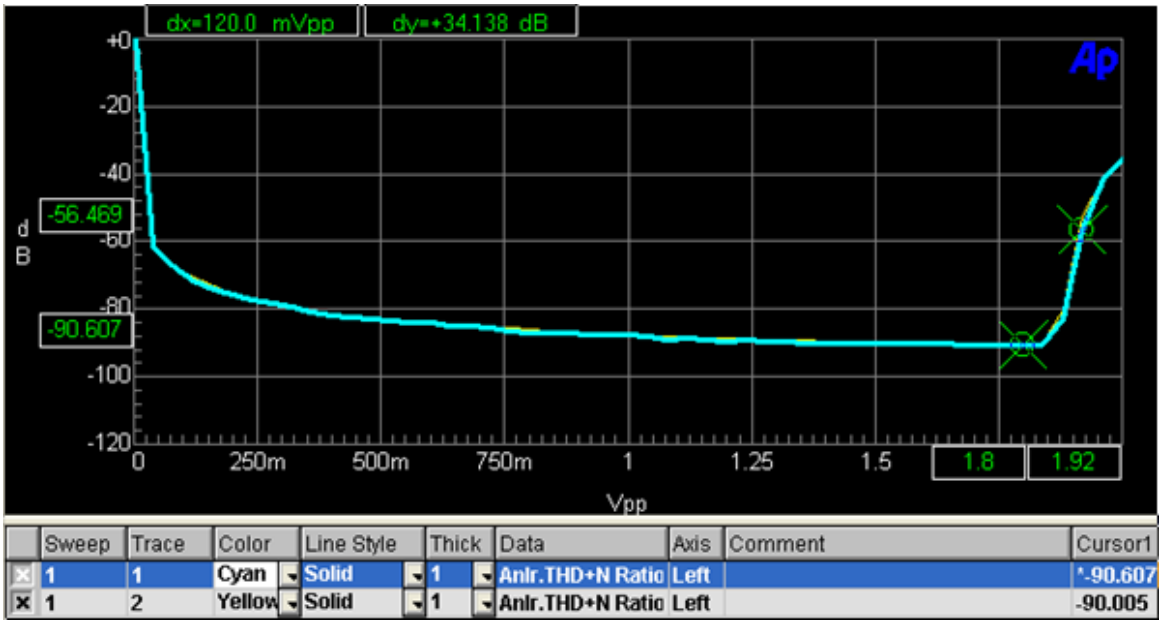


THD+N curve:

Non direct driver PA:



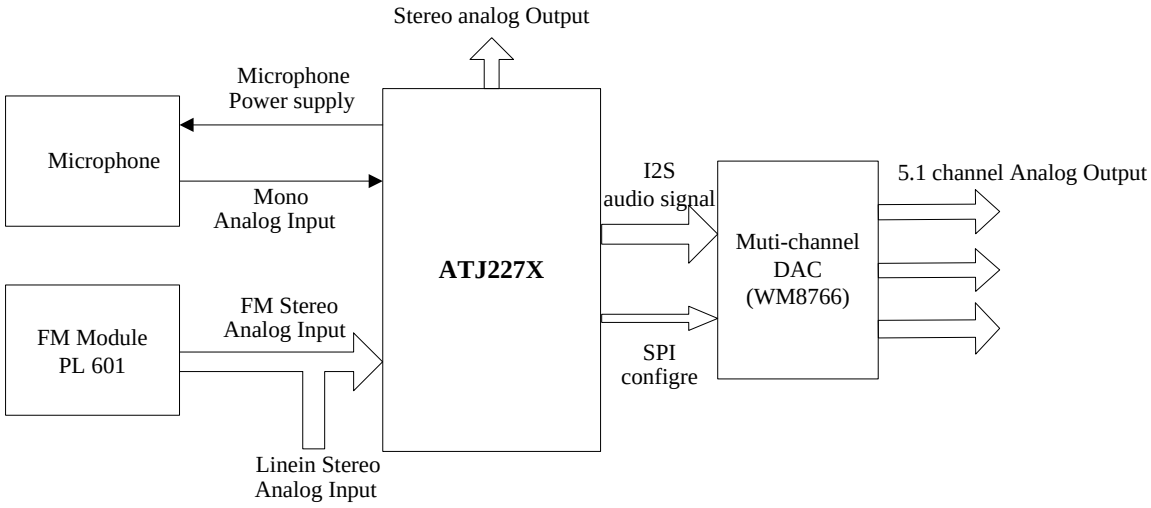
Direct driver PA:



ADC

Characteristics	Min	Typical	Max	Unit
Dynamic Range (10mVpp Input)		86dB@48kSR 87dB@44kSR		dB
Total Harmonic Distortion+Noise		-82.5@44kSR		dB

8.3 Solution Block Diagram



9 RTC

ATJ227X has a low frequency oscillator, which can choose build-in source or external one. It also has a RTC (Real Time Clock) with the alarm IRQ. The alarm IRQ can wake up the system. For protection purpose, the chip also has the watch dog circuit.

- A power supply pin:RTCVDD
- Built-in a 32k oscillator
- Internal or external oscillator optional
- RTC with a alarm IRQ which can wake up the system
- 2Hz IRQ
- 2 Timers with IRQ
- A watch dog which can be configured IRQ or Reset optional
- An S2_timer for status2 switching to status3.

RTC has 6 individual units: 2Hz, Calendar, Alarm, WD, Timer0/1 and S2_Timer. Each module is simply operated.

9.1.1 2HZ

2Hz IRQ will generate every 0.5 second if enable 2HZ. It can be cleared by writing 1 to the bit *2HIP*.

9.1.2 Calendar

When *RTCE*=1, ***RTC_DHMS*** and ***RTC_YMD*** count up with LOSC_CLK1. MCU can read the two registers at any time for getting the real time, but can not write the two registers. When *RTCE*=0, the two registers can be written to set the real time.

9.1.3 Alarm

When *RTCE*=*ALIE*=1, if ***RTC_DHMSALM*=*RTC_DHMS*** and ***RTC_YMDALM*=*RTC_YMD***, Alarm IRQ will generate, It can be cleared by writing 1 to the bit ***ALIP***.

9.1.4 Watch dog

Write 1 to *WDEN* will enable WD. when WD timer overflows, An internal reset or IRQ is generated. An internal reset is generated to force the system into reset status and then reboot.The WD timer overflows interval is set by *CLKSEL*.

Write 1 to *CLR* will clear the WD timer. The *CLR* will be cleared automatically after the WD timer cleared.

Write 1 to *IRQP* will clear the WD IRQ pending.

9.1.5 TIMER0/1

When EN=1, RTC_T0 count down until equal to zero, If ZIEN=1, An IRQ will generate when RTC_T0=0. The IRQ can be cleared by writing 1 to ZIPD.

When EN=0, RTC_T0 can be written, but timer0 do not work.

There are 2 timers: timer0 and timer1, The two timers are the same logic.

9.1.6 S2_TIMER

The duration of sleep mode can be set by the S2_Timer. When the S2_Timer counts up to the settings, Standby Controller will enter the shut-down mode. The S2_Timer can be enabled or disabled.

9.1.7 Register Description

RTC Block Base Address

Name	Physical Base Address	KSEG1 Base Address
RTC	0x10018000	0xB0018000

RTC Block Configuration Registers List

Register Name	Offset	Description
RTC_CTL0	0x0000	RTC Control Register 0
RTC_DHMSALM	0x0004	RTC Day Hour Minute and Second Alarm Register

RTC_YMDALM	0x0008	RTC Year Month Date Alarm Register
RTC_TIMER	0x000C	RTC Timer Register
RTC_CTL1	0x0010	RTC Control Register 1
RTC_DHMS	0x0014	RTC Day Hour Minute and Second Register
RTC_YMD	0x0018	RTC Year Month Date Register
RTC_WDCTL	0x001C	RTC Watch Dog Control register
RTC_T0CTL	0x0020	RTC Timer0 Control register
RTC_T0	0x0024	RTC Timer0 Value
RTC_T1CTL	0x0028	RTC Timer1 Control register
RTC_T1	0x002C	RTC Timer1 Value

NOTE1: After the software writes the registers RTC_DHMS and RTC_YMD, if want to read it out, it is necessary to wait at least for 1s to make sure that the read value is correct.

NOTE2: When Seting the RTC, WD, TIMER0/1, the program must disable the conresponding enable bit at first and then enable it after seting the value.

9.1.7.1 RTC_CTL0

RTC Control Register 0

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:12	-	Reserved	R	0
11	RST	RTC Reset 1: Normal 0: Reset	R/W	1
10	VERI	Rtc Verify Clock Enable Switch RTC clock to 32k 1: Enable 0: Disable	R/W	0
9	LEAP	RTC Leap Year bit 1: leap year 0: not leap year	R	1
8:7	TEST	In test mode, select 4 test clock out to RTC test pad 0: 2Hz 1: 8Hz 2: 128Hz 3: 32KHz	R/W	0
6	EOSC	Signal send to External Crystal OSC	R/W	1
5	CKSS1	LOSC_CLK1 Source Select	R/W	0

		1: External Crystal OSC 0: Build-in OSC		
4	RTCE	RTC Enable 1: Enable 0: Disable	R/W	1
3:0	-	Reserved	R	0

Notes:

1. Bit 5: CKSS1 will only be reset when RTCVDD being cut off of power supply compeletely.
2. The supply of LOSC_CLK1 required Calendar and Alarm modules of precision low frequency CLK, therefore please choose precise External Crystal OSC in application.

9.1.7.2 RTC_DHMSALM

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0
20:16	HOUEAL	Alarm hour setting 00H – 17H	R/W	-
15:14	-	Reserved	R	0
13:8	MINAL	Alarm minute setting 00H – 3BH	R/W	-
7:6	-	Reserved	R	0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	-

9.1.7.3 RTC_YMDALM

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:23	-	Reserved	R	0
22:16	YEARL	Alarm year setting 00H – 63H	R/W	-
15:12	-	Reserved	R	0
11:8	MONAL	Alarm month setting 01H – 0CH	R/W	-
7:5	-	Reserved	R	0

4:0	DATEAL	Alarm day setting 01H – 1FH	R/W	-

9.1.7.4 RTC_TIMER

Set the time interval when S2 switching to S3

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:7	-	Reserved	R	0
6:4	DCOS	Select which Device clk Can be output through pad when debug 0: 4Hz 1: 8Hz 2: 128Hz 3: 512Hz 4: 1KHz 5: 32KHz（for device in VDD） 6: 32KHz（for device in SVDD） 7: NO selected clk	R/W	111
3	CKSS2	LOSC_CLK2 Source Select 1: External Crystal OSC 0: Built-in OSC	R/W	0
2:0	S2_TIMER	S2 to S3 timer 000: 2 minutes 001: 5minutes 010: 10 minutes 011: 15 minutes 100: 30 minutes 101: 60 minutes 110: 90 minutes 111: 120 minutes	R/W	00

Notes:

1. The reset of bit3: CKSS2 has nothing to do with the the power supply cut-off of RTCVDD.
2. LOSC_CLK2 provides with the module which has no precision requirement to CLK, therefore Built-in OSC of not very precious can be selected.

9.1.7.5 RTC_CTL1

RTC Control Register 1

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:4	-	Reserved	R	0
3	2HIE	2Hz IRQ Enable 1: Enable 0: Disable	R/W	0
2	ALIE	Alarm IRQ Enable 1: Enable 0: Dsiable	R/W	0
1	2HIP	2Hz IPQ pending bit, writing 1 to this bit will clear it	R/W	0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	R/W	0

9.1.7.6 RTC_DHMS

Offset=0x0014

Bits	Name	Description	R/W	Reset
31:27	-	Reserved	R	0
26:24	DAY	Time day setting 01H – 07H	R/W	-
23:21	-	Reserved	R	0
20:16	HOUR	Time hour setting 00H – 17H	R/W	-
15:14	-	Reserved	R	0
13:8	MIN	Time minute setting 00H – 3BH	R/W	-
7:6	-	Reserved	R	0
5:0	SEC	Time second setting 00H – 3BH	R/W	-

9.1.7.7 RTC_YMD

Offset=0x0018（RTCVDD）

Bits	Name	Description	R/W	Reset
31	-	Reserved	R	0
30:24	CENT	Time setting 00H – 63H	R/W	-
23	-	Reserved	R	0
22:16	YEAR	Time year setting 00H – 63H	R/W	-
15:12	-	Reserved	R	0
11:8	MON	Time month setting 01H – 0CH	R/W	-
7:5	-	Reserved	R	0
4:0	DATE	Time day setting 01H – 1FH	R/W	-

9.1.7.8 RTC_WDCTL

RTC Watch Dog Control register

Offset=0x001c

Bits	Name	Description	R/W	Reset
31..10	-	Reserved	R	0
9..7	-	Reserved	R	0
6	IRQP	Watch dog IRQ pending bit,writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Irq,1: Reset-. 1: Send Reset signal when watchdog overflow. 0: Send IRQ signal when watchdog overflow.	Rw	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot.	Rw	0
3..1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length 000 1 KHz 176 ms 001 512 Hz 352 ms 010 128 Hz 1.4 s 011 32 Hz 5.6 s 100 8 Hz 22.2 s 101 4 Hz 45 s 110 2 Hz 90 s	Rw	0

		111 1 Hz 180 s		
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0

9.1.7.9 RTC_T0CTL

RTC Timer0 Control register

Offset=0x0020

Bits	Name	Description	R/W	Reset
31..6	-	reserved	R	0
5	EN	Timer 0 Enable 0:Disable,1:Enable	RW	0
4..3	-	Reserved	R	0
2	RELO	Timer 0 Reload. 0:Not reload,1:Reload	RW	0
1	ZIEN	T0 Zero IRQ Enable When this bit is enabled, Timer0_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The timer only can count down

9.1.7.10 RTC_T0

RTC Timer0 value register

Offset=0x0024

Bits	Name	Description	R/W	Reset
31..24	-	Reserved	R	0
23..0	T0	Read or write current Timer0 value	RW	-

9.1.7.11 RTC_T1CTL

RTC Timer1 Control register

Offset=0x0028

Bits	Name	Description	R/W	Reset
31..6	-	Reserved	R	0

5	En	Timer0 Enable 0: Disable,1:Enable	RW	0
4..3	-	reserved	R	0
2	RELO	Timer1 Reload 0: Not reload,1:Reload	RW	0
1	ZIEN	Timer1 Zero IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The timer only can count down.

9.1.7.12 RTC_T1

RTC Timer1 Value register

Offset=0x002c

Bits	Name	Description	R/W	Reset
31..24	-	Reserved		
23..0	T1	Read or write current Timer1 value	RW	0

10 USB

Actions USB2.0 OTG (AOTG) is a Dual-Role-Device (DRD) controller which complies with On-The-Go Supplement to the USB2.0 Specification V1.0a.

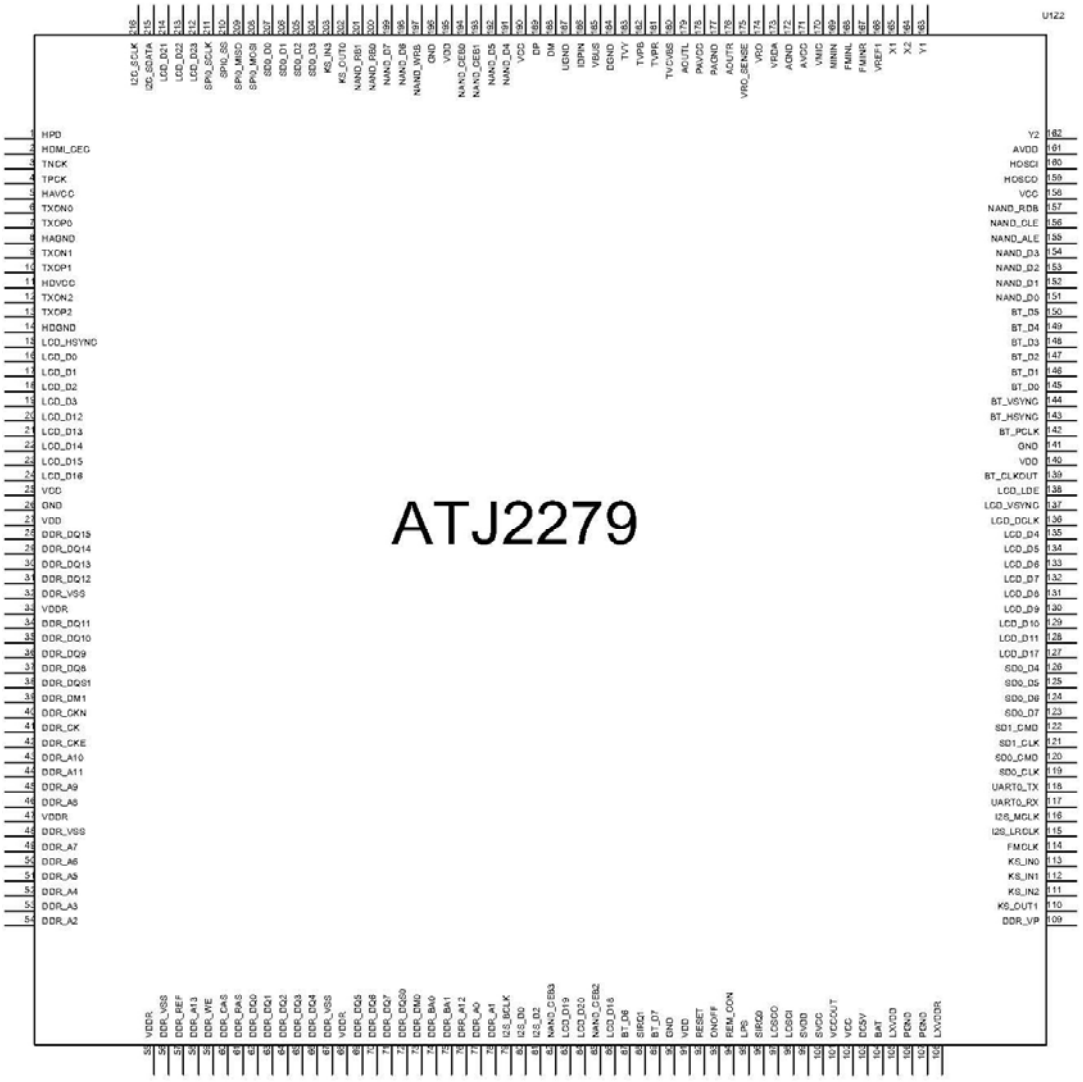
USB has the following features:

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports 2 IN endpoint and 2 OUT endpoint except endpoint0.
- Supports high-speed high-bandwidth Isochronous and Interrupt transfer.
- Partially configurable endpoint buffer size, endpoint type and single, double triple or quad buffering.
- Supports suspend, resume and power managements function.
- Support remote wakeup.

11 Pin Description

11.1 ATJ2279

11.1.1 Pin assignment



11.1.2 Pin Definition

PIN NO.	PIN Name	Function Name	I/O	Description
1	HPD	HPD	I	HDMI Hot Plug Detect
2	CEC	CEC	O	HDMICEC Output
3	TNCK	TNCK	AO	HDMI Differential TMDS Clock Output
4	TPCK	TPCK	AO	HDMI Differential TMDS Clock Output
5	HAVCC	HAVCC	PWRI	HDMI 3.1V Analog IO Power pin
6	TXON0	TXON0	AO	HDMI Channel 0 TMDS Differential Output
7	TXOP0	TXOP0	AO	HDMI Channel 0 TMDS Differential Output
8	HAGND	HAGND	GND	HDMI Analog Ground Pin
9	TXON1	TXON1	AO	HDMI Channel 1 TMDS Differential Output
10	TXOP1	TXOP1	AO	HDMI Channel 1TMDS Differential Output
11	HDVCC	HDVCC	PWRI	HDMI 3.1V digital IO Power pin
12	TXON2	TXON2	AO	HDMI Channel 2 TMDS Differential Output
13	TXOP2	TXOP2	AO	HDMI Channel 2 TMDS Differential Output
14	HDGND	HDGND	GND	HDMI Digital Ground Pin
15	LCD_HSYNC	LCD_HSYNC	O	Horizontal sync for RGB LCD panels.
		CE	O	CE signal of CPU LCD
16	LCD_D0	LCD_D0	O	LCD Data bus, RGB or CPU
17	LCD_D1	LCD_D1	O	LCD Data bus, RGB or CPU
18	LCD_D2	LCD_D2	O	LCD Data bus, RGB or CPU
19	LCD_D3	LCD_D3	O	LCD Data bus, RGB or CPU
20	LCD_D12	LCD_D12	O	LCD Data bus, RGB or CPU
		BT_D2	I/O	BT656 data bus
		LCD_D4	O	LCD Data bus, RGB or CPU
21	LCD_D13	LCD_D13	O	bus interface
		BT_D3	I/O	BT656 data bus
		LCD_D5	O	LCD data enable./WR signal of CPU bus interface
22	LCD_D14	LCD_D14	O	LCD Data bus, RGB or CPU
		BT_D4	I/O	BT656 data bus
		GPIOA26	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
23	LCD_D15	LCD_D15	O	LCD Data bus, RGB or CPU

		BT_D5	I/O	BT656 data bus
		GPIOA27	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
		LCD_D16	O	LCD Data bus, RGB or CPU
		BT_D6	I/O	BT656 data bus
		UART0_TX	O	UART transmit
24	LCD_D16	GPIOA28	IO	General purpose IO
25	VCC	VCC	PWRI	3.1V power supply
26	GND	GND	GND	GND
27	VDD	VDD	PWRI	1.2V power supply
28	DDR_DQ15	DDR_DQ15	I/O	DDR Data bus
29	DDR_DQ14	DDR_DQ14	I/O	DDR Data bus
30	DDR_DQ13	DDR_DQ13	I/O	DDR Data bus
31	DDR_DQ12	DDR_DQ12	I/O	DDR Data bus
32	VSS	VSS	GND	DDR GND
33	VDDR	VDDR	PWRI	DDR VDD
34	DDR_DQ11	DDR_DQ11	I/O	DDR Data bus
35	DDR_DQ10	DDR_DQ10	I/O	DDR Data bus
36	DDR_DQ9	DDR_DQ9	I/O	DDR Data bus
37	DDR_DQ8	DDR_DQ8	I/O	DDR Data bus
38	DDR_DQS1	DDR_DQS1	I	DDR DQS Input
39	DDR_DM1	DDR_DM1	O	DDR DQM output
40	DDR_CKN	DDR_CKN	O	DDR Clock- output
41	DDR_CK	DDR_CK	O	DDR Clock output
42	DDR_CKE	DDR_CKE	O	DDR Clock enable output
43	DDR_A10	DDR_A10	O	DDR Address bus output
44	DDR_A11	DDR_A11	O	DDR Address bus output
45	DDR_A9	DDR_A9	O	DDR Address bus output
46	DDR_A8	DDR_A8	O	DDR Address bus output
47	VDDR	VDDR	PWRI	DDR VDD
48	VSS	VSS	GND	DDR GND
49	DDR_A7	DDR_A7	O	DDR Address bus output
50	DDR_A6	DDR_A6	O	DDR Address bus output
51	DDR_A5	DDR_A5	O	DDR Address bus output
52	DDR_A4	DDR_A4	O	DDR Address bus output

53	DDR_A3	DDR_A3	O	DDR Address bus output
54	DDR_A2	DDR_A2	O	DDR Address bus output
55	VDDR	VDDR	PWRI	DDR VDD
56	VSS	VSS	GND	DDR GND
57	DDR_REF	DDR_REF	I	DDR STTL-2 voltage eference
58	DDR_A13	DDR_A13	O	DDR Address bus output
59	DDR_WRB	DDR_WRB	O	DDR Write output
60	DDR_CASB	DDR_CASB	O	DDR CAS output
61	DDR_RASB	DDR_RASB	O	DDR RAS output
62	DDR_DQ0	DDR_DQ0	I/O	DDR Data bus
63	DDR_DQ1	DDR_DQ1	I/O	DDR Data bus
64	DDR_DQ2	DDR_DQ2	I/O	DDR Data bus
65	DDR_DQ3	DDR_DQ3	I/O	DDR Data bus
66	DDR_DQ4	DDR_DQ4	I/O	DDR Data bus
67	VSS	VSS	GND	DDR GND
68	VDDR	VDDR	PWRI	DDR VDD
69	DDR_DQ5	DDR_DQ5	I/O	DDR Data bus
70	DDR_DQ6	DDR_DQ6	I/O	DDR Data bus
71	DDR_DQ7	DDR_DQ7	I/O	DDR Data bus
72	DDR_DQS0	DDR_DQS0	I	DDR DQS Input
73	DDR_DQM0	DDR_DQM0	O	DDR DQM output
74	DDR_BA0	DDR_BA0	O	DDR BA output
75	DDR_BA1	DDR_BA1	O	DDR BA output
76	DDR_A12	DDR_A12	O	DDR Address bus output
77	DDR_A0	DDR_A0	O	DDR Address bus output
78	DDR_A1	DDR_A1	O	DDR Address bus output
79	I2S_BCLK	I2S_BCLK	O	I2S BCLK
		GPIOB23	I/O	General purpose IO
		SPI1_SS	O	SPI SS output
80	I2S_D0	I2S_DO0	O	I2S Data Output0
		GPIOB25	I/O	General purpose IO
		SPI1_MISO	I/O	SPI MISO
81	I2S_D2	I2S_DO2	O	I2S Data Output2
		SPDIF	O	SPDIF TX
		GPIOA7	I/O	General purpose IO

		BT_CLKOUT	O	BT656 clock output, for sensor
		I2S_DI	I	I2S Data input
		Nand_CEB3	O	NAND Flash CEB3 output
		GPIOA5	I/O	General purpose IO
		UART1_RX	I	UART Receive
82	NAND_CEB3	Nor_CEB3	O	External SRAM Chip Enable
83	LCD_D19	LCD_D19	O	LCD Data bus, RGB or CPU
84	LCD_D20	LCD_D20	O	LCD Data bus, RGB or CPU
		Nand_CEB2	O	Nand Flash CEB2 output
		GPIOA4	I/O	General purpose IO
		UART1_TX	O	UART transmit
85	NAND_CEB2	Nor_CEB2	O	External SRAM Chip Enable
86	LCD_D18	LCD_D18	O	LCD Data bus, RGB or CPU
		BT_D6	I/O	BT656 data bus
		GPIOB12	I/O	General purpose IO
87	BT_D6	Nor_D14	I/O	External SRAM data bus
		SIRQ1	I	External Interrupt signal input
		GPIOA1	I/O	General purpose IO
88	SIRQ1	PWM1	O	Pulse Width Modulation signal output
		BT_D7	I/O	BT656 data bus
		GPIOB13	I/O	General purpose IO
89	BT_D7	Nor_D15	I/O	External SRAM data bus
90	GND	GND	GND	Ground
91	VDD	VDD	PWRI	1.2V power supply
92	RESET	RESET	I	System Reset, active low, Smith trigger
93	ONOFF	ONOFF	I	Standby/wake up signal from on/off key
94	REM_CON	REM_CON	AI	Romont line-in controller input to ADC
95	LPS	LPS	AI	Light photo sensor input
96	SIRQ0	SIRQ0	I	External Interrupt0
97	LOSCO	LOSCO	AO	32.768KHz Crystal Output
98	LOSCI	LOSCI	AI	32.768KHz Crystal input
99	SVDD	SVDD	PWRO	Standby control circuit Power SVDD, always on
100	SVCC	SVCC	PWRO	Standby control circuit Power SVCC, always on
101	VCCOUT	VCCOUT	PWR	VCC power supply, generate by on chip LDO

			O	
102	VCC	VCC	PWRO	VCC power supply, generate by on chip LDO
103	DC5V	DC5V	PWRI	DC5V power; external power supply, from USB or adapter
104	BAT	BAT	PWRI	BAT Power, where the power go into or come out from battery
105	LX_VDD	LX_VDD	PWRO	Buck DC/DC, where to connected with an inductance, source of VDD
106	PGND	PGND	GND	DC/DC GND
107	PGND	PGND	GND	DC/DC GND
108	LX_VDDR	LX_VDDR	PWRO	Buck DC/DC, where to connected with an inductance
109	DDR_VP	DDR_VP	PWRO	DDR power supply from PMU
110	KS_OUT1	KS_OUT1	O	Keyscan output
		GPIOB31	I/O	General purpose IO
111	KS_IN2	KS_IN2	I	Keyscan input
		GPIOB28	I/O	General purpose IO
		PWM2	O	Pulse Width Modulation signal output
112	KS_IN1	KS_IN1	I	Keyscan input
		GPIOB27	I/O	General purpose IO
113	KS_IN0	KS_IN0	I	Keyscan output
		GPIOB26	I/O	General purpose IO
114	FMCLK	FM_CLK	O	Output Clock signal for FM or others
		BT_CLKOUT	O	BT656 clock output, for sensor
115	I2S_LRCLK	I2S_LRCLK	O	I2S LRCLK
		GPIOB24	I/O	General purpose IO
		SPI1_MOSI	I/O	SPI MOSI
116	I2S_MCLK	I2S_MCLK	O	I2S MCLK
		GPIOB22	I/O	General purpose IO
		SPI1_SCLK	O	SPI CLK output
117	UART0_RX	UART0_RX	I	UART Reciever, or infrared remote control input
		GPIOA25	I/O	General purpose IO
		SPI0_SCLK	O	SPI CLK output
		Nor_A21	O	External SRAM address bus

		UART0_TX	O	UART transmit
		GPIOA24	I/O	General purpose IO
		SPI0_MOSI	I/O	SPI MOSI
118	UART0_TX	Nor_A20	O	External SRAM address bus
		SD0_CLKA	O	SDIO0 clock output
		MS_CLK	O	Memory stick clock output
119	SD0_CLK	GPIOA18	I/O	General purpose IO
		SD0_CMD	O	SDIO0 Command output
		MS_BS	O	Memory stick BS output
		GPIOA19	I/O	General purpose IO
120	SD0_CMD	Nor_A22	O	External SRAM address bus
		SD1_CLKA	O	SDIO1 clock output
		GPIOB0	I/O	General purpose IO
121	SD1_CLK	MS_CLK	O	Memory stick clock output
		SD1_CMD	I/O	SDIO1 Command output
		GPIOB1	I/O	General purpose IO
122	SD1_CMD	MS_BS	O	Memory stick BS output
		SD0_D7	I/O	SDIO Data bus
		MS_D7	I/O	Memory stick Date bus
		SD1_D3	I/O	SDIO Data bus
		GPIOA15	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
		Nor_A17	O	External SRAM address bus
123	SD0_D7	MS_D3	I/O	Memory Stick Data bus
		SD0_D6	I/O	SDIO Data bus
		MS_D6	I/O	Memory Stick Data bus
		SD1_D2	I/O	SDIO Data bus
		GPIOA14	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
		Nor_A16	O	External SRAM address bus
124	SD0_D6	MS_D2	I/O	Memory Stick Data bus
125	SD0_D5	SD0_D5	I/O	SDIO Data bus
		MS_D5	I/O	Memory Stick Data bus
		SD1_D1	I/O	SDIO Data bus
		GPIOA13	I/O	General purpose IO

		LCD_D5	O	LCD Data bus, RGB or CPU
		Nor_A15	O	External SRAM address bus
		MS_D1	I/O	Memory Stick Data bus
		SD0_D4	I/O	SDIO Data bus
		MS_D4	I/O	Memory Stick Data bus
		SD1_D0	I/O	SDIO Data bus
		GPIOA12	I/O	General purpose IO
		LCD_D4	O	LCD Data bus, RGB or CPU
		Nor_A14	O	External SRAM address bus
		MS_D0	I/O	Memory Stick Data bus
126	SD0_D4	SD0_D0	I/O	SDIO Data bus
		LCD_D17	O	LCD Data bus, RGB or CPU
		BT_D7	I/O	BT656 data bus
		UART0_RX	I	UART Reciever, or infrared remote control input
127	LCD_D17	GPIOA29	I/O	General purpose IO
		LCD_D11	O	LCD Data bus, RGB or CPU
		BT_D1	I/O	BT656 data bus
128	LCD_D11	LCD_D3	O	LCD Data bus, RGB or CPU
		LCD_D10	O	LCD Data bus, RGB or CPU
		BT_D0	I/O	BT656 data bus
129	LCD_D10	LCD_D2	O	LCD Data bus, RGB or CPU
		LCD_D9	O	LCD Data bus, RGB or CPU
		BT_VSYNC	I/O	BT656 Vsync
130	LCD_D9	LCD_D1	O	LCD Data bus, RGB or CPU
		LCD_D8	O	LCD Data bus, RGB or CPU
		BT_HSYNC	I/O	BT656 Hsync
131	LCD_D8	LCD_D0	O	LCD Data bus, RGB or CPU
132	LCD_D7	LCD_D7	O	LCD Data bus, RGB or CPU
133	LCD_D6	LCD_D6	O	LCD Data bus, RGB or CPU
134	LCD_D5	LCD_D5	O	LCD Data bus, RGB or CPU
135	LCD_D4	LCD_D4	O	LCD Data bus, RGB or CPU
		LCD_DCLK	O	Dot clock for the LCD panels
136	LCD_DCLK	WR	O	WR for CPU bus interface
		LCD_VSYNC	I/O	Vertical sync for LCD panels interface
137	LCD_VSYNC	RS	O	RS signal of CPU bus

		LCD_LDE	O	LCD data enable.
		RD	O	RD signal of CPU bus interface
138	LCD_LDE	BT_PCLK	I	BT656 pixel clock
		BT_CLKOUT	O	BT656 clock output, for sensor
		GPIOB5	I/O	General purpose IO
139	BT_CLKOUT	Nor_A5	O	External SRAM address bus
140	VDD	VDD	PWRI	1.2V supply
141	GND	GND	GND	Ground
		BT_PCLK	I	BT656 pixel clock
		GPIOB2	I/O	General purpose IO
		Nor_A2	O	External SRAM address bus
142	BT_PCLK	LCD_D16	O	LCD Data bus, RGB or CPU
		BT_HSYNC	I/O	BT656 Hsync
		GPIOB3	I/O	General purpose IO
		Nor_A3	O	External SRAM address bus
143	BT_HSYNC	LCD_D15	O	LCD Data bus, RGB or CPU
		BT_VSYNC	I/O	BT656 Vsync
		GPIOB4	I/O	General purpose IO
		Nor_A4	O	External SRAM address bus
144	BT_VSYNC	LCD_D13	O	LCD Data bus, RGB or CPU
		BT_D0	I/O	BT656 data bus
		GPIOB6	I/O	General purpose IO
		Nor_D8	I/O	External SRAM data bus
		PWM0	O	Pulse Width Modulation signal output
		UART1_RX	I	UART receive
145	BT_D0	LCD_D13	O	LCD Data bus, RGB or CPU
		BT_D1	I/O	BT656 data bus
		GPIOB7	I/O	General purpose IO
		Nor_D9	I/O	External SRAM data bus
		PWM1	O	Pulse Width Modulation signal output
		UART1_TX	O	UART transmit
146	BT_D1	LCD_D13	O	LCD Data bus, RGB or CPU
147	BT_D2	BT_D2	I/O	BT656 data bus
		GPIOB8	I/O	General purpose IO
		Nor_D10	I/O	External SRAM data bus

		LCD_D3	O	LCD Data bus, RGB or CPU
148	BT_D3	BT_D3	I/O	BT656 data bus
		GPIOB9	I/O	General purpose IO
		Nor_D11	I/O	External SRAM data bus
		LCD_D2	O	LCD Data bus, RGB or CPU
149	BT_D4	BT_D4	I/O	BT656 data bus
		GPIOB10	I/O	General purpose IO
		Nor_D12	I/O	External SRAM data bus
		LCD_D1	O	LCD Data bus, RGB or CPU
150	BT_D5	BT_D5	I/O	BT656 data bus
		GPIOB11	I/O	General purpose IO
		Nor_D13	I/O	External SRAM data bus
		LCD_D0	O	LCD Data bus, RGB or CPU
151	NAND_D0	Nand_D0	I/O	Nand Flash data bus
		GPIOA10	I/O	General purpose IO
		Nor_D0	I/O	External SRAM data bus
		LCD_D8	O	LCD Data bus, RGB or CPU
		SIRQ1	I	External Interrupt signal input
152	NAND_D1	Nand_D1	I/O	Nand Flash data bus
		GPIOA11	I/O	General purpose IO
		Nor_D1	I/O	External SRAM data bus
		LCD_D9	O	LCD Data bus, RGB or CPU
		PWM1	O	Pulse Width Modulation signal output
153	NAND_D2	Nand_D2	I/O	Nand Flash data bus
		SPI1_SCLK	O	SPI CLK output
		Nor_D2	I/O	External SRAM data bus
		LCD_D10	O	LCD Data bus, RGB or CPU
154	NAND_D3	Nand_D3	I/O	Nand Flash data bus
		SPI1_SS	O	SPI SS output
		Nor_D3	I/O	External SRAM data bus
		LCD_D11	O	LCD Data bus, RGB or CPU
155	NAND_ALE	Nand_ALE	O	Nand Flash address latch enable output
		Nor_A1	O	External SRAM address bus
		SPI0_SCLK	O	SPI CLK output
		LCD_D17	O	LCD Data bus, RGB or CPU

		Nand_CLE	O	Nand Flash command latch enable output
		Nor_A0	O	External SRAM address bus
		SPI0_SS	O	SPI SS output
156	NAND_CLE	LCD_D16	O	LCD Data bus, RGB or CPU
		NAND_RDB	O	Nand Flash read output
		SPI0_MISO	I/O	SPI MISO
		Nor_RD	O	External SRAM read enable, active low
		LCD_VSYNC	O	Vertical sync for RGB LCD panels.
157	NAND_RDB	RS	O	RS signal of LCD CPU bus interface
158	VCC	VCC	PWRI	3.1V
159	HOSCO	HOSCO	AO	24MHz Ccrystal Output
160	HOSCI	HOSCI	AI	24MHz Crystal input
161	AVDD	AVDD	PWRI	1.2V
162	Y2	Y2	AI	Touch Panel Y2
163	Y1	Y1	AI	Touch Panel Y1
164	X2	X2	AI	Touch Panel X2
165	X1	X1	AI	Touch Panel X1
166	VREF	VREF	PWR	Reference Voltage,with capacitance
167	FMINR	FMINR	AI	FM right channel input
168	FMINL	FMINL	AI	FM left channel input
169	MICIN	MICIN	AI	Microphone input
170	VMIC	VMIC	PWR O	The power suppley output for microphone
171	AVCC	AVCC	PWRI	VCC for audio circuit
172	AGND	AGND	GND	GND for audio circuit
173	VRDA	VRDA	AO	Connection with Cap; Just use for DAC Reference voltage
174	VRO	VRO	AO	Direct drive PA reference
175	VROS	VROS	AO	Direct drive PA sense
176	AOUTR	AOUTR	AO	Audio Analog Right channel output
177	PAGND	PAGND	GND	Power Amplify GND
178	PAVCC	PAVCC	PWRI	Power Amplify VCC output; Connection with Cap
179	AOUTL	AOUTL	AO	Audio Analog Left channel output
180	CVBS	CVBS	AO	CVBS Video output
181	Pr	Pr	AO	Pr Video output
182	Pb	Pb	AO	Pb Video output

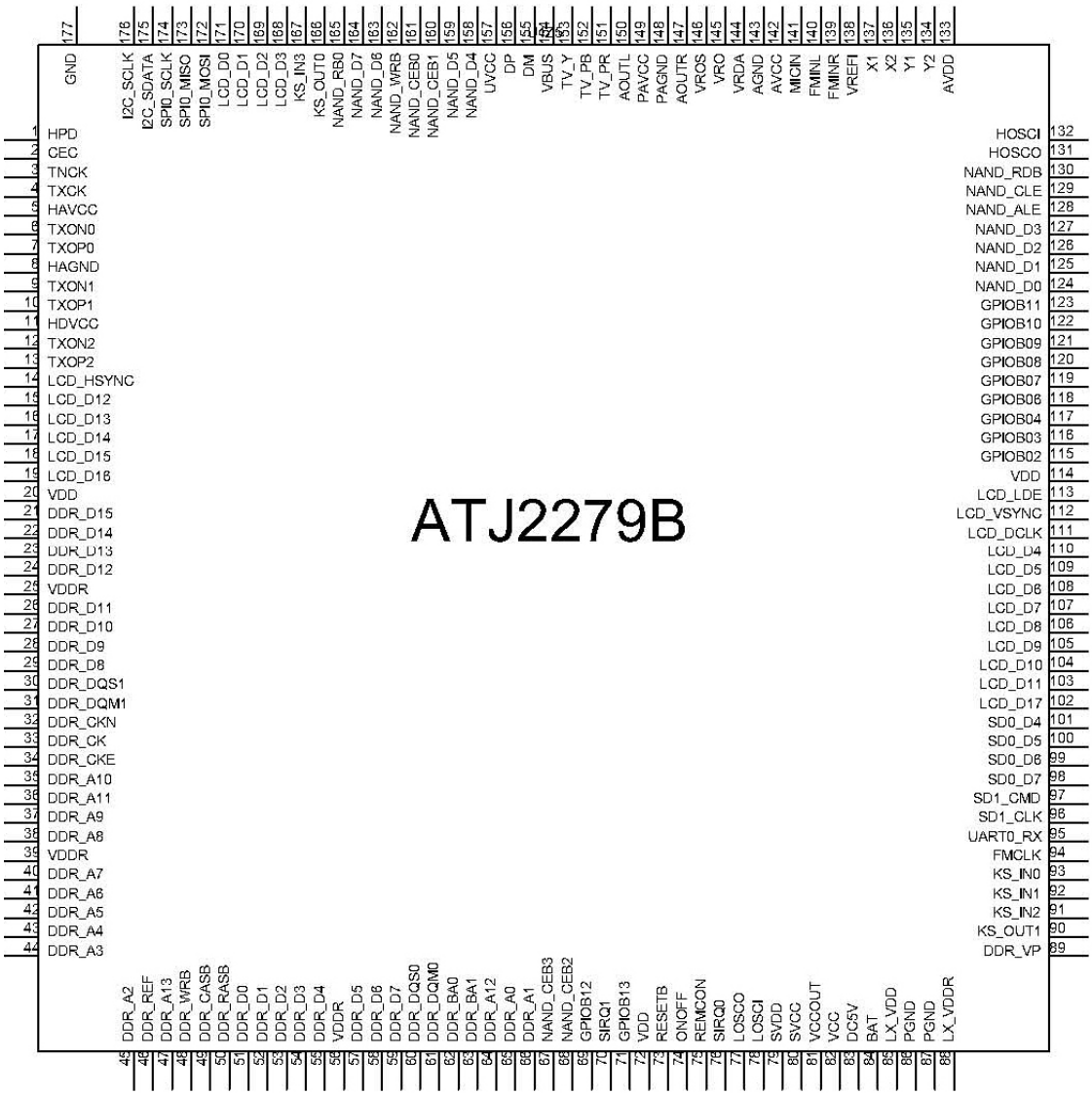
183	Y	Y	AO	Y Video output
184	DGND	DGND	GND	Ground for Video DAC
185	VBUS	VBUS	AI	USB device controller input pins; Detect the voltage for start the state machine
186	IDPIN	IDPIN	I	USB ID
187	UGND	UGND	GND	Ground for USB
188	DM	DM	AO	USB DM
189	DP	DP	AO	USB DP
190	VCC	VCC	PWRI	3.1V supply
191	NAND_D4	Nand_D4	I/O	Nand Flash data bus
		SPI1_MOSI	I/O	SPI MOSI
		Nor_D4	I/O	External SRAM data bus
		LCD_D12	O	LCD Data bus, RGB or CPU
192	NAND_D5	Nand_D5	I/O	Nand Flash data bus
		SPI1_MISO	I/O	SPI MISO
		Nor_D5	I/O	External SRAM data bus
		GPIOA0	I/O	General purpose IO
		LCD_D13	O	LCD Data bus, RGB or CPU
193	NAND_CEB1	Nand_CEB1	O	Nand Flash CEB1 output, boot Flash
		SD1_CLKB	O	SDIO clk output signal
		GPIOA3	I/O	General purpose IO
		Nor_CEB1	O	External SRAM chip enable
194	NAND_CEB0	Nand_CEB0	O	Nand Flash CEB0 output
		SD0_CLKB	O	SDIO clk output signal
		GPIOA2	I/O	General purpose IO
		Nor_CEB0/7	O	External SRAM chip enable
195	VDD	VDD	PWRI	1.2V supply
196	GND	GND	GND	Ground
197	NAND_WRB	NAND_WRB	O	Nand Flash write output
		SPI0_MOSI	I/O	SPI MOSI
		Nor_WR	O	External SRAM write enable, active low
		LCD_DCLK	O	Dot clock for the LCD panels
		WR	O	WR signal of LCD CPU bus interface
198	NAND_D6	Nand_D6	I/O	Nand Flash data bus
		GPIOA16	I/O	General purpose IO

		Nor_D6	I/O	External SRAM data bus
		LCD_D14	O	LCD Data bus, RGB or CPU
199	NAND_D7	Nand_D7	I/O	Nand Flash data bus
		GPIOA17	I/O	General purpose IO
		Nor_D7	I/O	External SRAM data bus
		LCD_D15	O	LCD Data bus, RGB or CPU
200	NAND_RB0	NAND_RB0	I	Nand Flash RB0 input
		GPIOA8	I/O	General purpose IO
		Nor_CEB4	O	External SRAM chip enable
201	NAND_RB1	NAND_RB1	I	Nand Flash RB1 input
		GPIOA9	I/O	General purpose IO
		Nor_CEB5	O	External SRAM chip enable
202	KS_OUT0	KS_OUT0	O	Key scan output
		GPIOB30	I/O	General purpose IO
203	KS_IN3	KS_IN3	I	Key scan input
		GPIOB29	I/O	General purpose IO
		PWM3	O	Pulse Width Modulation signal output
204	SD0_D3	SD0_D3	I/O	SDIO Data bus
		MS_D3	I/O	Memory Stick Data bus
		GPIOA23	I/O	General purpose IO
		LCD_D3	O	LCD Data bus, RGB or CPU
		Nor_A11	O	External SRAM address bus
205	SD0_D2	SD0_D2	I/O	SDIO Data bus
		MS_D2	I/O	Memory Stick Data bus
		GPIOA22	I/O	General purpose IO
		LCD_D2	O	LCD Data bus, RGB or CPU
		Nor_A10	O	External SRAM address bus
206	SD0_D1	SD0_D1	I/O	SDIO Data bus
		MS_D1	I/O	Memory Stick Data bus
		GPIOA21	I/O	General purpose IO
		LCD_D1	O	LCD Data bus, RGB or CPU
		Nor_A9	O	External SRAM address bus
207	SD0_D0	SD0_D0	I/O	SDIO Data bus
		MS_D0	I/O	Memory Stick Data bus
		GPIOA20	I/O	General purpose IO

		LCD_D0	O	LCD Data bus, RGB or CPU
		Nor_A8	O	External SRAM address bus
		SPI0_MOSI	I/O	SPI MOSI
		GPIOB16	I/O	General purpose IO
		UART1_CTSB	I	UART clear to send
		UART0_RX	I	UART Receiver, or infrared remote control input
208	SPI0_MOSI	Nor_A13	O	External SRAM address bus
		SPI0_MISO	I/O	SPI MISO
		GPIOB17	I/O	General purpose IO
		UART1_RX	I	UART receive
209	SPI0_MISO	PWM3	O	Pulse Width Modulation signal output
		SPI0_SS	I/O	SPI SS output
		GPIOB15	I/O	General purpose IO
		UART1_TX	I	UART clear to send
210	SPI0_SS	PWM2	O	Pulse Width Modulation signal output
		SPI0_SCLK	I/O	SPI clock output
		GPIOB14	I/O	General purpose IO
		UART1_RTSB	O	UART request to send
		UART0_TX	O	UART transmit
211	SPI0_SCLK	Nor_A12	O	External SRAM address bus
212	LCD_D23	LCD_D23	O	LCD Data bus, RGB or CPU
213	LCD_D22	LCD_D22	O	LCD Data bus, RGB or CPU
214	LCD_D21	LCD_D21	O	LCD Data bus, RGB or CPU
		I2C_SDATA	I/O	I2C data
		GPIOA31	I/O	General purpose IO
		UART1_TX	O	UART transmit
		Nor_A6	O	External SRAM address bus
215	I2C_SDATA	SPI0_MISO	I/O	SPI MISO
		I2C_SCLK	O	I2C clock output
		GPIOA30	I/O	General purpose IO
		UART1_RX	I	UART receive
		Nor_A7	O	External SRAM address bus
216	I2C_SCLK	SPI0_SS	O	SPI SS output

11.2 ATJ2279B

11.2.1 Pin assignment



11.2.2 Pin Definition

PIN NO.	PIN Name	Function Name	I/O	Description
1	HPD	HPD	I	HDMI Hot Plug Detecte
2	CEC	CEC	O	HDMICEC Output
3	TNCK	TNCK	AO	HDMI Differential TMDS Clock Output
4	TPCK	TPCK	AO	HDMI Differential TMDS Clock Output
5	HAVCC	HAVCC	PWRI	HDMI 3.1V Anolog IO Power pin
6	TXON0	TXON0	AO	HDMI Channel 0 TMDS Differential Output
7	TXOP0	TXOP0	AO	HDMI Channel 0 TMDS Differential Output
8	HAGND	HAGND	GND	HDMI Analog Ground Pin
9	TXON1	TXON1	AO	HDMI Channel 1 TMDS Differential Output
10	TXOP1	TXOP1	AO	HDMI Channel 1TMDS Differential Output
11	HDVCC	HDVCC	PWRI	HDMI 3.1V digital IO Power pin
12	TXON2	TXON2	AO	HDMI Channel 2 TMDS Differential Output
13	TXOP2	TXOP2	AO	HDMI Channel 2 TMDS Differential Output
14	LCD_HSYNC	LCD_HSYNC	O	Horizontal sync for RGB LCD panels.
		CE	O	CE signal of CPU LCD
15	LCD_D12	LCD_D12	O	LCD Data bus, RGB or CPU
		BT_D2	I/O	BT656 data bus
		LCD_D4	O	LCD Data bus, RGB or CPU
16	LCD_D13	LCD_D13	O	bus interface
		BT_D3	I/O	BT656 data bus
		LCD_D5	O	LCD data enable./WR signal of CPU bus interface
17	LCD_D14	LCD_D14	O	LCD Data bus, RGB or CPU
		BT_D4	I/O	BT656 data bus
		GPIOA26	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
18	LCD_D15	LCD_D15	O	LCD Data bus, RGB or CPU
		BT_D5	I/O	BT656 data bus
		GPIOA27	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
19	LCD_D16	LCD_D16	O	LCD Data bus, RGB or CPU
		BT_D6	I/O	BT656 data bus

		UART0_TX	O	UART transive
		GPIOA28	IO	General purpose IO
20	VDD	VDD	PWRI	1.2V power supply
21	DDR_DQ15	DDR_DQ15	I/O	DDR Data bus
22	DDR_DQ14	DDR_DQ14	I/O	DDR Data bus
23	DDR_DQ13	DDR_DQ13	I/O	DDR Data bus
24	DDR_DQ12	DDR_DQ12	I/O	DDR Data bus
25	VDDR	VDDR	PWRI	DDR VDD
26	DDR_DQ11	DDR_DQ11	I/O	DDR Data bus
27	DDR_DQ10	DDR_DQ10	I/O	DDR Data bus
28	DDR_DQ9	DDR_DQ9	I/O	DDR Data bus
29	DDR_DQ8	DDR_DQ8	I/O	DDR Data bus
30	DDR_DQS1	DDR_DQS1	I	DDR DQS Input
31	DDR_DM1	DDR_DM1	O	DDR DQM output
32	DDR_CKN	DDR_CKN	O	DDR Clock- output
33	DDR_CK	DDR_CK	O	DDR Clock output
34	DDR_CKE	DDR_CKE	O	DDR Clock enable output
35	DDR_A10	DDR_A10	O	DDR Address bus output
36	DDR_A11	DDR_A11	O	DDR Address bus output
37	DDR_A9	DDR_A9	O	DDR Address bus output
38	DDR_A8	DDR_A8	O	DDR Address bus output
39	VDDR	VDDR	PWRI	DDR VDD
40	DDR_A7	DDR_A7	O	DDR Address bus output
41	DDR_A6	DDR_A6	O	DDR Address bus output
42	DDR_A5	DDR_A5	O	DDR Address bus output
43	DDR_A4	DDR_A4	O	DDR Address bus output
44	DDR_A3	DDR_A3	O	DDR Address bus output
45	DDR_A2	DDR_A2	O	DDR Address bus output
46	DDR_REF	DDR_REF	I	DDR STTL-2 voltage eference
47	DDR_A13	DDR_A13	O	DDR Address bus output
48	DDR_WRB	DDR_WRB	O	DDR Write output
49	DDR_CASB	DDR_CASB	O	DDR CAS output
50	DDR_RASB	DDR_RASB	O	DDR RAS output
51	DDR_DQ0	DDR_DQ0	I/O	DDR Data bus
52	DDR_DQ1	DDR_DQ1	I/O	DDR Data bus

53	DDR_DQ2	DDR_DQ2	I/O	DDR Data bus
54	DDR_DQ3	DDR_DQ3	I/O	DDR Data bus
55	DDR_DQ4	DDR_DQ4	I/O	DDR Data bus
56	VDDR	VDDR	PWRI	DDR VDD
57	DDR_DQ5	DDR_DQ5	I/O	DDR Data bus
58	DDR_DQ6	DDR_DQ6	I/O	DDR Data bus
59	DDR_DQ7	DDR_DQ7	I/O	DDR Data bus
60	DDR_DQS0	DDR_DQS0	I	DDR DQS Input
61	DDR_DQM0	DDR_DQM0	O	DDR DQM output
62	DDR_BA0	DDR_BA0	O	DDR BA output
63	DDR_BA1	DDR_BA1	O	DDR BA output
64	DDR_A12	DDR_A12	O	DDR Address bus output
65	DDR_A0	DDR_A0	O	DDR Address bus output
66	DDR_A1	DDR_A1	O	DDR Address bus output
67	NAND_CEB3	Nand_CEB3	O	NAND Flash CEB3 output
		GPIOA5	I/O	General purpose IO
		UART1_RX	I	UART Receive
		Nor_CEB3	O	External SRAM Chip Enable
68	NAND_CEB2	Nand_CEB2	O	Nand Flash CEB2 output
		GPIOA4	I/O	General purpose IO
		UART1_TX	O	UART transmit
		Nor_CEB2	O	External SRAM Chip Enable
69	BT_D6	BT_D6	I/O	BT656 data bus
		GPIOB12	I/O	General purpose IO
		Nor_D14	I/O	External SRAM data bus
70	SIRQ1	SIRQ1	I	External Interrupt signal input
		GPIOA1	I/O	General purpose IO
		PWM1	O	Pulse Width Modulation signal output
71	BT_D7	BT_D7	I/O	BT656 data bus
		GPIOB13	I/O	General purpose IO
		Nor_D15	I/O	External SRAM data bus
72	VDD	VDD	PWRI	1.2V power supply
73	RESET	RESET	I	System Reset, active low, Smith trigger
74	ONOFF	ONOFF	I	Standby/wake up signal from on/off key
75	REM_CON	REM_CON	AI	Romont line-in controller input to ADC

76	SIRQ0	SIRQ0	I	External Interrupt0
77	LOSCO	LOSCO	AO	32.768KHz Crystal Output
78	LOSCI	LOSCI	AI	32.768KHz Crystal input
79	SVDD	SVDD	PWRO	Standby control circuit Power SVDD, always on
80	SVCC	SVCC	PWRO	Standby control circuit Power SVCC, always on
81	VCCOUT	VCCOUT	PWRO	VCC power supply, generate by on chip LDO
82	VCC	VCC	PWRO	VCC power supply, generate by on chip LDO
83	DC5V	DC5V	PWRI	DC5V power; external power supply, from USB or adapter
84	BAT	BAT	PWRI	BAT Power, where the power go into or come out from battery
85	LX_VDD	LX_VDD	PWRO	Buck DC/DC, where to connected with an inductance, source of VDD
86	PGND	PGND	GND	DC/DC GND
87	PGND	PGND	GND	DC/DC GND
88	LX_VDDR	LX_VDDR	PWRO	Buck DC/DC, where to connected with an inductance
89	DDR_VP	DDR_VP	PWRO	DDR power supply from PMU
90	KS_OUT1	KS_OUT1	O	Keyscan output
		GPIOB31	I/O	General purpose IO
91	KS_IN2	KS_IN2	I	Keyscan input
		GPIOB28	I/O	General purpose IO
		PWM2	O	Pulse Width Modulation signal output
92	KS_IN1	KS_IN1	I	Keyscan input
		GPIOB27	I/O	General purpose IO
93	KS_IN0	KS_IN0	I	Keyscan output
		GPIOB26	I/O	General purpose IO
94	FMCLK	FM_CLK	O	Output Clock signal for FM or others
		BT_CLKOUT	O	BT656 clock output, for sensor
95	UART0_RX	UART0_RX	I	UART Reciever, or infrared remote control input
		GPIOA25	I/O	General purpose IO
		SPI0_SCLK	O	SPI CLK output
		Nor_A21	O	External SRAM address bus
96	SD1_CLK	SD1_CLKA	O	SDIO1 clock output
		GPIOB0	I/O	General purpose IO
		MS_CLK	O	Memory stick clock output
97	SD1_CMD	SD1_CMD	I/O	SDIO1 Command output

		GPIOB1	I/O	General purpose IO
		MS_BS	O	Memory stick BS output
		SD0_D7	I/O	SDIO Data bus
		MS_D7	I/O	Memory stick Date bus
		SD1_D3	I/O	SDIO Data bus
		GPIOA15	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
		Nor_A17	O	External SRAM address bus
98	SD0_D7	MS_D3	I/O	Memory Stick Data bus
		SD0_D6	I/O	SDIO Data bus
		MS_D6	I/O	Memory Stick Data bus
		SD1_D2	I/O	SDIO Data bus
		GPIOA14	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
		Nor_A16	O	External SRAM address bus
99	SD0_D6	MS_D2	I/O	Memory Stick Data bus
		SD0_D5	I/O	SDIO Data bus
		MS_D5	I/O	Memory Stick Data bus
		SD1_D1	I/O	SDIO Data bus
		GPIOA13	I/O	General purpose IO
		LCD_D5	O	LCD Data bus, RGB or CPU
		Nor_A15	O	External SRAM address bus
100	SD0_D5	MS_D1	I/O	Memory Stick Data bus
		SD0_D4	I/O	SDIO Data bus
		MS_D4	I/O	Memory Stick Data bus
		SD1_D0	I/O	SDIO Data bus
		GPIOA12	I/O	General purpose IO
		LCD_D4	O	LCD Data bus, RGB or CPU
		Nor_A14	O	External SRAM address bus
		MS_D0	I/O	Memory Stick Data bus
101	SD0_D4	SD0_D0	I/O	SDIO Data bus
		LCD_D17	O	LCD Data bus, RGB or CPU
		BT_D7	I/O	BT656 data bus
		UART0_RX	I	UART Reciever, or infrared remote control input
102	LCD_D17	GPIOA29	I/O	General purpose IO

103	LCD_D11	LCD_D11	O	LCD Data bus, RGB or CPU
		BT_D1	I/O	BT656 data bus
		LCD_D3	O	LCD Data bus, RGB or CPU
104	LCD_D10	LCD_D10	O	LCD Data bus, RGB or CPU
		BT_D0	I/O	BT656 data bus
		LCD_D2	O	LCD Data bus, RGB or CPU
105	LCD_D9	LCD_D9	O	LCD Data bus, RGB or CPU
		BT_VSYNC	I/O	BT656 Vsync
		LCD_D1	O	LCD Data bus, RGB or CPU
106	LCD_D8	LCD_D8	O	LCD Data bus, RGB or CPU
		BT_HSYNC	I/O	BT656 Hsync
		LCD_D0	O	LCD Data bus, RGB or CPU
107	LCD_D7	LCD_D7	O	LCD Data bus, RGB or CPU
108	LCD_D6	LCD_D6	O	LCD Data bus, RGB or CPU
109	LCD_D5	LCD_D5	O	LCD Data bus, RGB or CPU
110	LCD_D4	LCD_D4	O	LCD Data bus, RGB or CPU
111	LCD_DCLK	LCD_DCLK	O	Dot clock for the LCD panels
		WR	O	WR for CPU bus interface
112	LCD_VSYNC	LCD_VSYNC	I/O	Vertical sync for LCD panels interface
		RS	O	RS signal of CPU bus
113	LCD_LDE	LCD_LDE	O	LCD data enable.
		RD	O	RD signal of CPU bus interface
		BT_PCLK	I	BT656 pixel clock
114	VDD	VDD	PWRI	1.2V supply
115	BT_PCLK	BT_PCLK	I	BT656 pixel clock
		GPIOB2	I/O	General purpose IO
		Nor_A2	O	External SRAM address bus
		LCD_D16	O	LCD Data bus, RGB or CPU
116	BT_HSYNC	BT_HSYNC	I/O	BT656 Hsync
		GPIOB3	I/O	General purpose IO
		Nor_A3	O	External SRAM address bus
		LCD_D15	O	LCD Data bus, RGB or CPU
117	BT_VSYNC	BT_VSYNC	I/O	BT656 Vsync
		GPIOB4	I/O	General purpose IO
		Nor_A4	O	External SRAM address bus

		LCD_D13	O	LCD Data bus, RGB or CPU
118	BT_D0	BT_D0	I/O	BT656 data bus
		GPIOB6	I/O	General purpose IO
		Nor_D8	I/O	External SRAM data bus
		PWM0	O	Pulse Width Modulation signal output
		UART1_RX	I	UART receive
		LCD_D13	O	LCD Data bus, RGB or CPU
119	BT_D1	BT_D1	I/O	BT656 data bus
		GPIOB7	I/O	General purpose IO
		Nor_D9	I/O	External SRAM data bus
		PWM1	O	Pulse Width Modulation signal output
		UART1_TX	O	UART transmit
		LCD_D13	O	LCD Data bus, RGB or CPU
120	BT_D2	BT_D2	I/O	BT656 data bus
		GPIOB8	I/O	General purpose IO
		Nor_D10	I/O	External SRAM data bus
		LCD_D3	O	LCD Data bus, RGB or CPU
121	BT_D3	BT_D3	I/O	BT656 data bus
		GPIOB9	I/O	General purpose IO
		Nor_D11	I/O	External SRAM data bus
		LCD_D2	O	LCD Data bus, RGB or CPU
122	BT_D4	BT_D4	I/O	BT656 data bus
		GPIOB10	I/O	General purpose IO
		Nor_D12	I/O	External SRAM data bus
		LCD_D1	O	LCD Data bus, RGB or CPU
123	BT_D5	BT_D5	I/O	BT656 data bus
		GPIOB11	I/O	General purpose IO
		Nor_D13	I/O	External SRAM data bus
		LCD_D0	O	LCD Data bus, RGB or CPU
124	NAND_D0	Nand_D0	I/O	Nand Flash data bus
		GPIOA10	I/O	General purpose IO
		Nor_D0	I/O	External SRAM data bus
		LCD_D8	O	LCD Data bus, RGB or CPU
		SIRQ1	I	External Interrupt signal input
125	NAND_D1	Nand_D1	I/O	Nand Flash data bus

		GPIOA11	I/O	General purpose IO
		Nor_D1	I/O	External SRAM data bus
		LCD_D9	O	LCD Data bus, RGB or CPU
		PWM1	O	Pulse Width Modulation signal output
126	NAND_D2	Nand_D2	I/O	Nand Flash data bus
		SPI1_SCLK	O	SPI CLK output
		Nor_D2	I/O	External SRAM data bus
		LCD_D10	O	LCD Data bus, RGB or CPU
127	NAND_D3	Nand_D3	I/O	Nand Flash data bus
		SPI1_SS	O	SPI SS output
		Nor_D3	I/O	External SRAM data bus
		LCD_D11	O	LCD Data bus, RGB or CPU
128	NAND_ALE	Nand_ALE	O	Nand Flash address latch enable output
		Nor_A1	O	External SRAM address bus
		SPI0_SCLK	O	SPI CLK output
		LCD_D17	O	LCD Data bus, RGB or CPU
129	NAND_CLE	Nand_CLE	O	Nand Flash command latch enable output
		Nor_A0	O	External SRAM address bus
		SPI0_SS	O	SPI SS output
		LCD_D16	O	LCD Data bus, RGB or CPU
130	NAND_RDB	NAND_RDB	O	Nand Flash read output
		SPI0_MISO	I/O	SPI MISO
		Nor_RD	O	External SRAM read enable, active low
		LCD_VSYNC	O	Vertical sync for RGB LCD panels.
		RS	O	RS signal of LCD CPU bus interface
131	HOSCO	HOSCO	AO	24MHz Ccrystal Output
132	HOSCI	HOSCI	AI	24MHz Crystal input
133	AVDD	AVDD	PWRI	1.2V
134	Y2	Y2	AI	Touch Panel Y2
135	Y1	Y1	AI	Touch Panel Y1
136	X2	X2	AI	Touch Panel X2
137	X1	X1	AI	Touch Panel X1
138	VREF	VREF	PWR	Reference Voltage,with capacitance
139	FMINR	FMINR	AI	FM right channel input
140	FMINL	FMINL	AI	FM left channel input

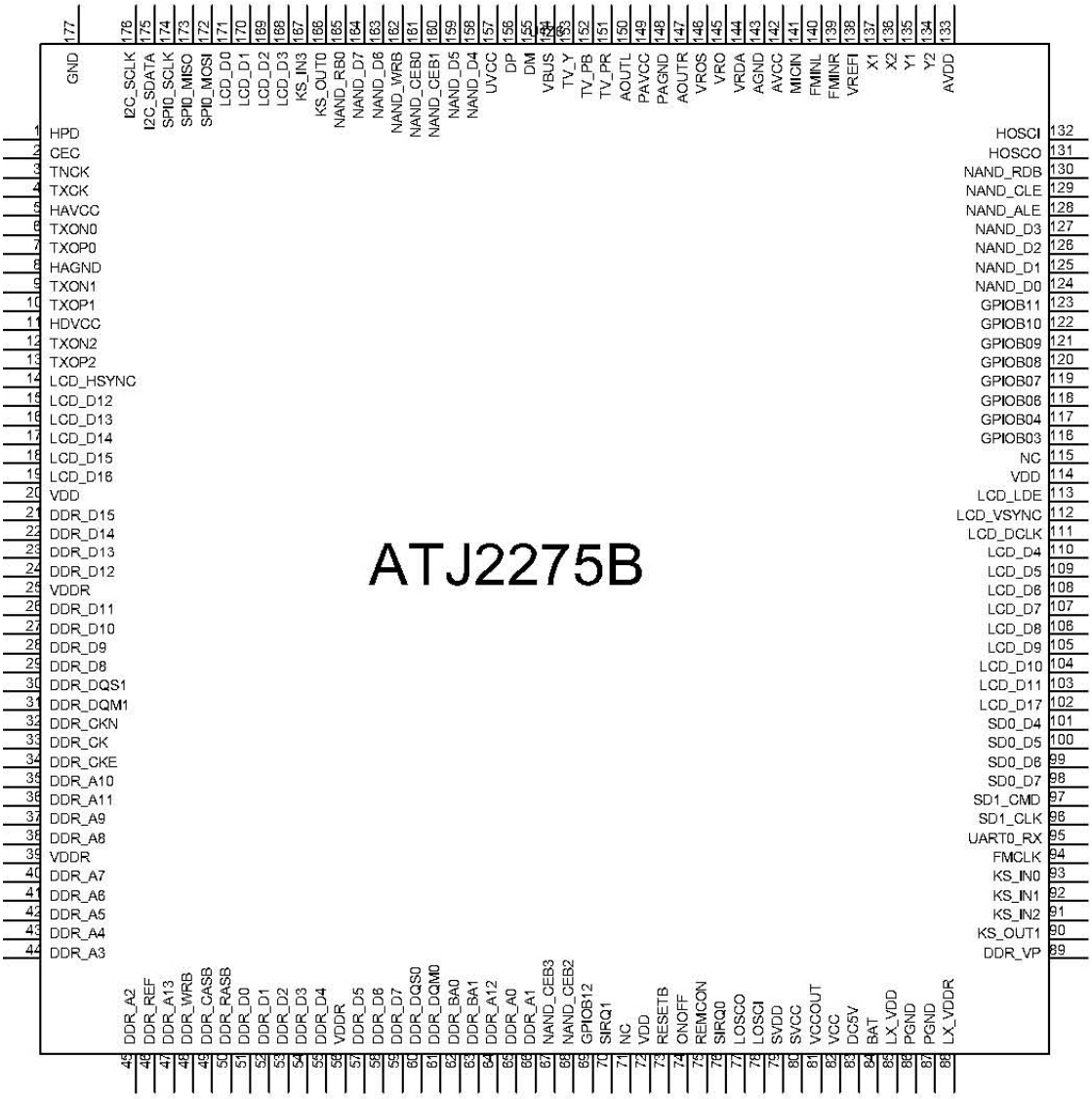
141	MICIN	MICIN	AI	Microphone input
142	AVCC	AVCC	PWRI	VCC for audio circuit
143	AGND	AGND	GND	GND for audio circuit
144	VRDA	VRDA	AO	Connection with Cap; Just use for DAC Reference voltage
145	VRO	VRO	AO	Direct drive PA reference
146	VROS	VROS	AO	Direct drive PA sense
147	AOUTR	AOUTR	AO	Audio Analog Right channel output
148	PAGND	PAGND	GND	Power Amplify GND
149	PAVCC	PAVCC	PWRI	Power Amplify VCC output; Connection with Cap
150	AOUTL	AOUTL	AO	Audio Analog Left channel output
151	Pr	Pr	AO	Pr Video output
152	Pb	Pb	AO	Pb Video output
153	Y	Y	AO	Y Video output
154	VBUS	VBUS	AI	USB device controller input pins; Detect the voltage for start the state machine
155	DM	DM	AO	USB DM
156	DP	DP	AO	USB DP
157	VCC	VCC	PWRI	3.1V supply
158	NAND_D4	Nand_D4	I/O	Nand Flash data bus
		SPI1_MOSI	I/O	SPI MOSI
		Nor_D4	I/O	External SRAM data bus
		LCD_D12	O	LCD Data bus, RGB or CPU
159	NAND_D5	Nand_D5	I/O	Nand Flash data bus
		SPI1_MISO	I/O	SPI MISO
		Nor_D5	I/O	External SRAM data bus
		GPIOA0	I/O	General purpose IO
		LCD_D13	O	LCD Data bus, RGB or CPU
160	NAND_CEB1	Nand_CEB1	O	Nand Flash CEB1 output, boot Flash
		SD1_CLKB	O	SDIO clk output signal
		GPIOA3	I/O	General purpose IO
		Nor_CEB1	O	External SRAM chip enable
161	NAND_CEB0	Nand_CEB0	O	Nand Flash CEB0 output
		SD0_CLKB	O	SDIO clk output signal
		GPIOA2	I/O	General purpose IO
		Nor_CEB0/7	O	External SRAM chip enable

		NAND_WRB	O	Nand Flash write output
		SPI0_MOSI	I/O	SPI MOSI
		Nor_WR	O	External SRAM write enable, active low
		LCD_DCLK	O	Dot clock for the LCD panels
162	NAND_WRB	WR	O	WR signal of LCD CPU bus interface
		Nand_D6	I/O	Nand Flash data bus
		GPIOA16	I/O	General purpose IO
		Nor_D6	I/O	External SRAM data bus
163	NAND_D6	LCD_D14	O	LCD Data bus, RGB or CPU
		Nand_D7	I/O	Nand Flash data bus
		GPIOA17	I/O	General purpose IO
		Nor_D7	I/O	External SRAM data bus
164	NAND_D7	LCD_D15	O	LCD Data bus, RGB or CPU
		NAND_RB0	I	Nand Flash RB0 input
		GPIOA8	I/O	General purpose IO
165	NAND_RB0	Nor_CEB4	O	External SRAM chip enable
		KS_OUT0	O	Keyscan output
166	KS_OUT0	GPIOB30	I/O	General purpose IO
		KS_IN3	I	Keyscan input
		GPIOB29	I/O	General purpose IO
167	KS_IN3	PWM3	O	Pulse Width Modulation signal output
		SD0_D3	I/O	SDIO Data bus
		MS_D3	I/O	Memory Stick Data bus
		GPIOA23	I/O	General purpose IO
		LCD_D3	O	LCD Data bus, RGB or CPU
168	LCD_D3	Nor_A11	O	External SRAM address bus
		SD0_D2	I/O	SDIO Data bus
		MS_D2	I/O	Memory Stick Data bus
		GPIOA22	I/O	General purpose IO
		LCD_D2	O	LCD Data bus, RGB or CPU
169	LCD_D2	Nor_A10	O	External SRAM address bus
170	LCD_D1	SD0_D1	I/O	SDIO Data bus
		MS_D1	I/O	Memory Stick Data bus
		GPIOA21	I/O	General purpose IO
		LCD_D1	O	LCD Data bus, RGB or CPU

		Nor_A9	O	External SRAM address bus
171	LCD_D0	SD0_D0	I/O	SDIO Data bus
		MS_D0	I/O	Memory Stick Data bus
		GPIOA20	I/O	General purpose IO
		LCD_D0	O	LCD Data bus, RGB or CPU
		Nor_A8	O	External SRAM address bus
172	SPI0_MOSI	SPI0_MOSI	I/O	SPI MOSI
		GPIOB16	I/O	General purpose IO
		UART1_CTSB	I	UART clear to send
		UART0_RX	I	UART Reciever, or infrared remote control input
		Nor_A13	O	External SRAM address bus
173	SPI0_MISO	SPI0_MISO	I/O	SPI MISO
		GPIOB17	I/O	General purpose IO
		UART1_RX	I	UART receive
		PWM3	O	Pulse Width Modulation signal output
174	SPI0_SCLK	SPI0_SCLK	I/O	SPI clock output
		GPIOB14	I/O	General purpose IO
		UART1_RTSB	O	UART request to send
		UART0_TX	O	UART transmite
		Nor_A12	O	External SRAM address bus
175	I2C_SDATA	I2C_SDATA	I/O	I2C data
		GPIOA31	I/O	General purpose IO
		UART1_TX	O	UART transmite
		Nor_A6	O	External SRAM address bus
		SPI0_MISO	I/O	SPI MISO
176	I2C_SCLK	I2C_SCLK	O	I2C clock output
		GPIOA30	I/O	General purpose IO
		UART1_RX	I	UART receive
		Nor_A7	O	External SRAM address bus
		SPI0_SS	O	SPI SS output
177	GND	GND	GND	Ground

11.3 ATJ2275B

11.3.1 Pin assignment



11.3.2 Pin Definition

PIN NO.	PIN Name	Function Name	I/O	Description
1	HPD	HPD	I	HDMI Hot Plug Detecte
2	CEC	CEC	O	HDMICEC Output
3	TNCK	TNCK	AO	HDMI Differential TMDS Clock Output
4	TPCK	TPCK	AO	HDMI Differential TMDS Clock Output
5	HAVCC	HAVCC	PWRI	HDMI 3.1V Anolog IO Power pin
6	TXON0	TXON0	AO	HDMI Channel 0 TMDS Differential Output
7	TXOP0	TXOP0	AO	HDMI Channel 0 TMDS Differential Output
8	HAGND	HAGND	GND	HDMI Analog Ground Pin
9	TXON1	TXON1	AO	HDMI Channel 1 TMDS Differential Output
10	TXOP1	TXOP1	AO	HDMI Channel 1TMDS Differential Output
11	HDVCC	HDVCC	PWRI	HDMI 3.1V digital IO Power pin
12	TXON2	TXON2	AO	HDMI Channel 2 TMDS Differential Output
13	TXOP2	TXOP2	AO	HDMI Channel 2 TMDS Differential Output
14	LCD_HSYNC	LCD_HSYNC	O	Horizontal sync for RGB LCD panels.
		CE	O	CE signal of CPU LCD
15	LCD_D12	LCD_D12	O	LCD Data bus, RGB or CPU
		BT_D2	I/O	BT656 data bus
		LCD_D4	O	LCD Data bus, RGB or CPU
16	LCD_D13	LCD_D13	O	bus interface
		BT_D3	I/O	BT656 data bus
		LCD_D5	O	LCD data enable./WR signal of CPU bus interface
17	LCD_D14	LCD_D14	O	LCD Data bus, RGB or CPU
		BT_D4	I/O	BT656 data bus
		GPIOA26	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
18	LCD_D15	LCD_D15	O	LCD Data bus, RGB or CPU
		BT_D5	I/O	BT656 data bus
		GPIOA27	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
19	LCD_D16	LCD_D16	O	LCD Data bus, RGB or CPU
		BT_D6	I/O	BT656 data bus

		UART0_TX	O	UART transive
		GPIOA28	IO	General purpose IO
20	VDD	VDD	PWRI	1.2V power supply
21	DDR_DQ15	DDR_DQ15	I/O	DDR Data bus
22	DDR_DQ14	DDR_DQ14	I/O	DDR Data bus
23	DDR_DQ13	DDR_DQ13	I/O	DDR Data bus
24	DDR_DQ12	DDR_DQ12	I/O	DDR Data bus
25	VDDR	VDDR	PWRI	DDR VDD
26	DDR_DQ11	DDR_DQ11	I/O	DDR Data bus
27	DDR_DQ10	DDR_DQ10	I/O	DDR Data bus
28	DDR_DQ9	DDR_DQ9	I/O	DDR Data bus
29	DDR_DQ8	DDR_DQ8	I/O	DDR Data bus
30	DDR_DQS1	DDR_DQS1	I	DDR DQS Input
31	DDR_DM1	DDR_DM1	O	DDR DQM output
32	DDR_CKN	DDR_CKN	O	DDR Clock- output
33	DDR_CK	DDR_CK	O	DDR Clock output
34	DDR_CKE	DDR_CKE	O	DDR Clock enable output
35	DDR_A10	DDR_A10	O	DDR Address bus output
36	DDR_A11	DDR_A11	O	DDR Address bus output
37	DDR_A9	DDR_A9	O	DDR Address bus output
38	DDR_A8	DDR_A8	O	DDR Address bus output
39	VDDR	VDDR	PWRI	DDR VDD
40	DDR_A7	DDR_A7	O	DDR Address bus output
41	DDR_A6	DDR_A6	O	DDR Address bus output
42	DDR_A5	DDR_A5	O	DDR Address bus output
43	DDR_A4	DDR_A4	O	DDR Address bus output
44	DDR_A3	DDR_A3	O	DDR Address bus output
45	DDR_A2	DDR_A2	O	DDR Address bus output
46	DDR_REF	DDR_REF	I	DDR STTL-2 voltage eference
47	DDR_A13	DDR_A13	O	DDR Address bus output
48	DDR_WRB	DDR_WRB	O	DDR Write output
49	DDR_CASB	DDR_CASB	O	DDR CAS output
50	DDR_RASB	DDR_RASB	O	DDR RAS output
51	DDR_DQ0	DDR_DQ0	I/O	DDR Data bus
52	DDR_DQ1	DDR_DQ1	I/O	DDR Data bus

53	DDR_DQ2	DDR_DQ2	I/O	DDR Data bus
54	DDR_DQ3	DDR_DQ3	I/O	DDR Data bus
55	DDR_DQ4	DDR_DQ4	I/O	DDR Data bus
56	VDDR	VDDR	PWRI	DDR VDD
57	DDR_DQ5	DDR_DQ5	I/O	DDR Data bus
58	DDR_DQ6	DDR_DQ6	I/O	DDR Data bus
59	DDR_DQ7	DDR_DQ7	I/O	DDR Data bus
60	DDR_DQS0	DDR_DQS0	I	DDR DQS Input
61	DDR_DQM0	DDR_DQM0	O	DDR DQM output
62	DDR_BA0	DDR_BA0	O	DDR BA output
63	DDR_BA1	DDR_BA1	O	DDR BA output
64	DDR_A12	DDR_A12	O	DDR Address bus output
65	DDR_A0	DDR_A0	O	DDR Address bus output
66	DDR_A1	DDR_A1	O	DDR Address bus output
67	NAND_CEB3	Nand_CEB3	O	NAND Flash CEB3 output
		GPIOA5	I/O	General purpose IO
		UART1_RX	I	UART Receive
		Nor_CEB3	O	External SRAM Chip Enable
68	NAND_CEB2	Nand_CEB2	O	Nand Flash CEB2 output
		GPIOA4	I/O	General purpose IO
		UART1_TX	O	UART transmit
		Nor_CEB2	O	External SRAM Chip Enable
69	GPIOB12	BT_D6	I/O	BT656 data bus
		GPIOB12	I/O	General purpose IO
		Nor_D14	I/O	External SRAM data bus
70	SIRQ1	SIRQ1	I	External Interrupt signal input
		GPIOA1	I/O	General purpose IO
		PWM1	O	Pulse Width Modulation signal output
71	NC			
72	VDD	VDD	PWRI	1.2V power supply
73	RESET	RESET	I	System Reset, active low, Smith trigger
74	ONOFF	ONOFF	I	Standby/wake up signal from on/off key
75	REM_CON	REM_CON	AI	Romont line-in controller input to ADC
76	SIRQ0	SIRQ0	I	External Interrupt0
77	LOSCO	LOSCO	AO	32.768KHz Crystal Output

78	LOSCI	LOSCI	AI	32.768KHz Crystal input
79	SVDD	SVDD	PWRO	Standby control circuit Power SVDD, always on
80	SVCC	SVCC	PWRO	Standby control circuit Power SVCC, always on
81	VCCOUT	VCCOUT	PWRO	VCC power supply, generate by on chip LDO
82	VCC	VCC	PWRO	VCC power supply, generate by on chip LDO
83	DC5V	DC5V	PWRI	DC5V power; external power supply, from USB or adapter
84	BAT	BAT	PWRI	BAT Power, where the power go into or come out from battery
85	LX_VDD	LX_VDD	PWRO	Buck DC/DC, where to connected with an inductance, source of VDD
86	PGND	PGND	GND	DC/DC GND
87	PGND	PGND	GND	DC/DC GND
88	LX_VDDR	LX_VDDR	PWRO	Buck DC/DC, where to connected with an inductance
89	DDR_VP	DDR_VP	PWRO	DDR power supply from PMU
90	KS_OUT1	KS_OUT1	O	Keyscan output
		GPIOB31	I/O	General purpose IO
91	KS_IN2	KS_IN2	I	Keyscan input
		GPIOB28	I/O	General purpose IO
		PWM2	O	Pulse Width Modulation signal output
92	KS_IN1	KS_IN1	I	Keyscan input
		GPIOB27	I/O	General purpose IO
93	KS_IN0	KS_IN0	I	Keyscan output
		GPIOB26	I/O	General purpose IO
94	FMCLK	FM_CLK	O	Output Clock signal for FM or others
		BT_CLKOUT	O	BT656 clock output, for sensor
95	UART0_RX	UART0_RX	I	UART Reciever, or infrared remote control input
		GPIOA25	I/O	General purpose IO
		SPI0_SCLK	O	SPI CLK output
		Nor_A21	O	External SRAM address bus
96	SD1_CLK	SD1_CLKA	O	SDIO1 clock output
		GPIOB0	I/O	General purpose IO
		MS_CLK	O	Memory stick clock output
97	SD1_CMD	SD1_CMD	I/O	SDIO1 Command output
		GPIOB1	I/O	General purpose IO

		MS_BS	O	Memory stick BS output
98	SD0_D7	SD0_D7	I/O	SDIO Data bus
		MS_D7	I/O	Memory stick Date bus
		SD1_D3	I/O	SDIO Data bus
		GPIOA15	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
		Nor_A17	O	External SRAM address bus
		MS_D3	I/O	Memory Stick Data bus
99	SD0_D6	SD0_D6	I/O	SDIO Data bus
		MS_D6	I/O	Memory Stick Data bus
		SD1_D2	I/O	SDIO Data bus
		GPIOA14	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
		Nor_A16	O	External SRAM address bus
		MS_D2	I/O	Memory Stick Data bus
100	SD0_D5	SD0_D5	I/O	SDIO Data bus
		MS_D5	I/O	Memory Stick Data bus
		SD1_D1	I/O	SDIO Data bus
		GPIOA13	I/O	General purpose IO
		LCD_D5	O	LCD Data bus, RGB or CPU
		Nor_A15	O	External SRAM address bus
		MS_D1	I/O	Memory Stick Data bus
101	SD0_D4	SD0_D4	I/O	SDIO Data bus
		MS_D4	I/O	Memory Stick Data bus
		SD1_D0	I/O	SDIO Data bus
		GPIOA12	I/O	General purpose IO
		LCD_D4	O	LCD Data bus, RGB or CPU
		Nor_A14	O	External SRAM address bus
		MS_D0	I/O	Memory Stick Data bus
		SD0_D0	I/O	SDIO Data bus
102	LCD_D17	LCD_D17	O	LCD Data bus, RGB or CPU
		BT_D7	I/O	BT656 data bus
		UART0_RX	I	UART Reciever, or infrared remote control input
		GPIOA29	I/O	General purpose IO
103	LCD_D11	LCD_D11	O	LCD Data bus, RGB or CPU

		BT_D1	I/O	BT656 data bus
		LCD_D3	O	LCD Data bus, RGB or CPU
		LCD_D10	O	LCD Data bus, RGB or CPU
		BT_D0	I/O	BT656 data bus
104	LCD_D10	LCD_D2	O	LCD Data bus, RGB or CPU
		LCD_D9	O	LCD Data bus, RGB or CPU
		BT_VSYNC	I/O	BT656 Vsync
105	LCD_D9	LCD_D1	O	LCD Data bus, RGB or CPU
		LCD_D8	O	LCD Data bus, RGB or CPU
		BT_HSYNC	I/O	BT656 Hsync
106	LCD_D8	LCD_D0	O	LCD Data bus, RGB or CPU
107	LCD_D7	LCD_D7	O	LCD Data bus, RGB or CPU
108	LCD_D6	LCD_D6	O	LCD Data bus, RGB or CPU
109	LCD_D5	LCD_D5	O	LCD Data bus, RGB or CPU
110	LCD_D4	LCD_D4	O	LCD Data bus, RGB or CPU
		LCD_DCLK	O	Dot clock for the LCD panels
111	LCD_DCLK	WR	O	WR for CPU bus interface
		LCD_VSYNC	I/O	Vertical sync for LCD panels interface
112	LCD_VSYNC	RS	O	RS signal of CPU bus
		LCD_LDE	O	LCD data enable.
		RD	O	RD signal of CPU bus interface
113	LCD_LDE	BT_PCLK	I	BT656 pixel clock
		BT_CLKOUT	O	BT656 clock output, for sensor
		GPIOB5	I/O	General purpose IO
	BT_CLKOUT	Nor_A5	O	External SRAM address bus
114	VDD	VDD	PWRI	1.2V supply
115	NC			
		GPIOB3	I/O	General purpose IO
116	GPIOB3	Nor_A3	O	External SRAM address bus
		GPIOB4	I/O	General purpose IO
117	GPIOB4	Nor_A4	O	External SRAM address bus
		GPIOB6	I/O	General purpose IO
		Nor_D8	I/O	External SRAM data bus
		PWM0	O	Pulse Width Modulation signal output
118	GPIOB6	UART1_RX	I	UART receive

		GPIOB7	I/O	General purpose IO
		Nor_D9	I/O	External SRAM data bus
		PWM1	O	Pulse Width Modulation signal output
119	GPIOB7	UART1_TX	O	UART transmit
		GPIOB8	I/O	General purpose IO
120	GPIOB8	Nor_D10	I/O	External SRAM data bus
		GPIOB9	I/O	General purpose IO
121	GPIOB9	Nor_D11	I/O	External SRAM data bus
		GPIOB10	I/O	General purpose IO
122	GPIOB10	Nor_D12	I/O	External SRAM data bus
		GPIOB11	I/O	General purpose IO
123	GPIOB11	Nor_D13	I/O	External SRAM data bus
		Nand_D0	I/O	Nand Flash data bus
		GPIOA10	I/O	General purpose IO
		Nor_D0	I/O	External SRAM data bus
		LCD_D8	O	LCD Data bus, RGB or CPU
124	NAND_D0	SIRQ1	I	External Interrupt signal input
		Nand_D1	I/O	Nand Flash data bus
		GPIOA11	I/O	General purpose IO
		Nor_D1	I/O	External SRAM data bus
		LCD_D9	O	LCD Data bus, RGB or CPU
125	NAND_D1	PWM1	O	Pulse Width Modulation signal output
		Nand_D2	I/O	Nand Flash data bus
		SPI1_SCLK	O	SPI CLK output
		Nor_D2	I/O	External SRAM data bus
126	NAND_D2	LCD_D10	O	LCD Data bus, RGB or CPU
		Nand_D3	I/O	Nand Flash data bus
		SPI1_SS	O	SPI SS output
		Nor_D3	I/O	External SRAM data bus
127	NAND_D3	LCD_D11	O	LCD Data bus, RGB or CPU
		Nand_ALE	O	Nand Flash address latch enable output
		Nor_A1	O	External SRAM address bus
		SPI0_SCLK	O	SPI CLK output
128	NAND_ALE	LCD_D17	O	LCD Data bus, RGB or CPU
129	NAND_CLE	Nand_CLE	O	Nand Flash command latch enable output

		Nor_A0	O	External SRAM address bus
		SPI0_SS	O	SPI SS output
		LCD_D16	O	LCD Data bus, RGB or CPU
		NAND_RDB	O	Nand Flash read output
		SPI0_MISO	I/O	SPI MISO
		Nor_RD	O	External SRAM read enable, active low
		LCD_VSYNC	O	Vertical sync for RGB LCD panels.
130	NAND_RDB	RS	O	RS signal of LCD CPU bus interface
131	HOSCO	HOSCO	AO	24MHz Ccrystal Output
132	HOSCI	HOSCI	AI	24MHz Crystal input
133	AVDD	AVDD	PWRI	1.2V
134	Y2	Y2	AI	Touch Panel Y2
135	Y1	Y1	AI	Touch Panel Y1
136	X2	X2	AI	Touch Panel X2
137	X1	X1	AI	Touch Panel X1
138	VREF	VREF	PWR	Reference Voltage,with capacitance
139	FMINR	FMINR	AI	FM right channel input
140	FMINL	FMINL	AI	FM left channel input
141	MICIN	MICIN	AI	Microphone input
142	AVCC	AVCC	PWRI	VCC for audio circuit
143	AGND	AGND	GND	GND for audio circuit
144	VRDA	VRDA	AO	Connection with Cap; Just use for DAC Reference voltage
145	VRO	VRO	AO	Direct drive PA reference
146	VROS	VROS	AO	Direct drive PA sense
147	AOUTR	AOUTR	AO	Audio Analog Right channel output
148	PAGND	PAGND	GND	Power Amplify GND
149	PAVCC	PAVCC	PWRI	Power Amplify VCC output; Connection with Cap
150	AOUTL	AOUTL	AO	Audio Analog Left channel output
151	Pr	Pr	AO	Pr Video output
152	Pb	Pb	AO	Pb Video output
153	Y	Y	AO	Y Video output
154	VBUS	VBUS	AI	USB device controller input pins; Detect the voltage for start the state machine
155	DM	DM	AO	USB DM
156	DP	DP	AO	USB DP

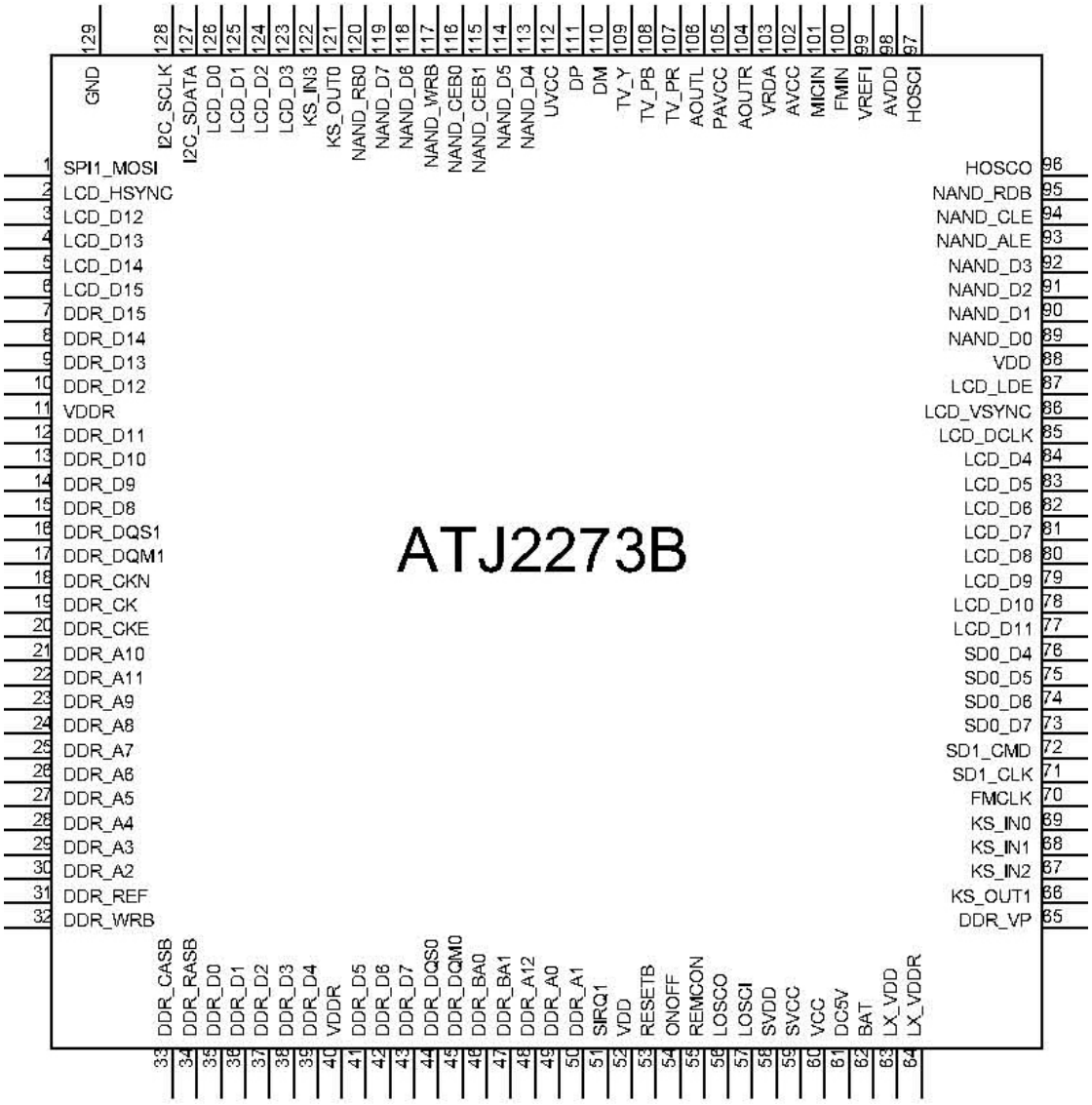
157	VCC	VCC	PWRI	3.1V supply
158	NAND_D4	Nand_D4	I/O	Nand Flash data bus
		SPI1_MOSI	I/O	SPI MOSI
		Nor_D4	I/O	External SRAM data bus
		LCD_D12	O	LCD Data bus, RGB or CPU
159	NAND_D5	Nand_D5	I/O	Nand Flash data bus
		SPI1_MISO	I/O	SPI MISO
		Nor_D5	I/O	External SRAM data bus
		GPIOA0	I/O	General purpose IO
		LCD_D13	O	LCD Data bus, RGB or CPU
160	NAND_CEB1	Nand_CEB1	O	Nand Flash CEB1 output, boot Flash
		SD1_CLKB	O	SDIO clk output signal
		GPIOA3	I/O	General purpose IO
		Nor_CEB1	O	External SRAM chip enable
161	NAND_CEB0	Nand_CEB0	O	Nand Flash CEB0 output
		SD0_CLKB	O	SDIO clk output signal
		GPIOA2	I/O	General purpose IO
		Nor_CEB0/7	O	External SRAM chip enable
162	NAND_WRB	NAND_WRB	O	Nand Flash write output
		SPI0_MOSI	I/O	SPI MOSI
		Nor_WR	O	External SRAM write enable, active low
		LCD_DCLK	O	Dot clock for the LCD panels
		WR	O	WR signal of LCD CPU bus interface
163	NAND_D6	Nand_D6	I/O	Nand Flash data bus
		GPIOA16	I/O	General purpose IO
		Nor_D6	I/O	External SRAM data bus
		LCD_D14	O	LCD Data bus, RGB or CPU
164	NAND_D7	Nand_D7	I/O	Nand Flash data bus
		GPIOA17	I/O	General purpose IO
		Nor_D7	I/O	External SRAM data bus
		LCD_D15	O	LCD Data bus, RGB or CPU
165	NAND_RB0	NAND_RB0	I	Nand Flash RB0 input
		GPIOA8	I/O	General purpose IO
		Nor_CEB4	O	External SRAM chip enable
166	KS_OUT0	KS_OUT0	O	Keyscan output

		GPIOB30	I/O	General purpose IO
167	KS_IN3	KS_IN3	I	Keyscan input
		GPIOB29	I/O	General purpose IO
		PWM3	O	Pulse Width Modulation signal output
168	LCD_D3	SD0_D3	I/O	SDIO Data bus
		MS_D3	I/O	Memory Stick Data bus
		GPIOA23	I/O	General purpose IO
		LCD_D3	O	LCD Data bus, RGB or CPU
		Nor_A11	O	External SRAM address bus
169	LCD_D2	SD0_D2	I/O	SDIO Data bus
		MS_D2	I/O	Memory Stick Data bus
		GPIOA22	I/O	General purpose IO
		LCD_D2	O	LCD Data bus, RGB or CPU
		Nor_A10	O	External SRAM address bus
170	LCD_D1	SD0_D1	I/O	SDIO Data bus
		MS_D1	I/O	Memory Stick Data bus
		GPIOA21	I/O	General purpose IO
		LCD_D1	O	LCD Data bus, RGB or CPU
		Nor_A9	O	External SRAM address bus
171	LCD_D0	SD0_D0	I/O	SDIO Data bus
		MS_D0	I/O	Memory Stick Data bus
		GPIOA20	I/O	General purpose IO
		LCD_D0	O	LCD Data bus, RGB or CPU
		Nor_A8	O	External SRAM address bus
172	SPI0_MOSI	SPI0_MOSI	I/O	SPI MOSI
		GPIOB16	I/O	General purpose IO
		UART1_CTSB	I	UART clear to send
		UART0_RX	I	UART Reciever, or infrared remote control input
		Nor_A13	O	External SRAM address bus
173	SPI0_MISO	SPI0_MISO	I/O	SPI MISO
		GPIOB17	I/O	General purpose IO
		UART1_RX	I	UART receive
		PWM3	O	Pulse Width Modulation signal output
174	SPI0_SCLK	SPI0_SCLK	I/O	SPI clock output
		GPIOB14	I/O	General purpose IO

		UART1_RTSB	O	UART request to send
		UART0_TX	O	UART transmite
		Nor_A12	O	External SRAM address bus
175	I2C_SDATA	I2C_SDATA	I/O	I2C data
		GPIOA31	I/O	General purpose IO
		UART1_TX	O	UART transmite
		Nor_A6	O	External SRAM address bus
		SPI0_MISO	I/O	SPI MISO
176	I2C_SCLK	I2C_SCLK	O	I2C clock output
		GPIOA30	I/O	General purpose IO
		UART1_RX	I	UART receive
		Nor_A7	O	External SRAM address bus
		SPI0_SS	O	SPI SS output
177	GND	GND	GND	Ground

11.4 ATJ2273B

11.4.1 Pin assignment



11.4.2 Pin Definition

PIN NO.	PIN Name	Function Name	I/O	Description
1	UART0_RX	UART0_RX	I	UART Reciever, or infrared remote control input
		GPIOB20	I/O	General purpose IO
		Nor_A19	O	External SRAM address bus
2	LCD_HSYNC	LCD_HSYNC	O	Horizontal sync for RGB LCD panels.
		CE	O	CE signal of CPU LCD
3	LCD_D12	LCD_D12	O	LCD Data bus, RGB or CPU
		BT_D2	I/O	BT656 data bus
		LCD_D4	O	LCD Data bus, RGB or CPU
4	LCD_D13	LCD_D13	O	bus interface
		BT_D3	I/O	BT656 data bus
		LCD_D5	O	LCD data enable./WR signal of CPU bus interface
5	LCD_D14	LCD_D14	O	LCD Data bus, RGB or CPU
		BT_D4	I/O	BT656 data bus
		GPIOA26	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
6	LCD_D15	LCD_D15	O	LCD Data bus, RGB or CPU
		BT_D5	I/O	BT656 data bus
		GPIOA27	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
7	DDR_DQ15	DDR_DQ15	I/O	DDR Data bus
8	DDR_DQ14	DDR_DQ14	I/O	DDR Data bus
9	DDR_DQ13	DDR_DQ13	I/O	DDR Data bus
10	DDR_DQ12	DDR_DQ12	I/O	DDR Data bus
11	VDDR	VDDR	PWRI	DDR VDD
12	DDR_DQ11	DDR_DQ11	I/O	DDR Data bus
13	DDR_DQ10	DDR_DQ10	I/O	DDR Data bus
14	DDR_DQ9	DDR_DQ9	I/O	DDR Data bus
15	DDR_DQ8	DDR_DQ8	I/O	DDR Data bus
16	DDR_DQS1	DDR_DQS1	I	DDR DQS Input
17	DDR_DM1	DDR_DM1	O	DDR DQM output
18	DDR_CKN	DDR_CKN	O	DDR Clock- output

19	DDR_CK	DDR_CK	O	DDR Clock output
20	DDR_CKE	DDR_CKE	O	DDR Clock enable output
21	DDR_A10	DDR_A10	O	DDR Address bus output
22	DDR_A11	DDR_A11	O	DDR Address bus output
23	DDR_A9	DDR_A9	O	DDR Address bus output
24	DDR_A8	DDR_A8	O	DDR Address bus output
25	DDR_A7	DDR_A7	O	DDR Address bus output
26	DDR_A6	DDR_A6	O	DDR Address bus output
27	DDR_A5	DDR_A5	O	DDR Address bus output
28	DDR_A4	DDR_A4	O	DDR Address bus output
29	DDR_A3	DDR_A3	O	DDR Address bus output
30	DDR_A2	DDR_A2	O	DDR Address bus output
31	DDR_REF	DDR_REF	I	DDR STTL-2 voltage eference
32	DDR_WRB	DDR_WRB	O	DDR Write output
33	DDR_CASB	DDR_CASB	O	DDR CAS output
34	DDR_RASB	DDR_RASB	O	DDR RAS output
35	DDR_DQ0	DDR_DQ0	I/O	DDR Data bus
36	DDR_DQ1	DDR_DQ1	I/O	DDR Data bus
37	DDR_DQ2	DDR_DQ2	I/O	DDR Data bus
38	DDR_DQ3	DDR_DQ3	I/O	DDR Data bus
39	DDR_DQ4	DDR_DQ4	I/O	DDR Data bus
40	VDDR	VDDR	PWRI	DDR VDD
41	DDR_DQ5	DDR_DQ5	I/O	DDR Data bus
42	DDR_DQ6	DDR_DQ6	I/O	DDR Data bus
43	DDR_DQ7	DDR_DQ7	I/O	DDR Data bus
44	DDR_DQS0	DDR_DQS0	I	DDR DQS Input
45	DDR_DQM0	DDR_DQM0	O	DDR DQM output
46	DDR_BA0	DDR_BA0	O	DDR BA output
47	DDR_BA1	DDR_BA1	O	DDR BA output
48	DDR_A12	DDR_A12	O	DDR Address bus output
49	DDR_A0	DDR_A0	O	DDR Address bus output
50	DDR_A1	DDR_A1	O	DDR Address bus output
51	SIRQ1	SIRQ1	I	External Interrupt signal input
		GPIOA1	I/O	General purpose IO
		PWM1	O	Pulse Width Modulation signal output

52	VDD	VDD	PWRI	1.2V power supply
53	RESET	RESET	I	System Reset, active low, Smith trigger
54	ONOFF	ONOFF	I	Standby/wake up signal from on/off key
55	REM_CON	REM_CON	AI	Romont line-in controller input to ADC
56	LOSCO	LOSCO	AO	32.768KHz Crystal Output
57	LOSCI	LOSCI	AI	32.768KHz Crystal input
58	SVDD	SVDD	PWRO	Standby control circuit Power SVDD, always on
59	SVCC	SVCC	PWRO	Standby control circuit Power SVCC, always on
60	VCC	VCC	PWRO	VCC power supply, generate by on chip LDO
61	DC5V	DC5V	PWRI	DC5V power; external power supply, from USB or adapter
62	BAT	BAT	PWRI	BAT Power, where the power go into or come out from battery
63	LX_VDD	LX_VDD	PWRO	Buck DC/DC, where to connected with an inductance, source of VDD
64	LX_VDDR	LX_VDDR	PWRO	Buck DC/DC, where to connected with an inductance
65	DDR_VP	DDR_VP	PWRO	DDR power supply from PMU
66	KS_OUT1	KS_OUT1	O	Keyscan output
		GPIOB31	I/O	General purpose IO
67	KS_IN2	KS_IN2	I	Keyscan input
		GPIOB28	I/O	General purpose IO
		PWM2	O	Pulse Width Modulation signal output
68	KS_IN1	KS_IN1	I	Keyscan input
		GPIOB27	I/O	General purpose IO
69	KS_IN0	KS_IN0	I	Keyscan output
		GPIOB26	I/O	General purpose IO
70	FMCLK	FM_CLK	O	Output Clock signal for FM or others
		BT_CLKOUT	O	BT656 clock output, for sensor
71	SD1_CLK	SD1_CLKA	O	SDIO1 clock output
		GPIOB0	I/O	General purpose IO
		MS_CLK	O	Memory stick clock output
72	SD1_CMD	SD1_CMD	I/O	SDIO1 Command output
		GPIOB1	I/O	General purpose IO
		MS_BS	O	Memory stick BS output
73	SD0_D7	SD0_D7	I/O	SDIO Data bus

		MS_D7	I/O	Memory stick Date bus
		SD1_D3	I/O	SDIO Data bus
		GPIOA15	I/O	General purpose IO
		LCD_D7	O	LCD Data bus, RGB or CPU
		Nor_A17	O	External SRAM address bus
		MS_D3	I/O	Memory Stick Data bus
		SD0_D6	I/O	SDIO Data bus
		MS_D6	I/O	Memory Stick Data bus
		SD1_D2	I/O	SDIO Data bus
		GPIOA14	I/O	General purpose IO
		LCD_D6	O	LCD Data bus, RGB or CPU
		Nor_A16	O	External SRAM address bus
74	SD0_D6	MS_D2	I/O	Memory Stick Data bus
		SD0_D5	I/O	SDIO Data bus
		MS_D5	I/O	Memory Stick Data bus
		SD1_D1	I/O	SDIO Data bus
		GPIOA13	I/O	General purpose IO
		LCD_D5	O	LCD Data bus, RGB or CPU
		Nor_A15	O	External SRAM address bus
75	SD0_D5	MS_D1	I/O	Memory Stick Data bus
		SD0_D4	I/O	SDIO Data bus
		MS_D4	I/O	Memory Stick Data bus
		SD1_D0	I/O	SDIO Data bus
		GPIOA12	I/O	General purpose IO
		LCD_D4	O	LCD Data bus, RGB or CPU
		Nor_A14	O	External SRAM address bus
		MS_D0	I/O	Memory Stick Data bus
76	SD0_D4	SD0_D0	I/O	SDIO Data bus
		LCD_D11	O	LCD Data bus, RGB or CPU
		BT_D1	I/O	BT656 data bus
77	LCD_D11	LCD_D3	O	LCD Data bus, RGB or CPU
		LCD_D10	O	LCD Data bus, RGB or CPU
		BT_D0	I/O	BT656 data bus
78	LCD_D10	LCD_D2	O	LCD Data bus, RGB or CPU
79	LCD_D9	LCD_D9	O	LCD Data bus, RGB or CPU

		BT_VSYNC	I/O	BT656 Vsync
		LCD_D1	O	LCD Data bus, RGB or CPU
		LCD_D8	O	LCD Data bus, RGB or CPU
		BT_HSYNC	I/O	BT656 Hsync
80	LCD_D8	LCD_D0	O	LCD Data bus, RGB or CPU
81	LCD_D7	LCD_D7	O	LCD Data bus, RGB or CPU
82	LCD_D6	LCD_D6	O	LCD Data bus, RGB or CPU
83	LCD_D5	LCD_D5	O	LCD Data bus, RGB or CPU
84	LCD_D4	LCD_D4	O	LCD Data bus, RGB or CPU
		LCD_DCLK	O	Dot clock for the LCD panels
85	LCD_DCLK	WR	O	WR for CPU bus interface
		LCD_VSYNC	I/O	Vertical sync for LCD panels interface
86	LCD_VSYNC	RS	O	RS signal of CPU bus
		LCD_LDE	O	LCD data enable.
		RD	O	RD signal of CPU bus interface
87	LCD_LDE	BT_PCLK	I	BT656 pixel clock
88	VDD	VDD	PWRI	1.2V supply
		Nand_D0	I/O	Nand Flash data bus
		GPIOA10	I/O	General purpose IO
		Nor_D0	I/O	External SRAM data bus
89	NAND_D0	LCD_D8	O	LCD Data bus, RGB or CPU
		Nand_D0	I/O	Nand Flash data bus
		GPIOA10	I/O	General purpose IO
		Nor_D0	I/O	External SRAM data bus
		LCD_D8	O	LCD Data bus, RGB or CPU
90	NAND_D0	SIRQ1	I	External Interrupt signal input
		Nand_D1	I/O	Nand Flash data bus
		GPIOA11	I/O	General purpose IO
		Nor_D1	I/O	External SRAM data bus
		LCD_D9	O	LCD Data bus, RGB or CPU
91	NAND_D1	PWM1	O	Pulse Width Modulation signal output
		Nand_D3	I/O	Nand Flash data bus
		SPI1_SS	O	SPI SS output
		Nor_D3	I/O	External SRAM data bus
92	NAND_D3	LCD_D11	O	LCD Data bus, RGB or CPU

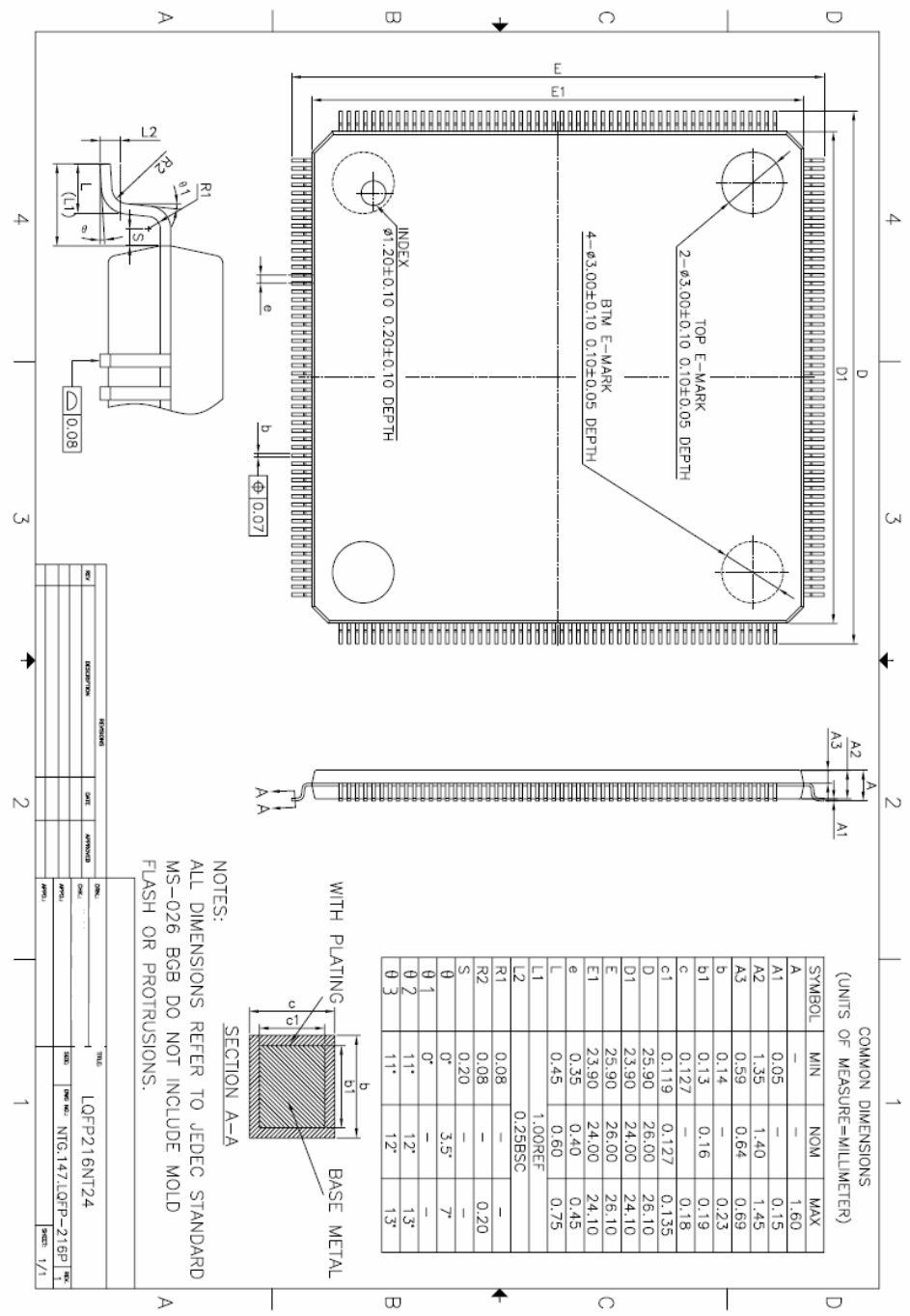
93	NAND_ALE	Nand_ALE	O	Nand Flash address latch enable output
		Nor_A1	O	External SRAM address bus
		SPI0_SCLK	O	SPI CLK output
		LCD_D17	O	LCD Data bus, RGB or CPU
94	NAND_CLE	Nand_CLE	O	Nand Flash command latch enable output
		Nor_A0	O	External SRAM address bus
		SPI0_SS	O	SPI SS output
		LCD_D16	O	LCD Data bus, RGB or CPU
95	NAND_RDB	NAND_RDB	O	Nand Flash read output
		SPI0_MISO	I/O	SPI MISO
		Nor_RD	O	External SRAM read enable, active low
		LCD_VSYNC	O	Vertical sync for RGB LCD panels.
		RS	O	RS signal of LCD CPU bus interface
96	HOSCO	HOSCO	AO	24MHz Ccrystal Output
97	HOSCI	HOSCI	AI	24MHz Crystal input
98	AVDD	AVDD	PWRI	1.2V
99	VREF	VREF	PWR	Reference Voltage,with capacitance
100	FMIN	FMIN	AI	FM input
101	MICIN	MICIN	AI	Microphone input
102	AVCC	AVCC	PWRI	VCC for audio circuit
103	VRDA	VRDA	AO	Connection with Cap; Just use for DAC Reference voltage
104	AOUTR	AOUTR	AO	Audio Analog Right channel output
105	PAVCC	PAVCC	PWRI	Power Amplify VCC output; Connection with Cap
106	AOUTL	AOUTL	AO	Audio Analog Left channel output
107	Pr	Pr	AO	Pr Video output
108	Pb	Pb	AO	Pb Video output
109	Y	Y	AO	Y Video output
110	DM	DM	AO	USB DM
111	DP	DP	AO	USB DP
112	VCC	VCC	PWRI	3.1V supply
113	NAND_D4	Nand_D4	I/O	Nand Flash data bus
		SPI1_MOSI	I/O	SPI MOSI
		Nor_D4	I/O	External SRAM data bus
		LCD_D12	O	LCD Data bus, RGB or CPU

114	NAND_D5	Nand_D5	I/O	Nand Flash data bus
		SPI1_MISO	I/O	SPI MISO
		Nor_D5	I/O	External SRAM data bus
		GPIOA0	I/O	General purpose IO
		LCD_D13	O	LCD Data bus, RGB or CPU
115	NAND_CEB1	Nand_CEB1	O	Nand Flash CEB1 output, boot Flash
		SD1_CLKB	O	SDIO clk output signal
		GPIOA3	I/O	General purpose IO
		Nor_CEB1	O	External SRAM chip enable
116	NAND_CEB0	Nand_CEB0	O	Nand Flash CEB0 output
		SD0_CLKB	O	SDIO clk output signal
		GPIOA2	I/O	General purpose IO
		Nor_CEB0/7	O	External SRAM chip enable
117	NAND_WRB	NAND_WRB	O	Nand Flash write output
		SPI0_MOSI	I/O	SPI MOSI
		Nor_WR	O	External SRAM write enable, active low
		LCD_DCLK	O	Dot clock for the LCD panels
		WR	O	WR signal of LCD CPU bus interface
118	NAND_D6	Nand_D6	I/O	Nand Flash data bus
		GPIOA16	I/O	General purpose IO
		Nor_D6	I/O	External SRAM data bus
		LCD_D14	O	LCD Data bus, RGB or CPU
119	NAND_D7	Nand_D7	I/O	Nand Flash data bus
		GPIOA17	I/O	General purpose IO
		Nor_D7	I/O	External SRAM data bus
		LCD_D15	O	LCD Data bus, RGB or CPU
120	NAND_RB0	NAND_RB0	I	Nand Flash RB0 input
		GPIOA8	I/O	General purpose IO
		Nor_CEB4	O	External SRAM chip enable
121	KS_OUT0	KS_OUT0	O	Keyscan output
		GPIOB30	I/O	General purpose IO
122	KS_IN3	KS_IN3	I	Keyscan input
		GPIOB29	I/O	General purpose IO
		PWM3	O	Pulse Width Modulation signal output
123	LCD_D3	SD0_D3	I/O	SDIO Data bus

		MS_D3	I/O	Memory Stick Data bus
		GPIOA23	I/O	General purpose IO
		LCD_D3	O	LCD Data bus, RGB or CPU
		Nor_A11	O	External SRAM address bus
		SD0_D2	I/O	SDIO Data bus
		MS_D2	I/O	Memory Stick Data bus
		GPIOA22	I/O	General purpose IO
		LCD_D2	O	LCD Data bus, RGB or CPU
124	LCD_D2	Nor_A10	O	External SRAM address bus
		SD0_D1	I/O	SDIO Data bus
		MS_D1	I/O	Memory Stick Data bus
		GPIOA21	I/O	General purpose IO
		LCD_D1	O	LCD Data bus, RGB or CPU
125	LCD_D1	Nor_A9	O	External SRAM address bus
		SD0_D0	I/O	SDIO Data bus
		MS_D0	I/O	Memory Stick Data bus
		GPIOA20	I/O	General purpose IO
		LCD_D0	O	LCD Data bus, RGB or CPU
126	LCD_D0	Nor_A8	O	External SRAM address bus
		I2C_SDATA	I/O	I2C data
		GPIOA31	I/O	General purpose IO
		UART1_TX	O	UART transmite
		Nor_A6	O	External SRAM address bus
127	I2C_SDATA	SPI0_MISO	I/O	SPI MISO
		I2C_SCLK	O	I2C clock output
		GPIOA30	I/O	General purpose IO
		UART1_RX	I	UART receive
		Nor_A7	O	External SRAM address bus
128	I2C_SCLK	SPI0_SS	O	SPI SS output
129	GND	GND	GND	Ground

12 Package Drawings

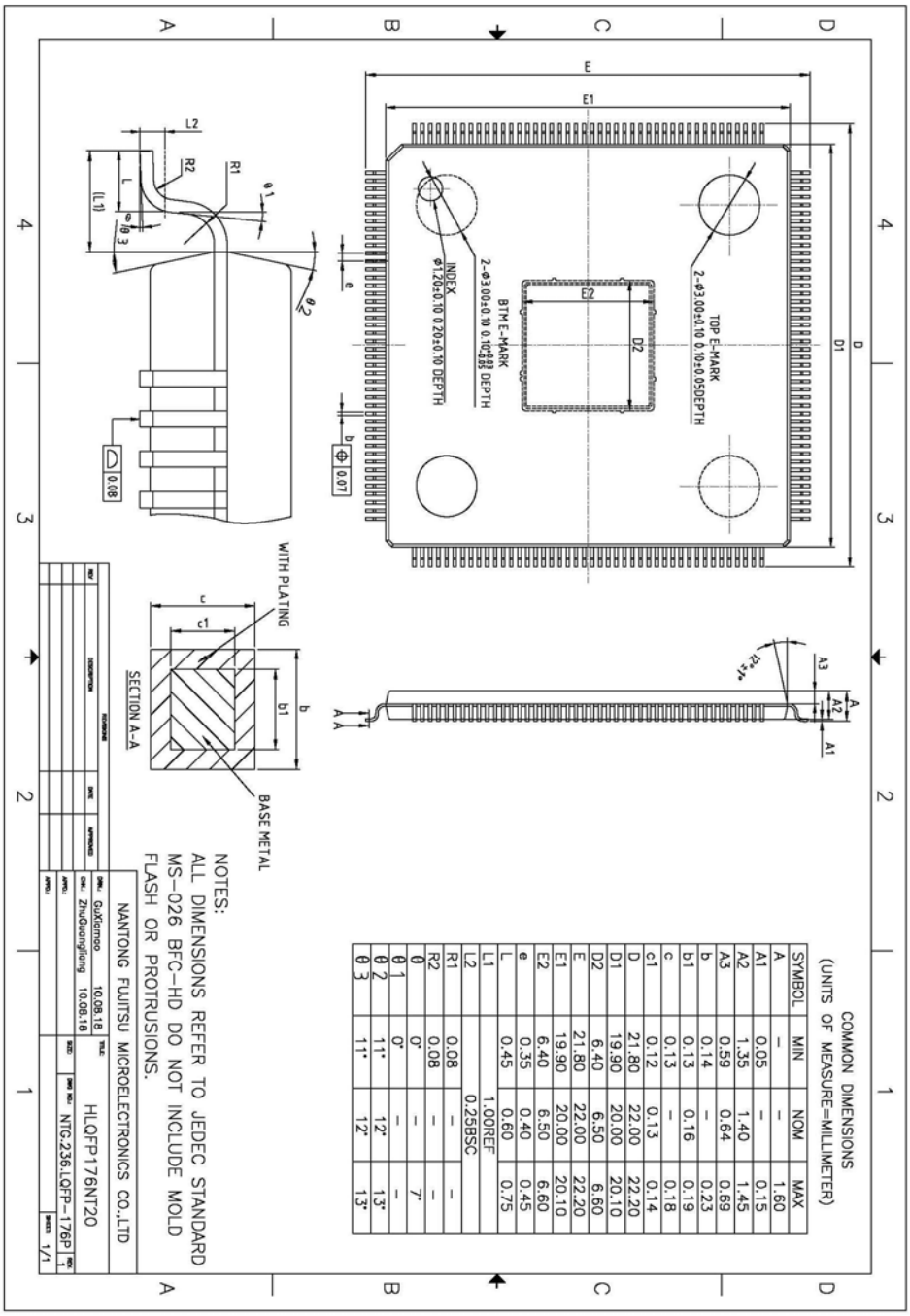
12.1 ATJ2279 Package Drawings



COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)

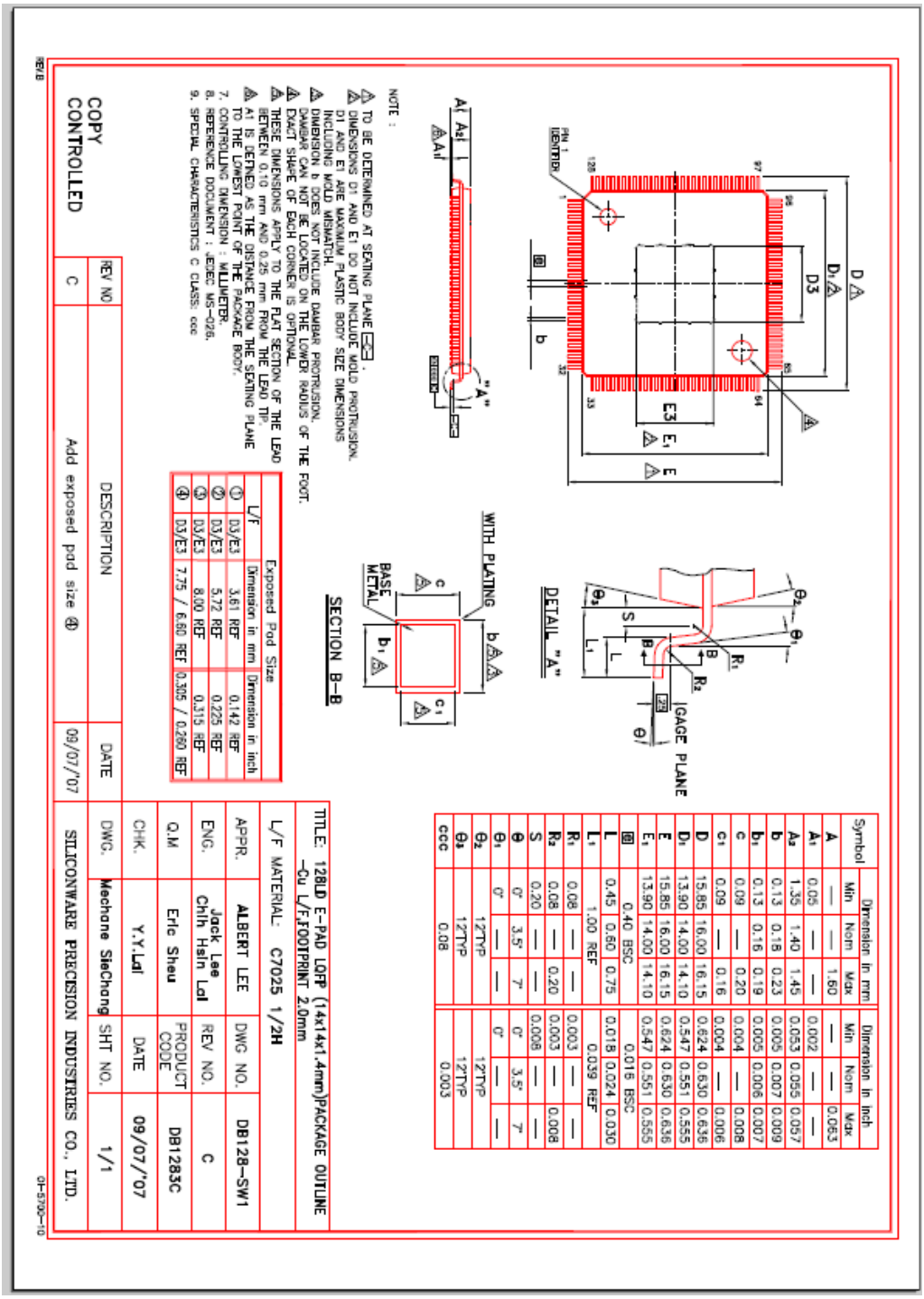
SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	–	0.23
b1	0.13	0.16	0.19
c	0.127	–	0.18
c1	0.119	0.127	0.135
D	25.90	26.00	26.10
D1	23.90	24.00	24.10
E	25.90	26.00	26.10
E1	23.90	24.00	24.10
e	0.35	0.40	0.45
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

12.2 ATJ2279B&2275B Package Drawings



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	–	0.23
b1	0.13	0.16	0.19
c	0.13	–	0.18
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
D2	6.40	6.50	6.60
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
E2	6.40	6.50	6.60
e	0.35	0.40	0.45
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	–
θ	0°	–	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

12.3 ATJ2273B Package Drawings



Symbol	Dimension in mm			Dimension in Inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.60	---	---	0.063
A1	0.05	---	---	0.002	---	---
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	---	0.20	0.004	---	0.008
c1	0.09	---	0.16	0.004	---	0.006
D	15.85	16.00	16.15	0.624	0.630	0.635
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.635
E1	13.90	14.00	14.10	0.547	0.551	0.555
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
R1	0.08	---	---	0.003	---	---
R2	0.08	---	0.20	0.003	---	0.008
S	0.20	---	---	0.008	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	---	---	0°	---	---
θ2		12°TYP			12°TYP	
θ3		12°TYP			12°TYP	
ccc		0.08			0.003	

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Exposed Pad Size			
L/F	Dimension in mm	Dimension in inch	
①	D3/E3	3.61 REF	0.142 REF
②	D3/E3	5.72 REF	0.225 REF
③	D3/E3	8.00 REF	0.315 REF
④	D3/E3	7.75 / 6.60 REF	0.305 / 0.260 REF

TITLE: 128LD E-PAD LQFP (14x14x1.4mm)PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm

L/F MATERIAL: C7025 1/2H

REV NO	DESCRIPTION	DATE	APPR.	ALBERT LEE	DWG NO.	DB128-SW1
C	Add exposed pad size ④	08/07/'07	ENG.	Jack Lee / Chih Hsin Lai	REV NO.	C
			Q.M	Eric Sheu	PRODUCT CODE	DB1283C
			CHK.	Y.Y.Lai	DATE	09/07/'07
			DWG.	Mechone SieChong	SHT NO.	1/1

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REV.B

13 Appendix

13.1 Acronym and Abbreviations

ADC: Analog-to-Digital Converter
AHB: Advanced High-Performance Bus
ALE: Address-Locked Enable
APB: Advanced Peripheral Bus
BIST: Built-in Self-Test
CLE: Command-Locked Enable
CP0: System Control Coprocessor
CRC: Cyclic Redundancy Check
CVBS: Composite Video Broadcasting Signal
DAC: Digital-to-Analog Converter
dB: Decibel
DC: Direct Current
DSP: Digital Signal Processing
DVB: Digital Video Broadcasting
EAV: End of Active Video
ECC: Error Correct Code
FIR: Fast Infrared
GPIO: General-Purpose Input/Output
I2C: Inter-Integrated Circuit
I2S: Inter-IC Sound
IR: Infrared
IrDA: Infrared Data Association
IRQ: Interrupt Request
JPEG: Joint Photographic Experts Group
Li-Ion: Lithium Ion (battery type)
LRADC: Low Resolution ADC
MAC: Multiplier Accumulator Control
MIPS: Million Instructions per Second
MIR: Mid Infrared
MJPEG: Motion JPEG
MMC: Multimedia Card
MMU: Memory Management Unit

MLC: Multi-level Cell
MPEG: Motion Picture Expert Group
MS: Memory stick card
NTSC: National Television Standards Committee
OLED: Polymer Light-Emitting Diode
PA: Power Amplifier
PAL: Phase Alteration Line
PFM: Pulse Frequency Modulation
PLL: Phase-Locked Loop
PMU: Power Management Unit
PWM: Pulse Width Modulation
RISC: Reduced Instruction Set Computing
RTC: Real-Time Clock
SAV: Start of Active Video
SD: Secure Digital memory card
SIR: Slow Infrared
SMC: State Machine Controller
SLC: Single-Level Cell
SOC: System on a Chip
SPEC: Specification
SPI: Serial Peripheral Interface
SPRAM: Scratch Pad RAM
SW: Software
THD: Total Harmonic Distortion
TLB: Translation Look-aside Buffer
TS: Transport Stream
UART: Universal Asynchronous Receiver Transmitter
WMA: Windows Media Audio
WMV: Windows Media Video

Actions Semiconductor Co., Ltd.
Address: Bldg.15-1, NO.1, HIT Rd., Tangjia, Zhuhai, Guangdong, China
Tel: +86-756-3392353
Fax: +86-756-3392251
Post Code: 519085
http://www.actions-semi.com
Business Email: mp-sales@actions-semi.com
Technical Service Email: mp-cs@actions-semi.com