Actions

炬力集成

ATJ331X Datasheet

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Contents

Revision History

Date	Revision	Description
2010-6-11	1.0	Initial Release;

1 Introduction

1.1 Overview

ATJ331X is a third generation single-chip highly integrated digital music system solution for devices dedicating to audio players etc. It includes an audio decoder with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. It also provides an interface to SPDIF, flash memory, LED/LCD, button and switch inputs, headphones, microphone and FM radio input and control. The chip supports WMA and other digital audio standards. For devices like USB-Disk, it can act as a USB mass storage slave device to personal computer system. In addition, its low power consumption leads to long battery life and an efficient and flexible on-chip DC-DC converter allowing many different battery configurations, including 1xAA, 1xAAA and Li-on. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphones. The A/D includes inputs for both Microphone and Analog Audio in to support voice recording and FM radio integration features. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio players.

1.2 Features

- Support WMA Decoder, bit rate 32-384Kbps, 8-48KHz;
- Digital Voice Recording (ADPCM);
- On-chip Multi-use RAM ((22K+3*256)*8bit) and PCM RAM (8K*8bit) that can be switched to be MCU memory space or DSP memory;
- Integrated MCU with DSU, the instruction set is compatible with Z80;
- Internal ZRAM1 ((16K-64)*8),ZRAM2((6K+256)*8) ,ZRAM3(14K*8) accessed by MCU;
- Internal 17Kx8 BROM build in Boot up and USB Upgrade firmware;
- Internal SRAM access time<7ns, MROM access time<16ns;
- External up to 4 (pcs) x 32M~4G bytes Nand type Flash accessed by MCU or DMA;
- External Smart Media Card;
- Support following memory card interface:
  Multi Media Card Specification Version 4.2 (1/4/8 bit mode)
  Secure Digital Card Specification Version 2.0 (1/4-bit mode)
  Memory Stick Version 1.43 (1/4-bit mode)

Memory Stick Pro Version 1.02 (1/4-bit mode)

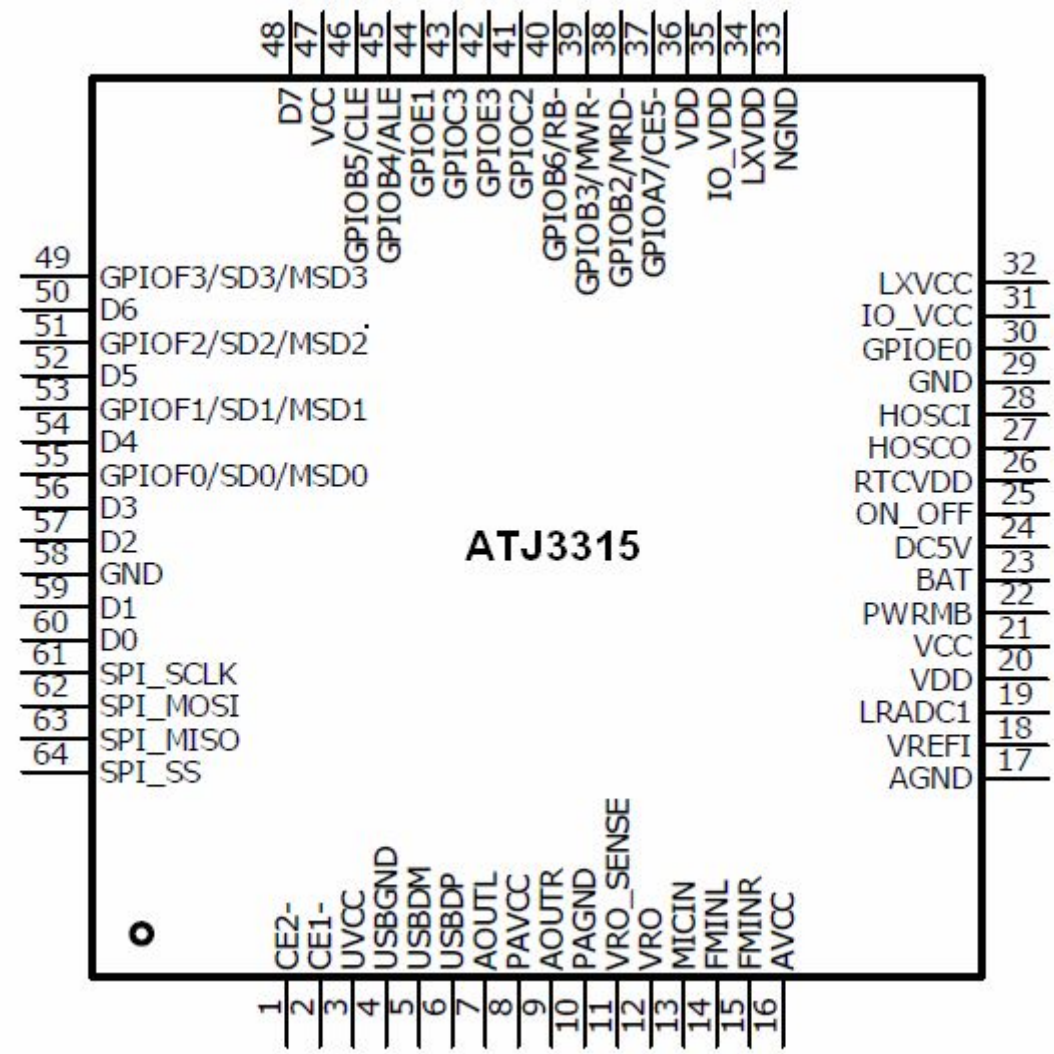
Memory Stick Pro-HG Version 1.01 (1/4/8-bit mode);

- Support 24MHz OSC with on-chip PLL for MCU and about 32KHz RC oscillator;
- 2-channel DMA,1-channel CTC and interrupt controller for MCU;
- Energy saving with dynamic power management, supporting 1 cell, 2 cell and Li-on;
- Support USB2.0 Compliance PHY+SIE,RD/WR:6MB/5MB (NAND Flash Base);
- Build in Stereo 16-bit Sigma-Delta D/A;
- Enough GPIOs for all applications;
- Support I²C/SPI/UART/IR/SPDIF interface;
- Support external 8080 Series LCM driver interface;
- Support FM Radio input and 40-level volume control;
- Support Stereo 16-bit Sigma-Delta A/D for Microphone/FM Input, sample rate at 8/12/16/22/24/32/48KHz;
- MCU running at 48MHz (typ), F/W can program from DC up to 48MHz transparently;
- D/A+PA SNR: without A weight>91dB;
- A/D SNR >90dB, support difference/2-channle microphone;
- Headphone driver output 2x20Mw @16ohm;
- Standby Leakage Current: <50uA (whole system);
- Low Power Consumption: <40mW@1.6V at typical audio decoder solution;
- Package at LQFP-64 (7x7mm)

2 Pin Description

2.1 ATJ3315

2.1.1 ATJ3315 Pin Assignment



2.1.2 ATJ3315 Pin Definition

Pin No.	Pin Name	I/O Type	Driver	Reset Default	PU/PD/Hold	Short Description
1	CE2-	O	7mA	H		Ext. memory chip enable 2
	GPIO_B1	BI		/		Bit1 of General purpose I/O port B.
2	CE1-	O	7mA	H		Ext. memory chip enable 1
	GPIO_B0	BI		/		Bit0 of General purpose I/O port B
3	UVCC	PWR	/	/		Power supply for USB
4	USBGND	PWR	/	/		USB ground
5	USBDM	A	/	H		USB data minus
6	USBDP	A	/	H		USB data plus
7	AOUTL	AO	/	/		Int. PA left channel analog output
8	PAVCC	PWR	/	/		Power supply for power amplifier
9	AOUTR	AO	/	/		Int. PA right channel analog output
10	PAGND	PWR	/	/		Power amplifier ground
11	VRO_SENSE	AI	/	/		PA Direct-drive Virtual Ground Feedback
12	VRO	AO	/	/		PA Direct-drive Virtual Ground Reference Output
13	MICIN	AI	/	/		Microphone pre-amplifier input
14	FMINL	AI	/	/		Left channel of FM line input
15	FMINR	AI	/	/		Right channel of FM line input
16	AVCC	PWR	/	/		power supply of Analog
17	AGND	PWR	/	/		Analog ground
18	VREFI	AI	/	/		Voltage reference input

19	LRADC1	AI	/	/		Low resolution A/D input 1
20	VDD	PWR	/	/		Digital Core power
21	VCC	PWR	/	/		Digital power pin
22	PWRMB	AI	/	/		POWER mode select
23	BAT	I	/	/	PD200k	Battery Voltage input.
24	DC5V	AI	/	/		5.0V Voltage
25	ON_OFF	AI				System Standby control
26	RTCVDD	PWR				RTC Power Supply
27	HOSCO	AO	/	/		High frequency crystal OSC output
28	HOSCI	AI	/	/		High frequency crystal OSC input
29	GND	PWR	/	/		Ground
30	GPIO_E0	BI	10mA	Z		Bit0 of General purpose I/O port E
	MS_BS	O		/	PD50k	MS Card Command Interface
	VCCOUT	PWR		/		3.3V VCCOUT
31	IO_VCC	PWR	/	/		IO for VCC DC-DC
32	LXVCC	PWR	/	/		VCC DC-DC pin
33	NGND	PWR	/	/		NMOS Ground
34	LXVDD	PWR	/	/		VDD DC-DC pin
35	IO_VDD	PWR	/	Z		IO for VDD DC-DC
36	VDD	PWR	/	/		Digital Core power
37	CE5-	O	7mA	H		Ext. memory chip enable 5
	GPIO_A7	BI		/		Bit7 of General purpose I/O port A
	SIRQ-	I		/	PD50k or PU50k	System external Interrupt Request
38	MRD-	O	7mA	H		Ext. memory read strobe
	GPIO_B2	BI		/		Bit2 of General purpose I/O port B

39	MWR-	O	7mA	H		Ext. memory write strobe
	GPIO_B3	BI		/		Bit3 of General purpose I/O port B
40	RB1-	I	7mA	H	PU2.5k	Nand Type flash Ready/Busy status input.
	GPIO_B6	BI		/		Bit6 of General purpose I/O port B
41	GPIO_C2	O	7mA	Z		Bit2 of General purpose I/O port C
	UART_RX	I		/		UART RX
	I2S_LR	O				I2S LR
	SPDIF_RX	I		/		SPDIF RX
42	GPIO_E3	BI	10mA	Z		Bit3 of General purpose I/O port E
	MMC_CLK1	O		/		Clock1 for MMC/SD Card
	MS_CLK	O		/	PD50k	Clock for MS Card
43	GPIO_C3	BI	7mA	Z		Bit3 of General purpose I/O port C
	UART_TX	O		/		UART TX
	I2S_DATA	O		/		I2S DATA
	SPDIF_TX	O		/		SPDIF TX
44	GPIO_E1	BI	10mA	Z		Bit1 of General purpose I/O port E
	MMC_CMD	O		/		CMD of SD/MMC card interface
	MS_BS	O		/	PD50k	BS of MS card interface
45	ALE	O	7mA	L		Address latch enable for NAND flash
	GPIO_B4	BI		/		Bit4 of General purpose I/O port B
46	CLE	O	7mA	L		Command latch enable for NAND flash
	GPIO_B5	BI		/		Bit5 of General purpose I/O port B
47	VCC	PWR	/	/		Digital power pin

48	D7	BI	7mA	L	Hold	Bit7 of ext. memory data bus
	GPIO_D7	BI		/		Bit7 of General purpose I/O port D
49	GPIO_F3	BI	10mA	Z		Bit3 of General purpose I/O port F
	MMC_D3	BI		/	PU50k	Bit3 of MMC/SD Card data bus
	MS_D3	BI		/	PD50k	Bit3 of MS Card data bus
50	D6	BI	7mA	L	Hold	Bit6 of ext. memory data bus
	GPIO_D6	BI		/		Bit6 of General purpose I/O port D
51	GPIO_F2	BI	10mA	Z		Bit2 of General purpose I/O port F
	MMC_D2	BI		/	PU50k	Bit2 of MMC/SD Card data bus
	MS_D2	BI		/	PD50k	Bit2 of MS Card data bus
52	D5	BI	7mA	L	Hold	Bit5 of ext. memory data bus
	GPIO_D5	BI		/		Bit5 of General purpose I/O port D
53	GPIO_F1	BI	10mA	Z		Bit1 of General purpose I/O port F
	MMC_D1	BI		/	PU50k	Bit1 of MMC/SD Card data bus
	MS_D1	BI		/	PD50k	Bit1 of MS Card data bus
54	D4	BI	7mA	L	Hold	Bit4 of ext. memory data bus
	GPIO_D4	BI		/		Bit4 of General purpose I/O port D
55	GPIO_F0	BI	10mA	Z		Bit0 of General purpose I/O port F
	MMC_D0	BI		/	PU50k	Bit0 of MMC/SD Card data bus
	MS_D0	BI		/	PD50k	Bit0 of MS Card data bus
56	D3	BI	7mA	L	Hold	Bit3 of ext. memory data

						bus
	GPIO_D3	BI		/		Bit3 of General purpose I/O port D
57	D2	BI	7mA	L	Hold	Bit2 of ext. memory data bus
	GPIO_D2	BI		/		Bit2 of General purpose I/O port D
58	GND	PWR	/	/		Ground
59	D1	BI	7mA	L	Hold	Bit1 of ext. memory data bus
	GPIO_D1	BI		/		Bit1 of General purpose I/O port D
60	D0	BI	7mA	L	Hold	Bit0 of ext. memory data bus
	GPIO_D0	BI		/		Bit0 of General purpose I/O port D
61	GPIO_C7	BI	7mA	Z		Bit7 of General purpose I/O port C
	SPI_SCLK	O		/		Clock of SPI
62	GPIO_C6	BI	7mA	Z		Bit6 of General purpose I/O port C
	SPI_MOSI	BI		/		MOSI of SPI
63	GPIO_C5	BI	7mA	Z		Bit5 of General purpose I/O port C
	SPI_MISO	BI		/		MISO of SPI
64	GPIO_C4	BI	7mA	Z		Bit4 of General purpose I/O port C
	SPI_SS	BI		/		SS of SPI

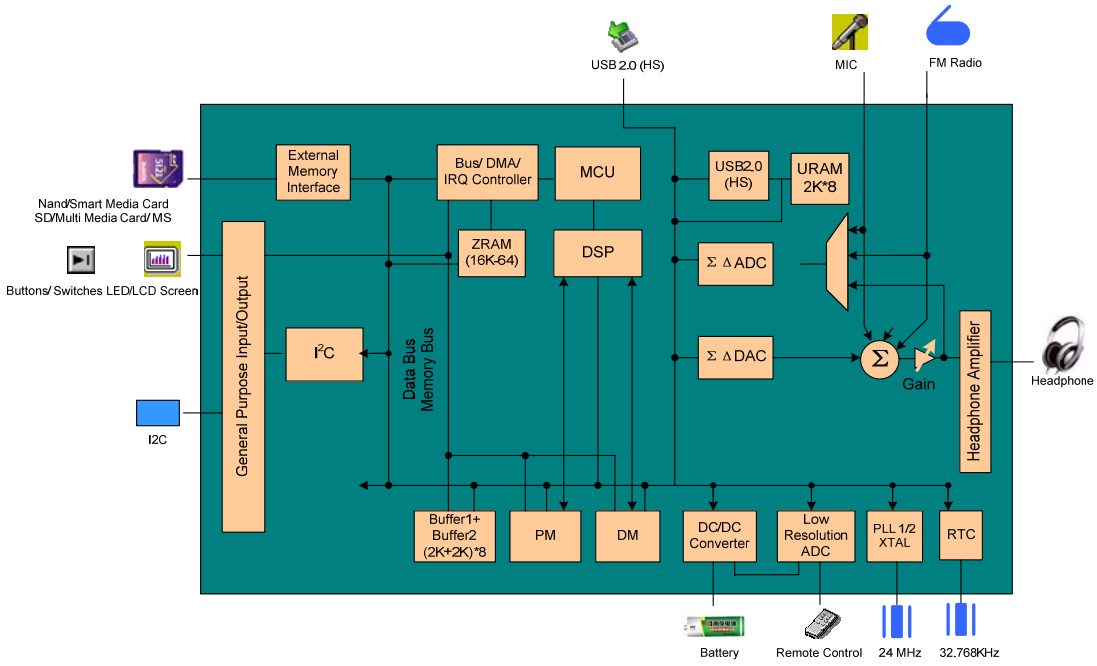
Note:

1: PWR—Power Supply
2: AI——Analog Input
3: AO——Analog Output
4: O——Output
5: I———Input
6: BI——Bidirection
7: USCU, USCL——USCHIMITCU, USCHIMITCL

8: PU——Pull up

PD——Pull down

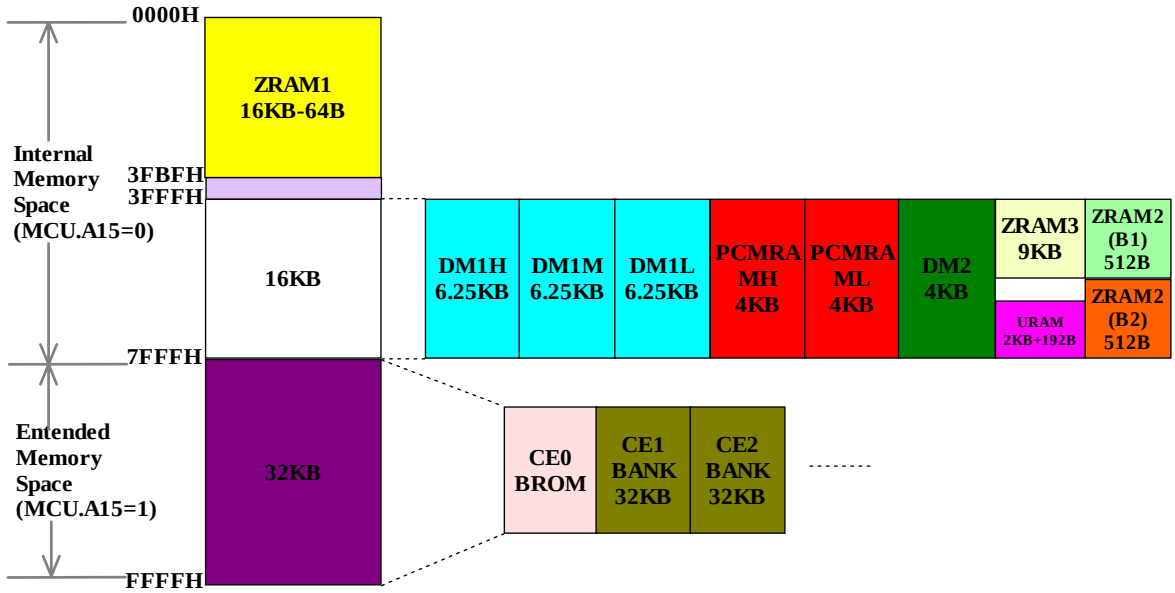
3 ATJ331X Block Diagram



4 Memory Mapping

4.1 Memory Map

ATJ331X provides both on-chip ROM and RAM memories to aid in system performance and integration.



	ZRAM1	0000H~3FBFH
	DM1H/DM1M/DM1L	4000H~58FFH
	PCMRAMH/PCMRAML	4000H~4FFFH
	DM2	4000H~4FFFH
	ZRAM3	4000H~63FFH
	URAM	7000H~78BFH
	ZRAM2(B1)	4000H~41FFH
	ZRAM2(B2)	4200H~43FFH
	CE1/CE2/CE3	8000H~FFFFH

4.1.1 Registers Description

4.1.1.1 ISRAMP (Internal SRAM Page Register, 05h)

Bits	Description	Access	Reset
7	0: DM1 is mapped to DSP 1: DM1 is mapped to MCU/DMA1/2/4/5	R/W	0
6	0: PCMRAMH is mapped to DSP 1: PCMRAMH is mapped to MCU/DMA1/2/4/5	R/W	0
5	0: PCMRAML is mapped to DSP 1: PCMRAML is mapped to MCU/DMA1/2/4/5	R/W	0
4	0: DM2 is mapped to DSP 1: DM2 is mapped to MCU/DMA1/2/4/5	R/W	0
3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+ URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2 (B1+B2)	R/W	0

5 System Control Module

5.1 Description

This chapter describes the extended 8 bit MCU with RAM access, its bus controller, direct memory access (DMA) controller, CTC module and interrupt controller.

5.2 Bus Controller

5.2.1 MCUCLK (MCU Clock Control Register, 00h)

Bits	Description	Access	Reset
7:6	**Number of Wait states for external memory access** 0 0: 0, zero wait state(default) 0 1: 1, one wait state 1 0: 2, two wait states 1 1: 3, three wait states If access internal BROM no wait state needed.	R/W	0
5:4	**MCU clock source select** 0 0: LOSC 0 1: HOSC 1 0: Reserved 1 1: MCU PLL The time needed for MCU clock source switch: （1） From LOSC to MCUPL, it has to wait for (pll_freq/losc) +1 cycle, for example losc=32768kHz, MCUPLL=60MHz, then, it has to wait for (60/0.032768)+1=1833 clocks. （2） From LOSC to HOSC, it has to wait: HOSC/ losc clock; From high frequency or PLL switch to LOSC, it has to wait for 1 clock.	R/W	0
3	Reserved	/	/
2:0	**MCU clock division control** 0 0 0 /01 (default) 0 0 1 /02 0 1 0 /04 0 1 1 /08 1 0 0 /16 1 0 1 /32 1 1 0 /64 1 1 1 /DC	R/W	0

It may take a while before MCU Clock Change. When the MCU clock is stopped (DC), there are several ways to recover the clock to non-divided LOSC clock source:

1. Push Reset button

2. POWER ON RESET
3. Alarm IRQ
4. SIRQ
5. USB wake up IRQ
6. LRADC1 IRQ

5.2.2 DMA12CD (DMA12 Clock Division Register, 029h)

Bits	Description	Access	Reset
7	Software reset. Writing 1 to this bit will reset system, after finishing it will be cleared. Its operation is equal to external reset- pin.	R/W	0
6	Software reset flag. 0: software reset not occurred, 1: software reset occurred. Writing 1 to this bit will clear it.	R/W	0
5:3	Reserved.	/	/
2:0	**DMA1/DMA2 Clock Division Control** 0 0 0 /01 0 0 1 /02 0 1 0 /04 0 1 1 /08 1 0 0 /16 1 0 1 /32 1 1 0 /64 1 1 1 /128	R/W	000

5.2.3 CESEL (Chip Enable Selection Register, 02h)

Bits	Description	Access	Reset
7	Multiplexing of GPIOA7 and CE5- 0: GPIOA7 1: CE5- When SIRQ Enabled, CE5- and GPIO is shielded for SIRQ	R/W	1
6	Multiplexing of GPIOA6 and CE4- 0: GPIOA6 1: CE4-	R/W	1

5	Multiplexing of GPIOA5 and CE3- 0: GPIOA5 1: CE3-	R/W	1
4	Multiplexing of GPIOB1 and CE2- 0: GPIOB1 1: CE2-	R/W	1
3	Multiplexing of GPIOB0 and CE1- 0: GPIOB0 1: CE1-	R/W	1
2:0	**Chip Enable Selection:** 000B, decode to CE0- 001B, decode to CE1- 010B, decode to CE2- 011B, decode to CE3- 100B, decode to CE4- 101B, decode to CE5- 110B, decode to CE6-(NO PIN) 111B, decode to CE7-(NO PIN)	R/W	000

5.2.4 MCUCTL (MCU-A15 Control Register, 04h)

Bits	Description	Access	Reset
7	Watch Dog Flag, 1 means WD reset or irq ever occurred. Writing 1 to this bit to clear it.	R/W	0
6	**External Reset flag,** 1 means external reset had been asserted, writing 1 to this bit to clear it.	R/W	0
5	**Low Bat NMI- pending.** The LBNMI- voltage can be set by the LB Register. If LBNMI- occurred, this bit will be set. Writing 1 to this bit will clear it.	R/W	0
4	Reserved	/	/

3	SIRQ trigger edge select: 0: negative edge 1:positive edge When SIRQ is enabled and this bit is set 0, the 200K PULL HIGH Register will be enabled. When SIRQ is enabled and this bit is set 1， the 200K PULL LOW Register will be enabled.	R/W	0
2	**SIRQ- Enable.** 0: disable 1: enable. SIRQ will be enabled by this bit, and it can be trigged by the signal connected to SIRQ- pin on the negative or positive edge selected by bit3 of this Register	R/W	0
1	**LBNMI- Enable.** 0: disable 1: enable.	R/W	0
0	**A15 control bit.** 0: force MCU's A15 to be 1, execute program from CE0 memory space. 1: for normal operation, the boot code after power on reset must be jp 800xh followed by an IO write to 04h to set this bit for normal operation.	R/W	0

5.2.5 GRAIO (General Random Access IO Register, 03Fh)

Bits	Description	Access	Reset
7:0	This register is a general random access IO and can be written and read by MCU/DMA1/DMA2/DMA4/DMA5	R/W	0

5.2.6 Module Reset Control Register 2

MRCR2 (Module Reset Control Register 2, 3Dh)

Bits	Description	Access	Reset
7	**RAM & ROM Bist Reset** 0 RESET 1 NORMAL	R/W	1

6	**On_OFF press status** 1: when the On_OFF Key is pressed down, the ON_OFF PIN's Voltage goes 0V。The Press Status Bit will be set to one. 0: When the On_OFF is up, the ON_OFF PIN's voltage go above 0.8V。 And then the Press Status Bit will be cleared to zero.	R/W	0
5	**ADC Reset** 0 RESET 1 NORMAL	R/W	1
4	**DAC Reset** 0 RESET 1 NORMAL	R/W	1
3	**USB Reset** 0 NORMAL 1 RESET (USB module is defaulted as reset status, but the register's default remains unchanged and is 1.)	R/W	1
2	**DMA4 Reset** 0 RESET 1 NORMAL	R/W	1
1	**IRC GPIO mapping select** 0 mapping to GPIO F5 1 mapping to GPIO C2	R/W	1
0	**DMA1 & DM2 Reset** 0 RESET 1 NORMAL	R/W	1

5.3 DMA Channel 1

5.3.1 DMA1SADDR0 (DMA1 Source Address 0 Register, 06h)

Bits	Description	Access	Reset
7:0	DMA1SA[7:0]	R/W	X

5.3.2 DMA1SADDR1 (DMA1 Source Address 1 Register, 07h)

Bits	Description	Access	Reset
7:0	DMA1SA[15:8]	R/W	X

5.3.3 DMA1SADDR3 (DMA1 Source Address 3 Register, 09h)

Bits	Description	Access	Reset
7	**External Memory Select,** 0: Internal Memory, 1: external memory	R/W	0
6	**Int. Memory select,** 0:ZRAM1, 1: DM1/PCMRAM/DM2/ZRAM2 (B1, B2, URAM)/ ZRAM3	R/W	0
5:3	Reserved	/	/
2:0	DMA1SA[25:23]	R/W	X

5.3.4 DMA1ISA (DMA1 IPM/IDM/ZRAM2 SRC Address Register, 0Ah)

Bits	Description	Access	Reset
7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2 (B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 7000h-78BFh	R/W	Xxx

5.3.5 DMA1DADDR0 (DMA1 Destination Address 0 Register, 0Bh)

Bits	Description	Access	Reset
7:0	DMA1DA[7:0]	R/W	Xxh

5.3.6 DMA1DADDR1 (DMA1 Destination Address 1 Register, 0Ch)

Bits	Description	Access	Reset
7:0	DMA1DA[15:8]	R/W	Xxh

5.3.7 DMA1DADDR3 (DMA1 Destination Address 3 Register, 0Eh)

Bits	Description	Access	Reset
7	**External Memory Select,** 0: Int. Memory, 1: external memory	R/W	0
6	**Int. Memory select,** 0: ZRAM1, 1: DM1/PCMRAM/DM2/ZRAM2 (B1, B2, URAM) /ZRAM3	R/W	0
5:3	Reserved	/	/

2:0	DMADA[25:23] CEx select bit 000: CE0- selected 001: CE1- selected 010: CE2- selected 011: CE3- selected 100: CE4- selected 101: CE5- selected 110: CE6- selected 111: CE7- selected	R/W	X

5.3.8 DMA1IDA (DMA1 IPM/IDM/ZRAM2 DST Address Register, 0Fh)

Bits	Description	Access	Reset
7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2(B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 7000h-78BFh	R/W	000

5.3.9 DMA1BCL (DMA1 Byte Counter Low, 10h)

Bits	Description	Access	Reset
7:0	DMA1BC[7:0]	R/W	Xx

5.3.10 DMA1BCH (DMA1 Byte Counter High Register, 011h)

Bits	Description	Access	Reset
7	Reserved	/	/
6:0	DMA1BC[14:8], maximum transferred byte is 32Kbytes	R/W	Xx

5.3.11 DMA1M (DMA1 Mode Register, 012h)

Bits	Description	Access	Reset
7:6	DMA1 wait state select 0 0 0 wait state 0 1 1 wait state 1 0 2 wait states 1 1 3 wait states	R/W	0
5	Reserved	/	/
4	**DMA1 DST down count,** 0: up count, 1: down count	R/W	0
3	**DMA1 SRC down count,** 0: up count, 1: down count	R/W	0
2	Reserved	/	/
1	**DMA1 DST is IO.** 0: Memory 1: IO	R/W	0
0	**DMA1 SRC is IO.** 0: Memory 1: IO	R/W	0

5.3.12 DMA1COM (DMA1 Command Register, 013h)

Bits	Description	Access	Reset
7	**DMA1 TC IRQ enable.** 0: Disable IRQ. 1: Enable IRQ when DMA1 finishes the whole block transfer.	R/W	0

6	**DMA1 Half Transfer IRQ enable.** 0: Disable IRQ. 1: Enable IRQ when DMA1 finishes half of the block transfer.	R/W	0
5	**DMA1 Continue Block Transfer enable.** 0: Disable continuous block transfer mode and bit 1 of this register will be cleared when the last byte of the block is transferred. 1: enables continuous block transfer mode and bit 1 of this register will not be cleared and SRC Address Counter/DST Address Counter/Byte Length Counter will be reloaded with their corresponding registers when DMA1 finishes the block transfer.	R/W	0
4	**DMA1 Priority** 0: DMA1 Low priority 1: DMA1 High priority. When both DMA1 Priority and DMA2 Priority are set or cleared simultaneously, the priority is in first start-first-finish style.	R/W	0
3:2	**External Trigger** 0 0 DRQ1A, UART/IR TX DRQ 0 1 DRQ1B, DSP Codec Input DRQ 1 0 DRQ1C, SPI TX DRQ 1 1 DRQ1D, SPDIF TX DRQ	R/W	0
1	**External DRQ trigger enable,** 0: Disable external DRQ trigger, 1: Enable.	R/W	0
0	**DMA1 Start.** After TC the bit will be cleared. The low-go-high edge of this bit will load SRC start address, DST start address, byte count into the current working counters.	R/W	0

5.4 DMA Channel 2

5.4.1 DMA2SA0 (DMA2 Source Address 0 Register, 014h)

Bits	Description	Access	Reset
7:0	DMA2SA[7:0]	R/W	Xx

5.4.2 DMA2SA1 (DMA2 Source Address 1 Register, 015h)

Bits	Description	Access	Reset
7:0	DMA2SA[15:8]	R/W	Xx

5.4.3 DMA2SA3 (DMA2 Source Address 3 Register, 017h)

Bits	Description	Access	Reset
7	External Memory Select, 0: Internal Memory,1: external memory	R/W	0
6	Internal Memory select 0:ZRAM1, 1: DM1/PCMRAM/DM2/ZRAM2 (B1, B2, URAM) /ZRAM3	R/W	0
5:3	Reserved	/	/
2:0	DMA2SA[25:23] CEx select bit 000: CE0- selected 001: CE1- selected 010: CE2- selected 011: CE3- selected 100: CE4- selected 101: CE5- selected 110: CE6- selected 111: CE7- selected	R/W	X

5.4.4 DMA2ISA (DMA2 IPM/IDM/ZRAM2 SRC Address Register, 018h)

Bits	Description	Access	Reset
7:3	Reserved	/	/

2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2 (B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 7000h-78BFh	R/W	Xxx

5.4.5 DMA2ISA0 (DMA2 Destination Address 0 Register, 019h)

Bits	Description	Access	Reset
7:0	DMA2DA[7:0]	R/W	Xx

5.4.6 DMA2ISA1 (DMA2 Destination Address 1 Register, 01Ah)

Bits	Description	Access	Reset
7:0	DMA2DA[15:8]	R/W	Xx

5.4.7 DMA2ISA3 (DMA2 Destination Address 3 Register, 01Ch)

Bits	Description	Access	Reset
7	**External Memory Select,** 0: Internal Memory, 1: External memory	R/W	0
6	Internal Memory select 0: ZRAM1, 1: DM1/PCMRAM/DM2/ZRAM2 (B1, B2, URAM) /ZRAM3	R/W	0
5:3	Reserved	/	/

2:0	DMA2DA[25:23] CEx select bit 000: CE0- selected 001: CE1- selected 010: CE2- selected 011: CE3- selected 100: CE4- selected 101: CE5- selected 110: CE6- selected 111: CE7- selected	R/W	X

5.4.8 DMA2IDA (DMA2 IPM/IDM/ZRAM2 DST Address Register, 01Dh)

Bits	Description	Access	Reset
7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2 (B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 7000h-78BFh	R/W	Xxx

5.4.9 DMA2BCL (DMA2 Byte Count low Register, 01Eh)

Bits	Description	Access	Reset
7:0	DMA2BC[7:0]	R/W	Xx

5.4.10 DMA2BCH (DMA2 Byte Count High Register, 01Fh)

Bits	Description	Access	Reset
7	Reserved	/	/
6:0	DMA2BC[14:8]	R/W	Xx

5.4.11 DMA2M (DMA2 Mode Register, 020h)

Bits	5.4.11.1 Description	Access	Reset
7:6	DMA2 wait state select 0 0 0 wait state 0 1 1 wait state 1 0 2 wait states 1 1 3 wait states	R/W	0
5	Reserved	/	/
4	DMA2 DST down count. 0: Up count, 1: Down count.	R/W	0
3	DMA2 SRC down count. 0: Up count, 1: Down count.	R/W	0
2	Reserved	/	/
1	DMA2 DST is IO. 0: Memory, 1: IO.	R/W	0
0	DMA2 SRC is IO. 0: Memory, 1: IO.	R/W	0

5.4.12 DMA2COM (DMA2 Command Register, 021h)

Bits	Description	Access	Reset
7	DMA2 TC IRQ Enable. 0: Disable IRQ. 1: Enable IRQ when DMA2 finishes whole block transfer.	R/W	0

6	DMA2 Half Transfer IRQ enable. 0: Disable IRQ. 1: Enable IRQ when DMA2 finishes half of the block transfer.	R/W	0
5	DMA2 Continue Block Transfer Enable. 0: disables continuous block transfer mode and bit 1 of this register will be cleared when the last byte of the block is transferred. 1 enables continuous block transfer mode and bit 1 of this register will not be cleared and SRC Address Counter/DST Address Counter/Byte Length Counter will be reloaded with their corresponding registers when DMA2 finishes the block transfer.	R/W	0
4	DMA2 Priority, 0: DMA2 low priority, 1: DMA2 high priority When both DMA1 Priority and DMA2 Priority are set or cleared simultaneously, the priority is in first start first finished style.	R/W	0
3:2	External DRQ trigger select 0 0 DRQ2A, UART/IR RX DRQ 0 1 DRQ1B, DSP Input DRQ 1 0 DRQ2C, SPI RX DRQ 1 1 DRQ2D, SPDIF RX DRQ	R/W	0
1	External DRQ trigger enable, 0: Disable external DRQ trigger, 1: Enable.	R/W	0
0	DMA2 Start. After TC the bit will be cleared. The low-go-high edge of this bit will load SRC start address, DST start address, byte count into the current working counters.	R/W	0

5.5 CTC

5.5.1 CTCPRES (CTC Prescale Register, 022h)

Bits	Description	Access	Reset
7	CTC1 enable 0: Disable, 1: Enable.	R/W	0
6	CTC2 enable 0: Disable, 1: Enable.	R/W	0

5	CTC1 IRQ pending bit Writing 1 to this bit will clear it.	R/W	0
4	CTC2 IRQ pending bit Writing 1 to this bit will clear it.		
3:0	Pre-scale register. 0000: CTC1/CTC2 clock is /1 of the HOSC. 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 1001: /512 Others are reserved	R/W	0

NOTE: CTC1 is a Non-Maskable interrupt for Z80, but CTC2 is a maskable interrupt for z80.
Please refer to register 25h bit7.

5.5.2 CTCTPL (CTC T Period Low Register, 023h)

When 25h.bit7 = 0

CTCTPL (CTC1 T Period Low Register, 023h)

Bits	Description	Access	Reset
7:0	TPERIOD[7:0], period low byte register of CTC	RW	xx

When 25h.bit7 = 1

CTCTPL(CTC2 T Period Low Register, 023h)

Bits	Description	Access	Reset
7:0	TPERIOD[7:0], period low byte register of CTC	RW	xx

5.5.3 CTCTPH (CTC T Period High Register, 024h)

When 25h.bit7 = 0

CTCTPH (CTC1 T Period High Register, 024h)

Bits	Description	Access	Reset
7:0	TPERIOD[15:8], period register of CTC	RW	xx

When 25h.bit7 = 1

CTCTPH (CTC2 T Period High Register, 024h)

Bits	Description	Access	Reset
7:0	TPERIOD[15:8], period register of CTC	RW	xx

NOTE: The two T period registers are both for CTC1 and CTC2, using a bit to select page. The bit is 25h.bit7. When 25h.bit7 is “0”, the two registers are for CTC1. Otherwise, they are for CTC2.

5.6 Interrupt Controller

NOTE: all interrupt PENDING bits will not be influeneced by ENABLE bit.

5.6.1 DMACISTA (DMA/CTC IRQ Status Register, 025h)

Bits	Description	Access	Reset
7	CTC1/2 T period register select. 0: T period resisters are for CTC1 1: T period resisters are for CTC2	RW	0
6	DMA2 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
5	DMA2 End Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
4	DMA1 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
3	DMA1 End Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
2	SIRQ- Pending, writing 1 to this bit will clear it.	R/W	0
1	Reserved.	/	/
0	Software controlled DMA1/DMA2 reset signal, The low-go-high edge of this bit will generate a pulse to reset DMA1/DMA2 state machine, bytes counter, and clear H.W DRQ, etc status. After the pulse the bit will be cleared to 0.	R/W	0

5.6.2 MISTA (Master Interrupt Status Register, 026h)

Bits	Description	Access	Reset
7	A/D Interrupt(3) 1. Wire-Control IRQ 2. Audio ADC IRQ 3. Charge Status IRQ This bit will be automatically cleared only when all the A/D INT pending bits are cleared, otherwise it is unchanged.	R/W	0
6	Reserved	/	/
5	RTC Interrupt.(4) 1. Watch Dog IRQ 2. RTC Timer IRQ 3. RTC Alarm IRQ 4. 2HZ RTC IRQ This bit will be automatically cleared only when all the RTC INT pending bits are cleared, otherwise it is unchanged.	R/W	0
4	DMA1/2/4/SD/MMC/MS/CTC Interrupt (6) 1. DMA1 TC/Half Transfer IRQ 2. DMA2 TC/Half Transfer IRQ 3. DMA4 IRQ 4. SD/MMC Transfer end IRQ，FIFO IRQ or SDIO IRQ 5. MS Transfer Finished IRQ 6. CTC IRQ This bit will be automatically cleared only when all the DMA1/2/4/SD/MMC/MS/CTC INT pending bits are cleared, otherwise it is unchanged.	R/W	0
3	SIRQ/I2C/SPI/RB Interrupt(4) 1. External IRQ (SIRQ) 2. I2C IRQ 3. SPI RX/TX IRQ 4. RB1/RB2 RDY IRQ or State Machine Ending IRQ This bit will be automatically cleared only when all the SIRQ/I2C/SPI/RB INT pending bits are cleared, otherwise it is unchanged.	R/W	0
2	Reserved	R/W	0

1	UART/IR/SPDIF/IRC Interrupt(2) 1. UART/IR RX IRQ 2. SPDIF Block In IRQ or Data In IRQ 3. IRC RX IRQ This bit will be automatically cleared only when all the UART/IR/SPDIF/IRC INT pending bits are cleared, otherwise it is unchanged.	R/W	0
0	DSP interrupt (4) Pending, This bit will be automatically cleared only when All the DSP INT pending bit is cleared, otherwise unchanged.	R/W	0

5.6.3 MIEN (Master Interrupt Enable Register, 027h)

Bits	Description	Access	Reset
7	A/D interrupt Enable, 0: Disable, 1: Enable.	R/W	0
6	Reserved	/	/
5	RTC interrupt Enable, 0: Disable, 1: Enable.	R/W	0
4	DMA1/2/4/SD/MMC/MS/CTC Interrupt Enable. 0: Disable. 1: Enable	R/W	0
3	SIRQ/I2C/SPI/RB Interrupt Enable. 0: Disable, 1: Enable.	R/W	0
2	USB Interrupt Enable, 0: Disable, 1: Enable.	R/W	0
1	UART/IR/SPDIF/IRC Interrupt Enable, 0: Disable, 1: Enable.	R/W	0
0	DSP Interrupt Enable, 0: Disable, 1: Enable.	R/W	0

6 USB2.0 OTG

6.1 Description

Actions USB2.0 OTG (AOTG) is a Dual-Role-Device (DRD) controller which complies with On-The-Go Supplement to the USB2.0 Specification V1.0a.

6.2 Feature

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a;
- UTMI+ level2 Transceiver Macrocell Interface;
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP);
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (no HUB support);
- Supports full-speed or high-speed in peripheral mode;
- Supports 2 IN endpoint and 1 OUT endpoint except endpoint0;
- Supports bulk Isochronous and Interrupt transfer;
- Partially configurable endpoint buffer size, endpoint type and single, double triple or quad buffering;
- Integrated synchronous RAM as endpoint FIFOs;
- Supports suspend, resume and power managements function;
- Support remote wakeup;
- Support Udisk mode high speed DMA panel;

7 I2C Interface

7.1 Description

I2C can be configured as either a master or slave device. In master mode it generates the clock (I2C_SCL) and initiates transactions on the data line (I2C_SDA). Data on the I2C bus is byte oriented. Multi-Master mode, 10-bit address and Hi-speed mode are not supported.

7.2 Feature

- Two-wire Serial interface.
- 100Khz and 400Khz Compatibility

7.3 Register Description

I2C module registers

Address	Name	Description
84H	I2CADDR	I2C Address Register
85H	I2CCTL	I2C Control Register
86H	I2CSTA	I2C Status Register
87H	I2CDAT	I2C Data Register

7.3.1 I2CADDR (I2C Address Register, 084h)

This register is for setting I2C slave address in master or slave mode.

Bits	Description	Access	Reset
7:1	I2C Slave Address.	R/W	0

0	In master mode, R/W control bit In slave mode: I2C Slave Address Match. 0: match, send IRQ to MCU; 1: not match, do not send IRQ In master mode, address 7-bit is used to setting the slave address, so the I2C data register just store the data. In slave mode, address 7-bit is used to compare with the address that master sending out. So the I2C data register can store the address and data.	R/W	0

7.3.2 I2CCTL (I2C Control Register, 085h)

This register is for enabling I2C and I2C IRQ, selecting I2C operating mode, ACK generation.

Bits	Description	Access	Reset
7	I2C Enable. 0: Disable 1: Enable I2C receive and transmit channel.	R/W	0
6	In master mode, operating mode select. 0: standard (100kbps) 1: fast (400kbps) In slave mode, Start IRQ enable. 0: Disable 1: Enable	R/W	0
5	I2C IRQ enable, 0:disable, 1:enable	R/W	0
4	I2C master or slave select. 0:master, 1:slave	R/W	0
3:2	I2C cond [1..0]. generates a bus control. (master mode only) 0 0 no effect 0 1 generate start condition 1 0 generate stop condition 1 1 SCL will be released to high level to generate the repeated start condition	R/W	0
1	Writing 1 to this bit will release the clock and data line to idle.	R/W	0
0	In transmitting ACK —ACK enable. Controls generation of an ACK signal in receiving mode 1: Do not generate an ACK at 9th SCL , 0: Generate an ACK signal at 9th SCL. In receiving ACK — Last Received Bit. Use the read only bit to check the ACK signals from the receiver (slave), or to monitor SDA operation of SDA when writing 11 to control reg bit[3..2] for repeated starts.	R/W	0

7.3.3 I2CSTA (I2C Status Register, 086h)

This register is for displaying current I2C status.

Bits	Description	Access	Reset
7	I2C Buffer Flag. Automatically cleared when I2C data reg is written or read Automatically set and the buffer is empty in transmit mode or the buffer is full in receiving mode. Writing 1 to this bit will clear it. transmit 0: Transmit in progress 1: Transmit complete receive 0: Receive in progress 1: Receive complete	R/W	0
6	I2C STOP bit. This bit is cleared when the I2C mode is disabled or when the start bit was detected at last. Writing 1 to this bit will clear it. 1: Indicate that the STOP bit was detected at last 0: STOP bit was not detected at last	R/W	0
5	I2C START bit. This bit is cleared when the I2C mode is disabled or when the stop bit was detected at last. Writing 1 to this bit will clear it. 1: Indicate that the START bit was detected at last 0: START bit was not detected at last	R/W	0
4	I2C R/W bit. Read/Write bit information. This bit holds the R/W bit information following the last address match. This bit is valid only from the address match to the next start bit, stop bit or NAK bit. 1: Read 0: Write	R/W	0
3	I2C D/A. Data/Address bit 1: indicate the last byte received or transmitted was data. 0: indicate the last byte received or transmitted was address.	R/W	0
2	I2C IRQ Pending bit. Writing 1 to this bit will clear it.	R/W	0

1	I2C overflow bit. Writing 1 to this bit will clear it. 1: A new byte is received while the previous byte has not been read 0: No overflow	R/W	0
0	Reserved	/	/

NOTE: Whenever overflow is set, NAK will occur automatically.

7.3.4 I2CDAT (I2C Data Register, 087h)

This register is for writing data to or reading data from I2C Data Register.

Bits	Description	Access	Reset
7:0	I2C Data/Address[7:0]	R/W	00

8 SPI Interface

8.1 Description

ATJ331X SPI can be configured as either a master or a slave device. During a SPI transfer, data is shifted out and shifted in (transmitted and received) simultaneously. The SPI_SCK line synchronizes the shifting and sampling of the information. It is an output when the SPI is configured as a master or an input when the SPI is configured as a slave.

SPI uses a couple of parameters called clock polarity (CPOL) and clock phase (CPHA) to determine when data is valid with respect to the clock signal. CPOL determines whether the leading edge is defined to be the rising or falling edge of the clock (and vice versa for the trailing edge). CPHA determines whether the leading edge is used for setup or sample (and vice versa for the trailing edge). The following table summarizes the various settings.

CPOL/CPHA	Leading Edge	Trailing Edge	SPI Mode
0/0	Sample, rising	Setup, falling	0
0/1	Setup, rising	Sample, falling	1
1/0	Sample, falling	Setup, rising	2
1/1	Setup, falling	Sample, rising	3

8.2 Feature

- Master and slave modes of operation.
- DMA interface supporting data transfer from bulk memory to the synchronous serial interface
- Support SPI full-duplex mode and half-duplex mode.
- Master and slave mode boot options to download the code image from the SPI norflash.

8.3 Register Description

SPI module registers

Address	Name	Description
A8H	SPICTL	SPI Control Register
A9H	SPIIRQ	SPI IRQ Register
AAH	SPISTA	SPI Status Register
ABH	SPICLKDIV	SPI Clock Divide Control Register
ACH	SPIDAT	SPI Data Register
ADH	SPIBCL	SPI Byte Count Low Register
AEH	SPIBCH	SPI Byte Count High Register

8.3.1 SPICTL (SPI Control Register, A8h)

This register is used for enabling SPI module, selecting SPI mode and SPI SS output voltage.

Bits	Description	Access	Reset
7	**SPI Enable** 0: Disable; 1: Enable SPI receiving and transmiting channel	R/W	0
6	**SPI master/slave select** 0: Master 1: Slave	R/W	0
5	**LSB/MSB First Select** 0: Transmit and receive MSB first 1: Transmit and receive LSB first	R/W	0
4	**SPI SS pin control output,** this bit is valid only in master mode 1: Output high 0: Output low	R/W	1

3:2	**SPI mode select** CPOL CPHA 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3	R/W	11
1	**Two wire mode enable bit** 0: Normal 4 wire mode 1: Two wire mode, use two pins only, SPI_CLK and SPI_MOSI	R/W	00
0	**SPI full-duplex or half-duplex mode select** 0: Full-duplex mode 1: Half-duplex mode	R/W	0

8.3.2 SPIIRQ (SPI IRQ Register, A9h)

This register is for enabling SPI DRQ/IRQ and selecting SPI DRQ/IRQ trigger threshold.

Bits	Description	Access	Reset
7	**SPI TX DRQ Enable** 0: Disable 1: Enable	R/W	0
6	**SPI RX DRQ Enable** 0: Disable 1: Enable	R/W	0
5	**SPI TX IRQ/DRQ trigger threshold Control.** 0: Trigger SPI TX IRQ/DRQ when SPI TX FIFO is half empty 1: Trigger SPI TX IRQ/DRQ when SPI TX FIFO is empty	R/W	0
4	**SPI RX IRQ/DRQ trigger threshold Control.** 0: Trigger SPI RX IRQ/DRQ when SPI RX FIFO is half full 1: Trigger SPI RX IRQ/DRQ when SPI RX FIFO is not empty	R/W	0
3	**SPI TX IRQ Pending,** 0: No TX IRQ Pending 1: TX IRQ Pending. Writing 1 to this bit will clear it.	R/W	0
2	**SPI RX IRQ Pending** 0: No RX IRQ Pending 1: RX IRQ Pending. Writing 1 to this bit will clear it.	R/W	0
1	**SPI TX IRQ Enable** 0: Disable, 1: Enable	R/W	0
0	**SPI RX IRQ Enable** 0: Disable, 1: Enable	R/W	0

8.3.3 SPISTA (SPI Status Register, AAh)

This register is used for displaying current SPI FIFO status.

Bits	Description	Access	Reset
7	**SPI TX FIFO Empty** 0: Not empty 1: Empty	R	1
6	**SPI TX FIFO Full** 0: Not full 1: Full	R	0
5	**SPI RX FIFO Empty** 0: Not empty 1: Empty	R	1
4	**SPI RX FIFO Full** 0: Not full 1: Full	R	0
3	**SPI TX FIFO error Pending.** Writing 1 to this bit will clear it and reset the TX FIFO, otherwise it is unchanged.	R/W	0
2	**SPI RX FIFO error Pending.** Writing 1 to this bit will clear it and reset the TX FIFO, otherwise it is unchanged.	R/W	0
1	**SPI Transfer Complete** This bit is set to 1 at the end of an SPI transfer, and cleared by the read or write to the SPI Data Register.	R/W	0
0	Reserved	/	/

8.3.4 SPICLKDIV (SPI Clock Divide Control Register, ABh)

This register is used for setting SPI source clock divide factor, and selecting SPI read mode.

Bits	Description	Access	Reset
7	**SPI read clock delay enable bit (valid only in half-duplex mode)** 0: Disable clock delay 1: Enable clock delay	R/W	0
6:0	**SPI Clock Divide Factor** (SPICLKFactor) [6:0] if SPI Clock Divide Factor is 0, SPI CLK = MCU PLL, other SPI CLK = (MCU PLL) / (SPICLKFactor[6:0]*2)	R/W	1111111

8.3.5 SPIDAT (SPI Data Register, ACh)

This register is used for writing data to SPI TX FIFO or reading data from SPI RX FIFO.

Bits	Description	Access	Reset
7:0	**SPI Data[7:0]** Writing this field will send 1 byte to 8bitx8 levels depth SPI FIFO. Reading this field will fetch 1 byte from 8bitx8 levels depth SPI FIFO.	R/W	X

8.3.6 SPIBCL (SPI Bytes Count Low Register, ADh)

This register is used for setting SPI bytes counter low bits in the SPI norflash mode.

Bits	Description	Access	Reset
7:0	**Bytes Counter Low bits [7: 0]**	R/W	0

8.3.7 SPIBCH (SPI Bytes Count High Register, AEh)

This register is used for setting SPI bytes counter high bits, selecting SPI data I/O mode and high read rate mode delay time in the SPI norflash mode.

Bits	Description	Access	Reset
7	**SPI data I/O mode select** 0: 1x I/O mode select 1: 2x I/O mode select	R/W	0
6	Reserved	/	/
5:4	**SPI read clock delay time (valid when SPI read clock delay is enabled)** 00: Delay 2 ns 01: Delay 4 ns 10: Delay 8 ns 11: Delay 12 ns	R/W	00
3	**Read Start Control**, write 1 to start Read clock (when the transfer is finished, this bit will be cleared antomatically)	R/W	0

2	**SPI write or read select bit.** 0: Select write 1: Select read	R/W	0
1:0	**Bytes Counter High bits [1: 0]**	R/W	0

9 UART Interface

9.1 Description

UART is dedicated to asynchronous serial communication with FIFO as data buffer for full-duplex operation. UART protocol contains a start bit, 5~8 data bits, a parity bit and a stop bit. The start bit must be 0 and the stop bit must be 1. Before communication, UART operation mode must set to be the same as remote terminal, such as baud rate, number of data bits, even/odd/no parity etc. Baud rate is up to 1.5MBaud and LSB first in TX/RX.

Two 8-level by 8 bits FIFO are used to buffer data for TX and RX.

9.2 Feature

It is the high-speed data transmission with rate up to 1.5Mbps in UART mode.

9.3 Register Description

UART Module Registers

Address	Name	Description
79H	BAUDRATE	UART Baud Rate Register
7AH	UART2CTL	UART Control Register
7BH	UAIRDAT	UART FIFO DATA Register
7CH	Reserved	Reserved
7DH	UARTMS	UART Mode & FIFO Status Register
7EH	UARTRQS	UART DRQ/IRQ Enable/Status Register

UART Baud Rate Register

Prescale Value	13		1.625		1	
Baud Rate	**Divisor**	**%Error**	**Divisor**	**%Error**	**Divisor**	**%Error**
600	192	0.16%	-	-	-	-
1200	96	0.16%	-	-	-	-
1800	64	0.16%	-	-	-	-
2000	58	0.53%	-	-	-	-
2400	48	0.16%	-	-	-	-
3600	32	0.16%	256	0.16%	-	-
4800	24	0.16%	192	0.16%	-	-
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
38400	3	0.16%	24	0.16%	39	0.16%
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	-	-	4	0.16%	-	-
460800	-	-	2	0.16%	-	-
750000	-	-	-	-	2	0.00%
921600	-	-	1	0.16%	-	-
1500000	-	-	-	-	1	0.00%

9.3.1 BAUDRATE (UART Baud Rate Register, 079h)

This register is used for setting UIR baud rate.

Bits	Description	Access	Reset
7:0	Baud rate generator, clock division	R/W	00

9.3.2 UARTCTL (UART Control Register, 07Ah)

This register is used for selecting UART clock pre-scale, parity, stop bits, bits per

transmission.

Bits	Description	Access	Reset
7:6	Clock pre-scale select Bit 7 6 Pre-scale 0 0 /13 0 1 /13 1 0 /1.625 1 1 /1	R/W	0
5:3	Bit 5: STKP, Stick parity Bit 4: EPS, Even parity Bit 3: PEN, Parity enable PEN EPS STKP Selected Parity 0 x x None 1 0 0 Odd 1 1 0 Even 1 0 1 logic 1 1 1 1 logic 0	R/W	0
2	STOP select, if this bit is 0, 1 stop is generated in transmission. If this bit is 1 and 5 bits transmission is selected, 1.5 stop bit is generated. If this bit is 1 and 6/7/8 bits transmission is selected, 2 stop bits are generated. The receiver always checks 1 stop bit only.	R/W	0
1:0	WL[1:0], bits per transmission WL1 0 Bit per transmission 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits	R/W	0

9.3.3 UARTFDAT (UART FIFO DATA Register, 07Bh)

This register is used for writing data to UIR TX FIFO or reading data from UIR RX FIFO.

Bits	Description	Access	Reset
7:0	UART FIFO Data, writing to this port will write data to UART TX FIFO, reading from this port will read data from UART RX FIFO	R/W	x

9.3.4 UARTMS (UART Mode & FIFO Status Register, 07Dh)

This register is used for displaying the current UART FIFO status.

Bits	Description	Access	Reset
7	Reserved	R/W	0
6	Reserved	R/W	0
5	UART TX FIFO Full. 1: full, 0: not full.	R	0
4	UART RX FIFO Empty. 1: empty, 0: not empty.	R	1
3	Reserved	R/W	0
2:0	Reserved	R/W	0

9.3.5 UARTRQS (UART DRQ/IRQ Enable/Status Register, 07Eh)

This register is used for enabling UIR, selecting UIR DRQ/IRQ trigger threshold, and displaying current UIR FIFO status.

Bits	Description	Access	Reset
7	UART/IR enable, 0:disable, 1:enable	R/W	0
6	FIFO mode control, for all UART FIFO 0: Issue DRQ when vacancy in TX FIFO or issue IRQ at least one data in RX FIFO, 1: Issue DRQ/IRQ when TX FIFO is half empty or RX FIFO is half full	R/W	0
5	UART/IR Receive Error*, 0: Receiving OK 1: Receiving error occurs. Writing 1 to this bit will clear the bit, otherwise the bit is unchanged.	R/W	0
4	UART/IR RX FIFO Error Writing 1 to this bit will clear it and reset the FIFO.	R/W	0
3	UART/IR TX FIFO Error Writing 1 to this bit will clear it and reset the FIFO.	R/W	0
2	UART/IR RX IRQ Pending Writing 1 to the bit to clear it, while 0 unchanged.	R/W	0

1	UART/IR IRQ/DRQ Enable. 0: Disable, 1: Enable.	R/W	0
0	UART TX FIFO Empty 0: Not empty 1: Empty	R	1

10 Infrared Remote Control Interface

10.1 Introduction

The infrared remote control interface can only receive signal transmitted by remote controller. If the signal is coding according to one of the following three modes: Toshiba 9012 code, 8 bits NEC code or Philips RC5 code, it can recognize them and under controlled.

10.2 Features

- Infrared remote control hardware decoder.
- Support three infrared remote control decode modes: Toshiba 9012 code, 8 bits NEC code and Philips RC5 code.

10.3 Register Description

Infrared remote control Module includes registers are showed as following table:

IRC Module Registers

Address	Name	Description
0x78	IRCCTL	Infrared Remote Control interface control Register
0x7f	IRCSTA	Infrared Remote Control interface state Register
0x3B	IRCDAT	Infrared Remote Control interface data Register

10.3.1 IRCCTL (Infrared Remote Control Interface Control Register, 0x78)

This register is used for enabling infrared remote control interface, selecting the infrared remote control coding mode and IRCDAT mapping type.

Bits	Description	Access	Reset

7	Infrared remote control interface enable. 0: IRC disable. 1: IRC enable.	R/W	0
6:5	Infrared remote control coding mode select. 00: 9012 code 01: 8 bits NEC code 10: RC5 code 11: Reserved	R/W	00
4	Reserved	/	/
3	IRC IRQ enable 0: Disable 1: Enable	R/W	0
2:1	IRCDAT mapping control bit 00: IRCDAT mapping to IRCKDC 01: IRCDAT mapping to IRCLUC 10: IRCDAT mapping to IRCHUC 11: IRCDAT mapping to IRCAKDC	R/W	00
0	Reserved	/	/

10.3.2 IRCSTA (Infrared Remote Control Interface State Register, 0x7f)

This register is used for displaying IRC status.

Bits	Description	Access	Reset
7	IRC flag. Automatically set when the IRC is receiving data, automatically clear when the data has been received. 1: receiving in progress 0: receiving complete	R	0
6	User code do not match pending bit. Automatically clear when new user code matches, otherwise do not change. 0: user code match. 1: user code does not match.	R	0
5	Key data code verify error pending bit. Automatically clear when new user code matches, otherwise do not change. 0: key data code verification ok. 1: key data code verification error.	R	0

4	IRC receive overflow pending bit, write 1 to this bit will clear it, otherwise don't change. 0: IRC receiving not overflow. 1: IRC receiveing overflow.	R/W	0
3	IRC IRQ pending bit. Write 1 to this bit will clear it, otherwise don't change.	R/W	0
2:1	Reserved	/	/
0	IRC repeat flag detect bit. Write 1 to this bit will clear it, otherwise don't change. 0: Repeat code is not detected. 1: Repeat code is detected.	R/W	0

NOTE: IRC will request IRQ only when user code matches and key data code verification is ok. The mechanism avoid IRQ request when receive error.

10.3.3 IRCLUC (Infrared Remote Control Low User Code Register, 0x3b)

This register is used for storing IRC low user code.

Bits	Description	Access	Reset
7:0	IRC user code [7:0]	R/W	0x00

10.3.4 IRCHUC (Infrared Remote Control High User Code Register, 0x3b)

This register is used for storing IRC high user code.

Bits	Description	Access	Reset
7:0	IRC user code [15:8]	R/W	0x00

10.3.5 IRCKDC (Infrared Remote Control Key Data Code Register, 0x3b)

This register is used for storing IRC key data code, it is read only.

Bits	Description	Access	Reset
7:0	IRC key data code [7:0]	R	0x00

10.3.6 IRCAKDC (Infrared Remote Control Anti Key Data Code Register, 0x3b)

This register is used for storing IRC anti key data code; it is read only for debug.

Bits	Description	Access	Reset
7:0	IRC anti key data code [7:0]	R	0x00

11 SPDIF Interface

11.1 Description

SPDIF is the abbreviation of Sony/Philips digital interface. The interface is primarily intended to carry stereophonic program, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible. Please refer to SPDIF standard documents for more detail information.

11.2 Register Description

SPDIF Module Registers

Address	Name	Description
80H	SPDIFCTL	SPDIF Control Register
81H	SPDIFSTA	SPDIF Status Register
82H	SPDIFDAT	SPDIF FIFO DATA Register
83H	SPDIFCH	SPDIF Channel Status Register

11.2.1 SPDIFCTL (SPDIF Control Register, 080h)

This register is used for enabling SPDIF and SPDIF DRQ/IRQ, selecting SPDIF DRQ/IRQ trigger threshold, and resetting SPDIF FIFO.

Bits	Description	Access	Reset
7	SPDIF Enable 0: Disable, 1: Enable.	R/W	0
6:5	Reserved	/	/
4	SPDIF DRQ trigger threshold control 0: Issue DRQ when vacancy in TX FIFO or issue IRQ at least one data in RX FIFO, 1: Issue DRQ/IRQ when TX FIFO is half empty or RX FIFO is half full	R/W	0

3	SPDIF DRQ Enable 0: Disable, 1: Enable.	R/W	0
2	SPDIF FIFO Reset 0: FIFO reset valid 1: FIFO reset invalid.	R/W	0
1	SPDIF Block In IRQ Enable 0: Disable, 1: Enable.	R/W	0
0	SPDIF Data In IRQ Enable 0: Disable, 1: Enable.	R/W	0

11.2.2 SPDIFSTA (SPDIF Status Register, 081h)

This register is used for displaying current SPDIF FIFO status.

Bits	Description	Access	Reset
7	SPDIF TX FIFO Full. 1: Full	R	0
6	SPDIF RX FIFO Empty. 1: Empty	R	1
5	SPDIF Block in IRQ pending Writing 1 to this bit will clear it, while 0 unchanged.	R/W	0
4	SPDIF Data in IRQ pending. Writing 1 to this bit will clear it, while 0 unchanged.	R/W	0
3	SPDIF TX FIFO error Pending. Writing 1 to this bit will clear it, otherwise unchanged.	R/W	0
2	SPDIF RX FIFO error Pending. Writing 1 to this bit will clear it, otherwise unchanged.	R/W	0
1	SPDIF Receive error Pending. Writing 1 to this bit will clear it, otherwise unchanged.	R/W	0
0	SPDIF TX FIFO Empty. 0: Empty, 1: Not empty.	R	0

11.2.3 SPDIFDAT (SPDIF FIFO DATA Register, 082h)

This register is used for writing data to SPDIF TX FIFO or reading data from SPDIF RX FIFO.

Bits	Description	Access	Reset

7:0	SPDIF FIFO DATA, Write: SPDIF TX FIFO. Read: SPDIF RX FIFO.	R/W	xxh

11.2.4 SPDIF Channel Status Register

For RX:

There is 32 bits status per 192 frames transfer. All these 4-byte status bits are mapped into this register. An internal read pointer is used to point to the current byte from which data will be returned at the next read. The internal read pointer increases after a read from this register. When SPDIF received all 192 frames of a block, SPDIF IRQ will be issued to notice MCU to read channel status. The internal pointer will be cleared when SPDIF is issued.

For TX:

Another 4 bytes status are also implemented for transmit, which are mapped into this register also. An internal write pointer is used to point to the byte position for next write. When read from this register, the internal write pointer will be cleared to point to the first byte of TX channel status. The write pointer will move to the next byte after a write to this register.

11.2.5 SPDIFCH (SPDIF Channel Status Register, 083h)

This register is used for setting SPDIF channel status.

Bits	Description	Access	Reset
7:0	SPDIF Channel status	R/W	xxh

12 Clock Management Unit

12.1 Description

ATJ331X has a low frequency oscillator, which can choose built-in source or external one. It also has a RTC (Real Time Clock) with the alarm IRQ. The alarm IRQ can wake up the system. For protection purpose, this chip also has the watch dog circuit. It also has a Timer with IRQ.

12.2 Feature

- An individual power supply pin: RTCVDD;
- Built-in a 32k oscillator
- Internal or external oscillator optional
- RTC with a alarm IRQ which can wake up the system
- 2Hz IRQ
- A Timer with IRQ
- A watch dog which can be configured IRQ or Reset optional

12.3 Register Description

12.3.1 RTC Control Register

IO address	Mnemonic	Description
0x43	RTC_CTL0	RTC Control 0 register
0x49	RTCREGUPDATE	RTC Register update Register
0x4a	RTC_CTL1	RTC Control 1 register
0x4b	TimerLB	Timer low Byte
0x4c	TimerMB	Timer middle Byte
0x4d	TimerHB	Timer high Byte
0x4e	WDCtl	Watch dog control register

When 43h.bit4 = 0

0x44	RTCTimeS	RTC Time Second Register
0x45	RTCTimeMin	RTC Time Minute Register
0x46	RTCTimeH	RTC Time Hour Register
0x47	RTCTimeD	RTC Time Day Register
0x48	RTCTimeMon	RTC Time Month Register

When 43h.bit4 = 1

0x44	RTCTimeYear	RTC Time Year Register
0x45	RTCAlmS	RTC Alarm Second Register
0x46	RTCALMM	RTC Alarm Minute Register
0x47	RTCALMH	RTC Alarm Hour Register
0x48	RTCrdm	RTC Random access Register

NOTE:

The following Register marked by RTCVDD, means “The register’s power is supplied by RTCVDD. And the register is reset by RTCVDD_OK.”

And that marked by VDD, means “The register’s power is supplied by RTCVDD. And the register is reset by VDD_rst.”

12.3.1.1 RTC_CTL0 (RTC Control 0 register. 0x43) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7	cal_en	Calendar enable 0: Sisable 1: Enable	R/W	0
6	en_almpd	Alarm pending enable. 0: Disable. The alarm pending bit is disabled. The pending bit is not set when alarm is occoured 1: Enable.	R/W	0
5	test_en	Test enable 0: Disable 1: Enable. The RTC’s LOSC is changed to HOSC	R/W	0
4	page_sel	Register page select register 0: IO registers “44h-48h” are RTC Time register. 1: IO registers “44h-48h” are RTC Alarm register, random register and RTC Time year register.	R/W	0
3	ext_losc_en	External LOSC enable 0: Disable	R/W	1

		1: Enable		
2	cal_clk_select	Calendar clock select 0: Select ILOSC 1: Select ELOSC	R/W	0
1	Leap year	RTC Leap Year bit 1: Leap year 0: Not leap year	R	1
0	alm_ip	Alarm IRQ pending bit. Writing 1 to this bit will clear it.	R/W	0

NOTE: The cal_en bit must be disabled when the RTC Time register being written, and all RTC Time registers must be written before cal_en is enabled when the timeis set, otherwise error will occurs.

12.3.1.2 RTCTimeS (RTC Time Second Register, 0x44) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserved	-	-
5:0	time_sec	Calendar Time Second[5:0]	R/W	0

12.3.1.3 RTCTimeMin (RTC Time Minute Register, 0x45) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserved	-	-
5:0	time_min	Calendar Time Minute[5:0]	R/W	0

12.3.1.4 RTCTimeH (RTC Time Hour Register, 0x46) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:5	-	Reserved	-	-
4:0	time_hour	Calendar Time Hour[4:0]	R/W	0

12.3.1.5 RTCTimeD (RTC Time Day Register, 0x47) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:5	-	Reserved	-	-
4:0	time_day	Calendar Time Day[4:0]	R/W	01

12.3.1.6 RTCTimeMon (RTC Time Month Register, 0x48) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:4	-	Reserve	-	-
3:0	time_mon	Calendar Time Month[3:0]	R/W	01

12.3.1.7 RTCTimeYear (RTC Time Year Register, 0x44) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7	-	Reserved	-	-
6:0	time_year	Calendar Time Year[6:0]	R/W	0

12.3.1.8 RTCAlmS (RTC Alarm Second Register, 0x45) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserved	-	-
5:0	alm _sec	Alarm Second[5:0]	R/W	0

12.3.1.9 RTCALMM (RTC Alarm Minute Register, 0x46) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserved	-	-
5:0	alm _min	Alarm Minute [5:0]	R/W	0

12.3.1.10 RTCALMH (RTC Alarm Hour Register, 0x47) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:5	-	Reserved	-	-
4:0	alm _hour	Alarm Hour [4:0]	R/W	0

12.3.1.11 RTCrdm (RTC Random Access Register, 0x48) (RTCVDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:0	random	These bits can be accessed by CPU freely.	R/W	0

12.3.1.12 RTCREGUPDATE (RTC Register update control Register,0x49) (RTCVDD)

Bits	Bit	Description	Access	Reset

	Mnemonic			
7:0	update	The RTCVDD register update control register. When writing the RTC registers (except RTCREGUPDATE register or bit “alm_ip”), the RTC registers’ values will not be updated immediately. The value is written to backup registers (in VDD) first. Just when writing RTCREGUPDATE register A5H, the RTCVDD registers’ values are update with the backup registers’ value. RTCREGUPDATE register is automatically reset as 5AH after the RTCVDD register is update. NOTE: 1. Do not write RTCVDD registers when this register value is A5H. 2. When writing the bit “alm_ip”, it will take effect immediately. No need to write this register.	R/W	0x5a

12.3.1.13 RTC_CTL1 (RTC Control 1 register. 0x4a) (VDD)

Bits	Bit Mnemonic	Description	Access	Reset
7	2hz_en	2hz IRQ enable 0: Disable 1: Enable	R/W	0
6	timer_en	RTC Timer enable 0: Disable 1: Enable	R/W	0
5	clk_sel	Watch dog, 2hz, timer‘s clock select bit: 0: pmu_clk_div 1: ELOSC	R/W	0
4:2	–	Reserved		/
1	2hz_ip	2hz IRQ pending bit Writing 1 to this bit will clear it.	R/W	0
0	timer_ip	Timer IRQ pending bit Writing 1 to this bit will clear it.	R/W	0

12.3.1.14 TimerLB (Timer low Byte, 0x4b) (VDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:0	timerlb	Low byte of timer Register Timer is a down counter with LOSC as clock. When the Counter Overflow, timer_ip will occur.	R/W	X

		Timer_ip = [1/(Time bit[23:0]+1)] *FLOSC		

12.3.1.15 TimerMB (Timer middle Byte, 0x4c) (VDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:0	timermb	Middle byte of LOSC Divider Register	R/W	X

12.3.1.16 TimerHB (Timer high Byte, 0x4d) (VDD)

Bits	Bit Mnemonic	Description	Access	Reset
7:0	timerhb	High byte of timer Register	R/W	X

12.3.1.17 WDCtl (watch dog control register, 0x4e) (VDD)

Bits	Bit Mnemonic	Description	Access	Reset
7	wd_en	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, either an internal reset (WDRST-) is generated to force the system into reset status and then reboot, or an IRQ is sent to CPU.	R/W	0
6:4	clk_sel	Watch Dog timer clock select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1khz 176 ms 001 512hz 352 ms 010 256hz 703ms 011 128hz 1.4 s 100 64hz 2.8s 101 32hz 5.6 s 110 16hz 11.2s 111 8hz 22.5 s	R/W	010
3	clr	Clear bit, write 1 to clear WD timer, cleared automatically	W	0
2	mode_sel	Watchdog IRQ or Reset- Select. 0: Sent reset when Dog timer overflows 1: Sent IRQ when Dog timer overflows	R/W	0
1	wd_flag	Watch dog overflow flag 1: Means WD reset or irq ever occurred. Writing 1 to this bit Clears it.	R/W	0

		0:not occurred This bit is reset by powerok signal。		
0	-	Reserved	/	X

12.3.2 HOSC/PLL

12.3.2.1 HFCCTL (High frequency crystal control Register, 040h)

Bits	Description	Access	Reset
7	High Frequency Crystal Oscillator Enable. 0: Disable, 1: Enable	R/W	0
6	Power ok status. 0: Power on, 1: Power on finished.	R	0
5:4	Reserved	/	/
3:2	**High frequency crystal Oscillator GMMIN select bits** 00 gain=3.2 01 gain=6.1 10 gain=8.0 11 gain=10.1	R/W	01
1:0	Reserved	/	/

12.3.2.2 CK48MCTL (CK48MCTL control Register, 042h)

Bits	Description	Access	Reset
7: 6	Reserved	R/W	0
5	CK48M Enable 0: Disable 1: Enable	R/W	0
4:0	Reserved.	/	/

12.3.2.3 MCUPLL (MCU PLL Control, 28h)

Bits	Description	Access	Reset
7	**MCU PLL Enable** 0: Disable 1: Enable	R/W	0
6:2	**MCU PLL output select**	R/W	00000

	0 0 0 x x 12MHz 0 0 1 0 0 16MHz 0 0 1 0 1 20MHz 0 0 1 1 0 24MHz 0 0 1 1 1 28MHz 0 1 0 0 0 32MHz 0 1 0 0 1 36MHz 0 1 0 1 0 40MHz 0 1 0 1 1 44MHz 0 1 1 0 0 48MHz 0 1 1 0 1 52MHz 0 1 1 1 0 56MHz 0 1 1 1 1 60MHz 1 0 0 0 0 64MHz 1 0 0 0 1 68MHz 1 0 0 1 0 72MHz 1 0 0 1 1 76MHz 1 0 1 0 0 80MHz 1 0 1 0 1 84MHz 1 0 1 1 0 88MHz 1 0 1 1 1 92MHz 1 1 0 0 0 96MHz 1 1 0 0 1 100MHz 1 1 0 1 0 104MHz 1 1 0 1 1 108MHz 1 1 1 0 0 112MHz 1 1 1 0 1 116MHz 1 1 1 1 0 120MHz 1 1 1 1 1 124MHz		
1:0	Reserved	/	/

12.3.3 Clock Selection Unit

12.3.3.1 MCSR1 (Module Clock Select Register 1, 2Bh)

Bits	Description	Access	Reset

7	UART Controller Clock Select 0 DC 1 CK48M	R/W	0
6	SPDIF Controller Clock Select 0 DC 1 CK48M	R/W	0
5:4	SPI Controller Clock Select 0 x DC 1 0 HOSC 1 1 MCU PLL	R/W	00
3	I2C Controller Clock Select 0 DC 1 HOSC	R/W	0
2:0	Reserved	/	/

12.3.3.2 MCSR2 (Module Clock Select Register 2, 2Ch)

Bits	Description	Access	Reset
7:2	Reserved	/	/
1:0	DMA1 and DMA2 Clock Select 0 0 LOSC 0 1 HOSC 1 0 MCU PLL 1 1 DC	R/W	11

13A/D D/A and Headphone Driver

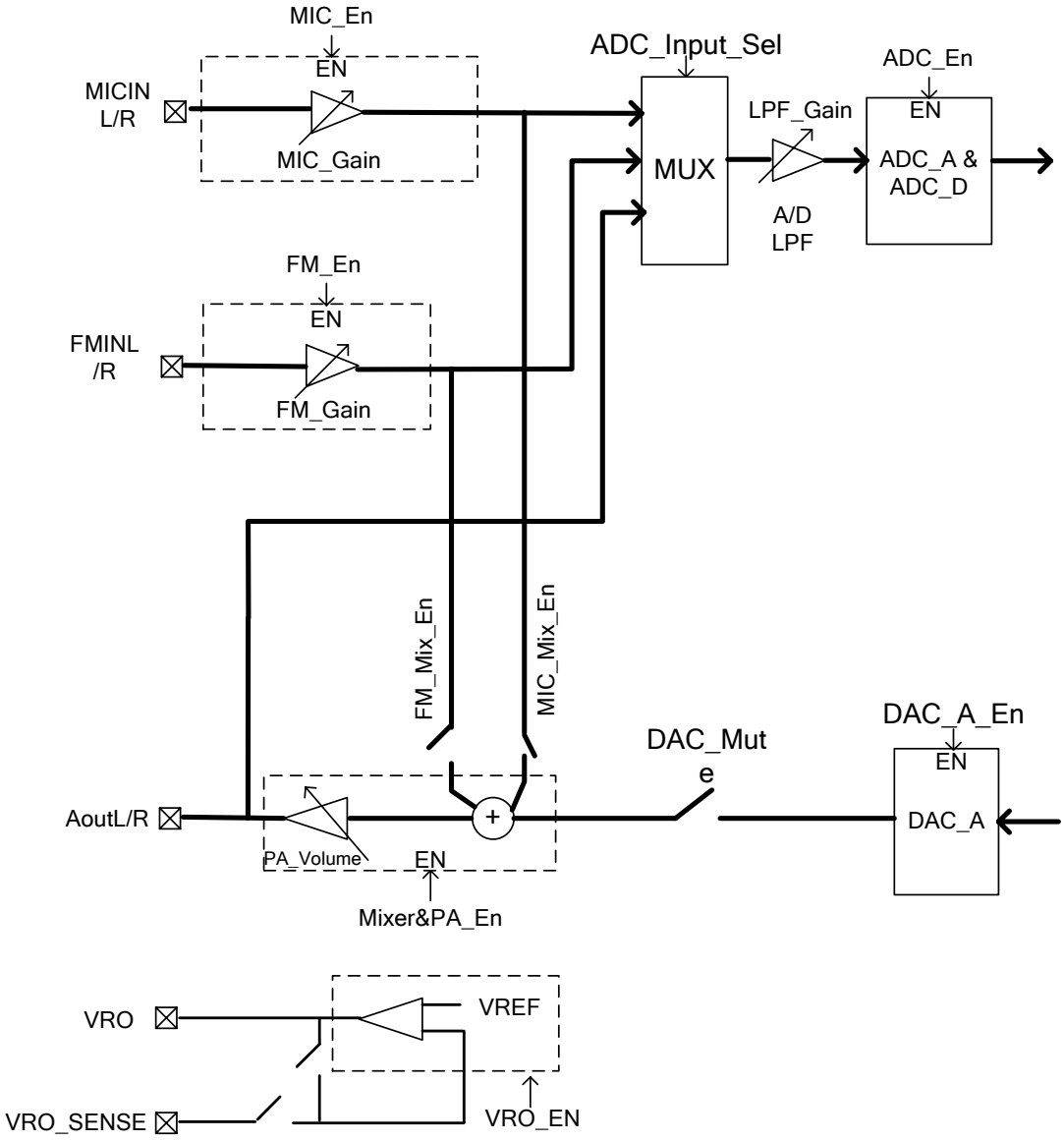
13.1 Introduction

The D/A A/D module includes a Sigma-Delta DAC, a Sigma-Delta ADC which supports Microphone/FM/Line input. Both DAC and ADC support 48k/44.1k/32k/24k/22.05k/16k/12k/11.025k/8k sample rate. Its on-chip 20mW power amplifier can support to drive 32/16ohm earphone.

13.2 Feature

- Build in Stereo 20-bit Sigma-Delta DAC
- Build in Stereo 21-bit Sigma-Delta ADC
- Build in Stereo Headphone driver
- Support sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48kHz
- Support Microphone/FM/Line Input to ADC
- Max output: 2×20mW@16ohm

13.3 ADDA Analog Diagram



13.4 DAC

The audio DAC is an on-chip Sigma-Delta Modulator, a 16 bit high performance DAC is composed of it. The DAC interface support 8-level play back FIFO (16 X 16bits PCM data for L/R channel) and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256×FS

clock for over-sampling, while 24MHz supports 48K/32K/24K/16K/12K/8KHz with 256×FS for over-sampling.

13.5 ADC

The audio ADC is an on-chip Sigma-Delta Analog-to-Digital Converter, which support input from MIC or external FM or LINEIN. The ADC interface support 16-level FIFO (16 X 16bits X 2 PCM data for L/R channel) and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256×FS clock for over-sampling, while 24MHz supports 48K/32K/24K/16K/12K/8KHz with 256×FS for over-sampling.

14 GPIO/MULTIFUNCTION

14.1 Description

There are totally 45 GPIOs which can be used as output/input separately or simultaneously. Each GPIO is used as a multifunction with other function pin. Set the relevant register before using the needed function.

14.2 Feature

- 45 GPIOs which can be used as output/input separately or simultaneously
- Different level of static driving current and dynamic driving capacity
- Maximum frequency of GPIOs up to 30MHz
- Flexible alternation of multifunction, especially in SD/MMC/MS module

14.3 Register Description

GPIO/MFP includes registers as following:

Address	Name	Description
0xEE	MFPSEL	MFP Select Register
0xED	GPIOAOUTEN	GPIOA Output Enable
0xEF	GPIOAINEN	GPIOA Input Enable
0xF0	GPIOADAT	GPIOA Data
0xF1	GPIOBOUTEN	GPIOB Output Enable
0xF2	GPIOBINEN	GPIOB Input Enable
0xF3	GPIOBDAT	GPIOB Data
0xF4	GPIOCOUTEN	GPIOC Output Enable
0xF5	GPIOCINEN	GPIOC Input Enable
0xF6	GPIOCDAT	GPIOC Data
0xF7	GPIODOUTEN	GPIOD Output Enable
0xF8	GPIODINEN	GPIOD Input Enable
0xF9	GPIODDAT	GPIOD Data

0xFA	GPIOEOUTEN	GPIOE Output Enable
0xFB	GPIOEINEN	GPIOE Input Enable
0xFC	GPIOEDAT	GPIOE Data
0xFD	GPIOFOUTEN	GPIOF Output Enable
0xFE	GPIOFINEN	GPIOF Input Enable
0xFF	GPIOFDAT	GPIOF Data

14.3.1 MFPSEL (MFP Select Register, 0EEh)

Bits	Description	Access	Reset
7	GPIO_A1, GPIO_A[4:3], GPIO_C[1:0] and ICE multifunction 0: ICE Port 1: GPIO_A1, GPIO_A[4:3], GPIO_C[1:0]	R/W	0
6	GPIOB7 and RB2- multifunction 0: RB2- 1: GPIOB7	R/W	0
5	GPIOB6 and RB1- multifunction 0: RB1- 1: GPIOB6	R/W	0
4	GPIOB5 and CLE multifunction 0: CLE 1: GPIOB5	R/W	0
3	GPIOB4 and ALE multifunction 0: ALE 1: GPIOB4	R/W	0
2	GPIOB3 and MWR- multifunction 0: MWR- 1: GPIOB3	R/W	0
1	GPIOB2 and MRD- multifunction 0: MRD- 1: GPIOB2	R/W	0
0	GPIOD[7:0] and DATA multifunction 0: DATA BUS 1: GPIOD[7:0]	R/W	0

14.3.2 GPIOAOUTEN (GPIO_A Output Enable Register, 0EDh)

Bits	Description	Access	Reset
7	GPIO_A7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_A6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_A5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_A4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_A3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_A2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_A1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_A0 Output enable, 0: Disable, 1: Enable.	R/W	0

14.3.3 GPIOAINEN (GPIO_A Input Enable Register, 0EFh)

Bits	Description	Access	Reset
7	GPIO_A7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_A6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_A5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_A4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_A3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_A2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_A1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_A0 Input enable, 0: Disable, 1: Enable.	R/W	0

14.3.4 GPIOADAT (GPIO_A Data Output/Input Register, 0F0h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

14.3.5 GPIOBOUTEN (GPIO_B Output Enable Register, 0F1h)

Bits	Description	Access	Reset
7	GPIO_B7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_B6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_B5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_B4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_B3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_B2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_B1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_B0 Output enable, 0: Disable, 1: Enable.	R/W	0

14.3.6 GPIOBINEN (GPIO_B Input Enable Register, 0F2h)

Bits	Description	Access	Reset
7	GPIO_B7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_B6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_B5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_B4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_B3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_B2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_B1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_B0 Input enable, 0: Disable, 1: Enable.	R/W	0

14.3.7 GPIOBDAT (GPIO_B Data Output/Input Register, 0F3h)

Bits	Description	Access	Reset

7:0	Output/Input Data[7:0]	R/W	xxh

14.3.8 GPIOCOUTEN (GPIO_C Output Enable Register, 0F4h)

Bits	Description	Access	Reset
7	GPIO_C7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_C6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_C5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_C4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_C3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_C2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_C1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_C0 Output enable, 0: Disable, 1: Enable.	R/W	0

14.3.9 GPIOCINEN (GPIO_C Input Enable Register, 0F5h)

Bits	Description	Access	Reset
7	GPIO_C7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_C6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_C5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_C4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_C3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_C2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_C1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_C0 Input enable, 0: Disable, 1: Enable.	R/W	0

14.3.10 GPIOCDAT (GPIO_C Data Output/Input Register, 0F6h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

14.3.11 GPIODOUTEN (GPIO_D Output Enable Register, 0F7h)

Bits	Description	Access	Reset
7	GPIO_D7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_D6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_D5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_D4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_D3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_D2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_D1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_D0 Output enable, 0: Disable, 1: Enable.	R/W	0

14.3.12 GPIODINEN (GPIO_D Input Enable Register, 0F8h)

Bits	Description	Access	Reset
7	GPIO_D7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_D6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_D5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_D4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_D3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_D2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_D1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_D0 Input enable, 0: Disable, 1: Enable.	R/W	0

14.3.13 GPIODDAT (GPIO_D Data Output/Input Register, 0F9h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

14.3.14 GPIOEOUTEN (GPIO_E [4:0] Output Enable Register, 0FAh)

Bits	Description	Access	Reset
7:6	0 0 Reserved 0 1 Reserved 1 0 GPIOE4 Output LOSC. 1 1 GPIOE4Output HOSC. If bit7 is set, GPIOE4 can only output OSC.	R/W	0
5	Reserved	R/W	0
4	GPIO_E4 Output Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_E3 Output Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_E2 Output Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_E1 Output Enable, 0: Disable, 1: Enable	R/W	0
0	GPIO_E0 Output Enable, 0: Disable, 1: Enable	R/W	0

14.3.15 GPIOEINEN (GPIO_E [4:0] Input Enable Register, 0FBh)

Bits	Description	Access	Reset
7:5	Reserved	/	/
4	GPIO_E4 Input Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_E3 Input Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_E2 Input Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_E1 Input Enable, 0: Disable, 1: Enable	R/W	0

0	GPIO_E0 Input Enable, 0: Disable, 1: Enable	R/W	0

14.3.16 GPIOEDAT (GPIO_E [4:0] Data Output/Input Register, 0FCh)

Bits	Description	Access	Reset
7:5	Reserved	/	/
4:0	Output/Input Data[4:0]	R/W	xxh

14.3.17 GPIOFOUTEN (GPIO_F [7:0] Output Enable Register, 0FDh)

Bits	Description	Access	Reset
7	GPIO_F7 Output Enable, 0: Disable, 1: Enable	R/W	0
6	GPIO_F6 Output Enable, 0: Disable, 1: Enable	R/W	0
5	GPIO_F5 Output Enable, 0: Disable, 1: Enable	R/W	0
4	GPIO_F4 Output Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_F3 Output Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_F2 Output Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_F1 Output Enable, 0: Disable, 1: Enable。	R/W	0
0	GPIO_F0 Output Enable, 0: Disable, 1: Enable	R/W	0

14.3.18 GPIOFINEN (GPIO_F [7:0] Input Enable Register, 0FEh)

Bits	Description	Access	Reset
7	GPIO_F7 Input Enable, 0: Disable, 1: Enable	R/W	0

6	GPIO_F6 Input Enable, 0: Disable, 1: Enable	R/W	0
5	GPIO_F5 Input Enable, 0: Disable, 1: Enable	R/W	0
4	GPIO_F4 Input Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_F3 Input Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_F2 Input Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_F1 Input Enable, 0: Disable, 1: Enable	R/W	0
0	GPIO_F0 Input Enable, 0: Disable, 1: Enable	R/W	0

14.3.19 GPIOFDAT (GPIO_F [7:0] Data Output/Input Register, 0FFh)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

14.3.20 GPIOE0_VCCOUTSR (GPIOE0_VCCOUT Select Register, 088h)

Bits	Description	Access	Reset
7:2	Reserved	/	/
1	VCCOUT is used for FM power supply. 0: VCCOUT pin floating, no power out 1: VCCOUT=2.89V, there is a LDO from VCC to VCCOUT. If there is a capacitance at VCCOUT, you should wait a moment after setting this bit to 1.	R/W	0
0	GPIOE0 as a multi pin, it can use as VCCOUT for FM power supply. 0: GPIOE0 is used as MS_BS or GPIOE0 1: GPIOE0 is used as VCCOUT	R/W	0

15 PWM

15.1 Introduction

PWM output module is embedded in ATJ331X, in the purpose of controlling the external backlight IC conveniently. It supplies several output frequency and variable duty occupancy for adjusting the intensity of the LCD backlight.

15.2 Feature

- 2 selected sources :24M or 32K;
- Frequency dividing maximum to 4;
- Available frequency in end are 94K, 47K, 24K, 12K, 1K, 500Hz, 250Hz, 125Hz;
- 8 levels duty occupancy adjusting;
- High level or low level active selecting.

15.3 Register Description

Address	Name	Description
AFH	PWMCTL	PWM Control Register

15.3.1 PWMCTL (PWM Control Register, AFh)

Bits	Description	Access	Reset
7	**PWM Enable.** 0: Disable the PWM module 1: Enable the PWM module NOTE: when enableing the PWM Module, the GPIOC0 is used as the PWM pin, if the mofule disabled, the GPIOC0 is used as GPIOC0 or I2C_SCK	R/W	0

6	**Source Select.** 0: Choose 24Mhz as dividing source 1: Choose 32KHz as dividing source	R/W	1
5:4	**Frequency Divide.** Choose the divisor for dividing Dividing Source 94K 1K 00: /1 94K 1K 01: /2 47K 500Hz 10: /4 24K 250Hz (recommened) 11: /8 12K 125Hz	R/W	10
3	**Active Polarity Select.** 0: PWM is High level active 1: PWM is Low level active	R/W	0
2:0	**Active Duty Occupancy.** 000: 0/8 001: 1/8 010: 2/8 011: 3/8 100: 4/8 101: 5/8 110: 6/8 111: 7/8	R/W	100

16 Power Management Unit

16.1 Introduction

ATJ331X integrates a comprehensive power supply subsystem, including the following features:

- Supports two battery types: 1-cell alkaline/NIMH and Li-Ion battery, selected by PWRMB pin.
- Two integrated DC-DC converters: VDD and VCC. VDD can work in boost mode from 1-cell alkaline/NIMH, or work in buck mode from Li-ion cell, which supplies Core Power. The other can only work in boost mode from 1-cell alkaline/NIMH, which supplies I/O Power.
- Five linear regulators supply power directly from DC5V or Li-Ion cell. The outputs are VCC, VDD, AVCC, AVDD and FM_VCCOUT.
- Linear battery charger for Li-Ion cell.
- Battery voltage monitor, system monitors for temperature and wire-controller.
- ATJ331X power supply is designed to offer maximum flexibility and performance, while minimizing external component requirements.

16.2 Function Block Diagram

Figure 16-2-1 and Figure 16-2-2 show the two outputs VCC and VDD for the two supported battery types. Table 16-2-1 lists power supply modes in which VCC/VDD how to work.

The figures and the table can be used to understand how to set hardware connection relate to which subsystems, but they are not intended to be a complete architecture description.

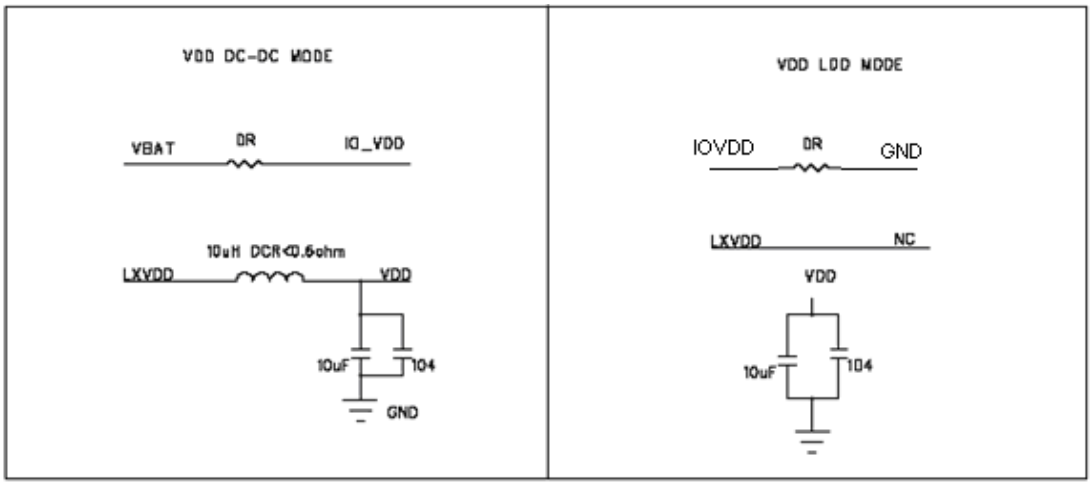


Figure 16-2-1 Li-Ion Supply Peripheral Connection

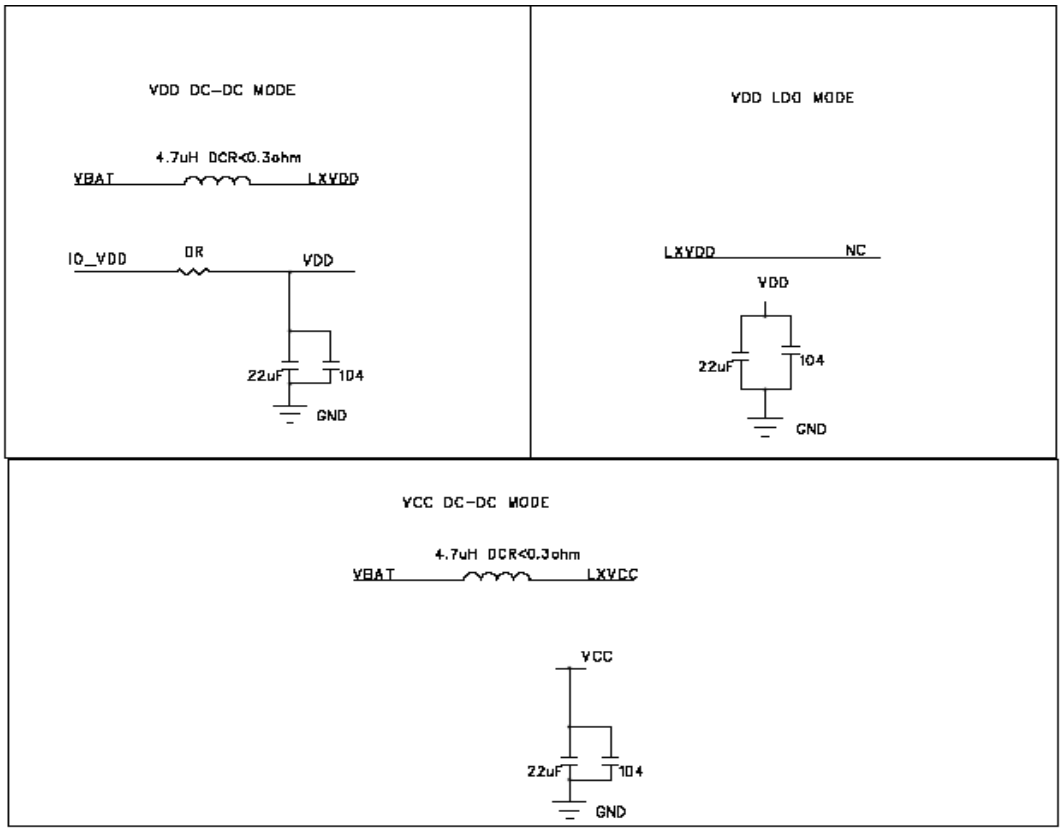


Figure 16-2-2 1-Cell Alkaline/NIMH Supply Peripheral Connection

Table 16-2-1 Power Supply Mode

Description	PWRMB	DC5V>4.3V	DCDC_VCC	VCC Regulator	DCDC_VDD	VDD Regulator
1 Alkaline/NIMH, 2 Inductor	1	N	Y	N	Y	N
1 Alkaline/NIMH, 1 Inductor for VCC	1	N	Y	N	N	Y
Li-ION, 1 Inductor for VDD	0	N	N	Y	Y	N
Li-ION, 2 Regulators	0	N	N	Y	N	Y
USB or Adapter, 2 Regulators	X	Y	N	Y	N	Y

16.3 DC-DC Converters

The DC-DC converter efficiently scales battery voltage to the required supply voltages. The DC-DC converters include several advanced features:

- Flexible battery support for either 1-cell alkaline/NIMH or Li-Ion batteries
- Synchronization DC-DC converter architecture
- Work in Pulse Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) automatically for different load current.

16.3.1 DC-DC Accurate and Maximum Output Current

The output voltages are highly precise within ±2%; they provide large currents with a significantly small dropout voltage within ±5%.

DC-DC Maximum Output Current

Block name		Loading
VCC DC-DC(boost mode)		BAT=1.0V, 85mA @ VCC=3.1V dropping 5% BAT=1.2V, 120mA @ VCC=3.1V dropping 5%
VDD DC-DC	boost mode	BAT=1.0V, 60mA @ VDD=1.7V dropping 5% BAT=1.2V, 80mA @ VDD=1.7V dropping 5%
	buck mode	BAT=3.4V, 80mA @ VDD=1.7V dropping 5%

16.3.2 DC-DC Converter Efficiency

Typical efficiency of the DC-DC converters under nominal condition is 80%.

16.4 Linear Regulators

ATJ331X integrates five linear regulators; they generate VCC, VDD, AVCC, AVDD and FM_VCCOUT.

Linear regulators are typically used when the system is powered from a 5-V supply or USB.

16.4.1 Regulators Output Voltage Set

The output voltage setting of VCC and VDD linear regulators is the same as DC-DC converter.

AVCC is typically set once during system initialization, AVCC=2.95V。The output voltage of AVCC linear regulator changes follows VCC setting.

FM_VCCOUT is enabled by setting register. The voltage is 2.89V.

16.4.2 Regulators Accurate and Maximum Output Current

The output voltages are highly precise within ±2%. They provide large currents with a significantly small dropout voltage within ±5%.

Regulators Maximum Output Current

Block name	Loading
VCC Regulator	BAT=3.4V or DC5V=4.5V, 200mA @ VCC=3.1V, decreasing 5%
VDD Regulator	VCC=3.1V, 80mA @ VDD=1.7V, decreasing 5%
AVCC Regulator	VCC=3.1V, 50mA @ AVCC, decreasing 2%
FM_VCCOUT	VCC=3.1V, 35mA @ FM_VCCOUT, decreasing 5%

16.5 Li-Ion Cell Charger

Some products in ATJ331X family integrate the charging for Li-Ion battery from a 5-V source connected to the DC5V pin. The battery charger is essentially a linear regulator that has current and voltage limits. Charge current is software-programmable. User can enable charger by setting register.

Li-Ion batteries can be charged as low as of 1C, 500 mA, or the DC5V current limit. USB charging is typically limited to 500 mA or less to meet compliance requirements. Typical charge times for a Li-Ion battery are 2 to 3 hours with >90% of the charge delivered.

There is 3 phases through all the charging process: When battery voltage is between 3.0V to 4.2V, the charging current is set by CHG Control Register, this phase is called constant current charging phase (CC for short). At this phase, the charging current is constant and the voltage of battery is going up slowly. When battery voltage is below 3.0V,the charging current is 1/10 of CC, this phase is called trickle charging phase or pre-charge. you can mask trickle charging by CHG Control Register bit4=1. When battery voltage gets to 4.2V, the battery voltage will be constant, and the charging current is reduced gradually, this phase is called constant voltage phase (CV for short).

The battery charge voltage is limited to 4.2 V when the reference voltage is 1.5V. If the reference voltage is changed, the limited voltage is changed correspondingly.

The Li-Ion charge is typically stopped when the charging current drops below 7.5% of the charge current set by CHG Control Register. The register CHG Control Register includes controls for the maximum charge current and the register CHG Detect Register includes controls for the stop charge current. While the charger is delivering the current greater than the stop charge limit, the register CHG STATUS is high. When the charging is complete, the bit goes low.

One can programmatically monitor the battery voltage by using the BATADC. The charger has its own voltage limiting that operates independently of the BATADC. But monitoring the battery voltage during the charge might be helpful for reporting the charge progress.

The battery charger is capable of generating a large amount of heat within ATJ331X, especially at the current above 400 mA. The dissipated power can be estimated: (5V – battery voltage) * current. At a max current (500mA) and a 3-V battery, the charger can dissipate 1 W.

The LRADC2 can be used to monitor the battery temperature or chip temperature. To ensure that the system operates correctly, it should be monitored at every 100 ms. It would be a good practice to check the output data of LRADC2 for two consecutive checks. If the battery temperature exceeds 45 C°, then the battery charge current must be reduced or the charger must be stopped.

16.6 A/D Converters

There is a low resolution 7 bit A/D for battery monitor and temperature monitor, the input voltage range of which is 1.4 to 4.4V at VBAT pin in Li-Ion supply mode, 0.7 to 2.2V at VBAT pin in 1-cell Alkaline supply mode, and 0.7 to 2.2V at LRADC2 pin.

There is a low resolution 6 bit A/D for wire control. The input voltage range of which is 0 to AVCC at LRADC1 pin.The A/D converter's working frequency is 64HZ default.

The impedance between BAT(or LRADC1 or LRADC2) and GND is up to MΩ。

The output data of BATADC can be calculated as the following formula:

LI-ION BATADC:

One LSB= $\frac{4.4-1.4}{2^7} * \frac{Vref}{1.5}$, when battery voltage= Vbat, ADC's data is n= $\frac{Vbat-1.4*\frac{Vref}{1.5}}{\frac{4.4-1.4}{2^7}*\frac{Vref}{1.5}}$, in which Vref is the reference voltage tested.

For example, if Vref=1.500V, then 1LSB=23.44mV, and the corresponding data from 1.4V to 1.42344V are 00h, the corresponding data from 1.42344V to 1.44688V are 01h/

1AAA BATADC:

One LSB= $\frac{2.2-0.7}{2^7} * \frac{Vref}{1.5}$, when battery voltage=Vbat, ADC's data is n= $\frac{Vbat-0.7*\frac{Vref}{1.5}}{\frac{2.2-0.7}{2^7}*\frac{Vref}{1.5}}$, in which Vref is the reference voltage tested.

For example, if Vref=1.500V, then 1LSB=11.72mV, and the corresponding data from 0.7V to 0.7119V are 00h, the corresponding data from 0.71172V to 0.72344V are 01h.

LRADC1/LRADC3/LRADC4/LRADC5:

One LSB= $\frac{AVCC}{2^6}$, when input voltage=V, the corresponding ADC is n= $\frac{V}{\frac{AVCC}{2^6}}$.

For example, if AVCC=2.87V，then 1LSB=44.84mV, and the corresponding data from 0V to 0.04484V are 00h, and the corresponding data from 0.04484V to 0.8968V are 01h.

LRADC1/LRADC3/LRADC4/LRADC5 use 1 ADC at different time, and LRADC3 and GPIO_F5 multiplexes, LRADC4 and GPIO_F6 multiplexes, LRADC5 and GPIO_F7 multiplexes.

16.7 Programmable Registers

16.7.1 SYSTEM_CTL_RTCVDD, (System Control Register, 0A5h) (RTCVDD)

System and standby control

Bits	Description	Access	Reset
7:6	SYSON key pressing length setting: 00: 60ms < t < 2s, set Short-press status flag; t>=2s, system startup or send Long-press status flag; 01: 60ms < t < 3s, send Short-press status flag; t>=3s, system startup or send Long-press status flag; 10: 60ms < t < 4s, send Short-press status flag; t>=4s, system startup or send Long-press status flag; 11: 60ms < t < 5s, send Short-press status flag; t>=5s, system startup or send Long-press staus flag; NOTE: please refer to REG[0A6H] for flag bit.	R/W	01
5	LB_ to standby enable in Li-ion mode 0: disable, shield low power to standby function; 1: enable, enable low power to standby function; The battery voltage for low power to standby can be set via REG[A5H.bit4:3].	R/W	1
4:3	LB (Low battery) voltage setting Li-ION 00 2.7V ***01 3.0V 1X 3.3V	R/W	01

2	VCC/VDD LDO over-current protection enable; 0: Disable 1: Enable	R/W	1
1	VCC/VDD too-low-voltage protection enable; 0: Disable 1: Enable Effective to lithium battery, but not for single power. For hard switch solution, if the system cannot start in case of fast-speed power on and power off, try to shield the bit to 0.	R/W	1
0	REG_ENPMU: 0: Disable VCC/VDD 1: Enable VCC/VDD When the status is turn from S3 to S1, the bit is set as 1.	R/W	1

NOTE: After the writing operation over the registers under RTCVDD, it is necessary to wait 3 Z80CLK cycle as well as 4 low frequency cycle for the real writing-in and the written value then can be read.

16.7.2 SYSTEM_CTL_VDD (SYSTEM Set Register, 0A6h)

System set register

System contril VDD, including long/short pressing flag, single-power standby setting, efuse enable setting and register switch page setting.

Bits	Description	Access	Reset
7	Short-press status flag: 0: no Short-press status flag, SYSON key not been pressed in short time. 1: has Short-press status, SYSON key been pressed in short time, and the time is within the setting value. Write 1 to this bit to clear it. NOTE (for design): Only after the bit is cleared to 0 and there is key, the next detection can be carried out and the next next status can only be sent when the time requirement has be met. It is the same as that of interrupt design of key. (For software): In hard switch solution, after the running of brom, it is necessary to write 1 to the bit and clear it to 0 for once in order to avoid the error of short key pressing when hard switch is cut off.	R/W	0

6	Long-press status flag: 0: no Long-press status flag, SYSON key not been pressed for long time. 1: has Long-press status status, SYSON key been pressed for long time and the time exceeds the setting value. If the key is not up, do not re-timing. One key status display, read-only.	R	X
5:4	Reserved	R/W	0
3	REG_IOVDD_R: whether IOVDD 300kohm's pull-down resistor controls effectively; 0: PWRMB=1, control IOVDD for no 300kohm pull-down. 1: PWRMB=1, control IOVDD for 300kohm pull-down.	R/W	1
2	IOVDD status: 0: IOVDD is low; 1: IOVDD is high.	R	X
1:0	Register switch page control 00: can operate page0 register before switch page 01: can operate page1 register after switch page 10: can operate page2 register after switch page 11: can operate page3 register after switch page (for CMU module)	R/W	00

NOTE: LB/LBNMI will be effective when BATADC is enabled.

16.7.3 VOUTCTL (DC-DC & Regulator Output Voltage Control Register, page0_089h)

The VOUT Control Resister controls the output voltage of VCC/VDD DC-DC converters and regulators.

Bits	Description	Access	Reset
7	PWRMB, refelecting power mode. 1—1 Alkaline/NIMH 0—Li-ION This bit is read only, which depend on pin PWRMB. The default is 0. For signal power solution, a 400kohm resistor shall be added between DC5V and VBAT, otherwise, if there is no battery connected, it will be regarded as PWRMB=0, Li-Ion mode.	R	x

6:4	VCC voltage level select 111 3.3V 110 3.2V 101 3.1V 100 3.0V 011 2.9V 010 2.8V 001 2.7V 000 2.6V VCC is typically set to 3.1V once during system initialization; it remains unchanged until operating these 3 bits. In test mode, the power-up is defaulted at 2.6V, VCC= 2.6V (AVCC =2.45V) (digital).	R/W	101
3:1	VDD(DC-DC & Regulator) voltage coarse control 000 1.3V 001 1.4V 010 1.5V 011 1.6V 100 1.7V 101 1.8V 110 1.9V 111 2.0V VDD is typically set to 1.7V once during system initialization; it remains unchanged until operating these 3 bits. User can set VDD at a lower voltage (1.6V) at light loading to reduce power dissipation. AVDD voltage set to be slight lower than VDD, 100mV; In test mode, power-up is defaulted at 1.3V, VDD=1.3V, AVDD =1.2V.	R/W	100
0	VDD (DC-DC & Regulator) voltage fine control (one control level=50mV); 0: Disable; 1: Enable	R/W	0

16.7.4 LBNMI & ADCIRQ (LBNMI & ADCIRQ Control Register, page0_08Ch)

PMU's NMI and IRQ to set registers.

Bits	Description	Access	Reset
7	LRADC1 IRQ Enable. 0: Disable, shield LRADC1 interrupt function; 1: Enable, enable LRADC1 interrupt function; LRADC1's interrupt voltage can be AVCC, or can be lower than 0.9*AVCC, decided via REG [8CH.bit6].	R/W	0
6	LRADC1 IRQ threshold. 0: Low, 0.9*AVCC. When the voltage of LRADC1 pin is lower than 0.9*AVCC, if LRADC1 IRQ enabled, the IOREG [8DH.bit6] will be pended. 1: High, AVCC. When the voltage of LRADC1 pin is lower than AVCC, if LRADC1 IRQ enabled, the IOREG [8DH.bit6] will be pended.	R/W	0
5	LRADC1 IRQ Pending. Writing 1 will clear this bit. When wire-control iuput is lower than IRQ threshold voltage, the pending bit is set to 1.	R/W	0
4	LBNMI_ enable, low power alarm enable bit. 0: Disable, shield low power alarm function. 1: Enable, enable low pwer alarm function. The bit shall be used together with BATADC's enable bit and only when BATADC enabled, the bit could be 1. Moreover, only when REG [04H.bit1]=1, low power alarm interrupt could happen. Low power interrupt pending bit is REG [04H.bit5]. The battery voltage producing low power alarm can be set by the following register.	R/W	0
3:2	LBNMI voltage setting One-Bat Li-ION 00 0.85V 3.0V 01 0.90V 3.1V 10 0.95V 3.3V 11 1.00V 3.5V When battery voltage is lower than the default 0.85V (single battery mode) or 3.0V (LI-ION battery mode), the system will send out low power alarm interrupt pending flag. Used together with LBNMI_ enable.	R/W	00
1:0	Reserved	R/W	10

16.7.5 LRADC1 (LRADC1 Data & Frequency Register, page0_08Dh)

Display LRADC1 output data and set ADC Frequency.

Bits	Description	Access	Reset
7	The all ADCs Frequency Source Select: The all A/D converter's working frequency is default as 128HZ. User can put the working frequency down to 64HZ by setting this bit 0 to consume little power. 0: 64HZ 1: 128HZ	R/W	1
6	LRADC1/3/4/5 Enable. 1: Enable 0: Disable.	R/W	0
5:0	Wire-control A/D converter LRADC1's data output. LRADC1 input voltage range is from 0 to AVCC.	R	x

NOTE: Only LRADC1 can send interrupt.

16.7.6 LRADC2 (LRADC2 Input Detect DATA Register, page0_08Eh)

The LRADC2 DATA Register display LRADC2 output data.

Bits	Description	Access	Reset
7	External DC5V supply presence 1: External 5V supply is present; 0: External 5V supply is not present;	R	x
6:0	7bit LRADC2 for BAT temperature. The Input voltage range is 0.7-2.2V. 1LSB= (2.2-0.7)V/27=11.72mV.	R	x

16.7.7 BATADC (Battery Voltage Detect DATA Register, page0_08Fh)

The BATADC Data Register displays battery A/D output data.

Bits	Description	Access	Reset
7	Battery A/D and LRADC2 (temperature sensor) enable. 1: Enable 0: Disable. (Enable as soon as power up because data can only be updated out after waiting for 8ms after enabling. It is not good to the low voltage detection of first power-up)	R/W	1
6:0	Battery 7bit Voltage ADC, to detect battery voltage. Input voltage range is: 1AAA: 0.7-2.2V Li-ion: 1.4-4.4V	R	x

The following register can only be accessed by MCU only when REG [A6H.bit1:0] is set to 01.
The registes used when the page0 is switched to page1 are as following:

16.7.8 VCCOUT CONTROL (VCCOUT Control Register, page1_088h)

Move the registers of SD CARD and AVCC registers of AUDIO to PMU. Moreover, FM_VCCOUT control is also in this register, shown as the following.

Bits	Description	Access	Reset
7:6	AVCC LDO margin tuning, voltage drops from VCC 00 0.15V 01 0.20V 10 0.25V 11 0.30V	R/W	00
5	SD_VCCOUT PMOS1 CTRL, loading capacity: 135mA: 0: Disable SD card VCCOUT output, shut down PMOS1 power switch. 1: Enable SD card VCCOUT output, open PMOS1 power switch. The PMOS1 driver current is 80mA when SDVCC is 5% than VCC.	R/W	0

4	SD_VCCOUT PMOS2 CTRL, loading capacity: 100mA: 0: Disable SD card VCCOUT output, shut down PMOS2 power switch. 1: Enable SD card VCCOUT output, open PMOS2 power switch. The PMOS1 driver current is 40mA when SDVCC is 5% than VCC.	R/W	0
3	FM_VCCOUT is used for FM power supply. 0: FM_VCCOUT pin floating, no power out 1: FM_VCCOUT=2.89V, FM_VCCOUT is a LDO. If there is a capacitance at FM_VCCOUT, you should wait a moment after set this bit 1.	R/W	0
2	GPIO as a multi pin, it can use as FM_VCCOUT for FM power supply. 0: GPIOE0 1: FM_VCCOUT	R/W	0
1	AVDD LDO Enable control: 0: AVDD LDO disable 1: AVDD LDO enable (Pay attention to power-up time sequency)	R/W	1
0	Reserved	R	X

16.7.9 LRADC3 (LRADC3 Data Register, page1_089h)

LRADC3 data register displays LRADC3 output data.

Bits	Description	Access	Reset
7	Reserved	R/W	0
6	LRADC3 CONTROL: 0: GPIO_F5 is used as GPIO_F5 1: GPIO_F5 is used as LRADC3	R/W	0
5:0	LRADC3 data output. LRADC3 input voltage range is from 0 to AVCC.	R	x

16.7.10 LRADC4 (LRADC4 Data Register, page1_08Ah)

LRADC4 data register displays LRADC4 output data.

Bits	Description	Access	Reset
7	Reserved	R/W	0
6	LRADC4 CONTROL: 0: GPIO_F6 is used as GPIO_F6 1: GPIO_F6 is used as LRADC4	R/W	0
5:0	LRADC4 data output LRADC4 input voltage range is from 0 to AVCC.	R	x

16.7.11 LRADC5 (LRADC5 Data Register, page1_08Bh)

Bits	Description	Access	Reset
7	CHG_POWER detection enable: 0: do not carry out CHG_POWER 1: carry out CHG_POWER, CHG_POWER is forced to change 0, supplied by battery, shall be updated afer a certain time.	R/W	1
6	LRADC5 CONTROL: 0: GPIO_F7 is used as GPIO_F7 1: GPIO_F7 is used as LRADC5	R/W	0
5:0	LRADC5's data output LRADC5 input voltage range is from 0 to AVCC.	R	x

16.7.12 CHG Control (Charger Control Register, page1_08Ch)

The Charge Control Register controls the battery charge features, including charger circuit activation, charger current configuration.

Bits	Description	Access	Reset

7	Charging power detection and cable plug-in/out detection flag bit CHG_POWER status: 1: charge power, detect cable plug-in. when DC5V's voltage> BAT+0.14V and >3.6V, and debounce time exceeds a certain value, the bit is 1. 0: no charge power, detect cable plug-out. When DC5V voltage< BAT+0.07V or <3.5V, and debounce time exceeds certain vakue, the bit is 1.	R	x
6	The debounce time of CHG_POWER: 0: CHG_POWER's rising debounce time is ms, CHG_POWER droping debounce time is ms. 1: CHG_POWER's rising debounce time us, CHG_POWER droping debounce time is us.	R/W	0
5	CHG_EN, Enable charge circuit 1: Enable charge circuit, no delay, has current immediately. 0: Disable charge circuit. Charge circuit will not work and consume little power. NOTE: Must enable USBVDD before using charger.	R/W	0
4	Trickle charging mask bit 0: Disable trickle charge. Whether battery voltage is below or up 3.0V, the charging current will be the value set by IOReg [page2_8CH.BIT3:0]. 1: Enable trickle charge. When battery voltage is below 3.0V, the charging current will be 1/10 of the value set by IOReg [page2_8CH.BIT3:0].	R/W	0

3:0	CHG_CURRENT Magnitude of the battery charge current, The current represented by each bits is as follows: 0000 25mA 0001 25mA 0010 50mA 0011 100mA 0100 150mA 0101 200mA 0110 250mA 0111 300mA 1000 350mA 1001 400mA 1010 450mA 1011 500mA Others Reserved The charging current is adjusted by using the calibration data of USB 6.2K resistor.	R/W	0101

16.7.13 CHGDET (Charge Detect Register, page1_08Dh)

The CHG status Detect Register detects magnitude of current charging current，charging phase and charging current status.

Bits	Description	Access	Reset
7	Over temperature display when charging: When the detected temperature of charging pipe exceeds the set value, the bit is 1. User can judge whether to decrease charging current or disable charging circuit according to the bit.	R	x
6	Reserved	R	x

5:4	Charging Phase Status: 0 0: Reserved 0 1: Pre-Charging 1 0: Constant-Current-Charging 1 1: Constant-Voltage-Charging The two bits will be available only when bit 7 of this register is set. Otherwise they will be always read as 00. There are 3 phases through all the charging process: Pre-C, CC and CV. The 2bits show which phase the charging at.	R	xx
3:1	Charge Current detect 000....0~25%*Ichg, Ichg is set by IOREG [page2_8CH.bit3:0], indicationg the current charging current is within the 30% of the set value. 001....25%~50%Ichg 010....50%~75%Ichg 011....75%~87%Ichg 100....above 87%Ichg Others: Reserved User can check the current charging current via the 3bits.	R	x
0	CHG_STATUS Charging Status. 0: Not charging, 1: Charging. 0: When the charging current is up to 1/10 of set by IOREG [page2_8CH.bit3:0] and last for 1 second, this bit will be from low to high. 1: When the charging current is down to 7.5% of set by IOREG [page2_8CH.bit3:0], this bit will be from high to low as soon as possible.	R	x

16.7.14 CHGASST (Charger Assistant Register, page1_08Eh)

The Charger Assistant Register supplies assistant functions to the Li-Ion battery charge features, such as charger temperature, terminal voltage and so on.

Bits	Description	Access	Reset
7	From VBAT to DC5V diode enable bit 0: Disable, default. 1: Enable	R/W	0

6	Reserved	R/W	1
5:4	Charge temperature protection control, set protection temperature. When the temperature of the charging circuit>the setting value, send over temperature flag, see Charge Detect Register。 00 100（101/116）℃ 01 120（111/127）℃ 10 135（123/139）℃ 11 150（135/153）℃	R/W	11
3:0	To Adjust Charger limit voltage, the minimum step is 0.1V. 0000 4.05V 0001 4.06V ..... 1110 4.19V 1111 4.20V The above data are the values when the charging current is not less than 10mA, and except for 4.2V which does not have offset, other levels will be relatively low, about 4~6mV.	R/W	1111

17 Electrical Characteristics

17.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	-10	+70	℃
Storage Temperature	Tstg	-55	+150	℃
Supply Voltage	DC5V	-0.3	6.0	V
	BAT	-0.3	4.5	V
	VCC/AVCC/PAVCC/UVCC/ VCCOUT/LXVCC	-0.3	3.6	V
	VDD/AVDD/RTCVDD	-0.3	2.2	V
	IO_VDD/LXVDD	-0.3	4.5	V
Input Voltage	+3.3V IO	-0.3	3.6	V

Note:

1) Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
2) All voltage values are with respect to GND
3) +3.3V IO/+1.8V IO are defined in the Pin list.

17.2 Recommended Power Supply

VCC = 3.1V Tamb = -10 °C to 70 °C

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.4	3.8	4.5	V

BAT（1*AAA）	0.9	1.2	1.8	V
RTCVDD(Li)	1.2	1.5	2.0	V
RTCVDD（1*AAA）	0.9	1.2	2.0	V
DC5V	3.9	5	5.5	V
VCC/UVCC/AVCC/PAVCC	2.8	3.1	3.4	V
VDD/AVDD	1.5	1.7	2.0	V

Note: According to different application, the VDD voltage can config differently. For optimum CPU perfomance, the VDD should be higher than 1.6V; for reduced the power consumption, the VDD can supply with 1.6V.

17.3 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T_O = 25℃, VCC = 0 V.

17.4 DC Characteristics

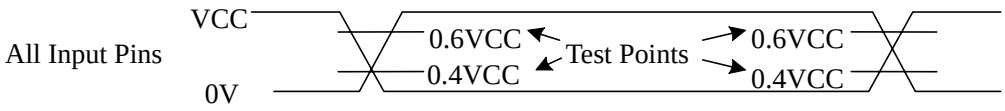
VCC = 3.1V Tamb =-10 °C to 70 °C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0.8	V
High-level input voltage	V_{IH}	2.0			V
Low-level output voltage	V_{OL}			0.4	V
High-level output voltage	V_{OH}	2.4			V

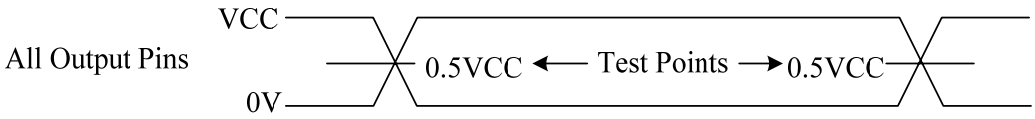
17.5 AC Characteristics

T_o = -10 to +70℃

17.5.1 AC Test Input Waveform

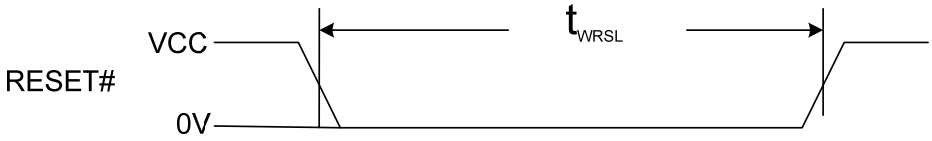


17.5.2 AC Test Output Measuring Points



17.5.3 Reset Parameter

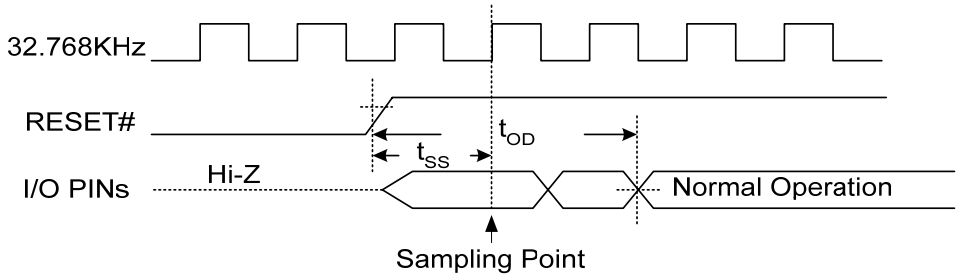
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	50	—	us



17.5.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit

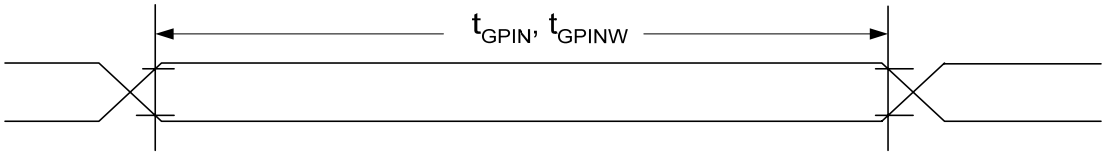
Data sampling time (from RESET#)	tss		—	61.04	us
Output delay time (from RESET#)	tOD		61.04	—	us



17.5.5 GPIO Interface Parameter

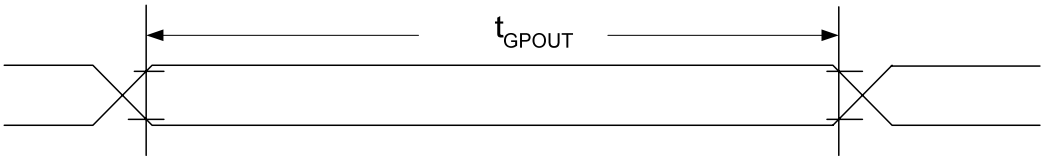
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$11/f_{mcuclk}$		s
GPIO output rise time	t_{GPRISE}		5	50	ns
GPIO output fall time	t_{GPFALL}		5	50	ns
Output level width	t_{GPOUT}		$11/f_{mcuclk}$		s

Notes 1. f_{MCUCLK} is the frequency that MCU is running upon.



Input Level Width

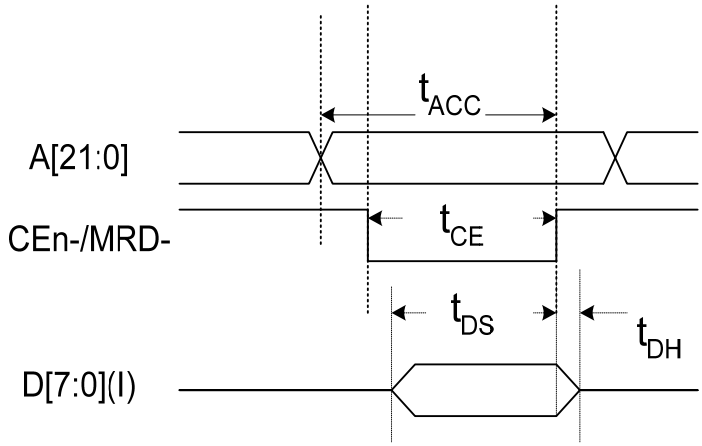
Output Rise/Fall Time



Output Level Width

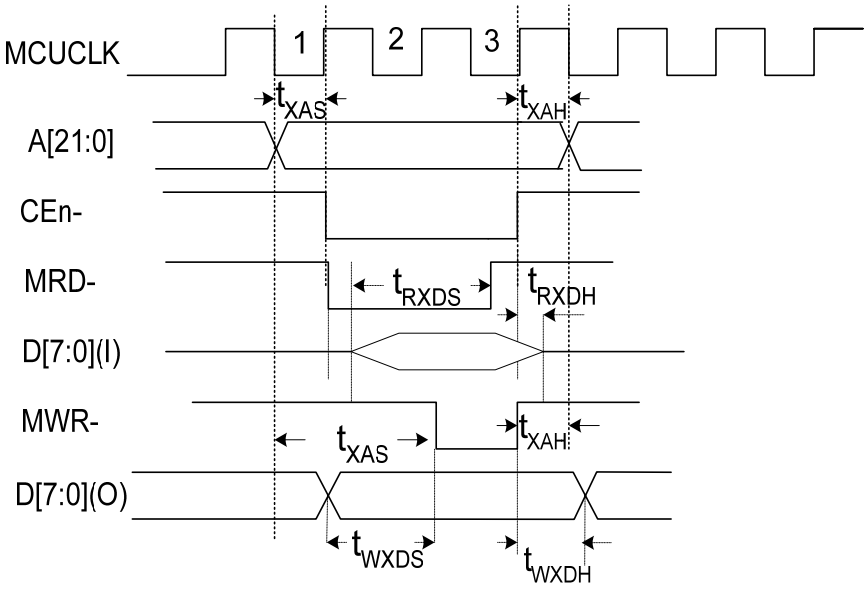
17.5.6 Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	90		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	90		ns
Data input setup time	t_{DS}	HOSC=24MHz	40		ns
Data input hold time	t_{DH}	HOSC=24MHz	15		ns



Ordinary ROM

17.5.7 External System Bus Parameter



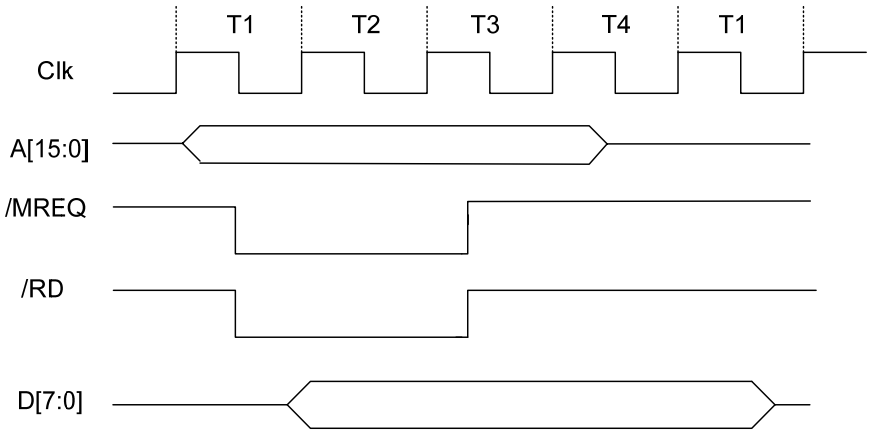
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	10		ns

	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

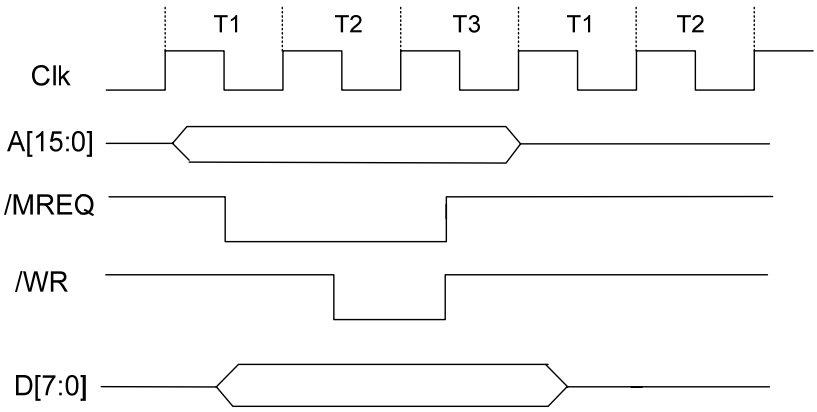
Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

17.5.8 Bus Operation



Memory Read Timing

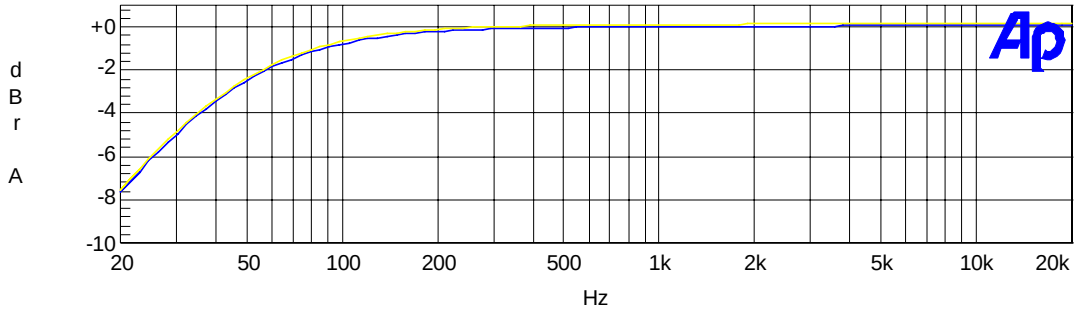


Memory Write Timing

17.5.9 Headphone Driver Characteristics

(T_o =-10 - +70℃, VDD = 1.6 V, VCC = 3.0 V, Sample Rate=32KHz, Volume Level=0x1F)

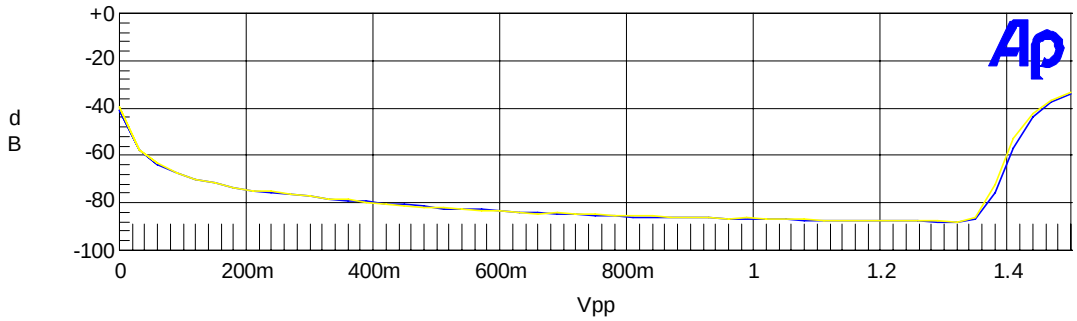
Characteristics	Min	Typ	Max	Unit
Dynamic Range –60 dBFS Input		-87		dB
Total Harmonic Distortion + Noise		-81		dB
Frequency Response 20-20KHz	-7.6	0		dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.3		Vpp
Inter channel Gain Mismatch(1KHz)		-66		dB



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.Level A	Left	
1	3	Yellow	Solid	1	Anlr.Level B	Left	

audio2722.at27

Frequency Response Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	
1	2	Yellow	Solid	1	Anlr.THD+N Ratio	Left	

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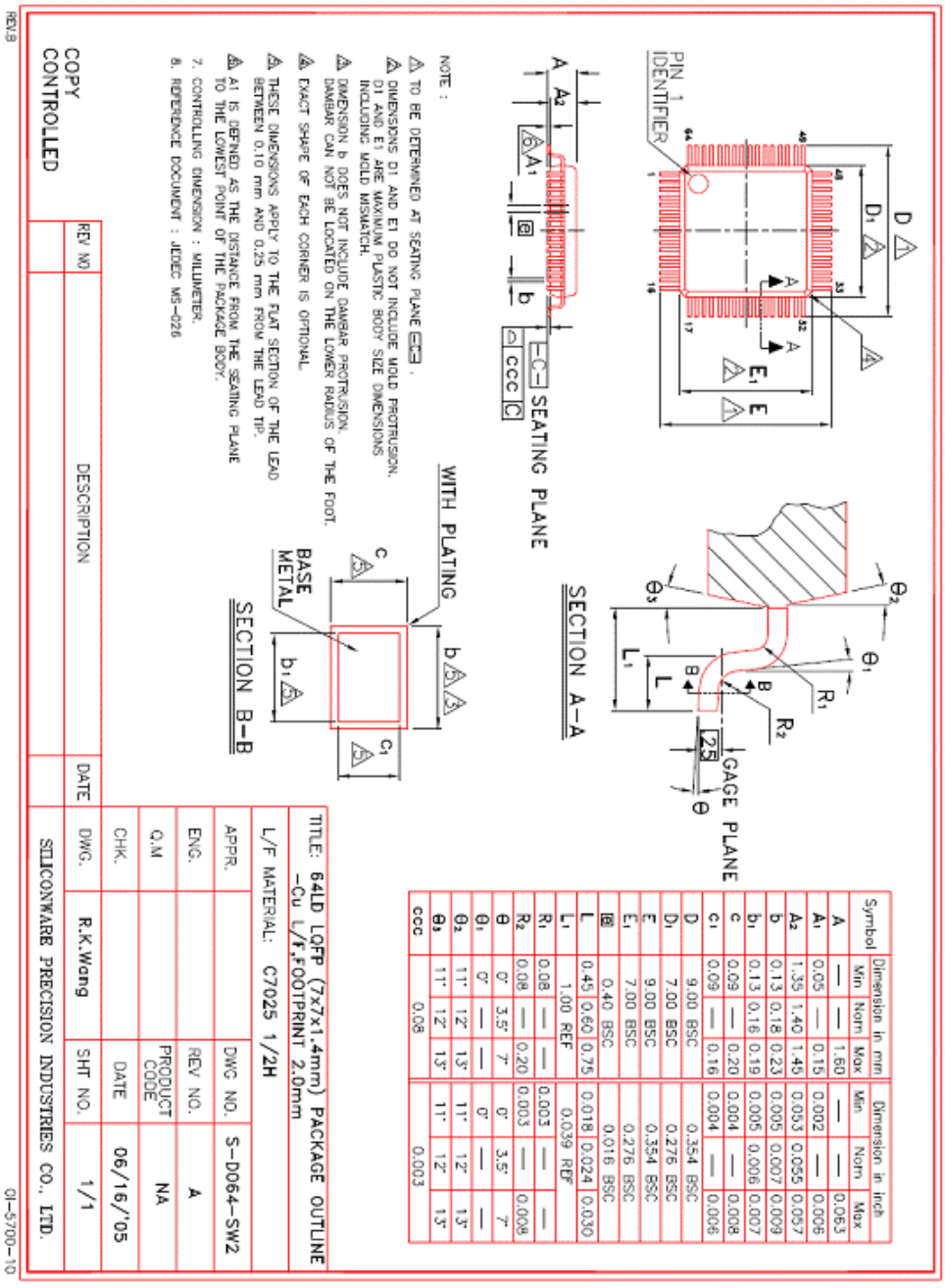
THD + N Amplitude Diagram of Headphone Driver

18 Package Drawing

18.1 ATJ3315 Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

19 Ordering Information

19.1 Recommended Soldering Conditions

Soldering Conditions for Surface-mount Devices

Soldering Process	Soldering Conditions
Infrared Ray Reflow	Peak package's surface temperature: 235℃ (Lead) or 260℃ (Lead Free)
	Reflow time: 30 seconds or less (210℃or more)—(Lead) or 60 seconds or less (217℃or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note:

The maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution:

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

19.2 Precaution against ESD for Semiconductors

When the strong electric field is exposed to a MOS device, the destruction of the gate oxide may occur and then it can ultimately degrade the device operation. Measures must be taken to stop the generation of static electricity as many as possible, and it is a must to quickly dissipate the static electricity when it occurs. Environmental control must be adequate enough. Humidifier should be used when it is dry. Recommend to avoid using insulators, which may easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container or a static shielding bag or objects made from conductive material. All test and measurement tools including work bench and floor should be grounded. The operator shall be grounded by using wrist strap. Semiconductor devices shall not be touched with bare hands. Similar precautions shall be taken for PW boards with semiconductor devices on it.

19.3 Handling of Unused Input Pins for CMOS

The cause for no connection to CMOS device inputs can be the malfunction. If no connection is provided for the input pins, the possible cause is that an internal input level may be generated due to noise, etc., which results in malfunction. CMOS devices behave differently from Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin shall be connected to VCC or GND with a resistor, if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device and follows the related specifications governing the devices.

19.4 Status before Initialization of MOS Devices

Power-on does not necessarily define the initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned on, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after the power-on.

20 Appendix

20.1 24.1 Acronym and Abbreviations

ACK—Acknowledgement
ADC—Analog Digital Convert
ATAIRQ—Advanced Technology Attachment Interrupt Request
CTC—Clock/Timer/Counter
DAC—Digital Analog Convert
DMA—Direct Memory Address
DRQ—Data Request
DST—Destination
DST—Destination
ECC—Error Correction Code
EM—External Memory
FIFO—First In First Out
HIP—Host Interface Port
HOSC—High Frequency Oscillator
IDM—Internal Data Memory
IPM—Internal Program Memory
IRQ—Interrupt Request
IR—Infra-red
LOSC—Low Frequency Oscillator
MIC—Microphone
NAK—Negative Acknowledgement
PLL—Phase Locked Loop
RTC—Real Time Clock
RB—Ready/Busy
SIRQ—System Interrupt Request
SPDIF—Sony/Philips Digital Interface
SPI—Serial Port Interface
SRC—Source
TC—Transmit Complete
UART—Universal Asynchronous Receiver/Transmitter

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