AZ DISPLAYS

SPECIFICATIONS FOR

LIQUID CRYSTAL DISPLAY

CUSTOMER APPROVAL
※ PART NO. : ATM1010L21 (AZ DISPLAYS)   VER1.0

APPROVAL		COMPANY CHOP	
CUSTOMER COMMENTS			

AZ DISPLAYS ENGINEERING APPROVAL		
DESIGNED BY	CHECKED BY	APPROVED BY
CXR		

DOCUMENT REVISION HISTORY

Change No.	Date	Subject And Reason	Version No.	Responser
1	2017.11.06	First issue	1.0	

CONTENTS

ATM1010L21 (AZ DISPLAYS) TFT MODULE V1.0

1. OVERVIEW

ATM1010L21 is 10.1" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs ,control circuit and LED backlight. By applying 1024×600 images are displayed on the 10.1" diagonal screen. Display 16.2M colors by R.G.B signal input.

General specification are summarized in the following table:

| ITEM	SPECIFICATION			
Display Area (mm)	222.72(W) x 125.28(H)			
Number of Pixels	1024(H) × 3 (RGB) × 600(V)			
Pixel Pitch (mm)	0.2175(W) x 0.2088(H)			
Color Pixel Arrangement	RGB vertical stripe			
Display Mode	Normally white			
Number of Colors	16.2M			
Brightness (cd/m^2)	410nit(typ)			
Response Time (ms)	25ms(typ.)			
Optimum Viewing Direction	6 O'clock(Max contrast ratio,Gray level inversion)			
Contrast Ratio	600:1			
Viewing Angle (CR≧10)	140degree (Horizontal.)			
	120degree (Vertical)			
Power Consumption (W)	3.16(typ.)			
Interface connection	LVDS			
Module Size (mm)		Min.	Typ.	Max.
	Horizontal (H)	234.7	235	235.3
	Vertical (V)	142.7	143	143.3
	Depth (D) w/o FPC	4.4	4.7	5.0
Assembly size(mm)	235.00(H) X 143.00(V) X 4.7(D)			
Module Weight (g)	275(typ)			
Backlight Unit	LED			
Surface Treatment	Anti-Glare			

2. ABSOLUTE MAXIMUM RATINGS

The following are maximun values which, if exceeded, may cause faulty operation ordamage to the unit.

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VDD VDD_LVDS	-0.3	3.96	V	
Analog Supply Voltage	AVDD	-0.5	14.85	V	
Gate On Voltage	VGH	-0.3	40	V	
Gate Off Voltage	VGL	-20	0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	12	40	V	
Signal Input Voltage	NIN0 ~ NIN3 PIN0 ~ PIN3 NINC,PINC	-0.5	5	V	
Forward Current (per LED)	If	-	40	mA	
Reverse Voltage (per LED)	VR	-	5	V	
Pulse forward current (per LED)	Ifp	-	100	mA	Note 1、2
Operation Temperature	Top	-20	70	℃	Note 3
Storage Temperature	Tstg	-30	80	℃	Note 3

Note1：Ifp Conditions ： Duty≦1/10@Pulse Width≦10msec

Note2：Each one of LED operation must be follow diagram of Ambient Temperature and Allowable Forward Current.

■ Ambient Temperature vs. Allowable Forward Current
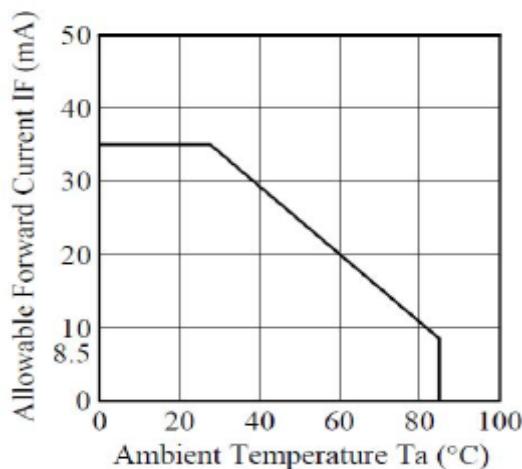
Note3：If users use the product out off the environmemtal operation range（temperature and humidity）, it will have visual quality concerns.

3. ELECTRICAL CHARACTERISTICS

3.1. TFT LCD

Item	Symbol	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	DVDD DVDD_LVDS	3	3.3	3.6	V	
Logic Input Voltage (LVDS:IN+,IN-)	VCM	$\dfrac{|VID|}{2}$	-	$2.4 - \dfrac{|VID|}{2}$	V	Note 1
	$|VID|$	200	-	600	mV	Note 1
	VTH	-	-	100	mV	VCM=1.2V Note 1
	VTL	-100	-	-	mV	
Analog Power Supply Voltage	AVDD	9.4	9.6	9.8	V	
Gate On Power Supply Voltage	VGH	17	18	19	V	
Gate Off Power Supply Voltage	VGL	-6.6	-6	-5.4	V	
Common Power Supply Voltage	VCOM	3.8	4.0	4.2	V	Note 2
Gamma Voltage	V1	-	9.02	-	V	
	V2	-	9.01	-	V	
	V3	-	7.62	-	V	
	V4	-	7.15	-	V	
	V5	-	6.85	-	V	
	V6	-	6.52	-	V	
	V7	-	6.46	-	V	
	V8	-	3.58	-	V	
	V9	-	3.5	-	V	
	V10	-	3.1	-	V	
	V11	-	2.76	-	V	
	V12	-	2.23	-	V	
	V13	-	0.67	-	V	
	V14	-	0.63	-	V	

Note1：LVDS signal

LVDS VINP

LVDS VINN
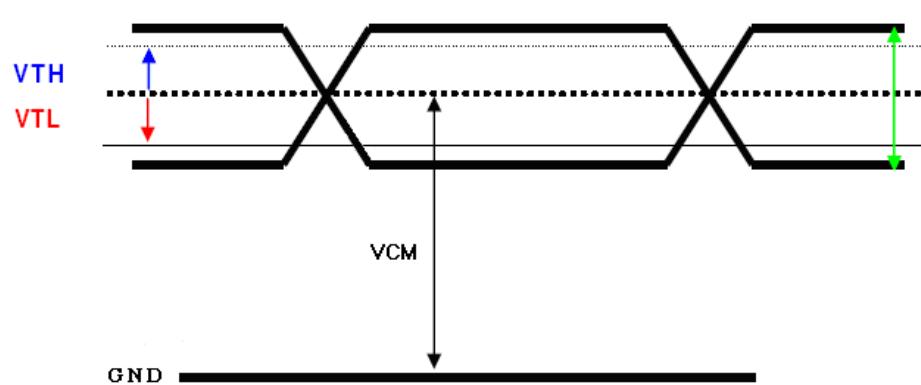
Note2：Please adjust VCOM to make the flicker level be minimum.

3.2.   TFT-LCD Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Gate on power current	IVGH	VGH =18V	-	0.5	1	mA	Note 1
Gate off power current	IVGL	VGL= -6V	-	0.5	1	mA	Note 1
Digital power current	IVDD	VDD = 3.3V	-	40	50	mA	Note 1
Analog power current	IAVDD	AVDD = 9.6V	-	35	45	mA	Note 1
Total Power Consumption	PC		-	480	621	mW	Note 1

Note 1: Typical: Under 256 gray pattern
   Maximum: Under black pattern
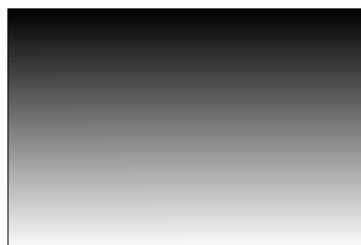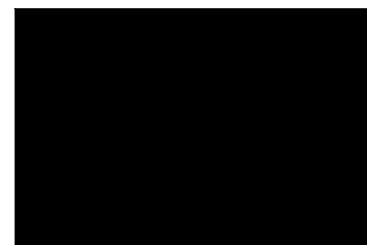
256 gray pattern   Black pattern

3.3.   Power、Signal sequence

Power On：DVDD→AVDD/VGL→VGH→Video &Logic Signal→Backlight
Power Off：Backlight→Video &Logic Signal→VGH→AVDD/VGL→DVDD

0<T1≦10ms
T2>0ms
T3>20ms
T4>0ms
T5>10ms
0<T6≦10ms
T12≧200ms

0ms<T7<50ms
0ms<T8<50ms
T9>0ms
T10>0ms
0<T11≦10ms
T13≧200ms
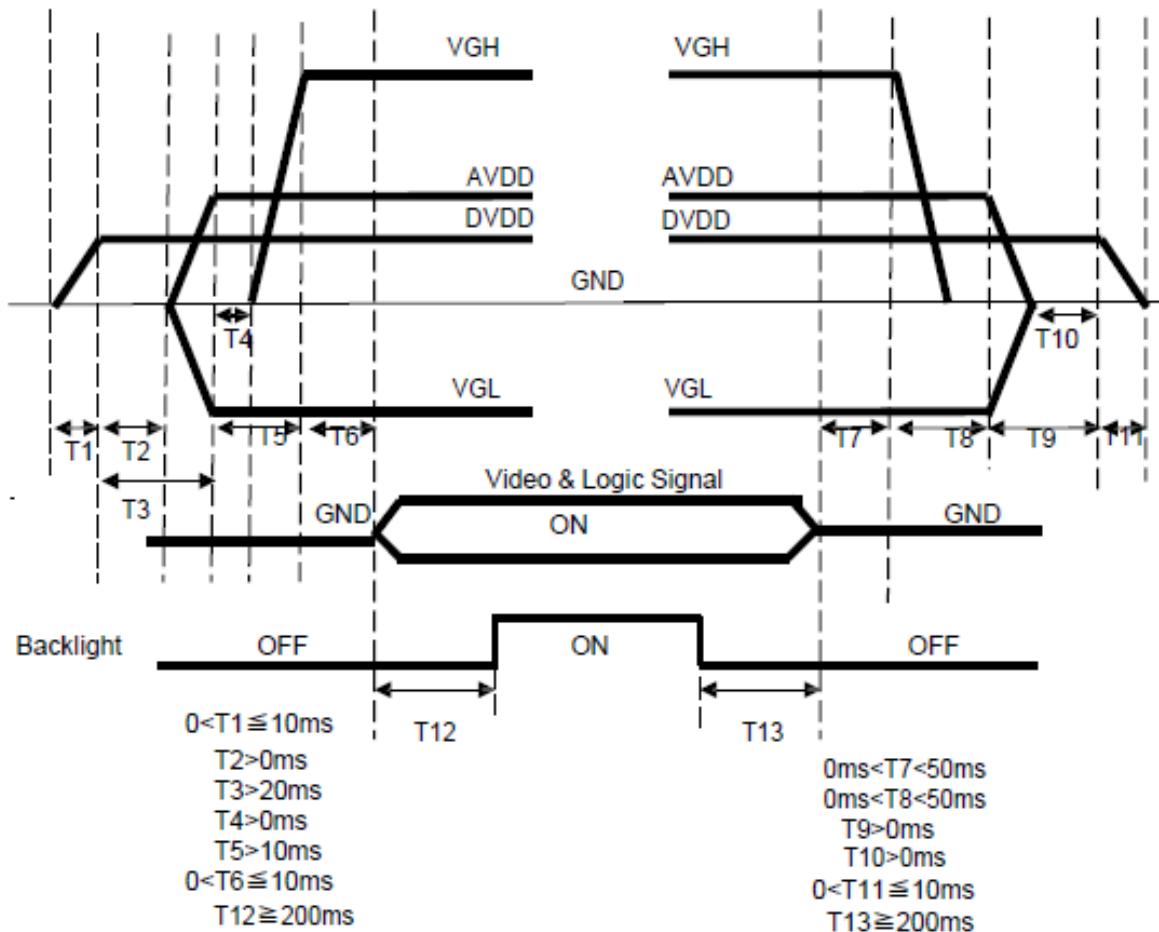
3.4.   Backlight

Ta=25℃

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
LED current	IL	Ta=25℃ (20mA/series)	--	140	--	mA	
LED voltage	VL	Ta=25℃ 20mA/series)	17.5	18.5	19.5	V	
Power consumption	WL	Ta=25℃ (20mA/series)	--	2.590	--	W	
LED Lifetime	-	Ta=25℃ IF=20mA	20000	--	--	Hr	

Remarks:
 *1) LED Circuit Diagram
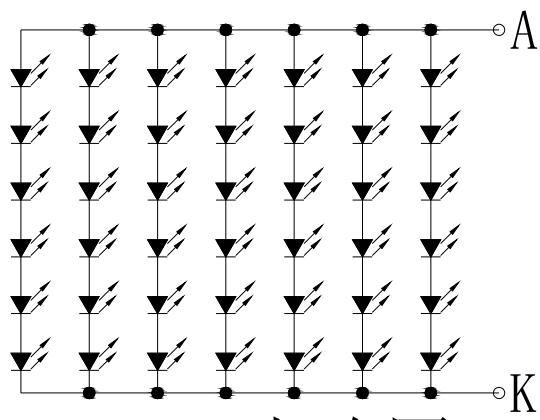
LED电路图
（6S7P=42LED）

*2) A:Anode(＋),K:Cathode(－)
*3) Suggestion: Using the constant current control to avoid the leakage light and brightness quality issue.
*4) Definition of Led lifetime:Luminance < Initial luminance 50%.

4. INTERFACE CONNECTION
4.1. CN1 (Input Signal)

FPC Connector is used for the module electronics interface. The recommended model is HIROSE FH28-60S-0.5SH(05), MOLEX 1040606017 or compatible.

PIN NO	SYMBOL	DESCRIPTION	NOTE
1	AGND	Analog ground	
2	AVDD	Analog power	
3	DVDD	Digital power	
4	GND	Digital ground	
5	VCOM	Common voltage	
6	DVDD	Digital power	
7	GND	Digital ground	
8	V14	Gamma correction voltage reference	
9	V13	Gamma correction voltage reference	
10	V12	Gamma correction voltage reference	
11	V11	Gamma correction voltage reference	
12	V10	Gamma correction voltage reference	
13	V9	Gamma correction voltage reference	
14	V8	Gamma correction voltage reference	
15	GND	Digital ground	
16	DVDD_LVDS	LVDS power	
17	GND	Digital ground	
18	PIND3	Positive LVDS differential data input	
19	NIND3	Negative LVDS differential data input	
20	GND	Digital ground	
21	PINC	Positive LVDS differential clock input	
22	NINC	Negative LVDS differential clock input	
23	GND	Digital ground	
24	PIND2	Positive LVDS differential data input	
25	NIND2	Negative LVDS differential data input	
26	GND	Digital ground	
27	PIND1	Positive LVDS differential data input	
28	NIND1	Negative LVDS differential data input	
29	GND	Digital ground	
30	PIND0	Positive LVDS differential data input	
31	NIND0	Negative LVDS differential data input	
32	GND	Digital ground	
33	GND_LVDS	LVDS ground	
34	GRB	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10KΩ，C=0.1μF)	
35	STBYB	Standby mode, normally pull high STBYB=" 1", normal operation STBYB=" 0",timing control, source driver will turn off, all output are high-Z	

36	SHLR	Left or right display control	Note 1
37	DVDD	Digital power	
38	UPDN	Up / down display control	Note 1
39	AGND	Analog ground	
40	AVDD	Analog power	
41	VCOM	Common voltage	
42	DITH	Dithering function enable control. Normally pull low DITHER = "1", Enable internal dithering function DITHER = "0", Disable internal dithering function	
43	GND	Digital ground	
44	DVDD	Digital Power	
45	GND	Digital ground	
46	V7	Gamma correction voltage reference	
47	V6	Gamma correction voltage reference	
48	V5	Gamma correction voltage reference	
49	V4	Gamma correction voltage reference	
50	V3	Gamma correction voltage reference	
51	V2	Gamma correction voltage reference	
52	V1	Gamma correction voltage reference	
53	GND	Digital ground	
54	DVDD	Digital power	
55	SELB	6bit/8bit mode select, SELB = "0", LVDS input data is 8bits SELB = "1", LVDS input data is 6bits	Note 2
56	VGH	Positive power for TFT	
57	DVDD	Digital power for Gate IC	
58	VGL	Negative power for TFT	
59	GND	Digital ground for Gate IC	
60	NC	Not connect	

Remarks：Mating connector：089K60-000100-G2-R (STARCONN)

Note 1:UPDN and SHLR control function

UD	LR	FUNCTION
0	1	Normal display
0	0	Inverse Left and Right
1	1	Inverse Up and Down
1	0	Inverse Left and Right Inverse Up and Down

Up

Left

Right

Down
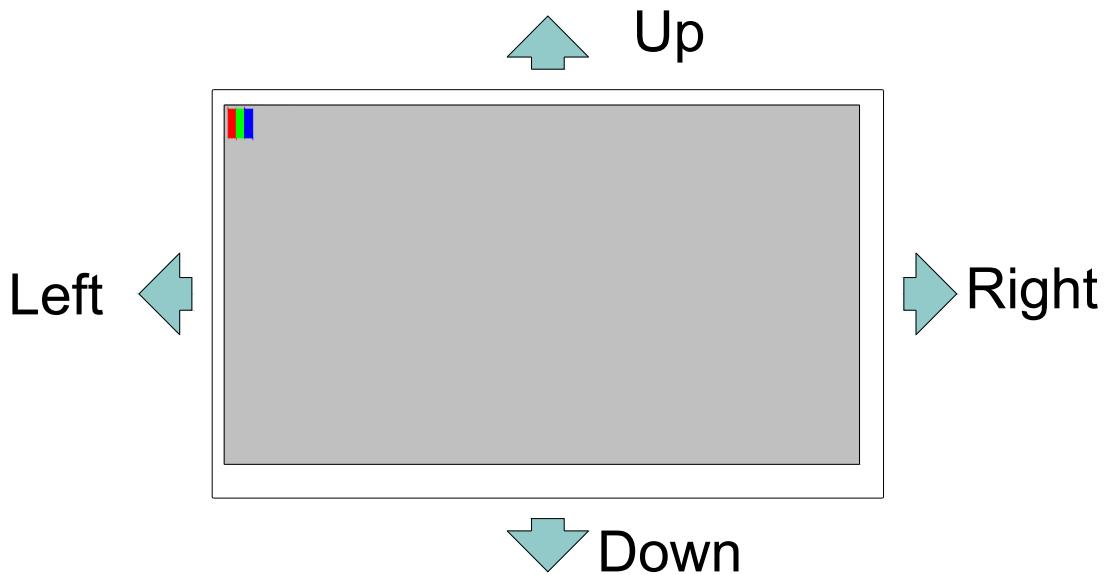
Note 2: if LVDS input data is 6bits,SELB must must be set to High
if LVDS input data is 8bit , SELB must be set to Low
DITH and SELB control function

DITH	SELB	FUCTION
0	1	Colors (262K)
0	0	Colors (262K)
1	1	Colors (262K)
1	0	Colors (16.2M)

4.2. CN2（backlight）

PIN NO	SYMBOL	FUNCTION
1	A	Anode
2	K	Cathode

Note：
Input connector : BHSR-02VS-1(JST)
Outlet connector: SM02B-BHSS-1(JST)

5. INPUT SIGNAL(DE ONLY MODE)

5.1. Timing Specification

ITEM			SYMBOL	MIN	TYP	MAX	UNIT
LVDS input signal sequence	CLK Frequency		tclk	45	51.2	57	MHz
LCD input signal sequence（Input LVDS Transmitter）	DENA	Horizontal	Horizontal total Time	tH	1324	1344	1364	tCLK
			Horizontal effective Time	tHA		1024		tCLK
			Horizontal Blank Time	tHB	300	320	340	tCLK
		Vertical	Vertical total Time	tV	625	635	645	tH
			Vertical effective Time	tVA		600		tH
			Vertical Blank Time	tVB	25	35	45	tH

5.2. Timing sequence(Timing chart)

### 5.2.1. Horizontal Timing Sequence:
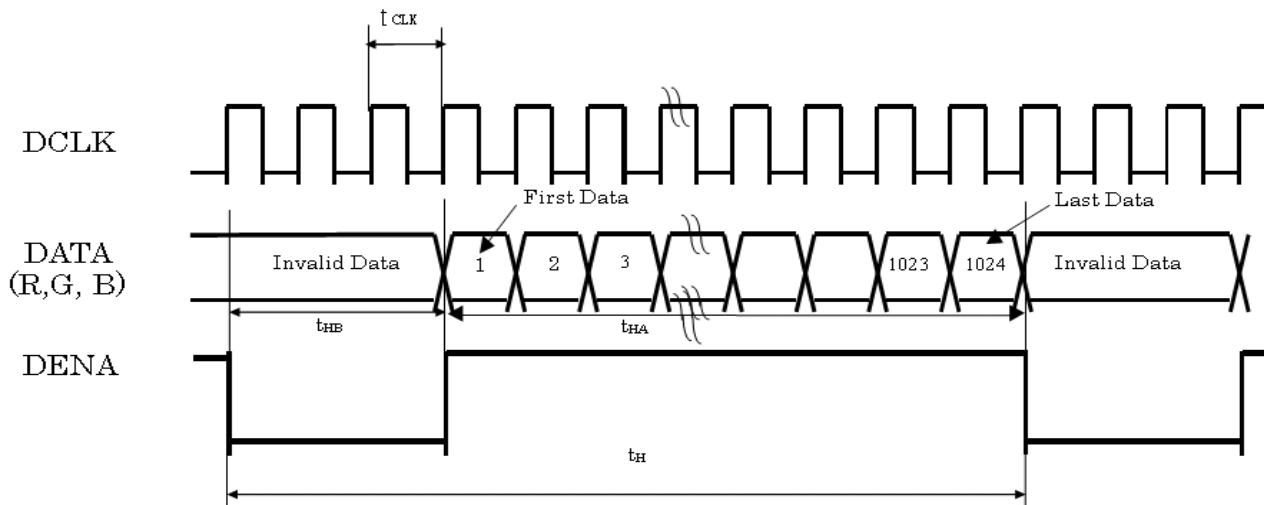
5.2.2. Vertical Timing Sequence:
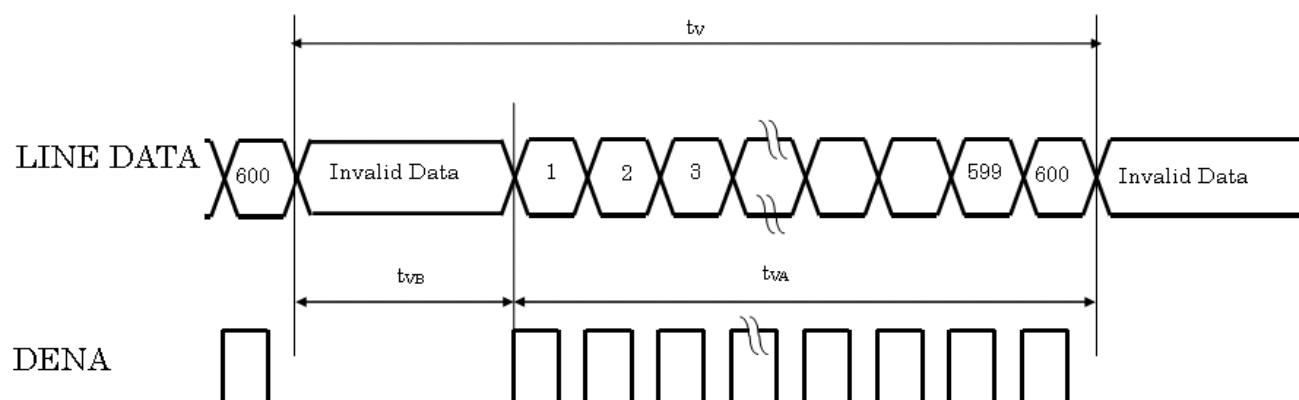
5.2.3. LVDS Input Data mapping

6 Bit LVDS input

PINC									
NINC									
PIND0 / NIND0	R0	G0	R5	R4	R3	R2	R1	R0	G0
PIND1 / NIND1	G1	B1	B0	G5	G4	G3	G2	G1	B1
PIND2 / NIND2	B2	DE	—	—	B5	B4	B3	B2	DE

PREVIOUS ←→ DATA for current CLK cycle ←→ NEXT

8 Bit LVDS input

PINC									
NINC									
PIND0 / NIND0	R0	G0	R5	R4	R3	R2	R1	R0	G0
PIND1 / NIND1	G1	B1	B0	G5	G4	G3	G2	G1	B1
PIND2 / NIND2	B2	DE	—	—	B5	B4	B3	B2	DE
PIND3 / NIND3	R6	-	B7	B6	G7	G6	R7	R6	-
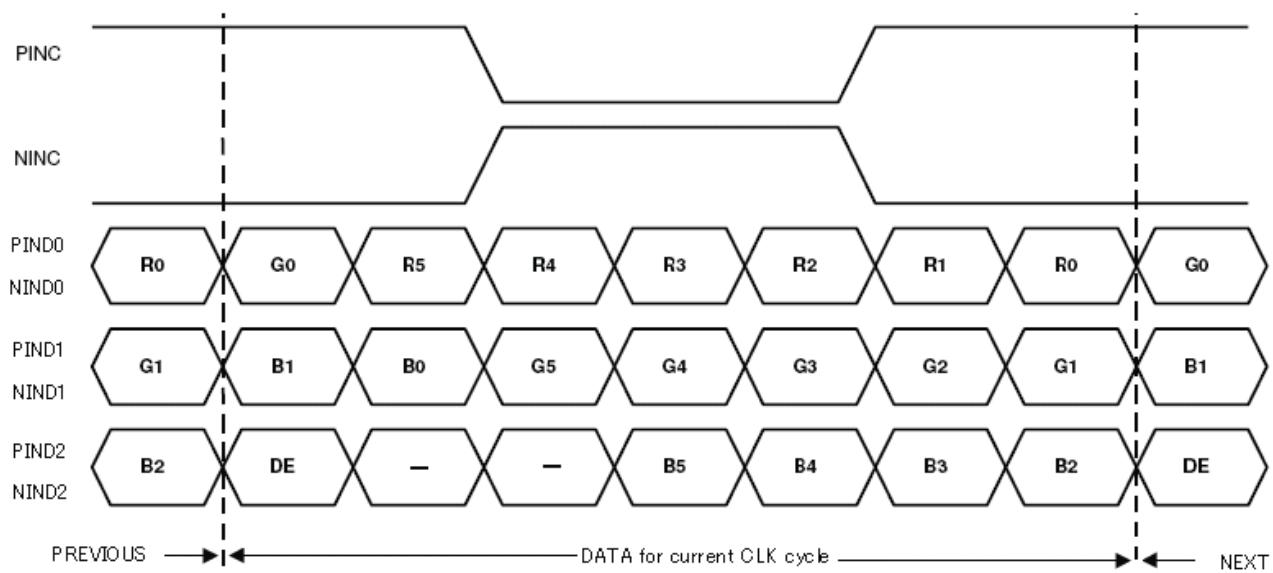
PREVIOUS ←→ DATA for current CLK cycle ←→ NEXT
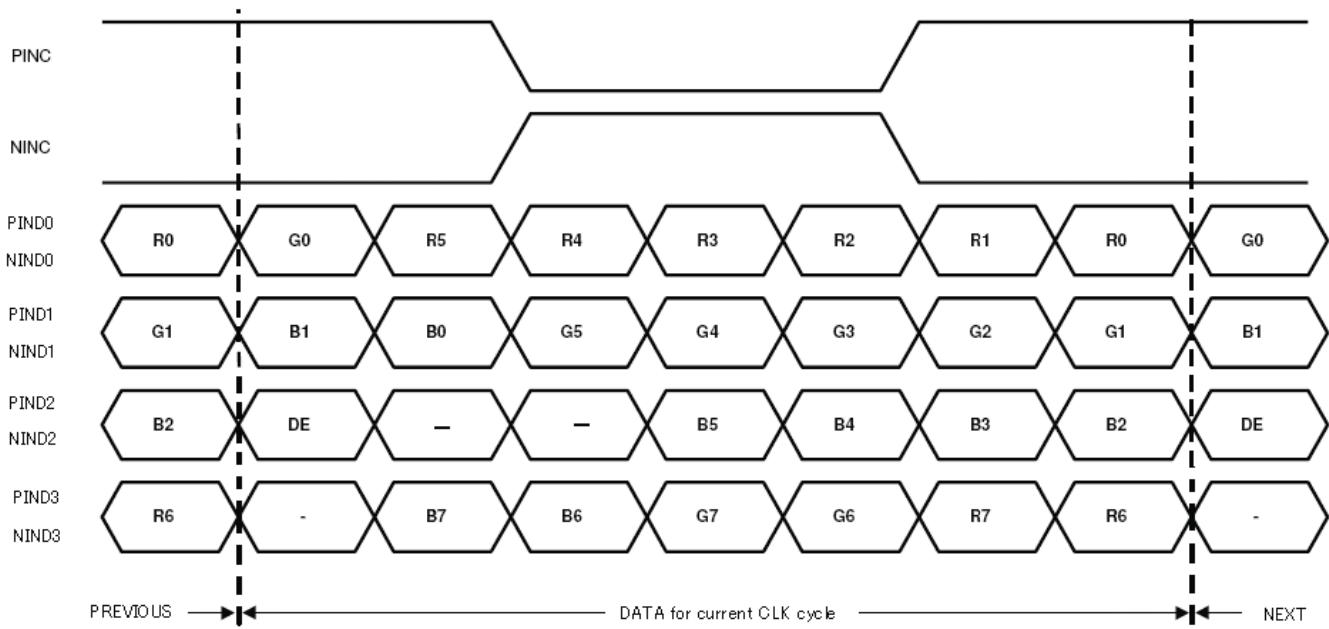
6. OPTICAL CHARACTERISTICS

Ta = 25℃, VCC=3.3V

ITEM		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Contrast Ratio		CR	Point-5	500	600		--	1,2,3
Luminance(CEN)		LW	Point-5	350	410		cd/m^2	1,3
Luminance Uniformity		ΔL		70	80		%	1,3
Response Time (White - Black)		Tr +Tf	Point-5	-	25	40	ms	1,3,5
NTSC		-	Point-5	45	50	-	%	1,4
Viewing Angle	Horizontal	Left(ψ)	CR≧10 Point-5	60	70	--	°	1,4
		Right(ψ)		60	70	--	°	1,4
	Vertical	Upper(θ)		40	50	--	°	1,4
		Down(θ)		60	70	--	°	1,4
Color Coordinate	White	Wx Wy	Point-5	0.273 0.289	0.313 0.329	0.353 0.369	--	1,3
	Red	Rx Ry		0.550 0.300	0.590 0.340	0.630 0.380		
	Green	Gx Gy		0.301 0.554	0.341 0.594	0.381 0.634		
	Blue	Bx By		0.117 0.075	0.157 0.115	0.197 0.155		

Note1： Measure condition: 25℃±2℃, 60±10%RH, under10 Lux in the dark room.BM-5A (TOPCON), viewing angle2°, IL=140 mA （Backlight current）, measurement after lighting on 10 mins.
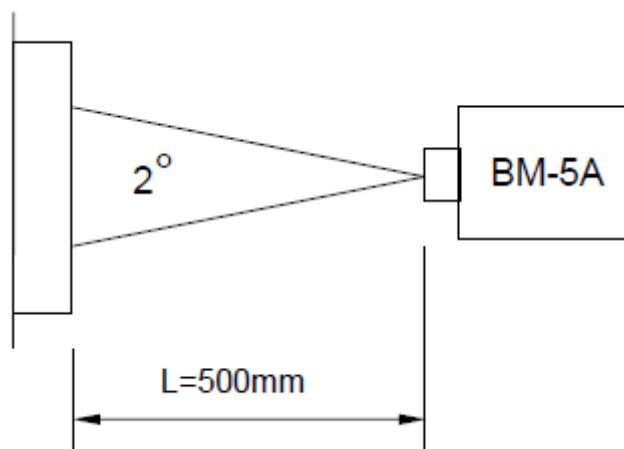
Note2：Definition of contrast ratio：
   Contrast Ratio (CR)= (White) Luminance of ON ÷ (Black) Luminance of OFF

Note3： Definition of luminance：Measure white lu minance on the point 5 as figure.6-1
 Definition of Luminance Uniformity: Measure white luminance on the point1~9 as figure.6-1

$$\triangle L = [L(MIN)/L(MAX)] \times 100$$
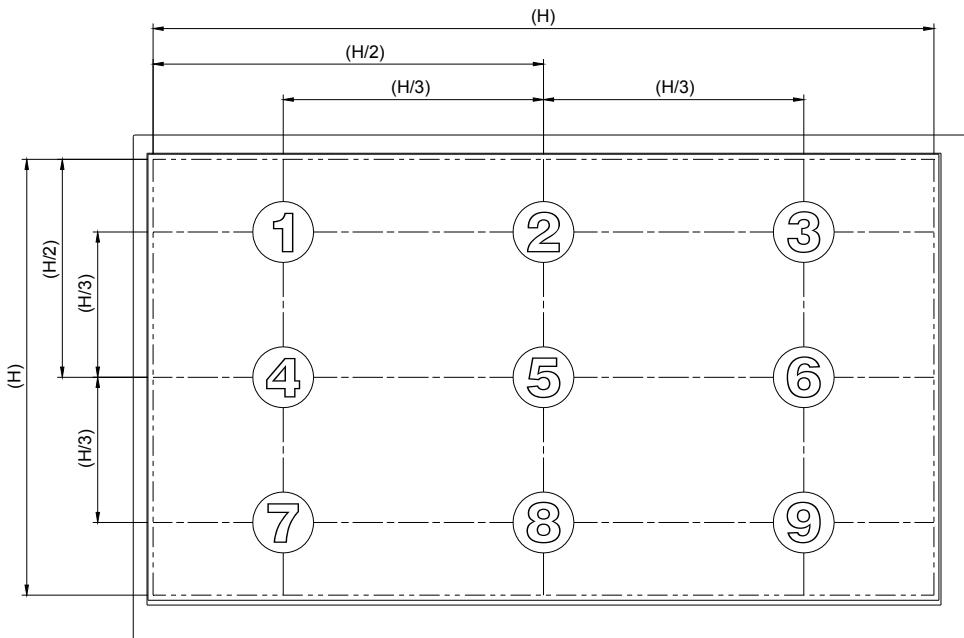
Fig.6-1 Measuring point

Note 4：Definition of Viewing Angle(θ , ψ),refer to Fig.6-2 as below：
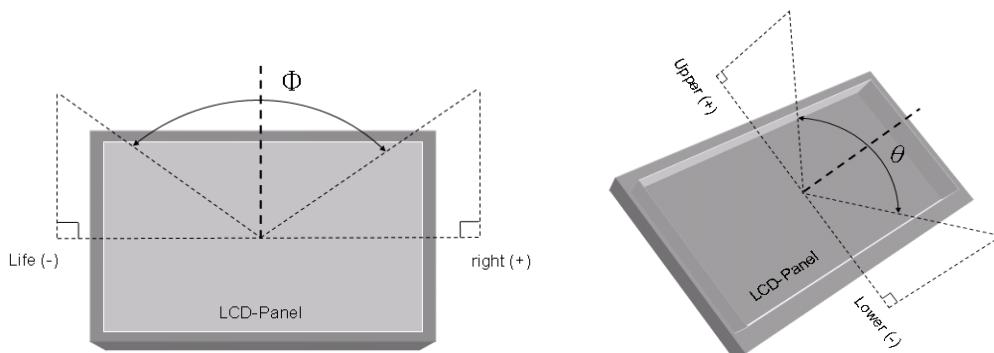
Fig.6-2 Definition of Viewing Angle

Note5：Definition of Response Time.(White-Black)
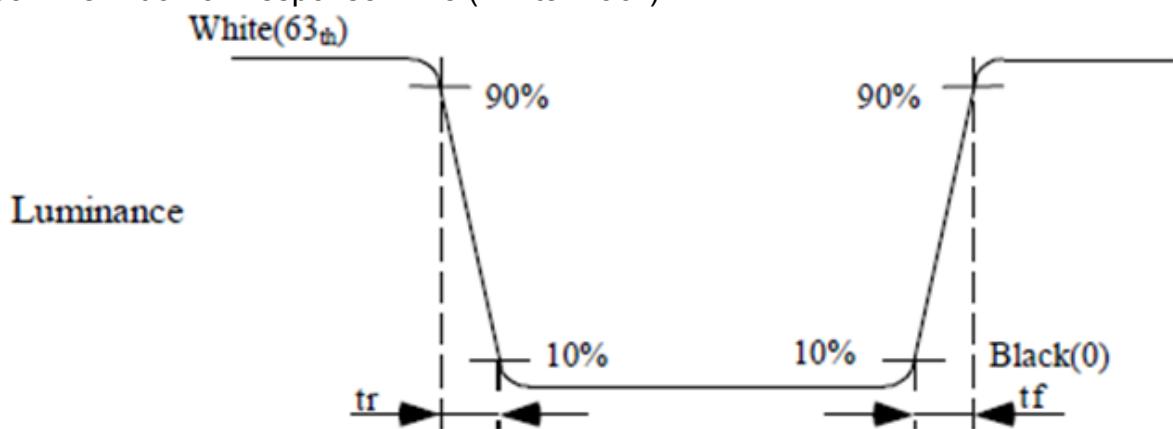
Fig.6-3 Definition of Response Time(White-Black)

7. RELIABILITY TEST

7.1. Temperature and humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	70℃ ;240hrs	
High Temperature Storage	80℃ ; 240hrs	
High Temperature High Humidity Operation	60℃ ; 90%RH ;240hrs	No condensation
Low Temperature Operation	-20℃ ; 240hrs	Backlight unit always turn on
Low Temperature Storage	-30℃ ; 240hrs	
Thermal Shock	–20℃(0.5hr) ~ 70℃(0.5hr) ; 200 Cycles	
Image Sticking	25℃ ; 4hrs	

Note 1：

Condition of Image Sticking test：25℃± 2℃

Operation with test pattern sustained for 4 hrs, then change to mid-gray pattern immediately.

After 5 mins, the mura must be disappeared completely .
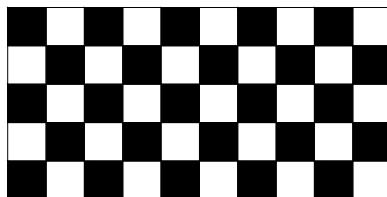
Image Sticking -pattern   Mid-Gray pattern
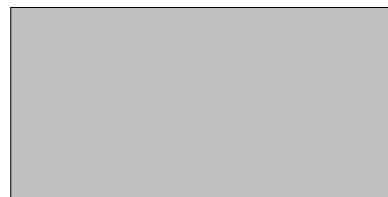
7.2. Shock and Vibration

ITEMS	CONDITIONS
Shock (Non-operation)	● Shock level: 980m/s^2(equal to 100G). ● Waveform: half sinusoidal wave,6ms. ● Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of three shock inputs.
Vibration (Non-operation)	● Frequency range:8~33.3Hz ● Stoke：1.3 mm ● Vibration: sinusoidal wave, perpendicular axis(both x, z axis: 2Hrs,y axis 4Hrs). ● Sweep: 2.9G,33.3 Hz -400 Hz ● Cycle: 15 min

7.3. Electrostatic Discharge

TEST ITEM	CONDITIONS	Note
ESD	150pF，330Ω，±8kV&±15kV air& contact test	1
	200pF，0Ω，±200V contact test	2

Note： Measure
   1: LCD glass and metal bezel
   2: IF connector pins

7.4. Judgment standard

The Judgment of the above test should be made as follow:

Pass: Normal display image and no line defect.

   Partial transformation of the module parts should be ignored.

Fail: No display image, Function NG, or line defects.

8. MENSION

*4.70±0.30

BHSR–02VS–1

230±10

30.30

W0.3±0.03

Set 2

P0.5(60-1)=29.5±0.03

30.5±0.07

4±0.30

0.5±0.10

DETAIL A(2:1)

70.30±1

PIN60

A

30/50

PIN1

118.85±1

*235.00(Out Line)
*226.00(Bezel Openg)
*222.72(A.A)

(116.65)

Display Center

RGB

3.65
5.29

(68.40)

5.76
4.15

*125.28(A.A)
*128.50(Bezel Openg)
*143.00(Out Line)
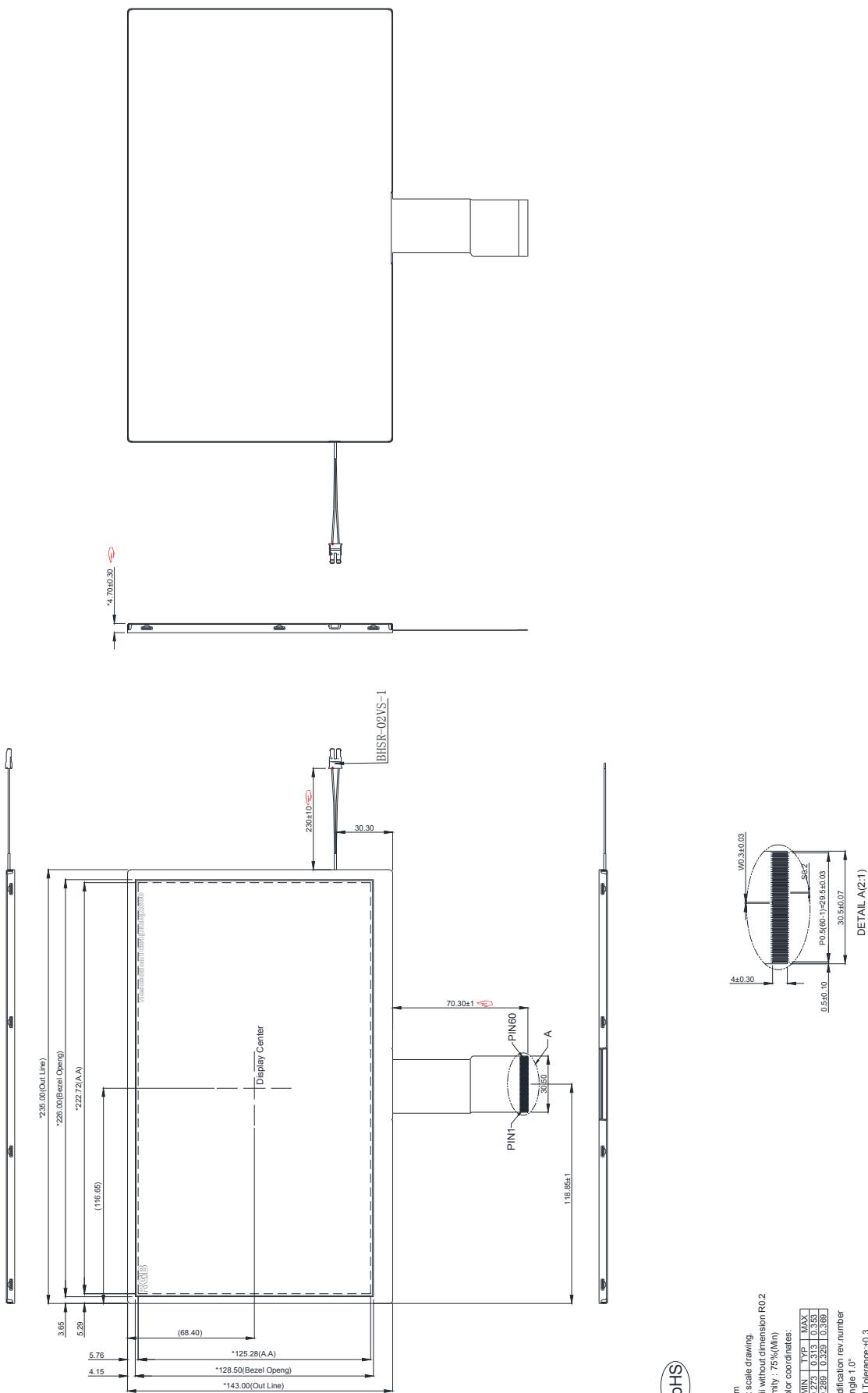
(RoHS)

Notes:

1.Unit:mm
2.Do not scale drawing.
3.All radii without dimension R0.2
4.Uniformity : 75%(Min)
5.The color coordinates:

	MIN	TYP	MAX
x	0.273	0.313	0.353
y	0.289	0.329	0.369

6. △ Modification rev.number
7.draft angle 1.0°
8.Genral Tolerance:±0.3
9. Mark mold cavity indentification in recess approximately
   where indicated.
10. "*" For important dimension,( ) for reference dimention
11. RoHS must be compiled.(Use Lead-free process)

AZ DISPLAYS

9. Packing form

   TBD

10. WARRANTY

    10.1 The period is within 12 months since the date of shipping out under normal using and storage conditions.

    10.2 The warranty will be avoided in case of defect induced by customer