

## Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 16-Kbyte Data Cache, 16-Kbyte Instruction Cache, Write Buffer
  - 220 MIPS at 200 MHz (1.1 MIPS/MHz)
  - Memory Management Unit
  - Embedded ICE In-circuit Emulation, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- GPS Engine
  - GPS Engine with Massive Parallel Correlation
  - Highest Acquisition and Tracking Sensitivity
  - Fast Time To First Fix (TTFF)
  - SBAS Support (WAAS, EGNOS)
  - NMEA 2.2 Data Format
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Addresses Internal and External Memories
- Embedded Memories
  - One 128-Kbyte Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - One 80-Kbyte Internal SRAM, Single-cycle Access at Maximum Processor or Matrix Speed
  - One 16-Kbyte Internal SRAM, Single-cycle Access at Maximum Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 Bits per Pixel in TFT Mode, Up to 16 Bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution up to 2048×2048, Supports Wider Screen Buffers
- 2D Graphics Accelerator
  - Line Draw, Block Transfer, Polygon Fill, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
- 4×4 Keypad Matrix Controller
- USB 2.0 Full-speed (12 Mbits per Second) Host Double Port and Device Port
- Ethernet MAC 10/100 Base T
- One Part 2.0A and Part 2.0B Compliant CAN Controller
- Two Multimedia Card Interfaces (MCI)
- Two Synchronous Serial Controllers (SSC)
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
- Two Master/Slave Serial Peripheral Interfaces (SPI)
- One Two-wire Interface (TWI)
- One AC97 Controller (AC97C)



## ARM926 SOC with Integrated GPS Baseband

### ATR0663

### Summary

### Preliminary

**NOTE:** This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

4949AS-GPS-09/06





- **Fully-featured System Controller, Including**
  - **Reset Controller (RTSC), Shut-down Controller (SHDC)**
  - **Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes**
  - **Clock Generator (CKGR)**
    - **32.768 KHz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock**
    - **3 to 20 MHz On-chip Oscillator and Two up to 240 MHz PLLs**
  - **Power Management Controller (PMC)**
  - **Advanced Interrupt Controller (AIC) and Debug Unit (DBGU)**
  - **Periodic Interval Timer (PIT), Watchdog Timer (WDT) and Double Real-time Timer (RTT)**
- **Five 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)**
- **Power Supplies:**
  - **1.08V to 1.32V for VDDCORE and VDDBU**
  - **3.0V to 3.6V for VDDOSC, VDDPLL and VDDIOP0 (Peripheral I/Os)**
  - **Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOP1 (Peripheral I/Os) and for VDDIOM0/VDDIOM1 (Memory I/Os)**
- **Temperature Range –40°C to +80°C**

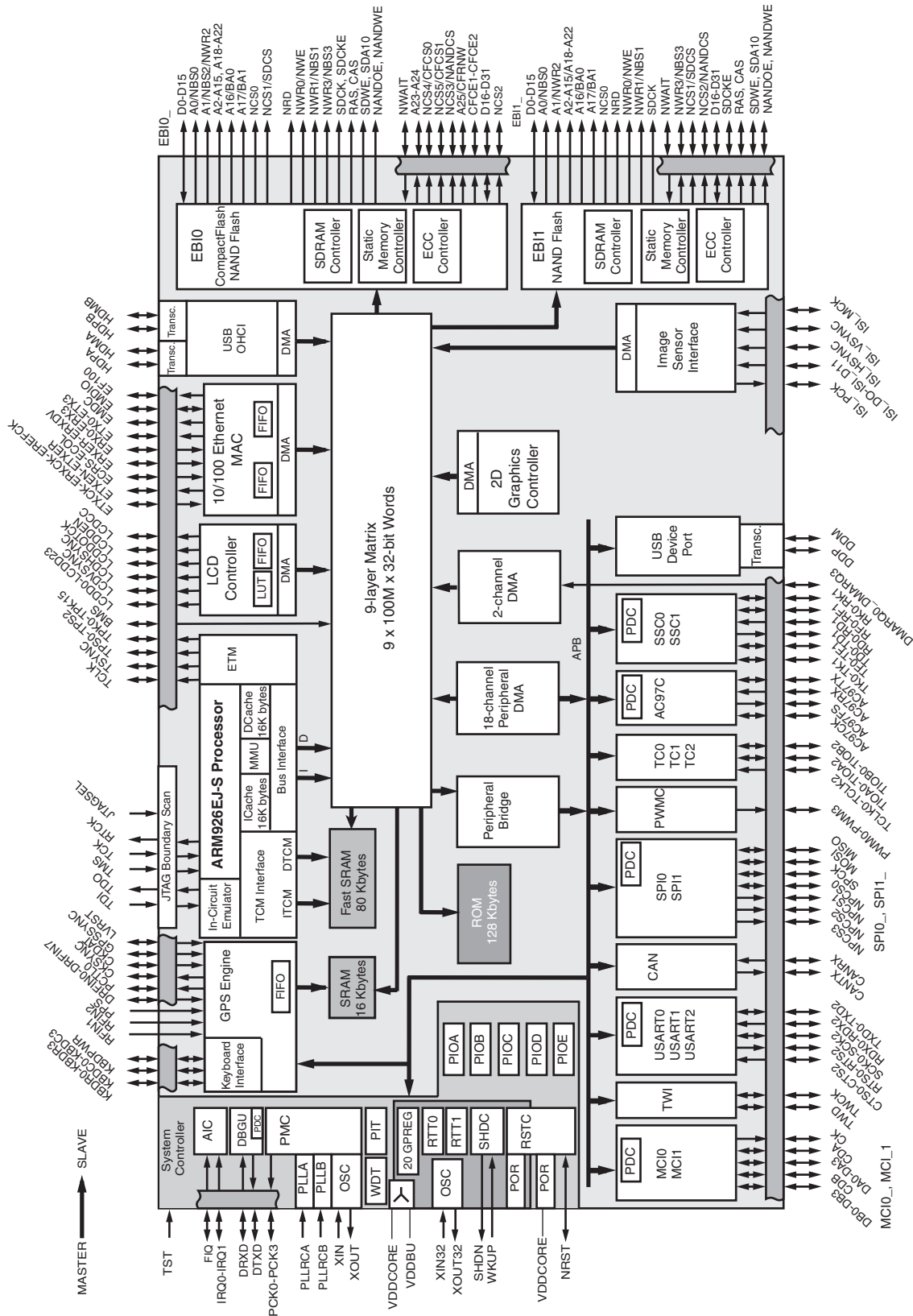
## 1. Description

The ATR0663 is based on an ARM926EJ-S processor with an integrated high-performance GPS engine and a rich peripheral set to provide a system level solution that minimizes space, power, and number of additional components required for the implementation of GPS-enabled products. The device is supplied in a 15 mm × 15 mm 324-pin TFBGA package. The GPS firmware is included in the BSP (Board Support Package) for Windows CE®.

The ATR0663 embeds an LCD controller strengthened by a 2D graphics accelerator, AC97 audio controller, a 20-channel DMA controller, and an image sensor interface. It also integrates several standard peripherals such as USB 2.0 full speed double host and device, USART, SPI, TWI, timer counters, PWM generators, multimedia card interface, and a CAN Controller. The ATR0663 architecture employs a 9-layer bus matrix that allows a maximum internal bandwidth of nine 32-bit busses. It also features two independent external memory busses, EB10 and EB11, capable of interfacing with a wide range of memory devices. The two external busses prevent bottlenecks and guarantee maximum performance.

In support of the ATR0663, the companion ATR0603 RF receiver maximizes the performance of the GPS engine while combining low cost and very low power consumption. In addition the ATR0610, a fully integrated low noise amplifier, copes with challenging reception environments and enables cost-sensitive passive antenna designs.

Figure 1-1. Block Diagram



## 2. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Min.	Typ.	Max.	Unit
Operating temperature (industrial)	-40		+85	°C
Storage temperature	-60		+150	°C
Voltage on input pins with respect to ground	-0.3		+5.5	V
Maximum operating voltage (VDDCORE and VDDBU)		1.32		V
Maximum operating voltage (VDDOSC, VDDPL, VDDIOMx and VDDIOPx)		3.6		V
Total DC output current on all I/O lines		500		mA

## 3. Electrical Characteristics

The following characteristics are applicable to the operating temperature range.  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise specified and are certified for a junction temperature up to  $T_J = 100^{\circ}\text{C}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
DC supply core		$V_{VDDCORE}$	1.08		1.32	V
DC supply backup		$V_{VDDBU}$	1.08		1.32	V
DC supply oscillator		$V_{VDDOSC}$	2.7		3.6	V
DC supply PLL		$V_{VDDPLL}$	2.7		3.6	V
DC supply memory 0 I/Os	Selectable by software in bus matrix	$V_{VDDIOM0}$	1.65/2.7		1.95/3.6	V
DC supply memory 1 I/Os	Selectable by software in bus matrix	$V_{VDDIOM1}$	1.65/2.7		1.95/3.6	V
DC supply peripheral 0 I/Os		$V_{VDDIOP0}$	3.0		3.6	V
DC supply peripheral 1 I/Os		$V_{VDDIOP1}$	1.65		3.6	V
Input low-level voltage		$V_{IL}$	-0.3		+0.8	V
Input high-level voltage	$V_{VDDIO} = V_{DDIOM}$ or $V_{DDIOP}$	$V_{IH}$	2		$V_{VDDIO} + 0.3$	V
Output low-level voltage		$V_{OL}$			0.4	V
Output high-level voltage	$V_{VDDIO} = V_{DDIOM}$ or $V_{DDIOP}$	$V_{OH}$	$V_{VDDIO} - 0.4$			V
Pull-up resistance	PA0-PA31, PB0-PB30, PC0-PC31, PD0-PD31, PE0-PE19	$R_{PULLUP}$	70	100	175	k $\Omega$
Output current	PA0-PA31, PB0-PB30, PC0-PC31, PD0-PD31, PE0-PE19	$I_O$			8	mA

### 3. Electrical Characteristics (Continued)

The following characteristics are applicable to the operating temperature range.  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise specified and are certified for a junction temperature up to  $T_J = 100^{\circ}\text{C}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Static current	On $V_{\text{DDCORE}} = 1.2\text{V}$ , MICK = 0 Hz, excluding POR All inputs driven TMS, TDI, TCK, NRST = 1 $T_A = 25^{\circ}\text{C}$	$I_{\text{sc}}$	TBD		TBD	$\mu\text{A}$
	On $V_{\text{DDCORE}} = 1.2\text{V}$ , MICK = 0 Hz, excluding POR All inputs driven TMS, TDI, TCK, NRST = 1 $T_A = 85^{\circ}\text{C}$		TBD		TBD	
	On $V_{\text{DDDBU}} = 1.2\text{V}$ , Logic cells consumption, excluding POR All inputs driven WKUP = 0 $T_A = 25^{\circ}\text{C}$		TBD		TBD	$\mu\text{A}$
	On $V_{\text{DDDBU}} = 1.2\text{V}$ , Logic cells consumption, excluding POR All inputs driven WKUP = 0 $T_A = 85^{\circ}\text{C}$		TBD		TBD	

### 4. GPS Performance

Table 4-1. GPS Performance Parameters

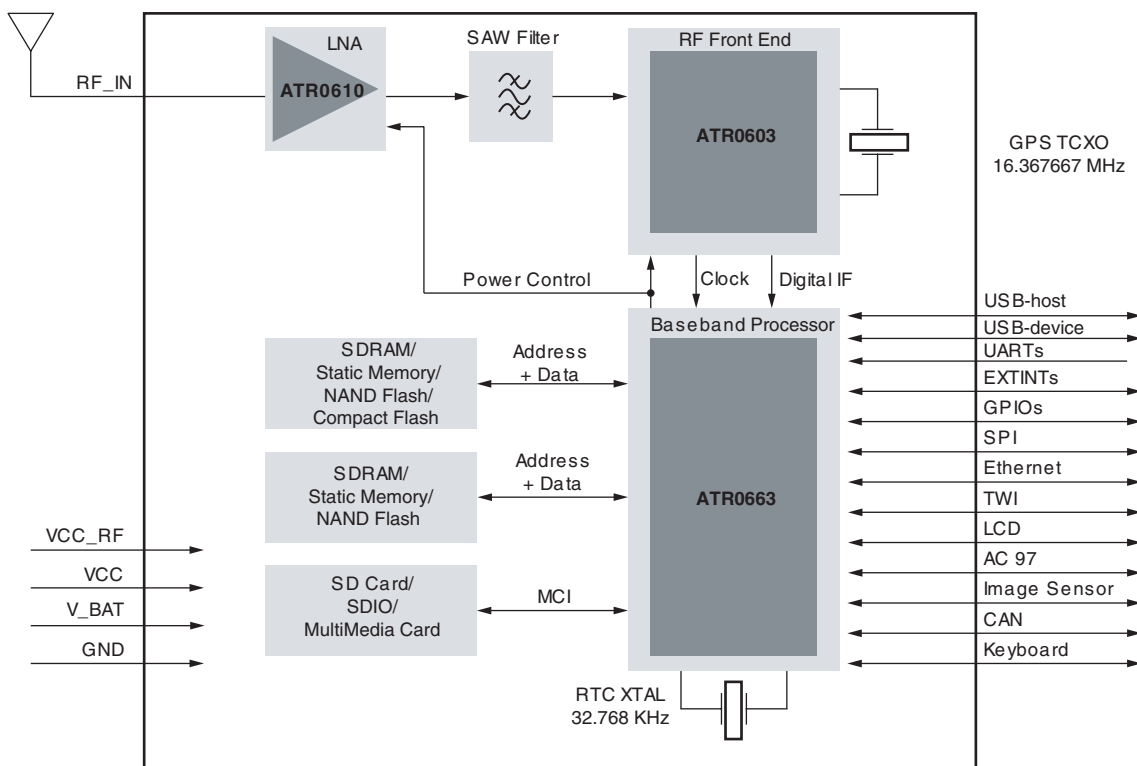
Characteristic	Test Conditions	Value
Position accuracy	Autonomous (without corrections) <sup>(4)</sup>	< 5.0m CEP (95%)
	With WAAS/EGNOS/MSAS corrections <sup>(4)</sup>	2.5m CEP (95%)
Acquisition time	Typical acquisition time <sup>(1, 2, 3, 4)</sup>	Hot start < 2 seconds Warm start < 33 seconds Cold start < 35 seconds, -144 dBm
	Typical reacquisition time <sup>(5)</sup>	< 2 seconds
Dynamics	Sensitivity	-148 dBm (acquisition) -159 dBm (tracking)
	Maximum velocity	425 m/s (951 mph)
	Altitude	-500m to +17,500m (-1600 to 57,400 ft)
	Data output rate	1 Hz
Communication	Standard NMEA-0183 V2.2 output messages	

- Notes:
1. Cold – No time/position/ephemeris
  2. Warm – Estimate of time and/or position, collecting ephemeris
  3. Hot – Up-to-date time/position/ephemeris
  4. Open sky, minimal multipath
  5. Open sky, minimal multipath, < 100s blockage of all satellites in view



## 5. Typical Architecture

Figure 5-1. Typical Chipset Architecture







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## Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

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