## Features

- **Highly Integrated DAB Front-end Solution Covering Band III Reception**
- **Convenient Internal Clock Generation, Single Reference Clock**
- **Fractional PLL for VHF**
- **Fully Integrated VCO**
- **High-precision Digitally Tunable Reference Oscillator**
- **Integrated High-performance LNA**
- **Very Flexible Programming of the AGC**
- **Automatically Aligned External Filter Tuning**
- **Simple Three-wire Digital Control Interface for Easy Handling**
- **Single Low Voltage (3.3V) Supply Operation**
- **Low Current Consumption Due to Several Power-down Options**
- **Small SMD Package (QFN 7 mm × 7 mm)**

## Applications

- **Commercial DAB Receivers**
- **DAB Receiver Solutions for Car Radio Applications**
- **Portable DAB Solutions**

broadcast radio

## 1. Description

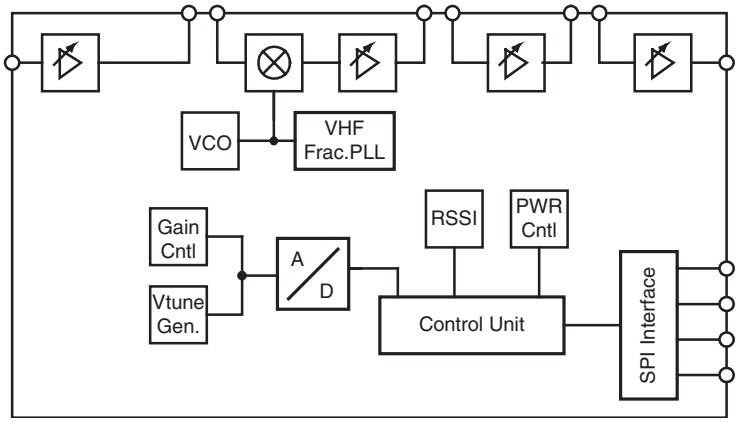
The ATR2733 is a front-end monolithic integrated circuit, manufactured using Atmel's silicon-germanium BiCMOS process (SiGMOS).

The ATR2733 carries out all functions of RF and IF processing, as well as the clock-signal generation for these functions. Therefore, there is an integrated fractional PLL, which, equivalent to most of the other functions, can be controlled via an external digital bus. The RF functions include LNA, down-conversion mixing, amplifying, detection, and gain control. An external SAW filter is required in the signal path after the RF functions. Additional amplifiers with detection and control functions are integrated IF functions.

The device offers several tuning support functions, and was created to simplify the design and manufacturing process. To this end, the number of external components are minimal.

The part fits perfectly to Atmel's DAB baseband processor ATR2740.

**Figure 1-1.** Block Diagram




# Integrated DAB One-chip Front End

# ATR2733

# Preliminary

**NOTE:** This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

4926AS–DAB–04/06

## 2. Pin Configuration

**Figure 2-1.** Pinning QFN48

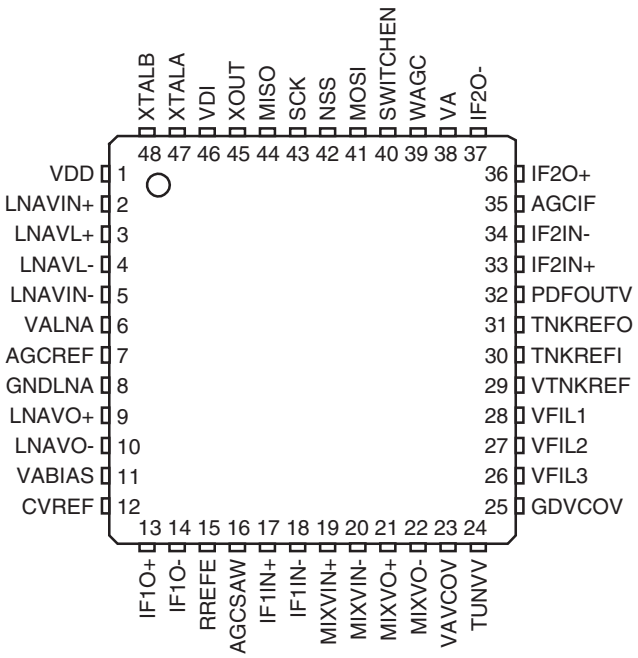



**Table 2-1.** Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1 | VDD | Supply for digital circuits |
| 2 | LNAVIN+ | Input for LNVGA for VHF (differential with pin 8) |
| 3 | LNAVL+ | Connection for "degeneration coil" (inductance) to GNDLNA for LNVGA for VHF |
| 4 | LNAVL- | Connection for "degeneration coil" (inductance) to GNDLNA for LNVGA for VHF |
| 5 | LNAVIN- | Input for LNVGA for VHF (differential with pin 5) |
| 6 | VALNA | Supply voltage for LNVGAs |
| 7 | AGCRF | Connection for capacitor for time constant of AGC of rf parts (LNVGAs, ext. PIN-diode) |
| 8 | GNDLNA | Ground for LNVGAs |
| 9 | LNAVO+ | (Differential) output of LNVGA for VHF and/or mixer for L-Bd. |
| 10 | LNAVO- | |
| 11 | VABIAS | Supply voltage for (internal) voltage and current bias reference circuits |
| 12 | CVREF | Connection for capacitor for filtering internal voltage/current reference circuits (capacitor to VABIAS) |
| 13 | IF1O+ | (Differential) output of IFVGA1 |
| 14 | IF1O- | |
| 15 | RREFE | Connection for resistor for current reference (resistor to ground) |
| 16 | AGCSAW | Connection for capacitor for time constant of AGC of mixer for VHF |
| 17 | IF1IN+ | (Differential) input of 1st IFVGA |
| 18 | IF1IN- | |

**Table 2-1.** Pin Description (Continued)



| Pin | Symbol | Function |
|---|---|---|
| 19 | MixVIN+ | (Differential) input of mixer for VHF |
| 20 | MixVIN- | |
| 21 | MixVO+ | (Differential) output of mixer for VHF |
| 22 | MixVO- | |
| 23 | VAVCOV | Supply voltage (VCO for VHF) |
| 24 | TUNVV | Tuning voltage for integrated VCO for VHF (connected to PLL loop filter) |
| 25 | GDVCOV | Ground (VCO for VHF) |
| 26 | VFIL3 | Voltage outputs for frequency tuning of filters for VHF: antenna filter, pre-selection filter |
| 27 | VFIL2 | |
| 28 | VFIL1 | |
| 29 | VTNKREF | Output voltage for tuning the "reference tank" (-varactor) |
| 30 | TNKREFI | Connection for "reference-tank" for generating the tuning voltages for the external VHF filters (-varactors) |
| 31 | TNKREFO | |
| 32 | PFDOUTV | Output of phase comparator for VCO for VHF (connected to PLL loop-filter) |
| 33 | IF2IN+ | (Differential) input of 2nd. IFVGA |
| 34 | IF2IN- | |
| 35 | AGCIF | Connection for capacitor for time constant of AGC of IF VGAs |
| 36 | IF2O+ | (Differential) Output of 2nd. IFVGA |
| 37 | IF2O- | |
| 38 | VA | Supply voltage |
| 39 | WAGC | "window AGC" - all AGCs "frozen" - currents to capacitors switched off - necessary during "Null Symbol" or also during unused symbols left out and powered down using "SWITCHEN" input |
| 40 | SWITCHEN | Input for selection between the two "enable" registers - fast change between reduced, "low current" mode and normal reception mode - current saving capability |
| 41 | MOSI | Inputs and outputs of serial bus (see serial bus protocol) |
| 42 | NSS | |
| 43 | SCK | |
| 44 | MISO | |
| 45 | XOUT | Crystal oscillator clock output to baseband<br>if used: ac-couple to baseband (single VCXO-concept)<br>if not used: short-circuit to GND |
| 46 | VDI | Supply voltage from baseband (1.65V ... 3.6V) for adaptation of interface to baseband |
| 47 | XTALA | Connection for crystal for reference clock |
| 48 | XTALB | |
| Paddle | GND | Ground |

# 3. Functional Description

The ATR2733 front-end IC was developed as a tuner IC for DAB reception. It was designed for operation in VHF BIII (174 MHz to 240 MHz). The front end contains gain-controlled LNAs and a VHF-band mixer with a fractional PLL. The IF path contains three gain-controlled amplifiers. The front-end IC allows the use of automatic tuning, which contains an adjustable input filter for VHF BIII and an adjustable preselection filter for VHF reception.

The high dynamic range of the RF inputs, the use of gain-controlled amplifiers and gain-controlled mixers in the RF and IF path (VHF band) offer the possibility of handling even strong RF input signals.

The RF and IF parts include AGC functional blocks, which are needed for proper operation. The thresholds are programmable via a simple serial bus.

The SPI bus is used to adjust and control all functional blocks.

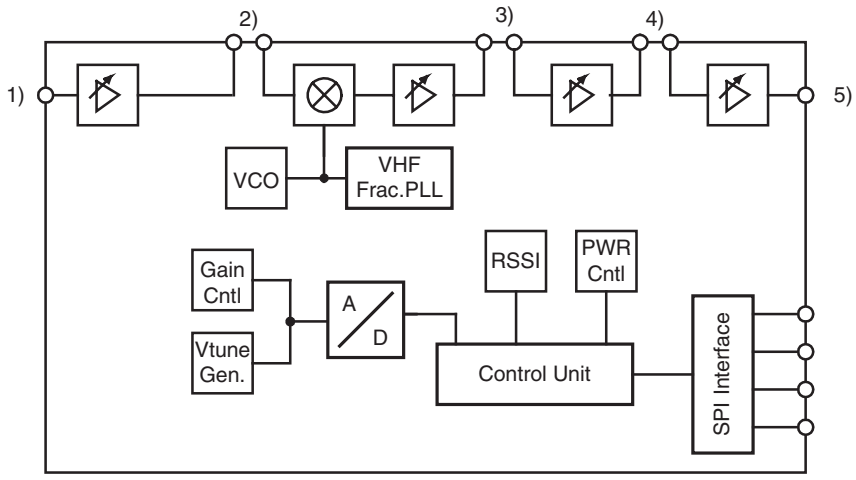
The following sections briefly describe the major functions and features.

## 3.1 Main Functions

The following description gives a short overview of the general signal flow using the ATR2733 front-end IC for reception of DAB signals. Numbers in the text refer to the numbers in Figure 3-1 on page 4:

A DAB signal in the antenna. the signal is band-pass filtered using a filter with low insertion loss. The internal variable gain LNA for Band III (3)) amplifies the signal. The signal leaves the IC at point (4), followed by an external preselection filter. This filter has an automatic tuner adjustment; that is, the tuning-voltage-generation block adjusts the pass band of this filter to the desired frequency. After passing this filter, the RF signal is down-mixed to a fixed IF frequency of 38.912 MHz. The IF signal is amplified and passed to a SAW filter (5). The first IF variable-gain amplifier is followed by an IF filter at position (6). This filter is used as an anti-alias-filter. Finally, the DAB signal is amplified using the 2nd IF amplifier. The signal leaves the front-end IC at (7), giving the signal to the DAB baseband IC.

**Figure 3-1.** Functional Block Diagram with Labelled Inputs and Outputs



## 3.2 AGC in General



There are three AGCs in the ATR2733, one for the RF signals (3), one for the very beginning of the IF path (mainly VHF mixer), and one for the IF amplifiers (5) down to the output to baseband (7).

In these AGCs, the output signals of the relevant blocks are amplified, weakly band-pass filtered, rectified, and, finally, low-pass filtered. The voltage derived in this power-measurement process is compared to a voltage threshold which can be digitally controlled by several bits, independently of each other. The setting is done via the control bus. Depending on the result of this comparison, charge pumps feed a positive or negative current in order to charge or discharge external capacitors. The voltage of these external capacitors is used to control the gains of practically all blocks in the signal path.

By means of the control bus, the current of the AGC charge pump can be selected as specified in the following table:

**Table 3-1.** Selection of Time Constant Factor

| MSB | | LSB | Time Constant Factor |
|---|---|---|---|
| 0 | 0 | 0 | Infinite |
| 0 | 0 | 1 | 32 |
| 0 | 1 | 0 | 16 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0.2 |

The input pin WAGC, set to logical 1, always sets all AGCs to time constant *Infinite* (meaning there is practically no current to the AGC capacitors), regardless of the actual status of the bus settings.

## 3.3 Device Support Functions

The ATR2733 has incorporated some very useful additional functions for handling the device and optimizing the performance. First of all, a very precise clocking engine is incorporated. To optimize the performance of this front end, a tuning support for alignment of the filters is featured by this part too, similar to Atmel's other radio front ends.

## 3.4 Tuning Support Functions

The ATR2733 includes three operational amplifiers, and three programmable digital-analog converters (DACs). These outputs are used for automatic filter alignment of the tunable VHF antenna filter and the preselection filter. DACs are incorporated in the ATR2733 for this tuning-support function.

For more details about the usage of the filter-tuning function contact your local Atmel sales office and ask for the application note covering this feature.

## 3.5 DAC Usage

There are two DAC modes: pure DAC and Loop/Offset mode. In the pure DAC mode the DAC sets a definite value. In the Loop/Offset mode the filter tuning voltage is derived from a reference tank circuit (inductor plus varicap). An offset value can be added to this voltage. This Loop/Offset mode is the most useful mode and recommended for most applications. Temperature compensation is also included in this mode.

## 3.6 RSSI Measurement

The ATR2733 offers the option of getting information about the field strength. This is not an absolute real-field-strength value, but an indication of in which range the field strength is available. This information can be obtained from the 8 low bits of the status register.

## 3.7 Clocking Engine in General

The ATR2733 incorporates a convenient and flexible clocking engine. This includes VCOs and PLLs for both bands, as well as a reference oscillator which can be precisely tuned using the SPI interface. Together, this results in low external component count, but offers high flexibility and convenience.

## 3.8 PLL Part

The Band III PLL, perform phase lock of the LO signal to an on-chip crystal reference oscillator. The Band III PLL incorporates a fractional part. This technique allows operation with an increased bandwidth of the PLL, which results in improved phase noise.

## 3.9 Fast Fractional PLL

The frequency of the VHF VCO is locked to a reference frequency by an on-chip fractional-N PLL circuit which guarantees superior phase-noise performance. The reference frequencies for the PLL block are generated by an on-chip oscillator.

The VCOs are fully integrated, which simplifies the design of the device and reduces the bill of materials of the application.

The down-converting to an IF frequency of 38.912 MHz for VHF signal is done by an additional on-chip VCO using an internal fractional-N PLL.

Due to the digital tuning option of the reference frequency, the ATR2733 is able to support the single reference clock design if the baseband can support such a feature (as the ATR2740 does).

## 3.10 Reference Oscillator

An on-chip crystal oscillator generates the reference signal which is fed to the reference divider. By applying a crystal to the pins XTALA and XTALB, this oscillator generates a highly stable reference signal.

Furthermore, the frequency of this reference oscillator can be digitally tuned via the SPI bus bits XOTi (i = 11, ..., 0) with a 12-bit step size.

## 3.11 Reference Divider

Starting from a minimum value, the scaling factor of the 6-bit reference divider is arbitrarily programmable by means of the SPI bus bits Ri (i = 5, ..., 0).

A programmable divider (dividing by 8 to 128) then outputs 64 kHz, which is a useful reference frequency for the VHF PLL.

Together with the fractional-N PLL, a step size of 16 kHz for the frequency setting of the VHF LO is ensured.

## 3.12 Main Divider

The main divider consists of a fully programmable 13-bit divider which defines a division ratio N. The applied division ratio is either N or N + 1, as specified by a special control unit. On average, the scaling factors SF = N + k / 4 can be selected where k = 0, 1, 2, or 3.

## 3.13 Phase Comparator and Charge Pump

The tri-state phase detector cause the charge pump to source or sink currents at the output pins PFDOUTV (for VHF) depending on the phase relation of its input signals, which are provided by the reference and the main dividers, respectively.

Internal lock detectors check if the phase difference of the phase detector's input signals are smaller than approximately 5 ns in 16 subsequent comparisons (in the case of VHF). These numbers ensure a less than 4-kHz offset from the final frequency when lock-detect bits VHF-PLLLD (SPI bus, output MISO) are set.

## 3.14 SSPI Bus



The bus interface can be adapted to the signal voltage as a result of the supply voltage of the external baseband processing unit connected to the bus. This is done with the help of a sensing pin, VDI, which checks the supply voltage of the processor. The interface adapts itself to any voltage between 1.65V and 3.5V.

### 3.14.1 Programming via SPI

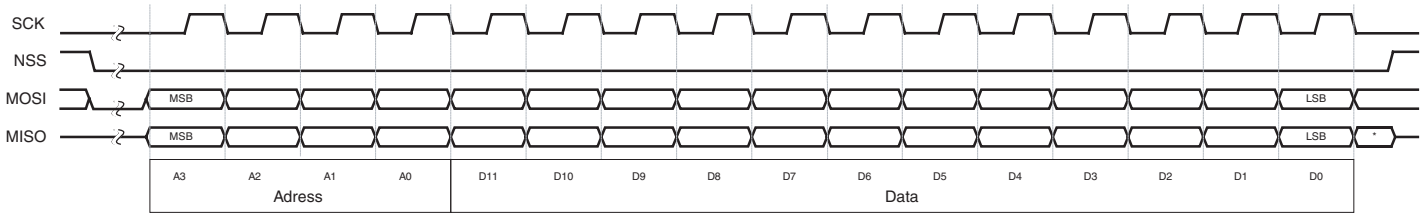
Some things need to be taken into account when programming the ATR2733 via the SPI interface: the data packet needs to be properly configured to write into the 14 different registers.

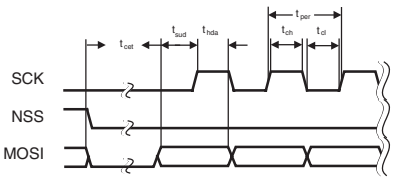
In principle, there are 16 registers. Fourteen of them are used to control the ATR2733. The two others, registers 15 and 16, are Test Mode Registers. All these registers need to be reset by writing “0” to every bit of each register one time, before starting the configuration of the ATR2733.

There are 4 address bits (bit 12 is address bit 0; bit 15 is address bit 3) which are used to select the correct register. These are followed by 12 data bits (LSB is bit 0; MSB is bit 11). There is a definite transmit order which needs to be considered: the MSB must be transmitted first (bit 15, address bit 3), and LSB (data bit 0) last.

Note: Unused and test mode register bits may not be documented in the datasheet and have to be set to “0” in customer applications. Information about the status of the device is available by reading one word (16 bits) out of the part.

**Figure 3-2.** Timing Diagram of the SPI Interface (16 Bits per Transfer)




$t_{cet}$: Clock enable time
$t_{sud}$: Data setup time
$t_{hda}$: Hold time of MOSI
$t_{per}$: Clock period
$t_{ch}$: Clock high time
$t_{cl}$: Clock low time

Note: It is absolutely necessary to set the NSS signal back to high after every SPI access.

## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.0 | V |
| Operating case temperature | $T_c$ | –40 to +100 | °C |
| Storage temperature | $T_{stg}$ | –40 to +150 | °C |

Notes: 1. The part may not survive all maximums applied simultaneously!

## 5. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction, case | $R_{thJC}$ | 35 | K/W |

## 6. Operating Range

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 to 3.5 | V |
| Ambient temperature | $T_{amb}$ | –40 to +85 | °C |

## 7. Electrical Characteristics

Test conditions (if not otherwise specified): $V_{CC}$ = +3.3V, $T_{amb}$ = +25°C, 50Ω input match

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| **1** | **Power Supply** | | | | | | | | |
| 1.1 | Supply voltage of front end ATR2733 | | | $V_{CC}$ | 3.0 | | 3.5 | | A |
| 1.2 | Supply voltage of baseband processor | | | $V_{Di}$ | 1.65 | | $V_{CC}$ | V | A |
| 1.3 | Leakage current, all off | | | $I_{leak}$ | | 3 | 25 | µA | A |
| **2** | **Power Control** | | | | | | | | |
| 2.1 | Power on/off delay | | | | | 1 | | µs | C |
| 2.2 | Power off/on delay | | | | | 5 | | ms | C |
| 2.3 | Supply current | Reception only VHF | | | | 150 | | mA | A |
| 2.5 | Power-off tuning voltage generation | Tuning generation not active | | | | 140 | | mA | B |
| 2.6 | Average current consumption | | | | | 80 | | mA | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 7. Electrical Characteristics (Continued)

Test conditions (if not otherwise specified): $V_{CC}$ = +3.3V, $T_{amb}$ = +25°C, 50Ω input match

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| **3** | **SPI Bus Interface** | | | | | | | | |
| 3.1 | BUS voltage high | | | $V_{BUSH}$ | $V_{Di}$ – 0.36 | | $V_{Di}$ + 0.3 | V | A |
| 3.2 | BUS voltage low | | | $V_{BUSL}$ | –0.3 | | 0.25 | V | A |
| 3.3 | Clock frequency | | | 1 / $t_{per}$ | | | 5 | MHz | A |
| 3.4 | Clock high time (SCK) | | | $t_{ch}$ | 0.4 × $t_{per}$ | | | | |
| 3.5 | Clock low time (SCK) | | | $t_{cl}$ | 0.4 × $t_{per}$ | | | | |
| 3.6 | Clock enable time | | | $t_{cet}$ | 5 | | | µs | |
| 3.7 | Data set-up time | | | $t_{sud}$ | 0.4 × $t_{per}$ | | | | |
| 3.8 | Hold time MOSI | | | $t_{hda}$ | 0.4 × $t_{per}$ | | | | |
| **4** | **Reference Crystal Oscillator** | | | | | | | | |
| 4.1 | Operating frequency | | | | 16 | 24.576 | 32 | MHz | C |
| 4.2 | Tuning range | | | | 120 | 210 | | ppm | A |
| 4.3 | Reference clock output voltage | Sine wave output | | | | 0.5 | | $V_{pp}$ | A |
| **5** | **VHF Fractional PLL** | | | | | | | | |
| 5.1 | LO frequency | | | | 200 | | 290 | MHz | A |
| **6** | **IF Interface** | | | | | | | | |
| 6.1 | IF frequency range | | | | 30 | 38.91 | 50 | MHz | D |
| 6.2 | Baseband output impedance | | | | | 56 | 100 | Ω | D |
| **7** | **VHF Band Operation** | | | | | | | | |
| 7.1 | Frequency range | | | $f_{Rfin}$ | 174 | | 240 | MHz | C |
| 7.4 | Sensitivity | 8 dB SNR at IF output to baseband, measured with sample application | | | | –98 | | dBm | C |
| 7.5 | Maximum input power level | | | | | –5 | | dBm | C |
| 7.6 | LNA input frequency range | | | | 170 | | 240 | MHz | C |
| 7.7 | LNA gain control range | | | | | 20 | | dB | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

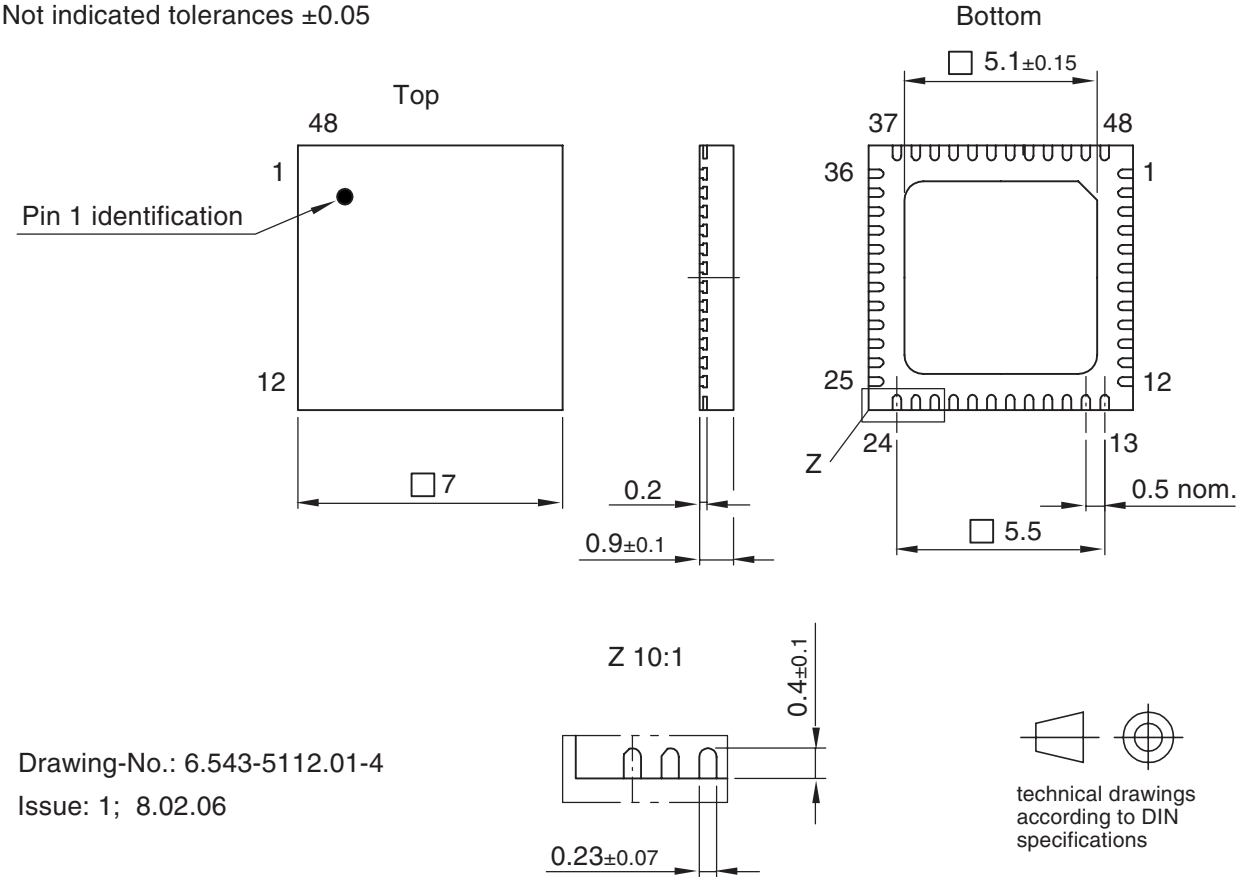
## 8. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| ATR2733-PLQW | QFN48 | 7 mm × 7 mm, 0.5 mm pitch, lead-free |
| ATR2733-PLPW | QFN48 | 7 mm × 7 mm, 0.5 mm pitch, lead-free |

## 9. Package Information

Package: VQFN_7 x 7_48L
Exposed pad 5.1 x 5.1
Dimensions in mm

Not indicated tolerances ±0.05




Drawing-No.: 6.543-5112.01-4
Issue: 1; 8.02.06

technical drawings
according to DIN
specifications

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