ATS250X Datasheet

Latest Version: 1.0

Aug 03, 2009

1 Declaration

Circuit diagrams and other information relating to products of Actions Semiconductor Company, Ltd. ("Actions") are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction is not necessarily given. Although the information has been examined and is believed to be accurate, Actions makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and disclaims any responsibility for inaccuracies. Information in this document is provided solely to enable use of Actions' products. The information presented in this document does not form part of any quotation or contract of sale. Actions assumes no liability whatsoever, including infringement of any patent or copyright, for sale and use of Actions' products, except as expressed in Actions' Terms and Conditions of Sale for. All sales of any Actions products are conditional on your agreement of the terms and conditions of recently dated version of Actions' Terms and Conditions of Sale agreement Dated before the date of your order.

This information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights, copyright, trademark rights, rights in trade secrets and/or know how, or any other intellectual property rights of Actions or others, however denominated, whether by express or implied representation, by estoppel, or otherwise.

Information Documented here relates solely to Actions products described herein supersedes, as of the release date of this publication, all previously published data and specifications relating to such products provided by Actions or by any other person purporting to distribute such information. Actions reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your Actions sales representative to obtain the latest specifications before placing your product order. Actions product may contain design defects or errors known as anomalies or errata which may cause the products functions to deviate from published specifications. Anomaly or "errata" sheets relating to currently characterized anomalies or errata are available upon request. Designers must not rely on the absence or characteristics of any features or instructions of Actions' products marked "reserved" or "undefined." Actions reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Actions' products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an

Officer of Actions and further testing and/or modification will be fully at the risk of the customer.

Copies of this document and/or other Actions product literature, as well as the Terms and Conditions of Sale Agreement, may be obtained by visiting Actions' website at http://www.actions-semi.com/ or from an authorized Actions representative. The word "ACTIONS", the Actions' LOGO, whether used separately and/or in combination, and the phase "ATS250X", are trademarks of Actions Semiconductor Company, Ltd., Names and brands of other companies and their products that may from time to time descriptively appear in this product data sheet are the trademarks of their respective holders; no affiliation, authorization, or endorsement by such persons is claimed or implied except as may be expressly stated therein.

ACTIONS DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE.

IN NO EVENT SHALL ACTIONS BE RELIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF ACTIONS OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER ACTIONS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES OR NOT.

Additional Support

Additional product and company information can be obtained by visiting the Actions website at: http://www.actions-semi.com

2 Contents

1 Declaration 2
2 Contents 4
3 Revision History 10
4 Introduction 11
5 Pin Description 13
5.1 ATS2501 13
5.1.1 ATS2501 Pin Assignment 13
5.1.2 ATS2501 Pin Definition 13
6 ATS250X Block Diagram 19
7 Memory Mapping 19
7.1 Memory Map 19
7.1.1 Registers Description 20
8 System Control Module 21
8.1 Description 21
8.2 Bus Controller 21
8.2.1 MCU Clock Control Register 21
8.2.2 DMA1/DMA2 Clock Division Register 22
8.2.3 Chip Enable Selection Register 23
8.2.4 MCU-A15 Control Register 24
8.2.5 General Random Access IO Register 25
8.3 DMA Channel 1 25
8.3.1 DMA1 Source Address 0 Register 25
8.3.2 DMA1 Source Address 1 Register 25
8.3.3 DMA1 Source Address 3 Register 25
8.3.4 DMA1 SRC Address Register 26
8.3.5 DMA1 Destination Address 0 Register 26
8.3.6 DMA1 Destination Address 1 Register 27
8.3.7 DMA1 Destination Address 3 Register 27
8.3.8 DMA1 DST Address Register 27
8.3.9 DMA1 Byte Counter Low Register 28

8.3.10 DMA1 Byte Counter High Register 28
8.3.11 DMA1 Mode Register 28
8.3.12 DMA1 Command Register 29
8.4 DMA Channel 2 30
8.4.1 DMA2 Source Address 0 Register 30
8.4.2 DMA2 Source Address 1 Register 30
8.4.3 DMA2 Source Address 3 Register 30
8.4.4 DMA2 SRC Address Register 30
8.4.5 DMA2 Destination Address 0 Register 31
8.4.6 DMA2 Destination Address 1 Register 31
8.4.7 DMA2 Destination Address 3 Register 31
8.4.8 DMA2 DST Address Register 32
8.4.9 DMA2 Byte Counter Low Register 32
8.4.10 DMA2 Byte Counter High Register 32
8.4.11 DMA2 Mode Register 33
8.4.12 DMA2 Command Register 33
8.5 CTC 34
8.5.1 CTC Prescale Register 34
8.5.2 CTC Period Low Register 35
8.5.3 CTC Period High Register 35
8.6 Interrupt Controller 35
8.6.1 DMA/CTC IRQ Status Register 35
8.6.2 Master Interrupt Status Register 36
8.6.3 Master Interrupt Enable Register 37
9 DSP 38
9.1 Description 38
10 USB2.0 OTG 39
11 I2C Interface 40
11.1 Description 40
11.2 Register Description 40
11.2.1 I2CADDR (I2C Address Register, 084h) 40
11.2.2 I2CCTL (I2C Control Register, 085h) 41
11.2.3 I2CSTA (I2C Status Register, 086h) 42
11.2.4 I2CDAT (I2C Data Register, 087h) 43
12 SPI Interface 44
12.1 Description 44

12.2 Register Description 44
12.2.1 SPICTL (SPI Control Register, A8h) 45
12.2.2 SPIIRQ (SPI IRQ Register, A9h) 46
12.2.3 SPISTA (SPI Status Register, AAh) 46
12.2.4 SPICLKDIV (SPI Clock Divide Control Register, ABh) 47
12.2.5 SPIDAT (SPI Data Register, ACh) 47
12.2.6 SPIBCL (SPI Bytes Count Low Register, ADh) 47
12.2.7 SPIBCH (SPI Bytes Count High Register, AEh) 48

13 UART Interface 49

13.1 Description 49

13.2 Register Description 49
13.2.1 BAUDRATE (UART Baud Rate Register, 079h) 50
13.2.2 UARTCTL (UART Control Register, 07Ah) 50
13.2.3 UARTFDAT (UART FIFO DATA Register, 07Bh) 51
13.2.4 UARTMS (UART Mode & FIFO Status Register, 07Dh) 52
13.2.5 UARTRQS (UART DRQ/IRQ Enable/Status Register, 07Eh) 52

14 Infrared Remote Control Interface 54

14.1 Introduction 54

14.2 Register Description 54

15 SPDIF Interface 57

15.1 Description 57

15.2 Register Description 57
15.2.1 SPDIFCTL (SPDIF Control Register, 080h) 57
15.2.2 SPDIFSTA (SPDIF Status Register, 081h) 58
15.2.3 SPDIFDAT (SPDIF FIFO DATA Register, 082h) 58
15.2.4 SPDIF Channel Status Register 59
15.2.5 SPDIFCH (SPDIF Channel Status Register, 083h) 59

16 Clock Management Unit 60

16.1 Description 60

16.2 LOSC/RTC 60
16.2.1 RTC Control Register 60
16.2.2 RTC IRQ Status Register 61
16.2.3 RTC Time HMS Low Register 61
16.2.4 RTC Time HMS High Register 61
16.2.5 RTC Time Day Register 62

16.2.6 RTC Time Year/Month Register 62
16.2.7 RTC Alarm HMS Low Register 62
16.2.8 RTC Alarm HMS High Register 63
16.2.9 LOSC Divider Low Byte Register 63
16.2.10 LOSC Divider Middle Byte Register 63
16.2.11 LOSC Divider High Byte Register 63
16.2.12 Watch Dog Register 64
16.3 HOSC/PLL 64
16.3.1 High Frequency Crystal Control Register 64
16.3.2 CK48M Control Register 65
16.3.3 MCU PLL Control Register 65
16.4 Clock Selection Unit 67
16.4.1 Module Clock Select Register 67
17 A/D D/A and Headphone Driver 67
17.1 Introduction 67
17.2 ADDA Analog Diagram 68
17.3 DAC 69
17.4 ADC 69
18 GPIO/MULTIFUNCTION 70
18.1 Description 70
18.2 Register Description 70
18.2.1 MFP Select Register 71
18.2.2 GPIO_A Output Enable Register 72
18.2.3 GPIO_A Input Enable Register 72
18.2.4 GPIO_A Data Output/Input Register 72
18.2.5 GPIO_B Output Enable Register 73
18.2.6 GPIO_B Input Enable Register 73
18.2.7 GPIO_B Data Output/Input Register 74
18.2.8 GPIO_C Output Enable Register 74
18.2.9 GPIO_C Input Enable Register 74
18.2.10 GPIO_C Data Output/Input Register 75
18.2.11 GPIO_D Output Enable Register 75
18.2.12 GPIO_D Input Enable Register 75
18.2.13 GPIO_D Data Output/Input Register 76
18.2.14 GPIO_E[4:0] Output Enable Register 76
18.2.15 GPIO_E[4:0] Input Enable Register 76

18.2.16 GPIO_E[4:0] Data Output/Input Register 77
18.2.17 GPIO_F [7:0] Output Enable Register 77
18.2.18 GPIO_F[7:0] Input Enable Register 78
18.2.19 GPIO_F[7:0] Data Output/Input Register 78
18.2.20 GPIOE0_VCCOUT Select Register 78

19 PWM 79

19.1 Introduction 79

19.2 Register Description 79

20 Power Management Unit 81

20.1 Introduction 81

20.2 Application Diagram 81

20.3 DC-DC Converters 83
20.3.1 DC-DC Output Voltage Setting 83
20.3.2 DC-DC Accurate and Maximum Output Current 83
20.3.3 DC-DC Converter Efficiency 84

20.4 Linear Regulators 85
20.4.1 Regulators Output Voltage Set 86
20.4.2 Regulators Accurate and Maximum Output Current 86

20.5 Li-Ion Cell Charger 86

20.6 A/D Converters 87
20.6.1 ADCEN Register 88
20.6.2 WCTLADC DATA Register 89
20.6.3 TEMPADC DATA Register 90
20.6.4 BATADC DATA Register 91

21 Electrical Characteristics 92

21.1 Absolute Maximum Ratings 92

21.2 Capacitance 92

21.3 DC Characteristics 92

21.4 AC Characteristics 93
21.4.1 AC Test Input Waveform 93
21.4.2 AC Test Output Measuring Points 93
21.4.3 Reset Parameter 94
21.4.4 Initialization Parameter 94
21.4.5 GPIO Interface Parameter 94

21.4.6 Ordinary ROM Parameter 95
21.4.7 External System Bus Parameter 96
21.4.8 Bus Operation 97
21.4.9 Headphone Driver Characteristics 98
22 Package Drawing 101
23 Ordering Information 102
23.1 Recommended Soldering Conditions 102
23.2 Precaution against ESD for Semiconductors 102
23.3 Handling of Unused Input Pins for CMOS 103
23.4 Status before Initialization of MOS Devices 103
24 Appendix 104
24.1 Acronym and Abbreviations 104

3 Revision History

Date	Revision	Description
2009-08-03	1.0	Initial Release

4 Introduction

ATS250X is a third generation single-chip highly-integrated digital music system solution for devices such as dedicated audio players. It includes a high performance dsp with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. ATS250X also provides an interface to SPDIF, flash memory, LED/LCD, button and switch inputs, headphones, and microphone, and FM radio input and control. It supports WMA and other digital audio standards. For devices like USB-Disk, it can act as a USB mass storage slave device to personal computer system. The Chip has low power consumption to allow long battery life and an efficient flexible on-chip DC-DC converter that allows many different battery configurations, including 1xAA, 1xAAA and Li-on. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphones. The A/D includes inputs for both Microphone and Analog Audio in to support voice recording and FM radio integration features. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio players.

Features

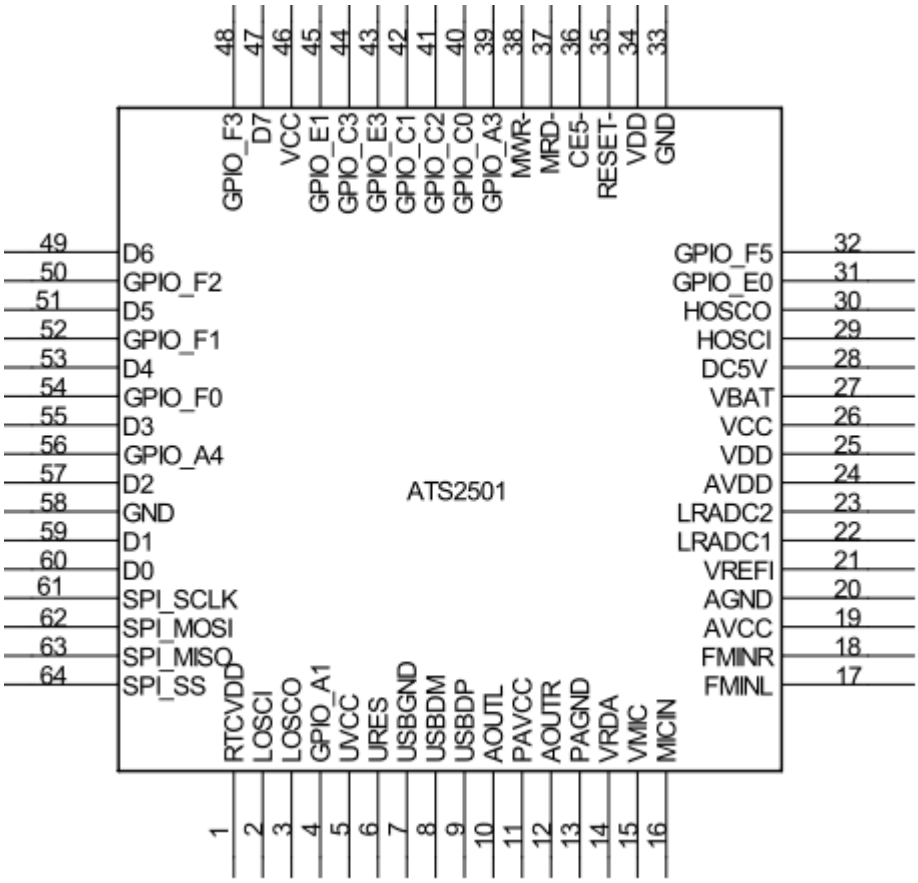
- Support WMA Decoder and Other Digital Audio Standards
- Digital Voice Recording (ADPCM)
- On-chip DSP data RAM1 6.25k*24bit, DSP data RAM2 4k*8bit and PCM RAM (8K*8bit) that can be switched to be MCU memory space.
- Integrated MCU with DSU, the instruction set is compatible with Z80
- Internal ZRAM1 ((16K-64)*8bits), ZRAM2(1k*8bit), ZRAM3 ((8k+2k+192)*8bits) accessed by MCU
- Internal BROM build in Boot up and USB Upgrade firmware
- Internal SRAM access time<7ns, MROM access time<16ns
- External up to 4(pcs)x 32M~4G bytes Nand type Flash accessed by MCU or DMA
- External Smart Media Card
- Support following memory card interface
  .Multi Media Card Specification Version 4.2 (1/4/8 bit mode)
  .Secure Digital Card Specification Version 2.0(1/4-bit mode)
  .Memory Stick Version 1.43(1/4-bit mode)
  .Memory Stick Pro Version 1.02(1/4-bit mode)
  .Memory Stick Pro-HG Version 1.01(1/4/8-bit mode)

- Support 24MHz OSC with on-chip PLL for MCU and about 32KHz RC oscillator
- 2-channel DMA,1-channel CTC and interrupt controller for MCU
- Energy saving with dynamic power management, supporting dry and lithium battery.
- Udisk Speed: for SLC Flash, read Speed up to 16MB/s; Write speed up to 6MB/s; For MLC Flash, Read Speed up to 16MB/s; Write Speed up to 4.5MB/s
- Build in Stereo 20-bit Sigma-Delta D/A
- Enough GPIOs For all applications
- Support I^2C/SPI/UART/IRC/SPDIF interface
- Support external 8080 Series LCM driver interface
- Support FM Radio input and 41 levels volume control
- Support Stereo 21-bit Sigma-Delta A/D for Microphone/FM Input, sample rate at 8/12/16/22/24/32/48KHz
- MCU run at 24MHz(typ),F/W can program from DC up to 48MHz transparently
- D/A+PA SNR :without A weight>91dB
- A/D SNR >90dB ,support Difference/2-channle Microphone
- Headphone driver output 2x20Mw @16ohm
- Standby Leakage Current: VCC:50uA@3.0V(MAX), VDD: 350uA@1.6V(MAX)
- Low Power Consumption : <40mW@1.6V at typical Audio decoder solution
- Package at LQFP-64(7x7mm)

5 Pin Description

5.1 ATS2501

5.1.1 ATS2501 Pin Assignment



5.1.2 ATS2501 Pin Definition

Pin No.	Pin Name	I/O Type	Driver	Reset Default	PU/PD	Description
1	RTCVDD	PWR	/	/		Digital Power pin of int. RTC
2	LOSCI	AI	/	/		Low frequency crystal OSC input
3	LOSCO	AO	/	/		Low frequency crystal OSC output
4	ICERST-	I	10mA	H	PU200K	DSU reset (active low)
	GPIOA1	BI		/		Bit1 of General purpose I/O port A
5	UVCC	PWR	/	/		Power supply for USB
6	URES	AO	/	/		USB precision Resistor
7	USBGND	PWR	/	/		USB ground
8	USBDM	A	/	H		USB data minus
9	USBDP	A	/	H		USB data plus
10	AOUTL	AO	/	/		Int. PA left channel analog output
11	PAVCC	PWR	/	/		Power supply for power amplifier
12	AOUTR	AO	/	/		Int. PA right channel analog output
13	PAGND	PWR	/	/		Power amplifier ground
14	VRDA	AO	/	/		Bypass capacitor connect pin for Int. D/A Reference voltage
15	MICIN	AI	/	/		Microphone pre-amplifier input
16	VMIC	PWR	/	/		Power supply for Microphone
17	FMINL	AI	/	/		Left channel of FM line input
18	FMINR	AI	/	/		Right channel of FM line input
19	AVCC	PWR	/	/		power supply of Analog
20	AGND	PWR	/	/		Analog ground
21	VREFI	AI	/	/		Voltage reference input
22	LRADC1	AI	/	/		Low resolution A/D input 1

23	LRADC2	AI	/	/		Low resolution A/D input 2
24	AVDD	PWR	/	/		Analog Core power pin
25	VDD	PWR	/	/		Digital Core power
26	VCC	PWR	/	/		Digital power pin
27	BAT	I	/	/	PD200k	Battery Voltage input.
28	DC5V	AI	/	/		5.0V Voltage
29	HOSCI	AI	/	/		High frequency crystal OSC input
30	HOSCO	AO	/	/		High frequency crystal OSC output
31	GPIO_E0	BI	6mA	Z		Bit0 of General purpose I/O port E
	MS_BS	O		/	PD50k	MS Card Command Interface
	VCCOUT	PWR		/		3.3V VCCOUT
32	GPIO_F5	BI	6mA	Z		Bit5 of General purpose I/O port F
	MMC_D5	BI		/	PU50k	Bit5of MMC/SD Card data bus
	MS_D1	BI		/	PD50k	Bit1 of MS Card data bus
33	GND	PWR	/	/		Ground
34	VDD	PWR	/	/		Digital Core power
35	RESET-	I	USCU	H	PD200k	System reset input (active low)
36	CE5-	O	2mA	H		Ext. memory chip enable 5
	GPIO_A7	BI		/		Bit7 of General purpose I/O port A
	SIRQ-	I		/	PD200k or PU200k	System external Interrupt Request
37	MRD-	O	2mA	H		Ext. memory read strobe
	GPIO_B2	BI		/		Bit2 of General purpose I/O port B
	MWR-	O	2mA	H		Ext. memory write strobe

38	GPIO_B3	BI		/		Bit3 of General purpose I/O port B
39	GPIO_A3	BI	2mA	/		Bit3 of General purpose I/O port A
	ICECK	I		Z		Clock input of DSU
40	GPIO_C0	BI	2mA	Z		Bit0 of General purpose I/O port C
	I2C_SCL	O		/		I2C serial clock
	ICEDI	I		/		Data input of DSU
41	GPIO_C2	O	2mA	Z		Bit2 of General purpose I/O port C
	UART_RX	I		/		UART RX
	SPDIF_RX	I		/		SPDIF RX
42	GPIO_C1	BI	2mA	Z		Bit1 of General purpose I/O port C
	I2C_SDA	O		/		I2C Serial data
	ICEDO	O		/		Data output of DSU
43	GPIO_E3	BI	6mA	Z		Bit3 of General purpose I/O port E
	MMC_CLK1	O		/		Clock1 for MMC/SD Card
	MS_CLK	O		/	PD50k	Clock for MS Card
44	GPIO_C3	BI	2mA	Z		Bit3 of General purpose I/O port C
	UART_TX	O		/		UART TX
	SPDIF_TX	O		/		SPDIF TX
45	GPIO_E1	BI	6mA	Z		Bit1 of General purpose I/O port E
	MMC_CMD	O		/		CMD of SD/MMC card interface
	MS_BS	O		/	PD50k	BS of MS card interface
46	VCC	PWR	/	/		Digital power pin
47	D7	BI	2mA	L		Bit7 of ext. memory data bus
	GPIO_D7	BI		/		Bit7 of General purpose I/O port D
48	GPIO_F3	BI	6mA	Z		Bit3 of General purpose I/O

						port F
	MMC_D3	BI		/	PU50k	Bit3 of MMC/SD Card data bus
	MS_D3	BI		/	PD50k	Bit3 of MS Card data bus
49	D6	BI	2mA	L		Bit6 of ext. memory data bus
	GPIO_D6	BI		/		Bit6 of General purpose I/O port D
50	GPIO_F2	BI	6mA	Z		Bit2 of General purpose I/O port F
	MMC_D2	BI		/	PU50k	Bit2 of MMC/SD Card data bus
	MS_D2	BI		/	PD50k	Bit2 of MS Card data bus
51	D5	BI	2mA	L		Bit5 of ext. memory data bus
	GPIO_D5	BI		/		Bit5 of General purpose I/O port D
52	GPIO_F1	BI	6mA	Z		Bit1 of General purpose I/O port F
	MMC_D1	BI		/	PU50k	Bit1 of MMC/SD Card data bus
	MS_D1	BI		/	PD50k	Bit1 of MS Card data bus
53	D4	BI	2mA	L		Bit4 of ext. memory data bus
	GPIO_D4	BI		/		Bit4 of General purpose I/O port D
54	GPIO_F0	BI	6mA	Z		Bit0 of General purpose I/O port F
	MMC_D0	BI		/	PU50k	Bit0 of MMC/SD Card data bus
	MS_D0	BI		/	PD50k	Bit0 of MS Card data bus
55	D3	BI	2mA	L		Bit3 of ext. memory data bus
	GPIO_D3	BI		/		Bit3 of General purpose I/O port D
56	GPIO_A4	BI	10mA	/		Bit3 of General purpose I/O port B
	ICEEN-	I		H	PU200k	DSU enable (active low)
57	D2	BI	2mA	L		Bit2 of ext. memory data bus
	GPIO_D2	BI		/		Bit2 of General purpose I/O port D
58	GND	PWR	/	/		Ground

59	D1	BI	2mA	L		Bit1 of ext. memory data bus
	GPIO_D1	BI		/		Bit1 of General purpose I/O port D
60	D0	BI	2mA	L		Bit0 of ext. memory data bus
	GPIO_D0	BI		/		Bit0 of General purpose I/O port D
61	GPIO_C7	BI	2mA	Z		Bit7 of General purpose I/O port C
	SPI_SCLK	O		/		Clock of SPI
62	GPIO_C6	BI	2mA	Z		Bit6 of General purpose I/O port C
	SPI_MOSI	BI		/		MOSI of SPI
63	GPIO_C5	BI	2mA	Z		Bit5 of General purpose I/O port C
	SPI_MISO	BI		/		MISO of SPI
64	GPIO_C4	BI	2mA	Z		Bit4 of General purpose I/O port C
	SPI_SS	BI		/		SS of SPI

NOTE:

1: PWR—Power Supply

2: AI——Analog Input

3: AO——Analog Output

4: O——Output

5: I———Input

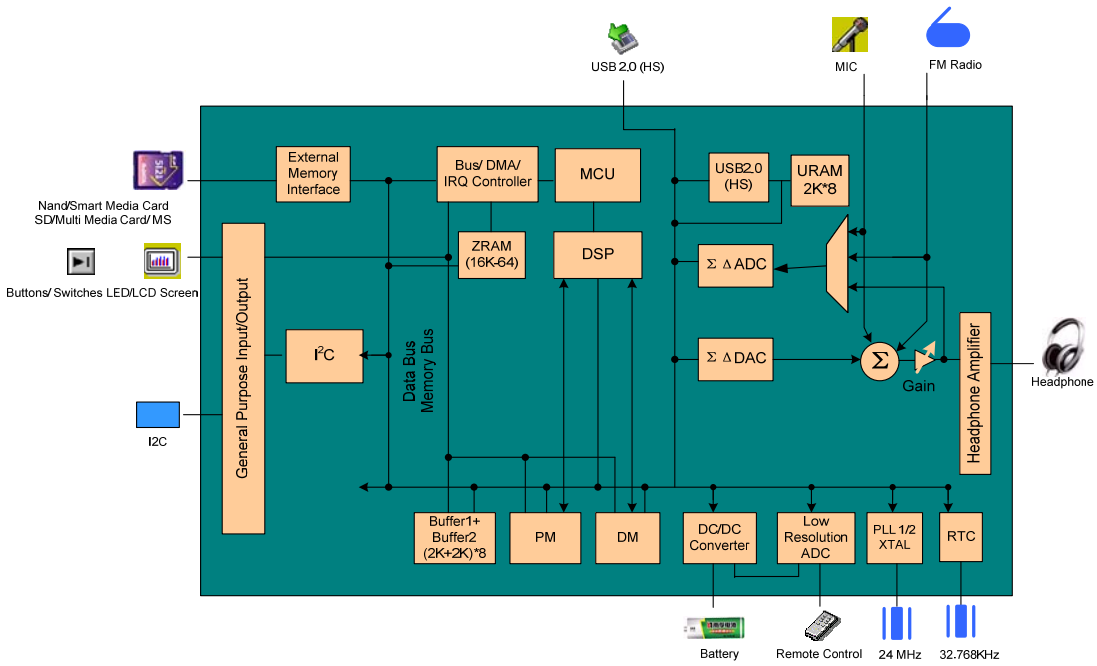
6: BI——Bidirection

7: USCU, USCL——USCHIMITCU, USCHIMITCL

8: PU——Pull up

PD——Pull down

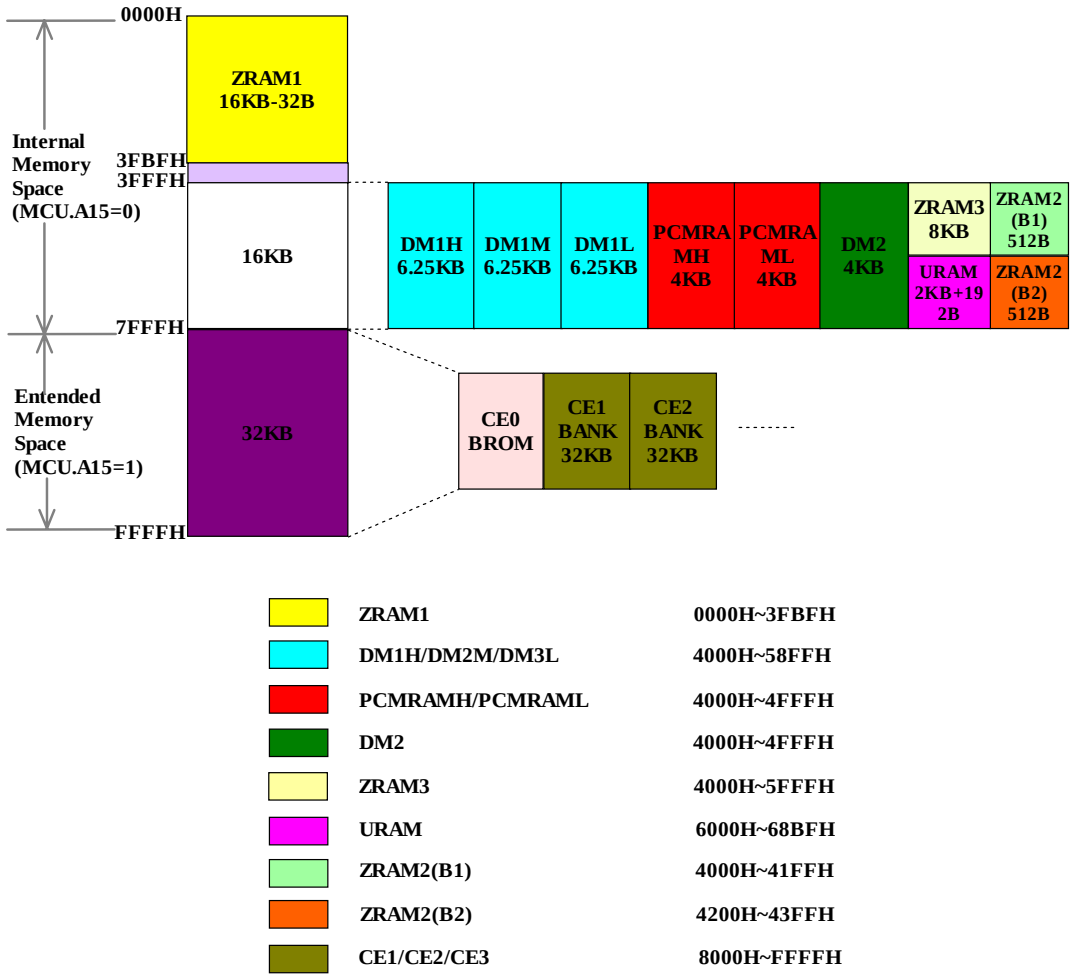
6 ATS250X Block Diagram



7 Memory Mapping

7.1 Memory Map

ATS250X provides both on-chip ROM and RAM memories to aid in system performance and integration.



Note: 3FBFH~3FFFH is mapping to the flash controller's register space.

7.1.1 Registers Description

ISRAMP (Internal SRAM Page Register, 05h)

Bits	Description	Access	Reset
7	0: DM1 is mapped to DSP 1: DM1 is mapped to MCU/DMA1/2/4/5	R/W	0
6	0: PCMRAMH is mapped to DSP 1: PCMRAMH is mapped to MCU/DMA1/2/4/5	R/W	0
5	0: PCMRAML is mapped to DSP 1: PCMRAML is mapped to MCU/DMA1/2/4/5	R/W	0
4	0: DM2 is mapped to DSP 1: DM2 is mapped to MCU/DMA1/2/4/5	R/W	0

3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+ URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2（B1+B2）	R/W	0

8 System Control Module

8.1 Description

This chapter describes the extended 8 bit mcu with RAM access, its bus controller, B1/B2 controller, reset management uint, direct memory access (DMA) controller, CTC module and interrupt controller

8.2 Bus Controller

8.2.1 MCU Clock Control Register

MCUCLK (**MCU Clock Control Register**, 00h)

Bits	Description	Access	Reset
7:6	**Number of Wait states for external memory access** 0 0: 0, zero wait state(default) 0 1: 1, one wait state 1 0: 2, two wait states 1 1: 3, three wait states If access internal BROM no wait state needed.	R/W	0

5:4	**MCU clock source select** 0 0: LOSC 0 1: HOSC 1 0: MCU PLL 1 1: reserved	R/W	0
3	Reserved	/	/
2:0	**MCU clock division control** 0 0 0 /01(default) 0 0 1 /02 0 1 0 /04 0 1 1 /08 1 0 0 /16 1 0 1 /32 1 1 0 /64 1 1 1 /DC	R/W	0

It may take a while before MCU Clock Change. When the MCU clock is stopped (DC), there are several ways to recover the clock to non-divided LOSC clock source:

1. Push Reset button
2. POWER ON RESET
3. Alarm IRQ
4. SIRQ
5. USB wake up IRQ
6. LRADC1 IRQ

8.2.2 DMA1/DMA2 Clock Division Register

DMA12CD (**DMA12 Clock Division Register**, 29h)

Bits	Description	Access	Reset
7:3	Reserved.	/	/

2:0	**DMA1/DMA2 Clock Division Control** 0 0 0 /01 0 0 1 /02 0 1 0 /04 0 1 1 /08 1 0 0 /16 1 0 1 /32 1 1 0 /64 1 1 1 /128	R/W	000

8.2.3 Chip Enable Selection Register

CESEL (**Chip Enable Selection Register**, 02h)

Bits	Description	Access	Reset
7	Multiplexing of GPIOA7 and CE5- 0: GPIOA7 1: CE5- When SIRQ Enabled, CE5- and GPIO is shielded for SIRQ	R/W	0
6	Multiplexing of GPIOA6 and CE4- 0: GPIOA6 1: CE4-	R/W	0
5	Multiplexing of GPIOA5 and CE3- 0: GPIOA5 1: CE3-	R/W	0
4	Multiplexing of GPIOB1 and CE2- 0: GPIOB1 1: CE2-	R/W	0
3	Multiplexing of GPIOB0 and CE1- 0: GPIOB0 1: CE1-	R/W	1

2:0	**Chip Enable Selection:** 000B,decode to CE0- 001B,decode to CE1- 010B,decode to CE2- 011B,decode to CE3- 100B,decode to CE4- 101B,decode to CE5- 110B,decode to CE6-(NO PIN) 111B,decode to CE7-(NO PIN)	R/W	000

8.2.4 MCU-A15 Control Register

MCUCTL (**MCU-A15 Control Register,** 04h)

Bits	Description	Access	Reset
7	**Watch Dog Flag,** 1 means WD reset or irq ever occurred. Writing 1 to this bit clears it.	R/W	0
6	**External Reset flag,** 1 means external reset had been asserted, writing 1 to this bit clears the bit	R/W	0
5	**Low Bat NMI- pending.** The LBNMI- voltage can be set by the LB Register. If LBNMI- occurred, this bit will be set. Writing 1 to this bit will clear it.	R/W	0
4	**Reserved**	/	/
3	SIRQ trigger edge select: 0: negative edge 1:positive edge When SIRQ is enabled and this bit is set 0, the 200K PULL HIGH Register will be enabled. When SIRQ is enabled and this bit is set 1, the 200K PULL LOW Register will be enabled.	R/W	0
2	**SIRQ- Enable.** 0: Disable 1: enable. SIRQ will be enable by this bit, and it can be trigged by signal connected to SIRQ- pin on negative or positive edge selected by bit3 of this Register	R/W	0

1	**LBNMI- Enable.** 0: Disable 1: enable.	R/W	0
0	**A15 control bit.** 0: force MCU's A15 to be 1, execute program from CE0 memory space. 1: for normal operation The boot code after power on reset must be jp 800xh followed by an IO write to 04h to set this bit for normal operation.	R/W	0

8.2.5 General Random Access IO Register

GRAIO (**General Random Access IO Register,** 03Fh)

Bits	Description	Access	Reset
7:0	This register is a general random access IO and can be written and read by MCU/DMA1/DMA2/DMA4/DMA5	R/W	0

8.3 DMA Channel 1

8.3.1 DMA1 Source Address 0 Register

DMA1SADDR0 (**DMA1 Source Address 0 Register,** 06h)

Bits	Description	Access	Reset
7:0	DMA1SA[7:0]	R/W	X

8.3.2 DMA1 Source Address 1 Register

DMA1SADDR1 (**DMA1 Source Address 1 Register,** 07h)

Bits	Description	Access	Reset
7:0	DMA1SA[15:8]	R/W	X

8.3.3 DMA1 Source Address 3 Register

DMA1SADDR3 (**DMA1 Source Address 3 Register,** 09h)

Bits	Description	Access	Reset
7	**External Memory Select,** 0:Internal Memory, 1:external memory	R/W	0
6	**Int. Memory select,** 0:ZRAM1,1: DM1/PCMRAM/ DM2/ZRAM2(B1,B2,URAM)/ ZRAM3	R/W	0
5:3	**Reserved**	/	/
2:0	DMA1SA[25:23]	R/W	X

8.3.4 DMA1 SRC Address Register

DMA1ISA (**DMA1 SRC Address Register,** 0Ah)

Bits	Description	Access	Reset
7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2(B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 6000H-68BFH	R/W	011

8.3.5 DMA1 Destination Address 0 Register

DMA1DADDR0 (**DMA1 Destination Address 0 Register,** 0Bh)

Bits	Description	Access	Reset
7:0	DMA1DA[7:0]	R/W	Xxh

8.3.6 DMA1 Destination Address 1 Register

DMA1DADDR1 (**DMA1 Destination Address 1 Register,** 0Ch)

Bits	Description	Access	Reset
7:0	DMA1DA[15:8]	R/W	Xxh

8.3.7 DMA1 Destination Address 3 Register

DMA1DADDR3 (**DMA1 Destination Address 3 Register,** 0Eh)

Bits	Description	Access	Reset
7	**External Memory Select,** 0: Int. Memory, 1: external memory	R/W	0
6	**Int. Memory select,** 0:ZRAM1, 1: DM1/PCMRAM/ DM2/ZRAM2(B1,B2,URAM)/ ZRAM3	R/W	0
5:3	**Reserved**	/	/
2:0	DMADA[25:23]	R/W	X

8.3.8 DMA1 DST Address Register

DMA1IDA (**DMA1 DST Address Register,** 0Fh)

Bits	Description	Access	Reset
7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2(B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 6000H-68BFH	R/W	011

8.3.9 DMA1 Byte Counter Low Register

DMA1BCL (DMA1 Byte Counter Low, 10h)

Bits	Description	Access	Reset
7:0	DMA1BC[7:0]	R/W	Xx

8.3.10 DMA1 Byte Counter High Register

DMA1BCH (**DMA1 Byte Counter High Register,** 011h)

Bits	Description	Access	Reset
7	Reserved	/	/
6:0	DMA1BC[14:8],Maximum transferred byte is 32Kbytes	R/W	Xx

8.3.11 DMA1 Mode Register

DMA1M (**DMA1 Mode Register,** 012h)

Bits	Description	Access	Reset
7:6	DMA1 wait state select 0 0 0 wait state 0 1 1 wait state 1 0 2 wait states 1 1 3 wait states	R/W	0
5	Reserved	/	/
4	DMA1 DST down count 0:Up count, 1: Down count	R/W	0
3	DMA1 SRC down count 0: Up count, 1: Down count	R/W	0
2	Reserved	/	/
1	DMA1 DST is IO. 0 : Memory 1: IO	R/W	0
0	DMA1 SRC is IO. 0 : Memory 1: IO	R/W	0

8.3.12 DMA1 Command Register

DMA1COM (**DMA1 Command Register,** 013h)

Bits	Description	Access	Reset
7	**DMA1 TC IRQ enable.** 0: Disable IRQ. 1: Enable IRQ when DMA1 finishes the whole block transfer.	R/W	0
6	**DMA1 Half Transfer IRQ enable.** 0: Disable IRQ. 1: Enable IRQ when DMA1 finishes half of the block transfer.	R/W	0
5	**DMA1 Continue Block Transfer enable.** 0: Disable continuous block transfer mode and Bit 1 of this register will be cleared when the last byte of the block is transferred. 1 enables Continuous block transfer mode and Bit 1 of this register will not be cleared and SRC Address Counter/DST Address Counter/Byte Length Counter will be reloaded with their corresponding registers when DMA1 finishes the block transfer.	R/W	0
4	**DMA1 Priority** 0: DMA1 Low priority 1: DMA1 High priority When both DMA1 Priority and DMA2 Priority are set or cleared simultaneously, the priority is in first start first finished style.	R/W	0
3:2	**External Trigger** 0 0 DRQ1A, UART TX DRQ 0 1 DRQ1B, DSP FIFO Input DRQ 1 0 DRQ1C, SPI TX DRQ 1 1 DRQ1D, SPDIF TX DRQ	R/W	0
1	**External DRQ trigger enable,** 0: Disable external DRQ trigger, 1: Enable.	R/W	0
0	**DMA1 Start.** After TC the bit will be cleared. The low-go-high edge of this bit will load SRC start address, DST start address, byte count into current working counters.	R/W	0

8.4 DMA Channel 2

8.4.1 DMA2 Source Address 0 Register

DMA2SA0 (**DMA2 Source Address 0 Register,** 014h)

Bits	Description	Access	Reset
7:0	DMA2SA[7:0]	R/W	Xx

8.4.2 DMA2 Source Address 1 Register

DMA2SA1 (**DMA2 Source Address 1 Register,** 015h)

Bits	Description	Access	Reset
7:0	DMA2SA[15:8]	R/W	Xx

8.4.3 DMA2 Source Address 3 Register

DMA2SA3 (**DMA2 Source Address 3 Register,** 017h)

Bits	Description	Access	Reset
7	**External Memory Select,** 0:Internal Memory, 1:external memory	R/W	0
6	**Int. Memory select,** 0:ZRAM1,1: DM1/PCMRAM/ DM2/ZRAM2(B1,B2,URAM)/ ZRAM3	R/W	0
5:3	**Reserved**	/	/
2:0	DMA1SA[25:23]	R/W	X

8.4.4 DMA2 SRC Address Register

DMA2ISA (**DMA2 SRC Address Register,** 018h)

Bits	Description	Access	Reset

7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2(B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 6000H-68BFH	R/W	011

8.4.5 DMA2 Destination Address 0 Register

DMA2ISA0 (**DMA2 Destination Address 0 Register,** 019h)

Bits	Description	Access	Reset
7:0	DMA2DA[7:0]	R/W	Xx

8.4.6 DMA2 Destination Address 1 Register

DMA2ISA1 (**DMA2 Destination Address 1 Register,** 01Ah)

Bits	Description	Access	Reset
7:0	DMA2DA[15:8]	R/W	Xx

8.4.7 DMA2 Destination Address 3 Register

DMA2ISA3 (**DMA2 Destination Address 3 Register,** 01Ch)

Bits	Description	Access	Reset
7	**External Memory Select,** 0:Internal Memory, 1:external memory	R/W	0

6	**Int. Memory select,** 0:ZRAM1,1: DM1/PCMRAM/ DM2/ZRAM2(B1,B2,URAM)/ ZRAM3	R/W	0
5:3	**Reserved**	/	/
2:0	DMA1SA[25:23]	R/W	X

8.4.8 DMA2 DST Address Register

DMA2IDA (**DMA2 DST Address Register,** 01Dh)

Bits	Description	Access	Reset
7:3	Reserved	/	/
2:0	Extended SRAM page address bit. 0 0 0: DM1 low byte 0 0 1: DM1 middle byte 0 1 0: DM1 high byte 0 1 1: ZRAM3+URAM 1 0 0: PCMRAM low byte 1 0 1: PCMRAM high byte 1 1 0: DM2 1 1 1: ZRAM2(B1+B2) B1: 4000H-41FFH B2: 4200H-43FFH URAM: 6000H-68BFH	R/W	011

8.4.9 DMA2 Byte Counter Low Register

DMA2BCL (**DMA2 Byte Count low Register,** 01Eh)

Bits	Description	Access	Reset
7:0	DMA2BC[7:0]	R/W	Xx

8.4.10 DMA2 Byte Counter High Register

DMA2BCH (**DMA2 Byte Count High Register,** 01Fh)

Bits	Description	Access	Reset
7	Reserved	/	/
6:0	DMA2BC[14:8]	R/W	Xx

8.4.11 DMA2 Mode Register

DMA2M (**DMA2 Mode Register,** 020h)

Bits	Description	Access	Reset
7:6	DMA2 wait state select 0 0 0 wait state 0 1 1 wait state 1 0 2 wait states 1 1 3 wait states	R/W	0
5	Reserved	/	/
4	DMA2 DST down count. 0: Up count, 1: Down count.	R/W	0
3	DMA2 SRC down count. 0: Up count, 1: Down count.	R/W	0
2	Reserved	/	/
1	DMA2 DST is IO. 0: Memory, 1: IO.	R/W	0
0	DMA2 SRC is IO. 0: Memory, 1: IO.	R/W	0

8.4.12 DMA2 Command Register

DMA2COM (**DMA2 Command Register,** 021h)

Bits	Description	Access	Reset
7	DMA2 TC IRQ Enable. 0: Disable IRQ. 1: Enable IRQ when DMA2 finishes whole block transfer.	R/W	0
6	DMA2 Half Transfer IRQ Enable. 0: Disable IRQ. 1: Enable IRQ when DMA2 finishes half of the block transfer.	R/W	0

5	DMA2 Continue Block Transfer Enable. 0: disables continuous block transfer mode and Bit 1 of this register will be cleared when the last byte of the block is transferred. 1 enables Continuous block transfer mode and Bit 1 of this register will not be cleared and SRC Address Counter/DST Address Counter/Byte Length Counter will be reloaded with their corresponding registers when DMA2 finishes the block transfer.	R/W	0
4	DMA2 Priority, 0: DMA2 low priority, 1: DMA2 high priority When both DMA1 Priority and DMA2 Priority are set or cleared simultaneously, the priority is in first start first finished style.	R/W	0
3:2	External DRQ trigger select 0 0 DRQ2A, UART RX DRQ 0 1 DRQ1B, DSP FIFO Input DRQ 1 0 DRQ2C, SPI RX DRQ 1 1 DRQ2D, SPDIF RX DRQ	R/W	0
1	External DRQ trigger enable, 0: Disable external DRQ trigger, 1: enable.	R/W	0
0	DMA2 Start. After TC the bit will be cleared. The low-go-high edge of this bit will load SRC start address, DST start address, byte count into current working counters.	R/W	0

8.5 CTC

8.5.1 CTC Prescale Register

CTCPRES (**CTC Prescale Register,** 022h)

Bits	Description	Access	Reset
7	CTC1 enable 0: Disable, 1: Enable.	R/W	0
6:0	Pre-scale, /1, /2 /3 /4 ..... /128. Clock source of CTC is HOSC.	R/W	X

8.5.2 CTC Period Low Register

CTCTPL (**CTC T Period Low Register,** 023h)

Bits	Description	Access	Reset
7:0	TPERIOD[7:0], period low byte register of CTC	R/W	Xx

8.5.3 CTC Period High Register

CTCTPH (**CTC T Period High Register,** 024h)

Bits	Description	Access	Reset
7:0	TPERIOD[15:8], period register of CTC	R/W	Xx

8.6 Interrupt Controller

8.6.1 DMA/CTC IRQ Status Register

DMACISTA (**DMA/CTC IRQ Status Register,** 025h)

Bits	Description	Access	Reset
7	CTC IRQ Pending, writing 1 to this bit will clear it.	R/W	0
6	DMA2 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
5	DMA2 End Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
4	DMA1 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
3	DMA1 End Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
2	SIRQ- Pending, writing 1 to this bit will clear it.	R/W	0
1	Reserved.	/	/
0	software controlled DMA1/DMA2 reset signal, The low-go-high edge of this bit will generate a pulse to reset DMA1/DMA2 state machine, bytes counter, and clear H.W DRQ, etc status. After the pulse the bit will be cleared to '0'.	R/W	0

8.6.2 Master Interrupt Status Register

MISTA (**Master Interrupt Status Register,** 026h)

Bits	Description	Access	Reset
7	A/D Interrupt(3) 1. Wire-Control IRQ 2. Audio ADC IRQ 3. Charge Status IRQ This bit will automatically cleared only when All the A/D INT pending bit is cleared, otherwise unchanged	R/W	0
6	Reserved	/	/
5	RTC Interrupt.(4) 1. Watch Dog IRQ 2. RTC Timer IRQ 3. RTC Alarm IRQ 4. 2HZ RTC IRQ This bit will automatically cleared only when All the RTC INT pending bit is cleared, otherwise unchanged	R/W	0
4	DMA1/2/4/SD/MMC/MS/CTC Interrupt(6) 1. DMA1 TC/Half Transfer IRQ 2. DMA2 TC/Half Transfer IRQ 3. DMA4 IRQ 4. SD/MMC Transfer end IRQ,FIFO IRQ or SDIO IRQ 5. MS Transfer Finished IRQ 6. CTC IRQ This bit will automatically cleared only when All the DMA1/2/4/SD/MMC/MS/CTC INT pending bit is cleared, otherwise unchanged	R/W	0
3	SIRQ/I2C/SPI/RB Interrupt(4) 1. External IRQ (SIRQ) 2. I2C IRQ 3. SPI RX/TX IRQ 4. RB1/RB2 RDY IRQ or State Machine Ending IRQ This bit will automatically cleared only when All the SIRQ/I2C/SPI/RB INT pending bit is cleared, otherwise unchanged	R/W	0
2	Reserved	R/W	0

1	UART/SPDIF/**IRC** Interrupt(2) 1. UART RX IRQ 2. SPDIF Block In IRQ or Data In IRQ **3. IRC RX IRQ** This bit will automatically cleared only when All the UART/SPDIF/IRC INT pending bit is cleared, otherwise unchanged	R/W	0
0	DSP interrupt(4) Pending, This bit will automatically cleared only when All the DSP INT pending bit is cleared, otherwise unchanged	R/W	0

8.6.3 Master Interrupt Enable Register

MIEN (**Master Interrupt Enable Register,** 027h)

Bits	Description	Access	Reset
7	A/D interrupt Enable, 0: Disable, 1: Enable.	R/W	0
6	Reserved	/	/
5	RTC interrupt Enable, 0: Disable, 1: Enable.	R/W	0
4	DMA1/2/4/SD/MMC/MS/CTC Interrupt Enable. 0:Disable.1:Enable	R/W	0
3	SIRQ/I2C/SPI/RB Interrupt Enable. 0: Disable, 1: Enable.	R/W	0
2	USB Interrupt Enable, 0: Disable, 1: Enable.	R/W	0
1	UART/SPDIF/IRC Interrupt Enable, 0: Disable, 1: Enable.	R/W	0
0	DSP Interrupt Enable, 0: Disable, 1: Enable.	R/W	0

9 DSP

9.1 Description

The Core is a high performance Digital Signal Processor (DSP) suitable for digital audio compounding functioins. The DSP is designed for low power handheld applications. All decoding data paths are optimized to ensure the best performance with the least silicon area.

10 USB2.0 OTG

Actions USB2.0 OTG (AOTG) is a Dual-Role-Device (DRD) controller which complies with On-The-Go Supplement to the USB2.0 Specification V1.0a.

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports 2 IN endpoint and 1 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint buffer size, endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup.
- Support Udisk mode high speed DMA panel

11 I2C Interface

11.1 Description

The I2C can be configured as either a master or slave device. In master mode it generates the clock (I2C_SCL) and initiates transactions on the data line (I2C_SDA). Data on the I2C bus is byte oriented. Multi-Master mode, 10-bit address and Hi-speed mode are not supported.

Pull-up resistors are required on both of the I2C lines. Typically external 2k-ohm resisters are used to pull up the signals.

Features:

- Two-wire Serial interface.
- 100Khz and 400Khz Compatibility

11.2 Register Description

I2C module registers

Address	Name	Description
84H	I2CADDR	I2C Address Register
85H	I2CCTL	I2C Control Register
86H	I2CSTA	I2C Status Register
87H	I2CDAT	I2C Data Register
2Bh	MCSR	Module Clock Select Register

11.2.1 I2CADDR (I2C Address Register, 084h)

This register is used for setting I2C slave address in master or slave mode.

Bits	Description	Access	Reset
7:1	I2C Slave Address.	R/W	0

0	In master mode, R/W control bit In slave mode: I2C Slave Address Match. 0: match, send IRQ to MCU 1: not match, don't send IRQ In master mode, address 7-bit is used to setting the slave address, so the I2C data register just store the data. In slave mode, address 7-bit is used to compare with the address that master sending out. So the I2C data register can store the address and data.	R/W	0

11.2.2 I2CCTL (I2C Control Register, 085h)

This register is used for enabling I2C and I2C IRQ, selecting I2C operating mode, ACK generation.

Bits	Description	Access	Reset
7	I2C Enable. 0: disable 1: enable I2C receive and transmit channel.	R/W	0
6	In master mode, operating mode select. 0: standard (100kbps) 1: fast (400kbps) In slave mode, Start IRQ enable. 0: disable 1: enable	R/W	0
5	I2C IRQ enable, 0:disable, 1:enable	R/W	0
4	I2C master or slave select. 0:master, 1:slave	R/W	0
3:2	I2C cond[1..0]. generate a bus control .(master mode only) 0 0 no effect 0 1 generate start condition 1 0 generate stop condition 1 1 SCL will be released to high level to generate repeated start condition	R/W	0
1	Writing 1 to this bit will release the clock and data line to idle.	R/W	0

0	in transmitting ACK —ACK enable. Controls generation of an ACK signal in receive mode 1: Do not generate an ACK at 9th SCL , 0: Generate an ACK signal at 9th SCL. In receiving ACK — Last Received Bit. Use the read only bit to check the ACK signals from the receiver(slave),or to monitor SDA operation of SDA when writing 11 to control reg bit[3..2] for repeated starts.	R/W	0

11.2.3 I2CSTA (I2C Status Register, 086h)

This register is used for displaying current I2C status.

Bits	Description	Access	Reset
7	I2C Buffer Flag. Automatically cleared when I2C data reg is written or read Automatically set when the buffer is empty in transmit mode or when the buffer is full in receive mode. Writing 1 to this bit will clear it. transmit 0: Transmit in progress 1: Transmit complete receive 0: Receive in progress 1: Receive complete	R/W	0
6	I2C STOP bit. This bit is cleared when the I2C mode is disable or when the start bit was detected last. Writing 1 to this bit will clear it. 1: Indicate that the STOP bit was detected last 0: STOP bit was not detected last	R/W	0
5	I2C START bit. This bit is cleared when the I2C mode is disable or when the stop bit was detected last. Writing 1 to this bit will clear it. 1: Indicate that the START bit was detected last 0: START bit was not detected last	R/W	0

4	I2C R/W bit. Read/Write bit information. This bit holds the R/W bit information following the last address match. This bit is valid only from the address match to the next start bit, stop bit or NAK bit. 1: Read 0: Write	R/W	0
3	I2C D/A. Data/Address bit 1: indicate the last byte received or transmitted was data. 0: indicate the last byte received or transmitted was address.	R/W	0
2	I2C IRQ Pending bit. Writing 1 to this bit will clear it.	R/W	0
1	I2C overflow bit. Writing 1 to this bit will clear it. 1: A new byte is receiving while the previous byte has not been read 0: No overflow	R/W	0
0	Reserved	/	/

Whenever overflow is set, NAK will occur automatically.

11.2.4 I2CDAT (I2C Data Register, 087h)

This register is used for writing data to or reading data from I2C Data Register.

Bits	Description	Access	Reset
7:0	I2C Data/Address[7:0]	R/W	00

12 SPI Interface

12.1 Description

ATS250X SPI can be configured as either a master or slave device. During an SPI transfer, data is shifted out and shifted in (transmitted and received) simultaneously. The SPI_SCK line synchronizes the shifting and sampling of the information. It is an output when the SPI is configured as a master or an input when the SPI is configured as a slave.

SPI uses a couple parameters called clock polarity (CPOL) and clock phase (CPHA) to determine when data is valid with respect to the clock signal. CPOL determines whether the leading edge is defined to be the rising or falling edge of the clock (and vice versa for the trailing edge). CPHA determines whether the leading edge is used for setup or sample (and vice versa for the trailing edge). The following table summarizes the various settings, more detail information as shown see SPI Mode Timing.

CPOL/CPHA	Leading Edge	Trailing Edge	SPI Mode
0/0	Sample, rising	Setup, falling	0
0/1	Setup, rising	Sample, falling	1
1/0	Sample, falling	Setup, rising	2
1/1	Setup, falling	Sample, rising	3

Features:

- Master and slave modes of operation.
- DMA interface supporting data transfer from bulk memory to the synchronous serial interface
- Support SPI full-duplex mode and half-duplex mode.
- Master and slave mode boot options to download the code image from the SPI norflash.

12.2 Register Description

SPI module registers

Address	Name	Description
A8H	SPICTL	SPI Control Register
A9H	SPIIRQ	SPI IRQ Register

AAH	SPISTA	SPI Status Register
ABH	SPICLKDIV	SPI Clock Divide Control Register
ACH	SPIDAT	SPI Data Register
ADH	SPIBCL	SPI Byte Count Low Register
AEH	SPIBCH	SPI Byte Count High Register
2Bh	MCSR	Module Clock Select Register

12.2.1 SPICTL (SPI Control Register, A8h)

This register is used for enabling SPI module, selecting SPI mode and SPI SS output voltage.

Bits	Description	Access	Reset
7	**SPI Enable** 0: disable; 1: enable SPI receive and transmit channel	R/W	0
6	**SPI master/slave select** 0: master 1: slave	R/W	0
5	**LSB/MSB First Select** 0: transmit and receive MSB first 1: transmit and receive LSB first	R/W	0
4	**SPI SS pin control output,** this bit is valid only in master mode 1: output high 0: output low	R/W	1
3:2	**SPI mode select** CPOL CPHA 00: mode 0 01: mode 1 10: mode 2 11: mode 3	R/W	11
1	**Two wire mode enable bit** 0: normal 4 wire mode 1: two wire mode, use two pins only, SPI_CLK and SPI_MOSI	R/W	00
0	**SPI full-duplex or half-duplex mode select** 0: full-duplex mode 1: half-duplex mode	R/W	0

12.2.2 SPIIRQ (SPI IRQ Register, A9h)

This register is used for enabling SPI DRQ/IRQ, and selecting SPI DRQ/IRQ trigger threshold.

Bits	Description	Access	Reset
7	**SPI TX DRQ Enable**, 0: disable, 1: enable	R/W	0
6	**SPI RX DRQ Enable**, 0: disable, 1: enable	R/W	0
5	**SPI TX IRQ/DRQ trigger threshold Control.** 0: trigger SPI TX IRQ/DRQ when SPI TX FIFO is half empty 1: trigger SPI TX IRQ/DRQ when SPI TX FIFO is empty	R/W	0
4	**SPI RX IRQ/DRQ trigger threshold Control.** 0: trigger SPI RX IRQ/DRQ when SPI RX FIFO is half full 1: trigger SPI RX IRQ/DRQ when SPI RX FIFO is not empty	R/W	0
3	**SPI TX IRQ Pending**, 0: No TX IRQ Pending, 1: TX IRQ Pending. Write 1 to this bit will clear it.	R/W	0
2	**SPI RX IRQ Pending**, 0: No RX IRQ Pending, 1: RX IRQ Pending. Write 1 to this bit will clear it.	R/W	0
1	**SPI TX IRQ Enable**, 0: disable, 1: enable	R/W	0
0	**SPI RX IRQ Enable**, 0: disable, 1: enable	R/W	0

12.2.3 SPISTA (SPI Status Register, AAh)

This register is used for displaying current SPI FIFO status.

Bits	Description	Access	Reset
7	**SPI TX FIFO Empty** 0: not empty 1: empty	R	1
6	**SPI TX FIFO Full** 0: not full 1: full	R	0
5	**SPI RX FIFO Empty** 0: not empty 1: empty	R	1
4	**SPI RX FIFO Full** 0: not full 1: full	R	0
3	**SPI TX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged.	R/W	0
2	**SPI RX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged.	R/W	0

1	**SPI Transfer Complete**—This bit is set to 1 at the end of an SPI transfer, and cleared by a read or write to the SPI Data Register.	R/W	0
0	**Reserved**	/	/

12.2.4 SPICLKDIV (SPI Clock Divide Control Register, ABh)

This register is used for setting SPI source clock divide factor, and selecting SPI read mode.

Bits	Description	Access	Reset
7	**SPI read clock delay enable bit (valid only in half-duplex mode)** 0: disable clock delay 1: enable clock delay	R/W	0
6:0	**SPI Clock Divide Factor** (SPICLKFactor) [6:0] if SPI Clock Divide Factor is 0, SPI CLK = MCU PLL, else SPI CLK = (MCU PLL) / (SPICLKFactor[6:0]*2)	R/W	1111111

12.2.5 SPIDAT (SPI Data Register, ACh)

This register is used for writing data to SPI TX FIFO or reading data from SPI RX FIFO.

Bits	Description	Access	Reset
7:0	**SPI Data[7:0]** Writing this field will send 1 byte to 8bitx8 levels depth SPI FIFO. Reading this field will fetch 1 byte from 8bitx8 levels depth SPI FIFO.	R/W	X

12.2.6 SPIBCL (SPI Bytes Count Low Register, ADh)

This register is used for setting SPI bytes counter low bits in the SPI norflash mode.

Bits	Description	Access	Reset
7:0	**Bytes Counter Low bits [7: 0]**	R/W	0

12.2.7 SPIBCH (SPI Bytes Count High Register, AEh)

This register is used to setting SPI bytes counter high bits, selecting SPI data I/O mode and high read rate mode delay time in the SPI norflash mode.

Bits	Description	Access	Reset
7	**SPI data I/O mode select** 0: 1x I/O mode select 1: 2x I/O mode select	R/W	0
6	**Reserved**	/	/
5:4	**SPI read clock delay time (valid when SPI read clock delay is enable)** 00: delay 2 ns 01: delay 4 ns 10: delay 8 ns 11: delay 12 ns	R/W	00
3	**Read Start Control**, write 1 to start Read clock（When transfer is finished, this bit will be auto cleared）	R/W	0
2	**SPI write or read select bit.** 0: select write 1: select read	R/W	0
1:0	**Bytes Counter High bits [1: 0]**	R/W	0

13 UART Interface

13.1 Description

UART is dedicated used for asynchronous serial communication with FIFO as data buffer for full-duplex operation. UART protocol contains a start bit, 5~8 data bits, a parity bit and a stop bit. The start bit must be 0 and the stop bit must be 1. Before communication, UART operation mode must set to be the same as remote terminal, such as baud rate, number of data bits, even/odd/no parity etc. Baud rate is up to 1.5MBaud and LSB first in TX/RX.

Two 8-level by 8 bits FIFO are used to buffer data for TX and RX.

Features:

- High-speed data transmission rate up to 1.5Mbps in UART mode.

13.2 Register Description

UART module registers table

Address	Name	Description
79H	BAUDRATE	UART Baud Rate Register
7AH	UART2CTL	UART Control Register
7BH	UARTFDAT	UART FIFO DATA Register
7CH	Reserved	Reserved
7DH	UARTMS	UART Mode & FIFO Status Register
7EH	UARTRQS	UART DRQ/IRQ Enable/Status Register
42H	CK48MCTL	UART Clock Source CK48M Control
2Bh	MCSR	Module Clock Select Register

UART Baud Rate Register

Prescale Value	13		1.625		1	
Baud	**Divisor**	**%Error**	**Divisor**	**%Error**	**Divisor**	**%Error**

Rate						
600	192	0.16%	-	-	-	-
1200	96	0.16%	-	-	-	-
1800	64	0.16%	-	-	-	-
2000	58	0.53%	-	-	-	-
2400	48	0.16%	-	-	-	-
3600	32	0.16%	256	0.16%	-	-
4800	24	0.16%	192	0.16%	-	-
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
38400	3	0.16%	24	0.16%	39	0.16%
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	-	-	4	0.16%	-	-
460800	-	-	2	0.16%	-	-
750000	-	-	-	-	2	0.00%
921600	-	-	1	0.16%	-	-
1500000	-	-	-	-	1	0.00%

13.2.1 BAUDRATE (UART Baud Rate Register, 079h)

This register is used for setting UART baud rate.

Bits	Description	Access	Reset
7:0	Baud rate generator, clock division	R/W	00

13.2.2 UARTCTL (UART Control Register, 07Ah)

This register is used for selecting UART clock pre-scale, parity, stop bits, bits per transmission.

Bits	Description	Access	Reset

7:6	Clock pre-scale select Bit 7 6 Pre-scale 0 0 /13 0 1 /13 1 0 /1.625 1 1 /1	R/W	0
5:3	Bit 5: STKP, Stick parity Bit 4: EPS, Even parity Bit 3: PEN, Parity enable PEN EPS STKP Selected Parity 0 x x None 1 0 0 Odd 1 1 0 Even 1 0 1 logic 1 1 1 1 logic 0	R/W	0
2	STOP select, if this bit is 0, 1 stop is generated in transmission. If this bit is 1 and 5 bits transmission is selected, 1.5 stop bit is generated. If this bit is 1 and 6/7/8 bits transmission is selected, 2 stop bits are generated. The receiver always checks 1 stop bit only.	R/W	0
1:0	WL[1:0], bits per transmission WL1 0 Bit per transmission 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits	R/W	0

13.2.3 UARTFDAT (UART FIFO DATA Register, 07Bh)

This register is used for writing data to UART TX FIFO or reading data from UART RX FIFO.

Bits	Description	Access	Reset
7:0	UART FIFO Data, writing to this port will write data to UART TX FIFO, reading from this port will read data from UART RX FIFO	R/W	x

13.2.4 UARTMS (UART Mode & FIFO Status Register, 07Dh)

This register is used for displaying current UART FIFO status.

Bits	Description	Access	Reset
7	Reserved	R/W	0
6	Reserved	R/W	0
5	UART TX FIFO Full. 1: full, 0: not full.	R	0
4	UART RX FIFO Empty. 1: empty, 0: not empty.	R	1
3	Reserved	R/W	0
2:0	Reserved	R/W	0

13.2.5 UARTRQS (UART DRQ/IRQ Enable/Status Register, 07Eh)

This register is used for enabling UART, selecting UART DRQ/IRQ trigger threshold, and displaying current UART FIFO status.

Bits	Description	Access	Reset
7	UART enable, 0:disable, 1:enable	R/W	0
6	FIFO mode control, for all UART FIFO 0: Issue DRQ when vacancy in TX FIFO or issue IRQ at least one data in RX FIFO, 1: Issue DRQ/IRQ when TX FIFO is half empty or RX FIFO is half full	R/W	0
5	UART Receive Error*, 0: Receive OK 1: Receive error occurs. Writing 1 to this bit will clear the bit, otherwise the bit is unchanged.	R/W	0
4	UART RX FIFO Error Writing 1 to this bit will clear it and reset the FIFO.	R/W	0
3	UART TX FIFO Error Writing 1 to this bit will clear it and reset the FIFO.	R/W	0
2	UART RX IRQ Pending Writing 1 to the bit to clear it, while 0 unchanged.	R/W	0

1	UART IRQ/DRQ Enable. 0: Disable, 1: Enable.	R/W	0
0	UART TX FIFO Empty 0: not empty 1: empty	R	1

14 Infrared Remote Control Interface

14.1 Introduction

The infrared remote control interface can only receive signal transmitted by remote controller. If the signal is coding according to one of the following three modes: Toshiba 9012 code, 8 bits NEC code, philips RC5 code, it can recognize and under controlled.

Features:

- Infrared remote control hardware decoder.
- Support three infrared remote control decode mode: Toshiba 9012 code, 8 bits NEC code, Philips RC5 code.

14.2 Register Description

Infrared remote control Module includes registers are showed as following table:

IRC module registers table

Address	Name	Description
0x78	IRCCTL	Infrared Remote Control interface control Register
0x7f	IRCSTA	Infrared Remote Control interface state Register
0x3B	IRCDAT	Infrared Remote Control interface data Register
0x3D	IRCMSEL	Infrared Remote Control IO Mapping Selet Register

IRCMSEL (**IRC IO MAPPING Selet**, 3Dh)

Bits	Description	Access	Reset
7: 2	Reserved	R/W	1
1	IRC GPIO mapping select 0 mapping to GPIO F5 1 mapping to GPIO C2	R/W	1
0	Reserved	R/W	1

IRCCTL (Infrared Remote Control interface control Register, 0x78)

This register is used for enabling infrared remote control interface, selecting infrared remote control coding mode and IRCDAT mapping type.

Bits	Description	Access	Reset
7	Infrared remote control interface enable. 0: IRC disable. 1: IRC enable.	R/W	0
6:5	Infrared remote control coding mode select. 00: 9012 code 01: 8 bits NEC code 10: RC5 code 11: Reserve	R/W	00
4	Reserve	/	/
3	IRC IRQ enable 0: disable 1: enable	R/W	0
2:1	IRCDAT mapping control bit. 00: IRCDAT mapping to IRCKDC. 01: IRCDAT mapping to IRCLUC. 10: IRCDAT mapping to IRCHUC. 11: IRCDAT mapping to IRCAKDC.	R/W	00
0	Reserve	/	/

IRCSTA (Infrared Remote Control interface state Register, 0x7f)

This register is used for displaying IRC status.

Bits	Description	Access	Reset
7	IRC flag. Automatically set when the IRC is receiving data, automatically clear when the data has been received. 1: receive in progress 0: receive complete	R	0
6	User code don't match pending bit. Automatically clear when new user code match, otherwise don't change. 0: user code match. 1: user code doesn't match.	R	0
5	Key data code verify error pending bit. Automatically clear when new key data code verify ok, otherwise don't change. 0: key data code verify ok. 1: key data code verify error.	R	0

4	IRC receive overflow pending bit, write 1 to this bit will clear it, otherwise don't change. 0: IRC receive not overflow. 1: IRC receive overflow.	R/W	0
3	IRC IRQ pending bit. Write 1 to this bit will clear it, otherwise don't change.	R/W	0
2:1	Reserve	/	/
0	IRC repeat flag detect bit. Write 1 to this bit will clear it, otherwise don't change. 0: repeat code is not detected. 1: repeat code is detected.	R/W	0

Note: when user code don't match and key data code verify error happen, IRC won't request IRQ, only when user code match and key data code verify ok happen, IRQ will be requested, this mechanism avoid IRQ request when receive error.

IRCLUC (Infrared Remote Control low user code Register, 0x3b)

This register is used for storing IRC low user code.

Bits	Description	Access	Reset
7:0	IRC user code [7:0]	R/W	0x00

IRCHUC (Infrared Remote Control high user code Register, 0x3b)

This register is used for storing IRC high user code.

Bits	Description	Access	Reset
7:0	IRC user code [15:8]	R/W	0x00

IRCKDC (Infrared Remote Control key data code Register, 0x3b)

This register is used for storing IRC key data code, it is just read only.

Bits	Description	Access	Reset
7:0	IRC key data code [7:0]	R	0x00

IRCAKDC (Infrared Remote Control anti key data code Register, 0x3b)

This register is used for storing IRC anti key data code, it is just read only for debug.

Bits	Description	Access	Reset
7:0	IRC anti key data code [7:0]	R	0x00

15 SPDIF Interface

15.1 Description

SPDIF is the abbreviation of Sony/Philips digital interface, the interface is primarily intended to carry stereophonic program, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible. See SPDIF standard documents for more detail information.

15.2 Register Description

SPDIF module registers table

Address	Name	Description
80H	SPDIFCTL	SPDIF Control Register
81H	SPDIFSTA	SPDIF Status Register
82H	SPDIFDAT	SPDIF FIFO DATA Register
83H	SPDIFCH	SPDIF Channel Status Register
2Bh	MCSR	Module Clock Select Register

15.2.1 SPDIFCTL (SPDIF Control Register, 080h)

This register is used for enabling SPDIF and SPDIF DRQ/IRQ, selecting SPDIF DRQ/IRQ trigger threshold, and resetting SPDIF FIFO.

Bits	Description	Access	Reset
7	SPDIF Enable. 0: Disable, 1: Enable.	R/W	0
6:5	Reserved.	/	/
4	SPDIF DRQ trigger threshold control. 0: Issue DRQ when vacancy in TX FIFO or issue IRQ at least one data in RX FIFO, 1: Issue DRQ/IRQ when TX FIFO is half empty or RX FIFO is half full	R/W	0
3	SPDIF DRQ Enable. 0: Disable, 1: Enable.	R/W	0

2	SPDIF FIFO Reset. 0: FIFO reset valid 1: FIFO reset invalid.	R/W	0
1	SPDIF Block In IRQ Enable. 0: Disable, 1: Enable.	R/W	0
0	SPDIF Data In IRQ Enable. 0: Disable, 1: Enable.	R/W	0

15.2.2 SPDIFSTA (SPDIF Status Register, 081h)

This register is used for displaying current SPDIF FIFO status.

Bits	Description	Access	Reset
7	SPDIF TX FIFO Full. 1: full.	R	0
6	SPDIF RX FIFO Empty. 1: empty.	R	1
5	SPDIF Block in IRQ pending Writing 1 to this bit will clear it, while 0 unchanged.	R/W	0
4	SPDIF Data in IRQ pending. Writing 1 to this bit will clear it, while 0 unchanged.	R/W	0
3	SPDIF TX FIFO error Pending. Writing 1 to this bit will clear it, otherwise unchanged.	R/W	0
2	SPDIF RX FIFO error Pending. Writing 1 to this bit will clear it, otherwise unchanged.	R/W	0
1	SPDIF Receive error Pending. Writing 1 to this bit will clear it, otherwise unchanged.	R/W	0
0	SPDIF TX FIFO Empty. 0: empty, 1: not empty.	R	0

15.2.3 SPDIFDAT (SPDIF FIFO DATA Register, 082h)

This register is used for writing data to SPDIF TX FIFO or reading data from SPDIF RX FIFO.

Bits	Description	Access	Reset
7:0	SPDIF FIFO DATA, Write: SPDIF TX FIFO. Read: SPDIF RX FIFO.	R/W	xxh

15.2.4 SPDIF Channel Status Register

For RX:

There is 32 bits status per 192 frames transfer. All these 4-byte status bits are mapped into this register. An internal read pointer is used to point to the current byte from which data will be returned at the next read. The internal read pointer increases after a read from this register. When SPDIF received all 192 frames of a block, SPDIF IRQ will be issued to notice MCU to read channel status. The internal pointer will be cleared when SPDIF is issued.

For TX:

Another 4 bytes status are also implemented for transmit, which are mapped into this register also. An internal write pointer is used to point to the byte position for next write. When read from this register, the internal write pointer will be cleared to point to the first byte of TX channel status. The write pointer will move to the next byte after a write to this register.

15.2.5 SPDIFCH (SPDIF Channel Status Register, 083h)

This register is used for setting SPDIF channel status.

Bits	Description	Access	Reset
7:0	SPDIF Channel status	R/W	xxh

16 Clock Management Unit

16.1 Description

ATS250X has a low frequency oscillator, which can choose build-in source or external one. It also have a RTC (Real Time Clock) with the alarm IRQ. The alarm IRQ can wake up the system. For protection purpose, this chip also has the watch dog circuit. It also has a Timer with IRQ.

Features

1. An individual power supply pin: RTCVDD
2. Built-in a 32k oscillator
3. Internal or external oscillator optional
4. RTC with a alarm IRQ which can wake up the system
5. 2Hz IRQ
6. A Timer with IRQ
7. A watch dog which can be configured IRQ or Reset optional

16.2 LOSC/RTC

16.2.1 RTC Control Register

RTCCTL (RTC Control Register, 043h)

Bits	Description	Access	Reset
7	RTC AlarmIRQ/calendar enable, 0: Disable AlarmIRQ and calendar, 1: Enable AlarmIRQ and calendar (POR- RESET).	R/W	0
6	RTC timer enable, 0: Disable RTC timer IRQ and timer counter, 1: Enable RTC timer IRQ and timer counter.	R/W	0
5	IRQ2HZEN, 0.5 sec IRQ Enable, 0: Disable, 1: Enable.	R/W	0
4:3	Reserved.	/	/
2	RTC Reset 1: Normal 0: Reset	R/W	1

1	Reserved	/	/
0	RTC time overflag Set when RTC time counter overflow, write 1 to clear it.	R/W	0

16.2.2 RTC IRQ Status Register

RTCIRQS (**RTC IRQ Status Register**, 044h)

Bits	Description	Access	Reset
7	External Crystal OSC Enable, 0: Disable, 1: Enable	R/W	1
6	RTC clock source select 0: internal OSC (about 32K), 1: external 32.768KHz OSC.	R/W	0
5	overflow read back, same as Bit 0 of Register 43H(Test Mode Only)	R/W	0
4	Reserved.	/	/
3	WATCH DOG counter status, (Test Mode Only)	R/W	0
2	RTC Alarm IRQ pending bit(POR- RESET), Writing 1 to this bit will clear it.	R/W	0
1	RTC timer IRQ pending bit, Writing 1 to this bit will clear it.	R/W	0
0	2Hz IRQ Pending Writing 1 to this bit will clear it.	R/W	0

16.2.3 RTC Time HMS Low Register

RTCTimeL (**RTC Time HMS Low Register**, 045h)

Bits	Description	Access	Reset
7:6	Time Minute[1:0] Register	R/W	xxh
5:0	Time Second[5:0] Register	R/W	xxh

16.2.4 RTC Time HMS High Register

RTCTimeM (**RTC Time HMS High Register**, 046h)

Bits	Description	Access	Reset
7:4	Time Hour[3:0] Register	R/W	xxh
3:0	Time Minute[5:2] Register	R/W	xxh

16.2.5 RTC Time Day Register

RTCTimeH (**RTC Time Day Register**, 047h)

Bits	Description	Access	Reset
7	Reserved.	/	/
6	Time Hour bit 4	R/W	x
5	Alarm Hour bit 4	R/W	x
4:0	Time Day Register.	R/W	xxh

16.2.6 RTC Time Year/Month Register

RTCALML (**RTC Time Month Register**, 048h)

Bits	Description	Access	Reset
7:4	TIME Year Register.(Power on Reset-)	R/W	xxh
3:0	TIME Month Register.	R/W	xxh

16.2.7 RTC Alarm HMS Low Register

RTCALMM (**RTC Alarm HMS Low Register**, 049h)

Bits	Description	Access	Reset
7:6	Alarm Minute[1:0] Register	R/W	xxh
5:0	Alarm Second[5:0] Register	R/W	xxh

16.2.8 RTC Alarm HMS High Register

RTCALMH (**RTC Alarm HMS High Register**, 04Ah)

Bits	Description	Access	Reset
7:4	Alarm Hour[3:0] Register	R/W	xxh
3:0	Alarm Minute[5:2] Register	R/W	xxh

16.2.9 LOSC Divider Low Byte Register

LOSCDLB (**Losc Divider Low Byte Register**, 04Bh)

Bits	Description	Access	Reset
7:0	LOSC Divider is a down counter with LOSC as clock. Low byte of LOSC Divider Register	R/W	xxh

16.2.10 LOSC Divider Middle Byte Register

LOSCDMB (**Losc Divider Middle Byte Register**, 04Ch)

Bits	Description	Access	Reset
7:0	Middle byte of LOSC Divider Register	R/W	xxh

16.2.11 LOSC Divider High Byte Register

LOSCDHB (**Losc Divider High Byte Register**, 04Dh)

Bits	Description	Access	Reset
7:0	High byte of LOSC Divider Register. When the Divider Counter Overflow, LDIVIRQ will occur. FLDIVIRQ = [1/(Reg4Bh+1)] *[1/(Reg4Ch+1)] *[1/(Reg4Dh+1)] *FLOSC	R/W	xxh

16.2.12 Watch Dog Register

WDOG (**Watch Dog Register**, 04Eh)

Bits	Description	Access	Reset
7	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot.	R/W	0
6:4	Watch Dog timer clock select, WDCKS Clock Selected Watch Dog Length 000 1 KHz 176 ms 001 512 Hz 352 ms 010 128 Hz 1.4 s 011 32 Hz 5.6 s 100 8 Hz 22.2 s 101 4 Hz 45 s 110 2 Hz 90 s 111 1 Hz 180 s	R/W	010
3	Clear bit, write 1 to clear WD timer, cleared automatically	R/W	0
2	Watchdog IRQ or Reset- Select.0: reset-, 1: IRQ. 0: when Watchdog timer times out, a watchdog timer reset will happen. 1: When Watchdog timer times out, a watchdog timer IRQ will happen.	R/W	0
1:0	Reserved.	/	/

16.3 HOSC/PLL

16.3.1 High Frequency Crystal Control Register

HFCCTL (**High frequency crystal control Register**, 040h)

Bits	Description	Access	Reset
7	High Frequency Crystal Oscillator Enable. 0 : Disable, 1 : Enable	R/W	0
6	Power ok status. 0: Power on,1: Power on finished	R	0
5:4	Reserved	/	/

3:2	High frequency crystal Oscillator GMMIN select bits	R/W	01
1:0	Reserved.	/	/

16.3.2 CK48M Control Register

CK48MCTL (**CK48MCTL control Register**, 042h)

Bits	Description	Access	Reset
7:6	Reserved.	RW	0
5	**CK48M Enable** 0: Disable 1: Enable	R/W	0
4:0	Reserved.		

16.3.3 MCU PLL Control Register

MCUPLL (**MCU PLL Control**, 28h)

Bits	Description	Access	Reset
7	**MCU PLL Enable** .0: Disable 1: Enable.	R/W	0

6:2	**MCU PLL output select.** 0 0 0 x x 12MHz 0 0 1 0 0 16MHz 0 0 1 0 1 20MHz 0 0 1 1 0 24MHz 0 0 1 1 1 28MHz 0 1 0 0 0 32MHz 0 1 0 0 1 36MHz 0 1 0 1 0 40MHz 0 1 0 1 1 44MHz 0 1 1 0 0 48MHz 0 1 1 0 1 52MHz 0 1 1 1 0 56MHz 0 1 1 1 1 60MHz 1 0 0 0 0 64MHz 1 0 0 0 1 68MHz 1 0 0 1 0 72MHz 1 0 0 1 1 76MHz 1 0 1 0 0 80MHz 1 0 1 0 1 84MHz 1 0 1 1 0 88MHz 1 0 1 1 1 92MHz 1 1 0 0 0 96MHz 1 1 0 0 1 100MHz 1 1 0 1 0 104MHz 1 1 0 1 1 108MHz 1 1 1 0 0 112MHz 1 1 1 0 1 116MHz 1 1 1 1 0 120MHz 1 1 1 1 1 124MHz	R/W	00000
1:0	Reserved.	/	/

16.4 Clock Selection Unit

16.4.1 Module Clock Select Register

MCSR (Module Clock Select Register , 2Bh)

Bits	Description	Access	Reset
7	**UART Controller Clock Select** 0 DC 1 CK48M	R/W	0
6	**SPDIF Controller Clock Select** 0 DC 1 CK48M	R/W	0
5:4	**SPI Controller Clock Select** 0 x DC 1 0 HOSC 1 1 MCU PLL	R/W	00
3	**I2C Controller Clock Select** 0 DC 1 HOSC	R/W	0
2:0	**Reserved**	/	/

17A/D D/A and Headphone Driver

17.1 Introduction

The D/A A/D module includes a Sigma-Delta DAC, a Sigma-Delta ADC which supports Microphone/FM/Line input. Both DAC and ADC support 48k/44.1k/32k/24k/22.05k/16k/12k/11.025k/8k sample rate. Its an on-chip 20mW power amplifier support to drive 32/16ohm earphone.

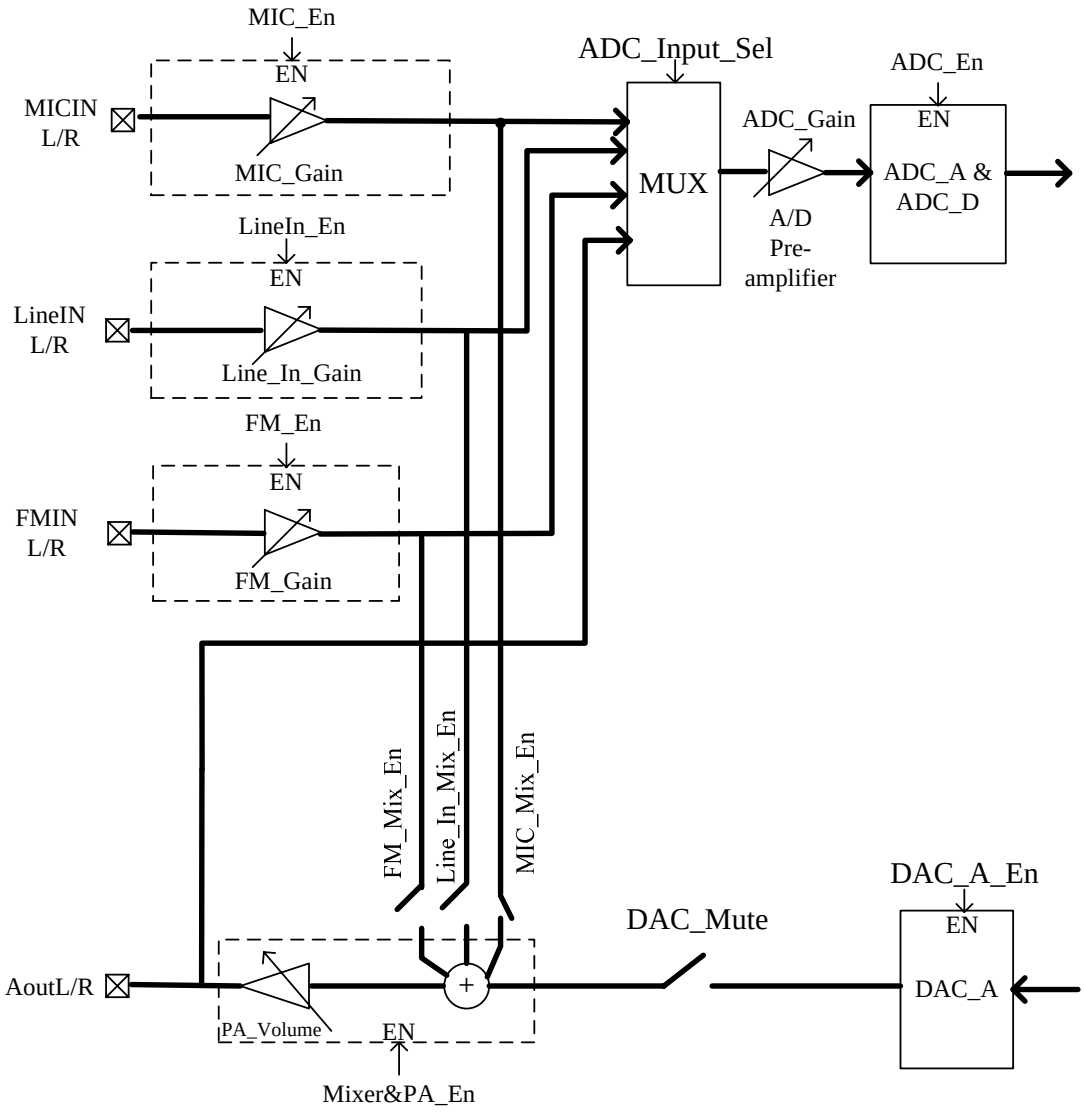
Features:

- Build in Stereo 20-bit Sigma-Delta DAC
- Build in Stereo 21-bit Sigma-Delta ADC
- Build in Stereo Headphone driver

- Support sample rate of 8/12/11.05/16/22/24/32/44.1/48k
- Support Microphone/FM /Line Input to ADC
- Support 20mW output to drive 16ohm earphone

17.2 ADDA Analog Diagram

ADDA Analog diagram



17.3 DAC

The audio DAC is an on-chip Sigma-Delta Modulator, a high performance DAC is composed of it. The DAC interface support 8-level play back FIFO and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256×FS clock for over-sampling, while 24MHz supports 48K/32K/24K/16K/12K/8KHz with 256×FS for over-sampling.

17.4 ADC

The audio ADC is an on-chip Sigma-Delta Analog-to-Digital Converter, which support input from MIC or external FM or LINEIN. The ADC interface support 16-level FIFO and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256×FS clock for over-sampling, while 24MHz supports 48K/32K/24K/16K/12K/8KHz with 256×FS for over-sampling.

18 GPIO/MULTIFUNCTION

18.1 Description

There are totally 45 GPIOs which can be used as output/input separately or simultaneously. Each GPIO is used as a multifunction with other function pin. Set the relevant register before using the needed function.

Features:

- 45 GPIOs which can be used as output/input separately or simultaneously
- Different level of static driving current and dynamic driving capacity
- Maximum frequency of GPIOs up to 30MHz
- Flexible alternation of multifunction, especially in SD/MMC/MS module

18.2 Register Description

GPIO/MFP includes such registers as follow:

Address	Name	Description
0xEE	MFPSEL	MFP Select Register
0xED	GPIOAOUTEN	GPIOA Output Enable
0xEF	GPIOAINEN	GPIOA Input Enable
0xF0	GPIOADAT	GPIOA Data
0xF1	GPIOBOUTEN	GPIOB Output Enable
0xF2	GPIOBINEN	GPIOB Input Enable
0xF3	GPIOBDAT	GPIOB Data
0xF4	GPIOCOUTEN	GPIOC Output Enable
0xF5	GPIOCINEN	GPIOC Input Enable
0xF6	GPIOCDAT	GPIOC Data
0xF7	GPIODOUTEN	GPIOD Output Enable
0xF8	GPIODINEN	GPIOD Input Enable
0xF9	GPIODDAT	GPIOD Data
0xFA	GPIOEOUTEN	GPIOE Output Enable
0xFB	GPIOEINEN	GPIOE Input Enable

0xFC	GPIOEDAT	GPIOE Data
0xFD	GPIOFOUTEN	GPIOF Output Enable
0xFE	GPIOFINEN	GPIOF Input Enable
0xFF	GPIOFDAT	GPIOF Data

18.2.1 MFP Select Register

MFPSEL (**Multi Function Pin Select Register**, 0EEh)

Bits	Description	Access	Reset
7	GPIO_A1, GPIO_A[4:3], GPIO_C[1:0] and ICE multifunction 0: ICE Port 1: GPIO_A1, GPIO_A[4:3], GPIO_C[1:0]	R/W	0
6	GPIOB7 and RB2- multifunction 0: RB2- 1: GPIOB7	R/W	0
5	GPIOB6 and RB1- multifunction 0: RB1- 1: GPIOB6	R/W	0
4	GPIOB5 and CLE multifunction 0: CLE 1: GPIOB5	R/W	0
3	GPIOB4 and ALE multifunction 0: ALE 1: GPIOB4	R/W	0
2	GPIOB3 and MWR- multifunction 0: MWR- 1: GPIOB3	R/W	0
1	GPIOB2 and MRD- multifunction 0: MRD- 1: GPIOB2	R/W	0
0	GPIOD[7:0] and DATA multifunction 0: DATA BUS 1: GPIOD[7:0]	R/W	0

18.2.2 GPIO_A Output Enable Register

GPIOAOUTEN (**GPIO_A Output Enable Register**, 0EDh)

Bits	Description	Access	Reset
7	GPIO_A7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_A6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_A5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_A4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_A3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_A2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_A1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_A0 Output enable, 0: Disable, 1: Enable.	R/W	0

18.2.3 GPIO_A Input Enable Register

GPIOAINEN (**GPIO_A Input Enable Register**, 0EFh)

Bits	Description	Access	Reset
7	GPIO_A7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_A6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_A5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_A4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_A3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_A2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_A1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_A0 Input enable, 0: Disable, 1: Enable.	R/W	0

18.2.4 GPIO_A Data Output/Input Register

GPIOADAT (**GPIO_A Data Output/Input Register**, 0F0h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

18.2.5 GPIO_B Output Enable Register

GPIOBOUTEN (**GPIO_B Output Enable Register**, 0F1h)

Bits	Description	Access	Reset
7	GPIO_B7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_B6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_B5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_B4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_B3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_B2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_B1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_B0 Output enable, 0: Disable, 1: Enable.	R/W	0

18.2.6 GPIO_B Input Enable Register

GPIOBINEN (**GPIO_B Input Enable Register**, 0F2h)

Bits	Description	Access	Reset
7	GPIO_B7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_B6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_B5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_B4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_B3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_B2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_B1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_B0 Input enable, 0: Disable, 1: Enable.	R/W	0

18.2.7 GPIO_B Data Output/Input Register

GPIOBDAT (**GPIO_B Data Output/Input Register**, 0F3h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

18.2.8 GPIO_C Output Enable Register

GPIOCOUTEN (**GPIO_C Output Enable Register**, 0F4h)

Bits	Description	Access	Reset
7	GPIO_C7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_C6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_C5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_C4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_C3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_C2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_C1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_C0 Output enable, 0: Disable, 1: Enable.	R/W	0

18.2.9 GPIO_C Input Enable Register

GPIOCINEN (**GPIO_C Input Enable Register**, 0F5h)

Bits	Description	Access	Reset
7	GPIO_C7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_C6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_C5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_C4 Input enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_C3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_C2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_C1 Input enable, 0: Disable, 1: Enable.	R/W	0

0	GPIO_C0 Input enable, 0: Disable, 1: Enable.	R/W	0

18.2.10 GPIO_C Data Output/Input Register

GPIOCDAT (**GPIO_C Data Output/Input Register**, 0F6h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

18.2.11 GPIO_D Output Enable Register

GPIODOUTEN (**GPIO_D Output Enable Register**, 0F7h)

Bits	Description	Access	Reset
7	GPIO_D7 Output enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_D6 Output enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_D5 Output enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_D4 Output enable, 0: Disable, 1: Enable.	R/W	0
3	GPIO_D3 Output enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_D2 Output enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_D1 Output enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_D0 Output enable, 0: Disable, 1: Enable.	R/W	0

18.2.12 GPIO_D Input Enable Register

GPIODINEN (**GPIO_D Input Enable Register**, 0F8h)

Bits	Description	Access	Reset
7	GPIO_D7 Input enable, 0: Disable, 1: Enable.	R/W	0
6	GPIO_D6 Input enable, 0: Disable, 1: Enable.	R/W	0
5	GPIO_D5 Input enable, 0: Disable, 1: Enable.	R/W	0
4	GPIO_D4 Input enable, 0: Disable, 1: Enable.	R/W	0

3	GPIO_D3 Input enable, 0: Disable, 1: Enable.	R/W	0
2	GPIO_D2 Input enable, 0: Disable, 1: Enable.	R/W	0
1	GPIO_D1 Input enable, 0: Disable, 1: Enable.	R/W	0
0	GPIO_D0 Input enable, 0: Disable, 1: Enable.	R/W	0

18.2.13 GPIO_D Data Output/Input Register

GPIODDAT (**GPIO_D Data Output/Input Register**, 0F9h)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

18.2.14 GPIO_E[4:0] Output Enable Register

GPIOEOUTEN (**GPIO_E[4:0] Output Enable Register**, 0FAh)

Bits	Description	Access	Reset
7:6	0 0 reserved 0 1 reserved 1 0 GPIOE4 Output LOSC. 1 1 GPIOE4Output HOSC. If bit7 is set, GPIOE4 can only output OSC.	R/W	0
5	Reserved	R/W	0
4	GPIO_E4 Output Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_E3 Output Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_E2 Output Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_E1 Output Enable, 0: Disable, 1: Enable	R/W	0
0	GPIO_E0 Output Enable, 0: Disable, 1: Enable	R/W	0

18.2.15 GPIO_E[4:0] Input Enable Register

GPIOEINEN (**GPIO_E[4:0] Input Enable Register**, 0FBh)

Bits	Description	Access	Reset
7:5	Reserved	/	/
4	GPIO_E4 Input Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_E3 Input Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_E2 Input Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_E1 Input Enable, 0: Disable, 1: Enable	R/W	0
0	GPIO_E0 Input Enable, 0: Disable, 1: Enable	R/W	0

18.2.16 GPIO_E[4:0] Data Output/Input Register

GPIOEDAT (**GPIO_E[4:0] Data Output/Input Register**, 0FCh)

Bits	Description	Access	Reset
7:5	Reserved	/	/
4:0	Output/Input Data[4:0]	R/W	xxh

18.2.17 GPIO_F [7:0] Output Enable Register

GPIOFOUTEN (**GPIO_F[7:0] Output Enable Register**, 0FDh)

Bits	Description	Access	Reset
7	GPIO_F7 Output Enable, 0: Disable, 1: Enable	R/W	0
6	GPIO_F6 Output Enable, 0: Disable, 1: Enable	R/W	0
5	GPIO_F5 Output Enable, 0: Disable, 1: Enable	R/W	0
4	GPIO_F4 Output Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_F3 Output Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_F2 Output Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_F1 Output Enable, 0: Disable, 1: Enable。	R/W	0
0	GPIO_F0 Output Enable, 0: Disable, 1: Enable	R/W	0

18.2.18 GPIO_F[7:0] Input Enable Register

GPIOFINEN (**GPIO_F[7:0] Input Enable Register**, 0FEh)

Bits	Description	Access	Reset
7	GPIO_F7 Input Enable, 0: Disable, 1: Enable	R/W	0
6	GPIO_F6 Input Enable, 0: Disable, 1: Enable	R/W	0
5	GPIO_F5 Input Enable, 0: Disable, 1: Enable	R/W	0
4	GPIO_F4 Input Enable, 0: Disable, 1: Enable	R/W	0
3	GPIO_F3 Input Enable, 0: Disable, 1: Enable	R/W	0
2	GPIO_F2 Input Enable, 0: Disable, 1: Enable	R/W	0
1	GPIO_F1 Input Enable, 0: Disable, 1: Enable	R/W	0
0	GPIO_F0 Input Enable, 0: Disable, 1: Enable	R/W	0

18.2.19 GPIO_F[7:0] Data Output/Input Register

GPIOFDAT (**GPIO_F[7:0] Data Output/Input Register**, 0FFh)

Bits	Description	Access	Reset
7:0	Output/Input Data[7:0]	R/W	xxh

18.2.20GPIOE0_VCCOUT Select Register

GPIOE0_VCCOUTSR (GPIOE0_VCCOUT Select Register，088h)

Bits	Description	Access	Reset
7:2	Reserved	/	/
1	VCCOUT is used for FM power supply. 0: VCCOUT pin floating, no power out 1: VCCOUT=2.89V, There is a LDO from VCC to VCCOUT. If there is a capacitance at VCCOUT, you should wait a moment after set this bit to 1.	R/W	0
0	GPIOE0 as a multi pin, it can use as VCCOUT for FM power supply. 0: GPIOE0 is used as MS_BS or GPIOE0 1: GPIOE0 is used as VCCOUT	R/W	0

19 PWM

19.1 Introduction

PWM output module is embedded in ATS250X, in the purpose of controlling the external backlight IC conveniently. It supplies several output frequency and variable duty occupancy for adjusting the intensity of the LCD backlight.

Features:

- 2 selected sources :24M or 32K
- Frequency dividing maximum to 4
- Available frequency in end are 94K, 47K, 24K, 12K, 1K, 500Hz, 250Hz, 125Hz
- 8 levels duty occupancy adjusting
- High level or low level active selecting

19.2 Register Description

Address	Name	Description
AFH	PWMCTL	PWM Control Register

PWMCTL (PWM Control Register, AFh)

Bits	Description	Access	Reset
7	**PWM Enable.** 0:Disable the PWM module 1:Enable the PWM module Note: when Enable the PWM Module, the GPIOC0 is used as the PWM pin, if disabled, the GPIOC0 is used as GPIOC0 or I2C_SCK	R/W	0
6	**Source Select.** 0: Choose 24Mhz as dividing source 1: Choose 32KHz as dividing source	R/W	1

5:4	**Frequency Divide.** Choose the divisor for dividing Dividing Source 94K 1K 00: /1 94K 1K 01: /2 47K 500Hz 10: /4 24K 250Hz (recommened) 11: /8 12K 125Hz	R/W	10
3	**Active Polarity Select.** 0:The PWM is High level active 1:The PWM is Low level active	R/W	0
2:0	**Active Duty Occupancy.** 000: 0/8 001: 1/8 010: 2/8 011: 3/8 100: 4/8 101: 5/8 110: 6/8 111: 7/8	R/W	100

20 Power Management Unit

20.1 Introduction

ATS250X integrates a comprehensive power supply subsystem, including the following features:

- Supports two battery types: 1-cell alkaline and Li-Ion batteries, selected by PWRM pin.
- Two integrated DC-DC converters: VDD and VCC. VDD can work in boost mode from 1-cell alkaline, or work in buck mode from Li-ion cell, which supplies Core Power. Another can only work in boost mode from 1-cell alkaline, which supplies I/O Power.
- Fiver linear regulators supply power directly from DC5V or Li-Ion cell. The outputs are VCC, VDD, AVCC, AVDD and VCCOUT. AVCC and AVDD supply analog power.
- Linear battery charger for Li-Ion cell.
- Battery voltage monitor, system monitors for temperature and wire-controller.
- ATS250X power supply is designed to offer maximum flexibility and performance, while minimizing external component requirements.

20.2 Application Diagram

Figure 20-1 and Figure 20-2 show the two outputs VCC and VDD for the two supported battery types. Table 20-1 lists power supply modes in which VCC/VDD how to work.

These three figures and the table can be used to understand how to set hardware connection relate to which subsystems, but they are not intended to be a complete architecture description.

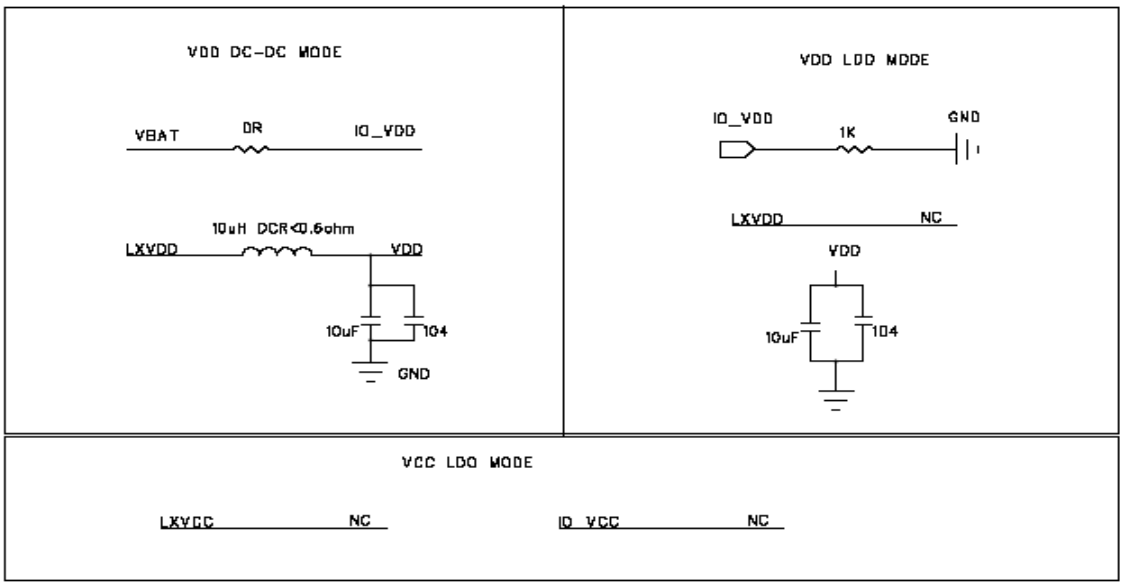


Figure 20-1: Li-Ion Supply Peripheral Connection Diagram

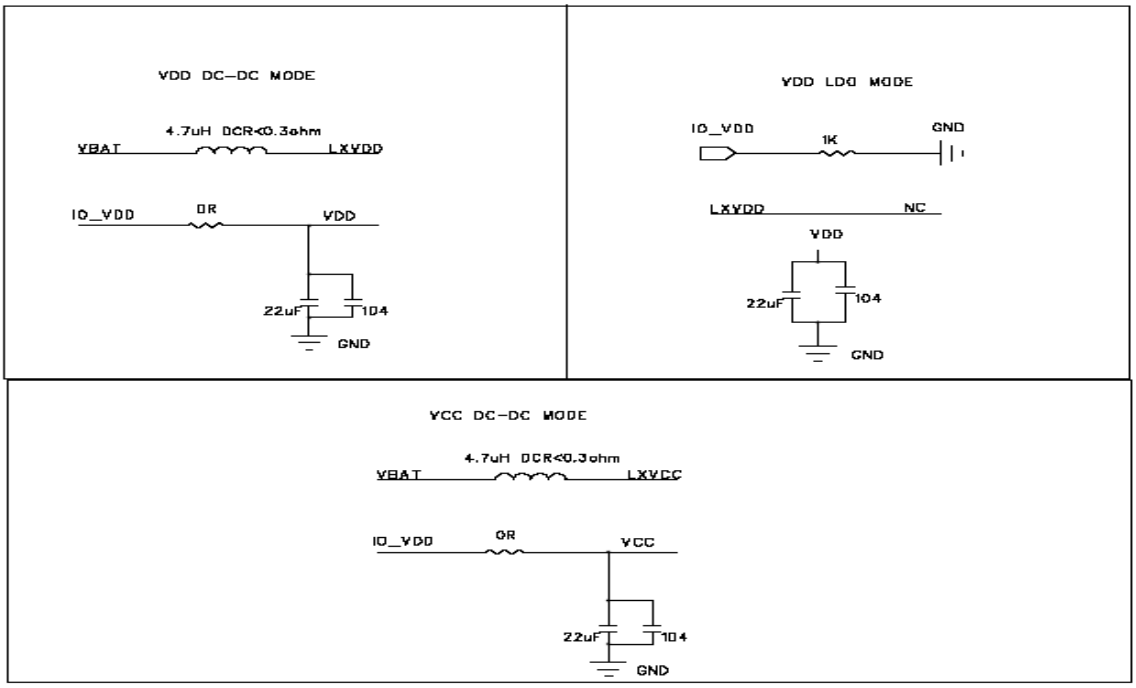


Figure 20-2: 1-Cell Alkaline Supply Peripheral Connection Diagram

Table 20-1: Power Supply Mode

Description	PWRM	DC5V>4.3V	DCDC_VCC	VCC Regulator	DCDC_VDD	VDD Regulator

1 Alkaline, 2 Inductor	0	N	Y, Boost	N	Y, Boost	N
1 Alkaline, 1 Inductor for VCC	0	N	Y, Boost	N	N	Y, From VCC
Li-ION, 1 Inductor for VDD	1	N	N	Y, From VBAT	Y, Buck	N
Li-ION, 2 Regulators	1	N	N	Y, From VBAT	N	Y, From VCC
USB or Adapter, 2 Regulators	X	Y	N	Y, From DC5V	N	Y, From VCC

20.3 DC-DC Converters

The DC-DC converter efficiently scales battery voltage to the required supply voltages. The DC-DC converters include several advanced features:

1. Flexible battery support for either 1-cell alkaline or Li-Ion batteries
2. Synchronization DC-DC converter architecture
3. Programmable output voltages
4. Programmable brownout detection thresholds
5. Work in Pulse Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) automatically for different load current.

20.3.1 DC-DC Output Voltage Setting

ATS250X DC-DC converter enables a low-power system and features programmable output voltages and control modes. Most products adjust VDD dynamically to provide the minimum voltage required for proper system operation.

VCC/VDD are typically set once during system initialization.

20.3.2 DC-DC Accurate and Maximum Output Current

The output voltages are highly precise within ±2%, They provide large currents with a significantly small dropout voltage within ±5%. Table20-2 shows data of maximum output

current.

Table 20-2: DC-DC Maximum Output Current

Block name		Loading
VCC DC-DC(boost mode)		BAT=1.0V, 85mA @ VCC=3.1V dropping 5% BAT=1.2V, 120mA @ VCC=3.1V dropping 5%
VDD DC-DC	boost mode	BAT=1.0V, 60mA @ VDD=1.7V dropping 5% BAT=1.2V, 80mA @ VDD=1.7V dropping 5%
	buck mode	BAT=3.4V, 80mA @ VDD=1.7V dropping 5%

20.3.3 DC-DC Converter Efficiency

Figure20-3 to Figure20-5 show data of typical efficiencies of the DC-DC converters under nominal conditions.

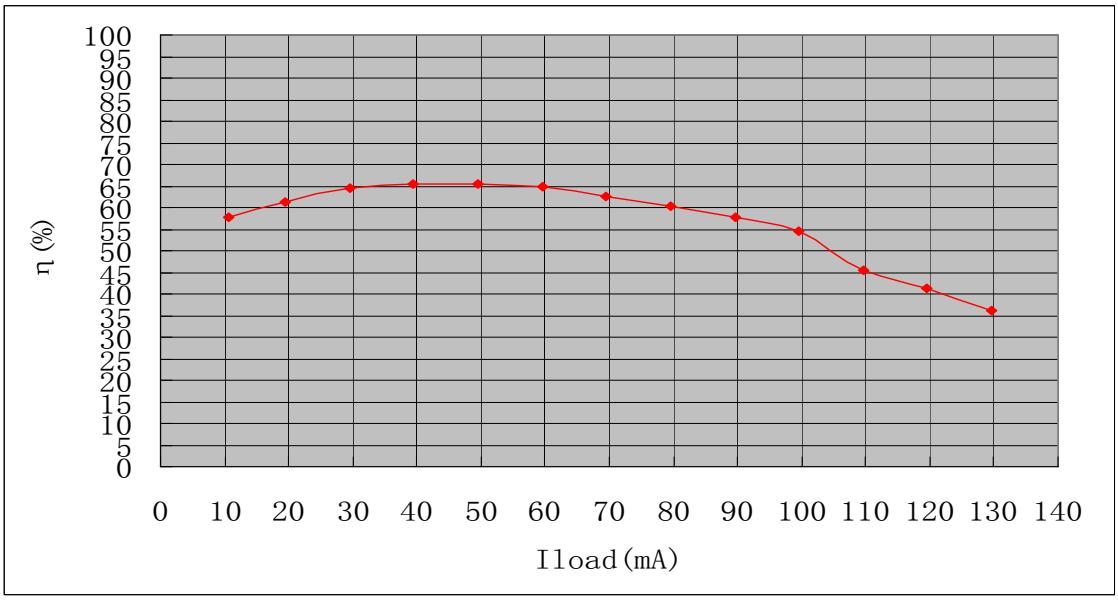


Figure 20-3: 1-Cell Alkaline Supply VCC Efficiency

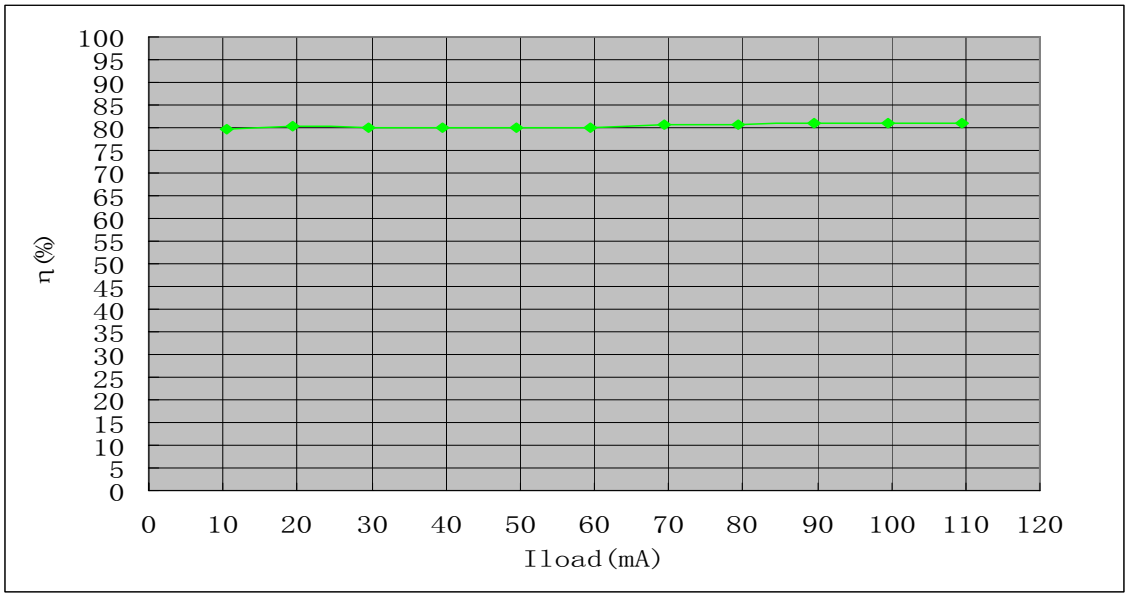


Figure 20-4: 1-Cell Alkaline Supply VDD Efficiency

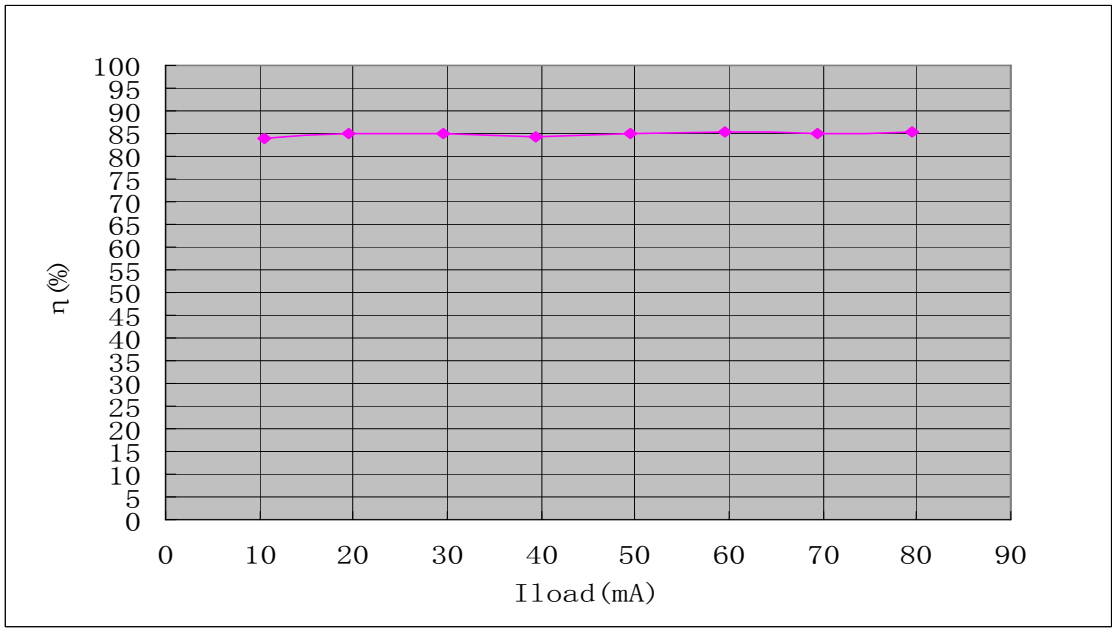


Figure 20-5: Li-Ion Supply VDD Efficiency

20.4 Linear Regulators

ATS250X integrates five linear regulators; they generate VCC, VDD, AVCC, AVDD and VCCOUT.

Linear regulators are typically used when the system is powered from a 5-V supply or USB.

If IO_VDD is pull down with 1KΩ to GND, the VDD regulator is active; If PWMR is high, VCC regulator is active.

20.4.1 Regulators Output Voltage Set

The output voltage setting of VCC and VDD linear regulators is the same as DC-DC converter, showing on section 20.4.1 DC-DC Output Voltage Set.

AVCC/AVDD are typically set once during system initialization, AVCC=2.85V, AVDD=1.7V. The output voltage of AVCC and AVDD linear regulators changes along with VCC and VDD

If VCCOUT is enable , its voltage is 2.89V.

20.4.2 Regulators Accurate and Maximum Output Current

The output voltages are highly precise within ±2%, They provide large currents with a significantly small dropout voltage within ±5%. Table20-3 shows data of maximum output current.

Table 20-3: Regulators Maximum Output Current

Block name	Loading
VCC Regulator	BAT=3.4V or DC5V=4.5V, 200mA @ VCC=3.1V, ↓5%
VDD Regulator	VCC=3.1V, 80mA @ VDD=1.7V, ↓5%
AVCC Regulator	VCC=3.1V, 50mA @ AVCC, ↓2%
AVDD Regulator	VCC=3.1V, 10mA @ AVDD, ↓5%
VCCOUT	VCC=3.1V, 30mA @ VCCOUT, ↓5%

20.5 Li-Ion Cell Charger

Some products in ATS250X family integrate charging for Li-Ion battery from a 5-V source connected to the DC5V pin. The battery charger is essentially a linear regulator that has current and voltage limits. Charge current is software-programmable. You can enable or disable charger by soft setting.When the voltage of DC5V is lower than 3.75V or VBAT and keeping 16ms at least, the charger circuit is disable automatically.

Li-Ion batteries can be charged at the lower of 1C, 500 mA, or the DC5V current limit. USB charging is typically limited to 500 mA or less to meet compliance requirements. Typical

charge times for a Li-Ion battery are 2 to 3 hours with >90% of the charge delivered.

There is 3 phases through all the charging process: When battery voltage is between 3.0V to4.2V. this phase is called constant current charging phase（CC for short）.At this phase, the charging current is constant and the voltage of battery is going up slowly. When battery voltage is below 3.0V, the charging current is 1/10 of CC, this phase is called trickle charging phase or pre-charge. You can mask trickle charging by soft setting. When battery voltage arrives 4.2V, the battery voltage will be constant, and the charging current is reduced gradually, this phase is called constant voltage phase.（CV for short）.

The battery charge voltage is limited to 4.2 V when the reference voltage is 1.5V. If the reference voltage is changed, the limited voltage is changed corresponding.

The Li-Ion charge is typically stopped when the charging current drops below 7.5% of the constant charge current.

One can programmatically monitor the battery voltage using the BATADC. The charger has its own voltage limiting that operates independently of the BATADC. But monitoring the battery voltage during the charge might be helpful for reporting the charge progress.

The battery charger is capable of generating a large amount of heat within ATS250X, especially at currents above 400 mA. The dissipated power can be estimated as: (5V – battery voltage) * current. At max current (500 mA) and a 3-V battery, the charger can dissipate 1 W.

The LRADC2 can be used to monitor the battery temperature or chip temperature. To ensure that the system operates correctly, it should be monitored every 100 ms. It would be good practice to check the output data of LRADC2 for two consecutive checks. If the battery temperature exceeds 45 C°, then the battery charge current must be reduced or the charger must be stopped.

20.6 A/D Converters

There is a low resolution 7 bit A/D for Battery monitor and temperature monitor, the input voltage range of which is 1.4 to 4.4V at VBAT pin in Li-Ion supply mode, 0.7 to 2.2V at VBAT pin in 1-cell Alkaline supply mode, and 0.7 to 2.2V at LRADC2 pin.

There is a low resolution 6 bit A/D for wire control. The input voltage range of which is 0 to AVCC at LRADC1 pin.The A/D converter's working frequency is 64HZ default.

The impedance between BAT(or LRADC1 or LRADC2) and GND is up to MΩ。

The output data of BATADC can be calculated as the following formula:

LI-ION BATADC:

One LSB= $\frac{4.4-1.4}{2^7} * \frac{Vref}{1.5}$, when battery voltage= Vbat, ADC's data is

n= $\frac{Vbat-1.4*\frac{Vref}{1.5}}{\frac{4.4-1.4}{2^7}*\frac{Vref}{1.5}}$, in which Vref is the reference voltage tested.

For example, if Vref=1.500V, then 1LSB=23.44mV, and the corresponding data from 1.4V to 1.42344V are 00h, the corresponding data from 1.42344V to 1.44688V are 01h/

1AAA BATADC:

One LSB= $\frac{2.2-0.7}{2^7}$ * $\frac{Vref}{1.5}$, when battery voltage=Vbat, ADC's data is n= $\frac{Vbat-0.7*\frac{Vref}{1.5}}{\frac{2.2-0.7}{2^7}*\frac{Vref}{1.5}}$, in which Vref is the reference voltage tested.

For example, if Vref=1.500V, then1LSB=11.72mV, and the corresponding data from 0.7V to 0.7119V are 00h, the corresponding data from 0.71172V to 0.72344V are 01h.

LRADC1:

One LSB= $\frac{AVCC}{2^6}$, when input voltage=V, the corresponding ADC is n= $\frac{V}{\frac{AVCC}{2^6}}$.

For example, if AVCC=2.87V， then 1LSB=44.84mV, and the corresponding data from 0V to 0.04484V are 00h, and the corresponding data from 0.04484V to 0.8968V are 01h.

20.6.1 ADCEN Register

ADEN (A/D Enable register, 08Ch)

Bits	Description	Access	Reset

7	0—1 Alkaline/NIMH 1—Li-ION This bit is read only, which depend on pin PWRM. The default is 0.	R	x
6	Wire-Control A/D IRQ threshold. 0: Low, 0.9*AVCC. When the voltage of LRADC1 pin is lower then 0.9*AVCC, if enable Wire-control A/D IRQ, the IOREG[8DH.bit6] will be pended. 1: High, AVCC. When the voltage of LRADC1 pin is lower then AVCC, if enable Wire-control A/D IRQ, the IOREG[8DH.bit6] will be pended.	R/W	0
5	Wire-Control A/D Enable. 1: Enable 0: Disable.	R/W	0
4	Temperature sensor/Battery A/D enable.1: Enable 0: Disable.	R/W	0
3:0	To Adjust Charger limit voltage, the minimum step is 0.1V. 0000 4.05V 0001 4.06V ..... 1110 4.19V 1111 4.20V The data accuracy is within +/-1%.	R/W	1111

20.6.2 WCTLADC DATA Register

WCTLADC (Wire-Control A/D data register，08Dh)

Bits	Description	Access	Reset
7	Wire-control A/D IRQ Enable. 0: Disable, disable the interrupt of Wire-control A/D 1:Enable, enable the interrupt of Wire-control A/D Wire-control A/D's interrupt voltage could be < AVCC, or <0.9*AVCC, determined by REG[8CH.bit6].	R/W	0
6	Wire-control A/D IRQ Pending. Write 1 will clear this bit. When Wire-control input < IRQ threshold voltage, the pending bit is set to 1.	R/W	0
5:0	Data output of Wire-control A/D converter. Wire-control A/D input voltage range is from 0 to AVCC.*	R	xx

*The relation of LRADC1 voltage and data as follows:

voltage(V)	0~1/64*AVCC	1/64*AVCC~2/64*AVCC	...	62/64*AVCC~63/64*AVCC	63/64*AVCC~AVCC
data	00H	01H	...	3EH	3FH

20.6.3 TEMPADC DATA Register

TEMPADC (temperature sensor input detect DATA register，08Eh)

Bits	Description	Access	Reset
7	External DC5V supply presence 1: External 5V supply is present; 0: External 5V supply is not present. When this bit is 0, it will change to 1 if the voltage of DC5V is higher than 4.3V, then VCC/VDD will be work in internal LDO mode and be supply by DC5V. When this bit is 1, it will change to 0 if the voltage of DC5V is lower than 3.75V or VBAT, VCC/VDD will be supply by battery supply, whether DC-DC work depends on connection of IOVCC/IOVDD.	R	x
6:0	7bit Temp ADC, used for BAT temperature。Temp sensor's Input voltage range is 0.7-2.2V. 1LSB=(2.2-0.7)V/27=11.72mV. *	R	xx

* The relation of TEMP voltage and data as follows:

1AAA supply

If *VREF=1.5V*					
voltage(V)	0.7~(0.7+1LSB)	(0.7+1LSB)~(0.7+2LSB)	...	(2.2-2LSB)~(2.2-1SLB)	(2.2-1LSB)~2.2
data	00H	01H	...	7EH	7FH
If *VREF=k*1.5V*					
voltage(V)	k*0.7~k*(0.7+1LSB)	k*(0.7+1LSB)~k*(0.7+2LSB)	...	k*(2.2-2LSB)~k*(2.2-1SLB)	k*(2.2-1LSB)~k*2.2

data	00H	01H	...	7EH	7FH

20.6.4 BATADC DATA Register

BATADC (Battery voltage detect DATA register，08Fh)

Bits	Description	Access	Reset
7	Reserved	R/W	x
6:0	Battery 7bit Voltage ADC, used to detect Battery voltage。 Input voltage range is: 1AAA: 0.7-2.2V Li-ion: 1.4-4.4V	R	xx

* The relation of battery voltage and data as follows:

1AAA supply:

If *VREF=1.5V*					
voltage(V)	0.7~(0.7+1LSB)	(0.7+1LSB)~(0.7+2LSB)	...	(2.2-2LSB)~(2.2-1SLB)	(2.2-1LSB)~2.2
data	00H	01H	...	7EH	7FH
If *VREF=k*1.5V*					
voltage(V)	k*0.7~k*(0.7+1LSB)	k*(0.7+1LSB)~k*(0.7+2LSB)	...	k*(2.2-2LSB)~k*(2.2-1SLB)	k*(2.2-1LSB)~k*2.2
data	00H	01H	...	7EH	7FH

Li-Ion supply: the voltage above should multiply 2

21 Electrical Characteristics

21.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	1.6	-0.3~2.0	V
	VCC	3.0	-0.3~3.6	V
Input voltage	V_I		-0.3~3.6	V
Storage temperature	T_{stg}	25	-65~150	℃

Note:

1. T_O = 25℃（Operating Temperature）
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

21.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T_O = 25℃, VCC = 0 V.

21.3 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output	V_{OH}	I_{OH} = -6 mA	2.4			V

voltage						
Low-level output voltage	V_{OL}	I_{OL} = 6 mA			0.4	V
High-level input voltage	V_{IH}		0.6*VCC		VCC+0.6	V
Low-level input voltage	V_{IL}		-0.3		0.4*VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V			±5	uA
Tri-State leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V			±3	uA
GPIO Drive	I_{drive3}	GPIO_A4		10		mA
		GPIO_B3		2		
		GPIO_E0		6		

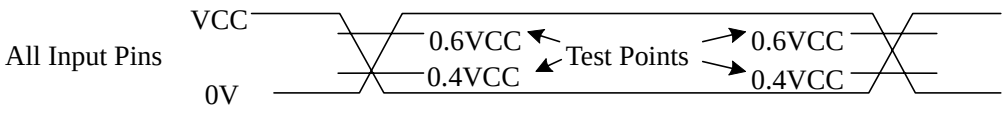
NOTES:

1. T_o = -10 to +70℃, VDD = 1.6 V, VCC = 3.0 V

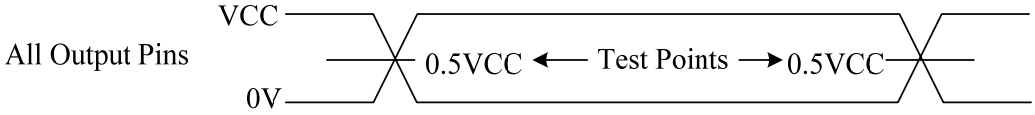
21.4 AC Characteristics

T_o = -10 to +70℃

21.4.1 AC Test Input Waveform

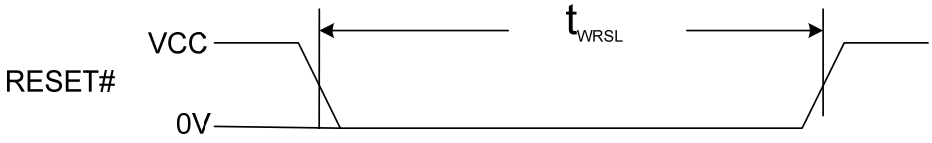


21.4.2 AC Test Output Measuring Points



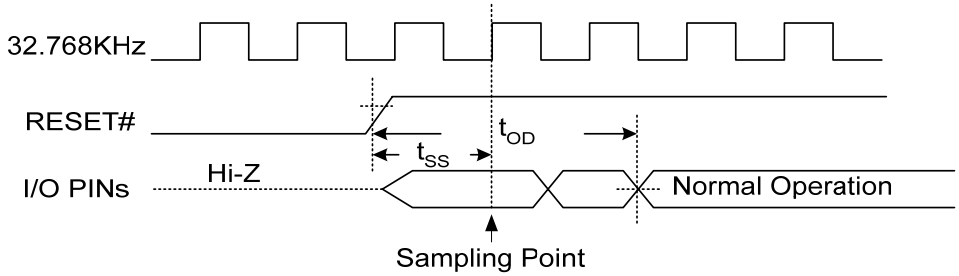
21.4.3 Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	50	—	us



21.4.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}		—	61.04	us
Output delay time (from RESET#)	t_{OD}		61.04	—	us

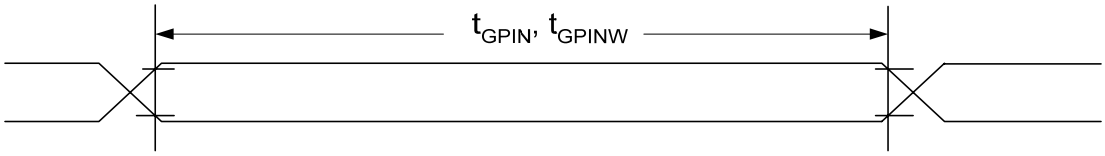


21.4.5 GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$11/f_{mcuclk}$		s
GPIO output rise time	t_{GPRISE}		5	50	ns
GPIO output fall time	t_{GPFALL}		5	50	ns

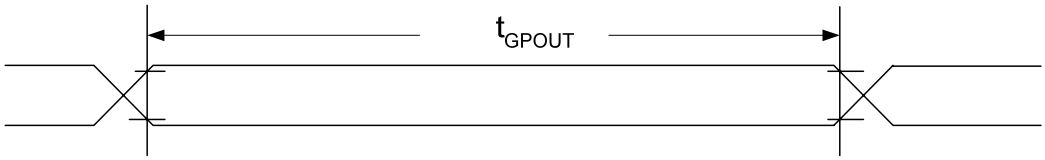
Output level width	t_{GPOUT}		$11/f_{mcuclk}$		s

Notes 1. f_{MCUCLK} is the frequency that MCU is running upon.



Input Level Width

Output Rise/Fall Time

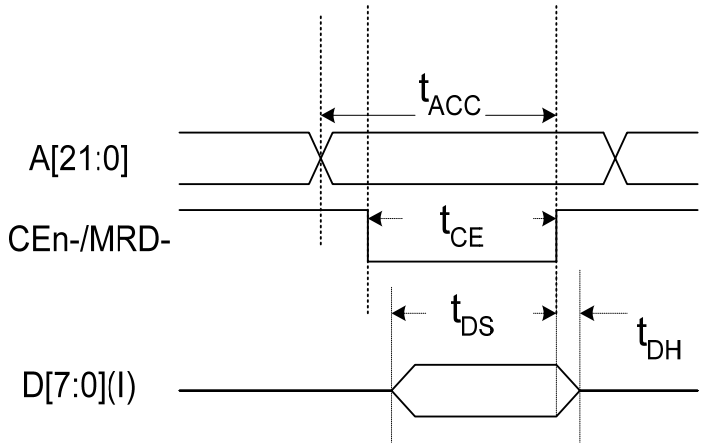


Output Level Width

21.4.6 Ordinary ROM Parameter

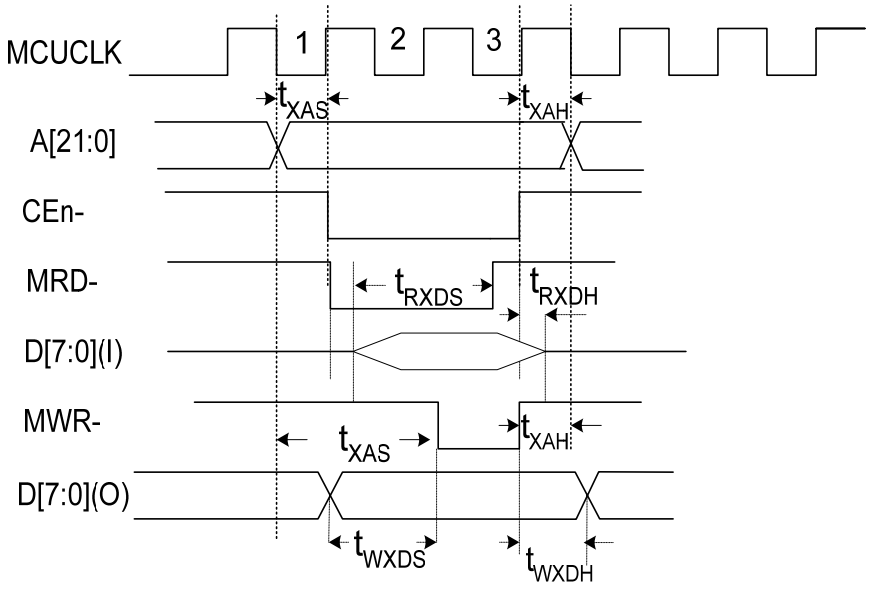
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	90		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	90		ns
Data input setup time	t_{DS}	HOSC=24MHz	40		ns

Data input hold time	t_{DH}	HOSC=24MHz	15		ns



Ordinary ROM

21.4.7 External System Bus Parameter



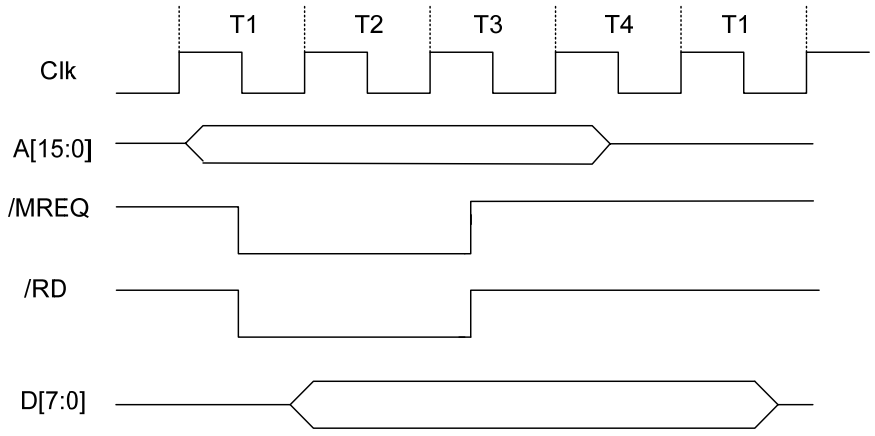
Parameter	Symbol	Condition	MIN.	MAX.	Unit

Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	10		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

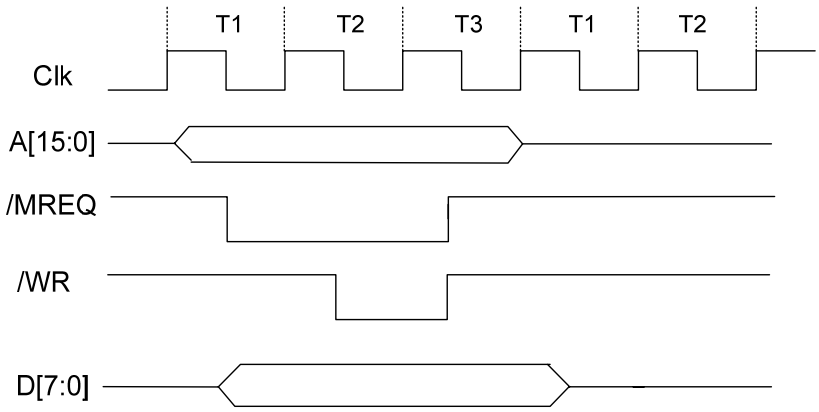
Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

21.4.8 Bus Operation



Memory Read Timing

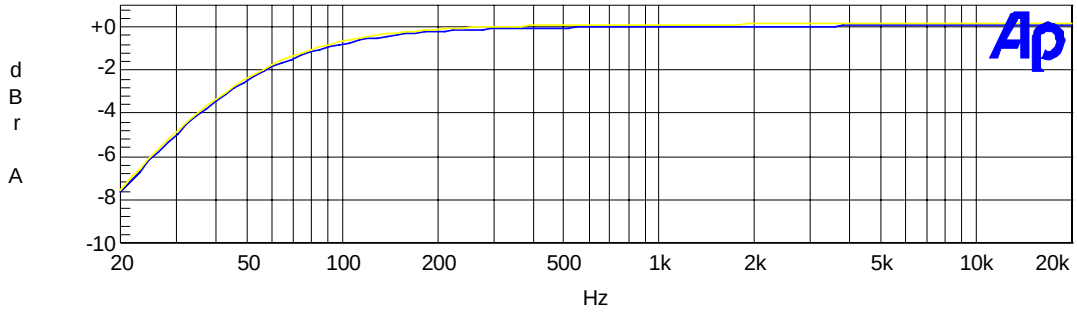


Memory Write Timing

21.4.9 Headphone Driver Characteristics

(T_o =-10 - +70℃, VDD = 1.6 V, VCC = 3.0 V, Sample Rate=32KHz, Volume Level=0x1F)

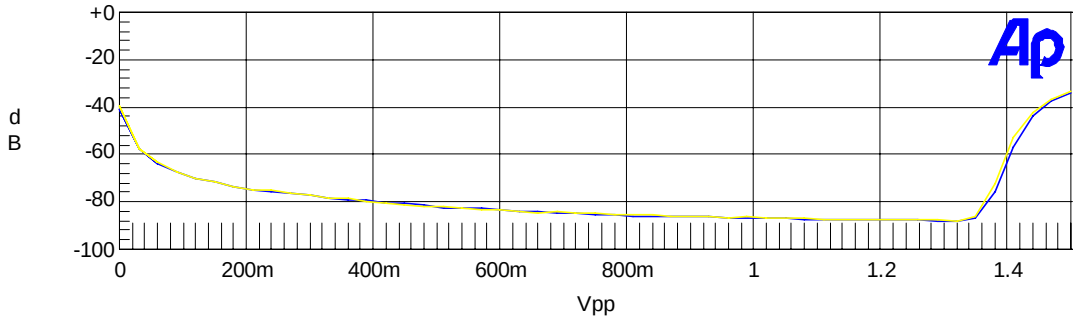
Characteristics	Min	Typ	Max	Unit
Dynamic Range –60 dBFS Input		-87		dB
Total Harmonic Distortion + Noise		-81		dB
Frequency Response 20-20KHz	-7.6	0		dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.3		Vpp
Inter channel Gain Mismatch(1KHz)		-66		dB



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.Level A	Left	
1	3	Yellow	Solid	1	Anlr.Level B	Left	

audio2722.at27

Frequency Response Diagram of Headphone Driver

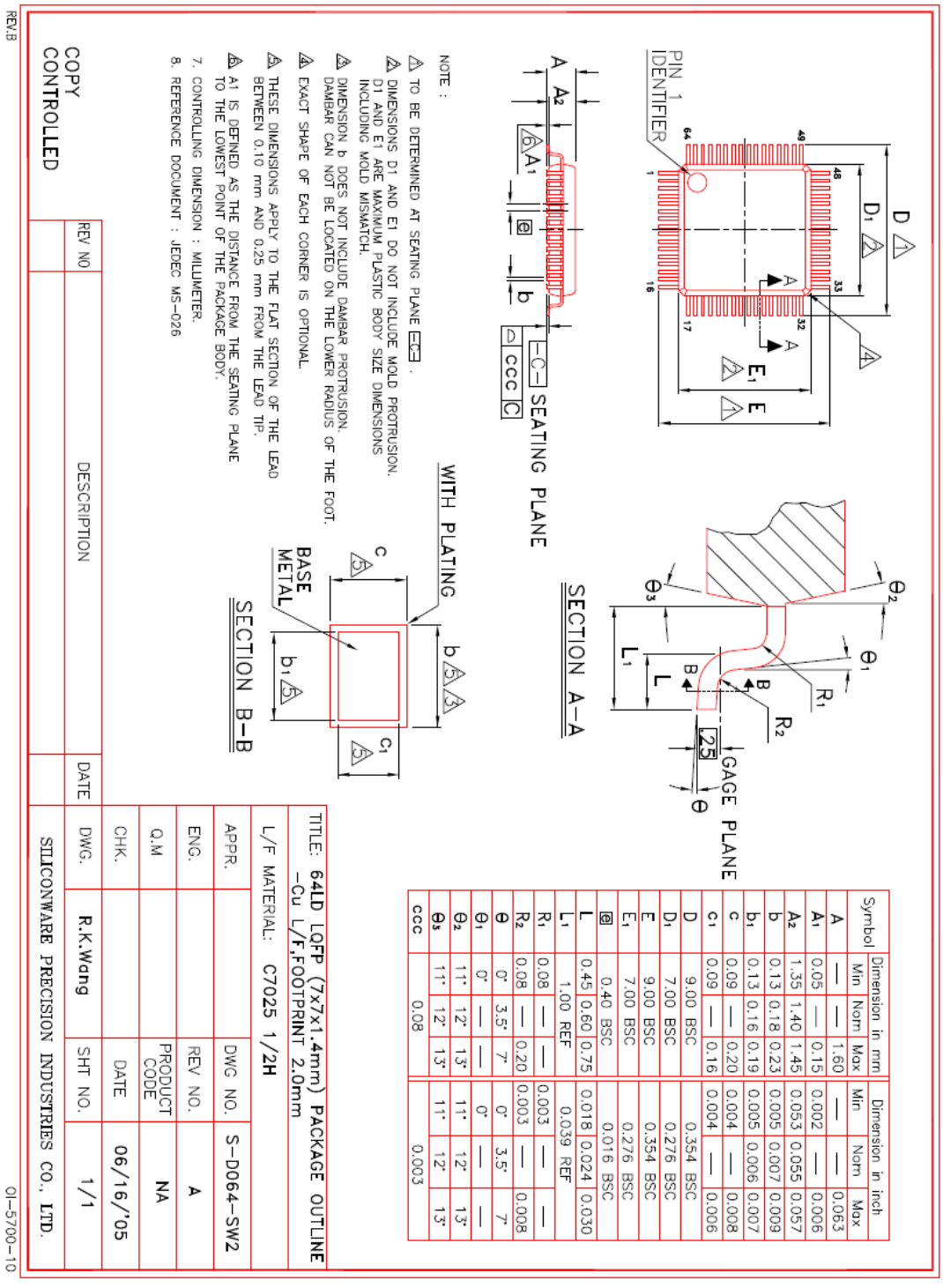


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	
1	2	Yellow	Solid	1	Anlr.THD+N Ratio	Left	

audio2722.at27

THD + N Amplitude Diagram of Headphone Driver

22 Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026

COPY CONTROLLED

REV NO	DESCRIPTION	DATE

TITLE: 64LD LQFP (7x7x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm

L/F MATERIAL: C7025 1/2H

APPR.		DWG NO.	S-D064-SW2
ENG.		REV NO.	A
Q.M		PRODUCT CODE	NA
CHK.		DATE	06/16/'05
DWG.	R.K.Wang	SHT NO.	1/1

SILICONWARE PRECISION INDUSTRIES CO., LTD.

REV.B

OI-5700-10

23 Ordering Information

23.1 Recommended Soldering Conditions

Soldering Conditions for Surface-mount Devices

Soldering Process	Soldering Conditions
Infrared Ray Reflow	Peak package's surface temperature: 235℃ (Lead) or 260℃ (Lead Free)
	Reflow time: 30 seconds or less (210℃or more)—(Lead) or 60 seconds or less (217℃or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note:

The maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution:

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

23.2 Precaution against ESD for Semiconductors

When the strong electric field is exposed to a MOS device, the destruction of the gate oxide may occur and then it can ultimately degrade the device operation. Measures must be taken to stop the generation of static electricity as many as possible, and it is a must to quickly dissipate the static electricity when it occurs. Environmental control must be adequate enough. Humidifier should be used when it is dry. Recommend to avoid using insulators, which may easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container or a static shielding bag or objects made from conductive material. All test and measurement tools including work bench and floor should be grounded. The operator shall be grounded by using wrist strap. Semiconductor devices shall not be touched with bare hands. Similar precautions shall be taken for PW boards with semiconductor devices on it.

23.3 Handling of Unused Input Pins for CMOS

The cause for no connection to CMOS device inputs can be the malfunction. If no connection is provided for the input pins, the possible cause is that an internal input level may be generated due to noise, etc., which results in malfunction. CMOS devices behave differently from Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin shall be connected to VCC or GND with a resistor, if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device and follows the related specifications governing the devices.

23.4 Status before Initialization of MOS Devices

Power-on does not necessarily define the initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned on, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after the power-on.

24 Appendix

24.1 Acronym and Abbreviations

ACK—Acknowledgement
ADC—Analog Digital Convert
ATAIRQ—Advanced Technology Attachment Interrupt Request
CTC—Clock/Timer/Counter
DAC—Digital Analog Convert
DMA—Direct Memory Address
DRQ—Data Request
DST—Destination
DST—Destination
ECC—Error Correction Code
EM—External Memory
FIFO—First In First Out
HIP—Host Interface Port
HOSC—High Frequency Oscillator
IDM—Internal Data Memory
IPM—Internal Program Memory
IRQ—Interrupt Request
IR—Infra-red
LOSC—Low Frequency Oscillator
MIC—Microphone
NAK—Negative Acknowledgement
PLL—Phase Locked Loop
RTC—Real Time Clock
RB—Ready/Busy
SIRQ—System Interrupt Request
SPDIF—Sony/Philips Digital Interface
SPI—Serial Port Interface
SRC—Source
TC—Transmit Complete
UART—Universal Asynchronous Receiver/Transmitter

Actions Semiconductor Co., Ltd.

Address: Bldg.15-1, NO.1, HIT Rd., Tangjia, Zhuhai, Guangdong, China
Tel: +86-756-3392353
Fax: +86-756-3392251
Post Code: 519085
http://www.actions-semi.com
Business Email: mp-sales@actions-semi.com
Technical Service Email: mp-cs@actions-semi.com