ATS2505 Datasheet

Latest Version: 1.0

2010-10-20

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Contents

Revision History

Date	Revision	Description
2010-10-20	1.0	New Release;

1 Introduction

ATS2505 is a single-chip highly-integrated digital music system solution for devices such as dedicated audio players. It includes a high performance dsp with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. ATS2505 also provides an interface nor flash memory, LED/LCD, button and switch inputs, and headphones. It supports WMA and other digital audio standards. ATS2505 also embedded an USB host controller to support the data control and playback audio files on u-disk or portable audio players, alongside with support of SD/MMC card which gives the end customers a luxury of a SD/MMC card plug-and-play element. For devices like USB-Disk, it can act as a USB mass storage slave device to personal computer system. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphones. Thus, ATS2505 provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio and video players.

Feature

Flip80251 Core

- Integrated MCU with EJTAG Debug Unit, the instruction set is compatible with 80C51/8xC251
- A pipelined architecture providing single cycle execution for most of the instructions when the pipeline is full
- MCU run at 24MHz(typ),F/W can program from DC up to 80MHz transparently

Audio and Video Engine

- WMA Decoder, bit rate 32-384Kbps, 8-48KHz
- Digital Voice Recording（ADPCM）
- Integrated Motion JPEG Video Decoder, up to 30fps@QCIF+

Internal memory

- On-chip PRAM251(28K*8) is mapped to MCU program memory space
- On-chp DRAM251A (8K*8), DRAM251B (8K*8) and DRAM251C (2K*8) mapped to MCU data and Stack memory space. And DRAM251B can also be mapped to the Motion Jpeg Decoder.
- On-chip Multi-Use RAM1 (（22K+64)*8bit) that can be switched to be MCU data memory space or Audio hardware codec memory.
- On-chip Multi-Use RAM2(4K*8bit) and PCM RAM (8K*8bit) that can be switched to be MCU program memory space or Audio hardware codec memory.
- On-chip USB RAM(URAM:560*32,B1/B2:1K*8) that can be switched to be MCU data memory space or USB controller memory
- On-chip JPEG RAM(JRAM1/JRAM2: 64*32bit, JRAM3:544*8bit,JRAM4:64*22bit) that can be switched to be MCU data memory space or Motion JPEG Decoder

- Internal (16K+12K)x8 BROM build in Boot up and USB Upgrade firmware and C-library
- Internal (26k+733)*8 ROM (ROM1:3423*24bit,ROM2:7104*16,ROM3:2880*8) for Audio hardware codec memory
- Internal SRAM and BROM can run up to 160MHz， AUDIO ROM can run up to 30MHz.

External Memory Support

- Support Managed NorFLASH
- Support following memory card interface
  .Multi Media Card Specification Version 4.3(1/4-bit mode)
  .Secure Digital Card Specification Version 3.0(1/4-bit mode)
  .Memory Stick Version 1.43(1/4-bit mode)
  .Memory Stick Pro Version 1.02(1/4-bit mode)
- Support Booting up directly from eMMC/SPI NorFlash.

Highly-Integrated System peripherals

- Support 32.768 KHz OSC with on-chip PLL, which can be adjusted to 24MHz through internal circuit.
- Internal 32KHz RC oscillator
- Energy saving with dynamic power management, supporting Li-on only
- USB 2.0 device support
- A variety of serial controllers supporting SPI, UART and I2C.
- Support Remote Control with the internal IRC for decoding
- Support LCM with 8bit CPU Interface.

Audio

- Support FM Radio input and 41 levels volume control
- Support Stereo 16-bit Sigma-Delta A/D for Microphone/FM Input/Line Input, sample rate at 8/12/16/22/24/32/44/48KHz
- D/A+PA SNR :without A weight>91dB
- Build in Stereo 16-bit Sigma-Delta D/A
- A/D SNR >90dB
- Headphone driver output 2x20mW @16ohm

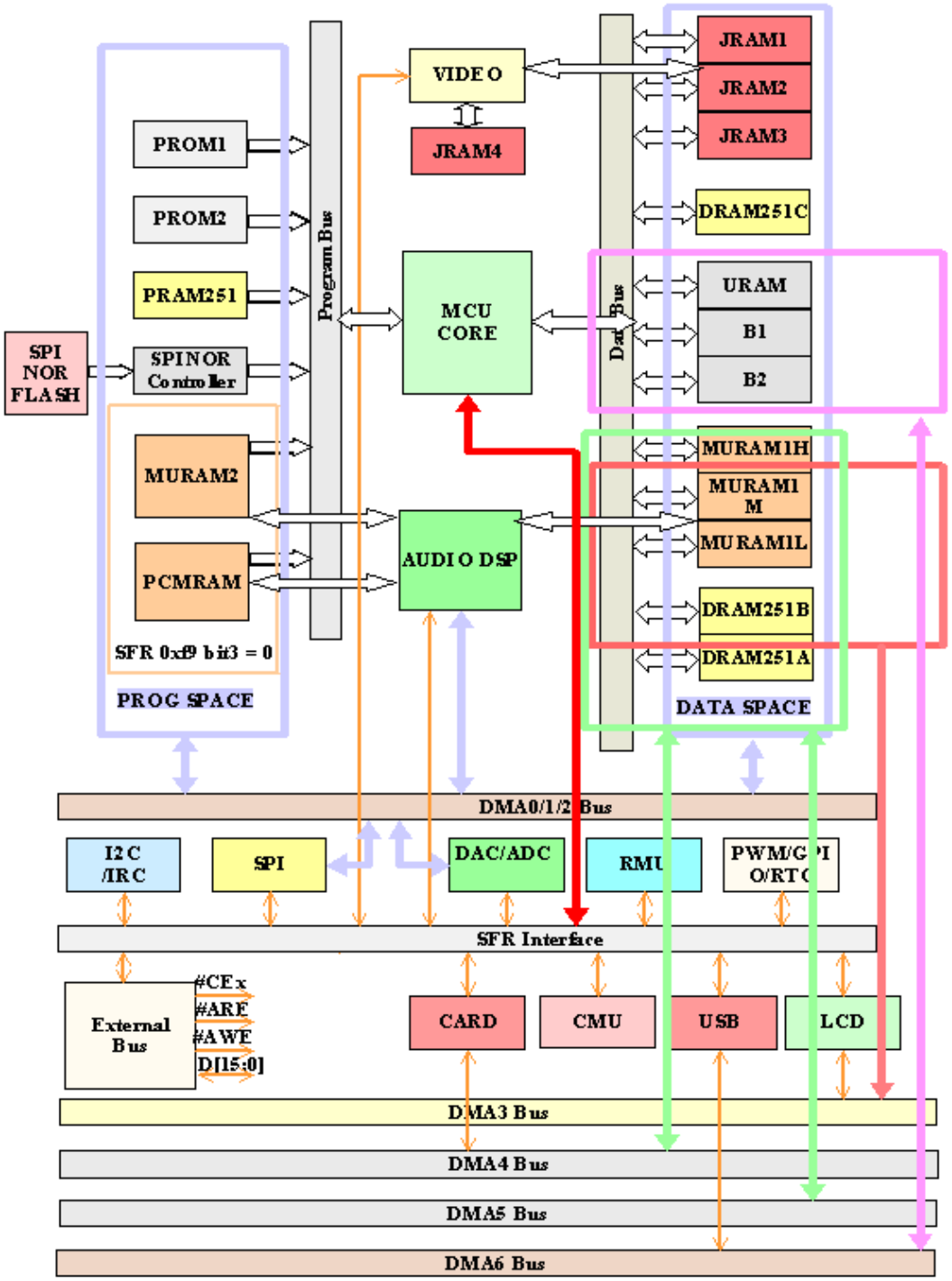
Power

- Operating voltage: I/O 3.3V, Core 1.8V
- Standby Leakage Current: <50uA (VCC and VDD are shut down, while RTCVDD is power on)
- Low Power Consumption: <40mW@1.6V at typical WMA decoder solution

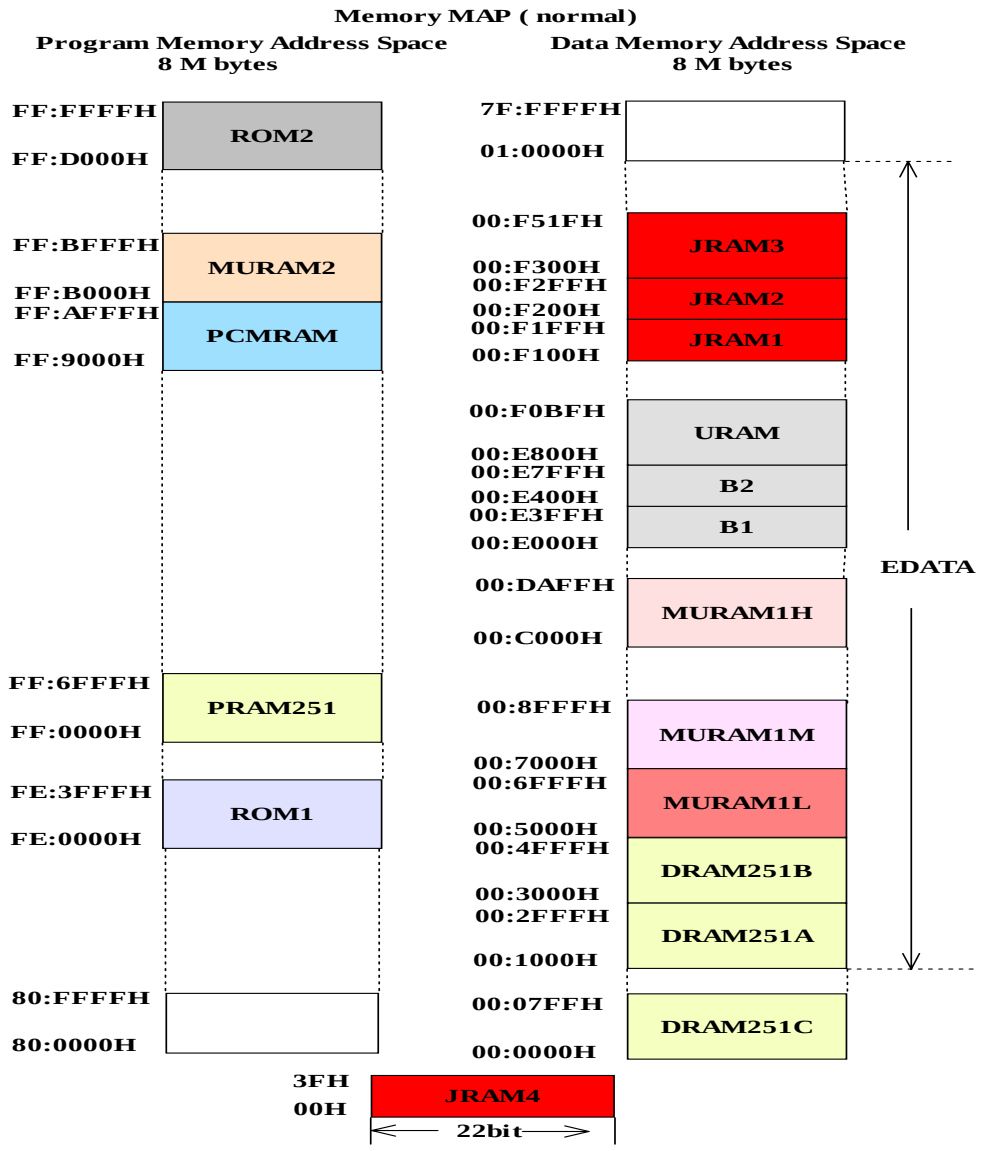
Manufacture

- Package at LQFP-64 (7x7mm)

1.1 Block Diagram



2 Memory Map



3 Register List

The block in red is the all bank registers occupied for the compatibility of dolphin80251 and Intel80251.

	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
0xF8		MBankCtl	NewPage	PageAddr				
0xF0	B							
0xE8	AIE							
0xE0	ACC							
0xD8								
0xD0	PSW	PSW1						
0xC8								
0xC0	AIF							
0xB8							SPH	
0xB0								
0xA8	IE0							
0xA0	P2	MPAGE						
0x98								
0x90							ExWait	
0x88	IF0						CCMCON	CCMVAL
0x80	SFRBANK	SPL	DPL	DPH	DPXL	BIRDINF		PCON

Register List of Each Module

Bank Number	Address in Bank	Mnemonic	Description	General Function
all bank	0xbe	SPH	Stack Pointer high byte	Core register
all bank	0x81	SPL	Stack Pointer low byte	
all bank	0x84	DPXL	Data Pointer extended byte	
all bank	0x83	DPH	Data Pointer high byte	
all bank	0x82	DPL	Data Pointer low byte	
all bank	0xd0	PSW	Program Status Word	
all bank	0xd1	PSW1	Program Status Word1	
all bank	0xe0	ACC	Accumulator	

all bank	0xf0	**B**	B Register	
all bank	0x96	**ExWait**	External bus access wait cycle register	ExBUS
all bank	0x80	**SFR_BANK**	SFR Banking control Register	Switch Bank
all bank	0xa0	**P2**	Port2 Register	Indirect addressing
all bank	0xa8	**IE0**	Interrupt Enable register 0	Interrupt control
all bank	0xe8	**AIE**	Additional Interrupt Enable register	
0x00	0xb7	**IPH0**	Interrupt Priority High register 0	
0x00	0xb8	**IPL0**	Interrupt Priority Low register 0	
0x00	0xf7	**AIPH**	Additional Interrupt Priority High register	
0x00	0xf8	**AIPL**	Additional Interrupt Priority Low register	
all bank	0x88	**IF0**	Interrupt Flag register 0	
all bank	0xc0	**AIF**	Additional interrupt flag register	
0x06	0xd8	**EXTINT**	External Interrupt Control	
all bank	0xf9	**MemBankCtl**	Memory banking control register	Page change management
all bank	0xfa	**NewPageAddr**	New page address register	
all bank	0xfb	**PageAddr**	Current Page Address register	
0x00	0xf5	**BankMissEntryH**	Bank Miss Entry Address High byte	
0x00	0xf6	**BankMissEntryL**	Bank Miss Entry Address Low byte	
0x01	0x90	**DMA0CTL0**	DMA0 Control Register 0	DMA0 register
0x01	0x91	**DMA0SADDR1**	DMA0 Source Address 1 Register	
0x01	0x92	**DMA0SADDR0**	DMA0 Source Address 0 Register	
0x01	0x93	**DMA0DADDR1**	DMA0 Destination Address 1 Register	
0x01	0x94	**DMA0DADDR0**	DMA0 Destination Address 0 Register	
0x01	0x95	**DMA0CTL1**	DMA0 Control Register 1	
0x01	0x97	**DMA0SZH**	DMA0 Transfer Size High Register	
0x01	0x98	**DMA0SZL**	DMA0 Transfer Size Low Register	
0x01	0x99	**DMA0IP**	DMA0 Interrupt Pending register	
0x02	0x90	**DMA1CTL0**	DMA1 Control Register 0	DMA1 register
0x02	0x91	**DMA1SADDR1**	DMA1 Source Address 1 Register	
0x02	0x92	**DMA1SADDR0**	DMA1 Source Address 0 Register	
0x02	0x93	**DMA1DADDR1**	DMA1 Destination Address 1	

			Register	
0x02	0x94	**DMA1DADDR0**	DMA1 Destination Address 0 Register	
0x02	0x95	**DMA1CTL1**	DMA1 Control Register 1	
0x02	0x97	**DMA1SZH**	DMA1 Transfer Size High Register	
0x02	0x98	**DMA1SZL**	DMA1 Transfer Size Low Register	
0x02	0x99	**DMA1IP**	DMA1 Interrupt Pending register	
0x03	0x90	**DMA2CTL0**	DMA2 Control Register 0	DMA2 register
0x03	0x91	**DMA2SADDR1**	DMA2 Source Address 1 Register	
0x03	0x92	**DMA2SADDR0**	DMA2 Source Address 0 Register	
0x03	0x93	**DMA2DADDR1**	DMA2 Destination Address 1 Register	
0x03	0x94	**DMA2DADDR0**	DMA2 Destination Address 0 Register	
0x03	0x95	**DMA2CTL1**	DMA2 Control Register 1	
0x03	0x97	**DMA2SZH**	DMA2 Transfer Size High Register	
0x03	0x98	**DMA2SZL**	DMA2 Transfer Size Low Register	
0x03	0x99	**DMA2IP**	DMA2 Interrupt Pending register	
0x05	0x90	**VOUT_CTL**	VCC/VDD voltage set Register	PMU
0x05	0x91	**VDD_DCDC_CTL**	DCDC Modulation and frequency set Register	
0x05	0x92	**VCC_CURRENT_CTL**	VCC DCDC and LDO current limit set Register	
0x05	0x94	**CHG_CTL**	Charge current and temperature set Register	
0x05	0x95	**CHG_DET**	Charge current and status detect Register	
0x05	0x97	**CHG_ASSISTANT**	Charge terminate voltage and temperature set Register	
0x05	0x9b	**PMUADC_CTL**	ADC frequency and enable Register	
0x05	0x9c	**BATADC_DATA**	BATADC data Register	
0x05	0x9d	**LRADC2_DATA**	LRADC2 data Register	
0x05	0x9e	**LRADC1_DATA**	LRADC1 data Register	
0x05	0xa7	**SYSTEM_CTL_RTCVDD**	System on/off and play/pause time set & LB voltage set Register	
0x05	0xa9	**PRESS_DISPLAY**	SYSON key-press status display Register	
0x06	0x98	**LCD_CTL**	LCD Control Register	LCD_DMA3

0x06	0x99	LCD_IF_CLK	LCD Interface Clock Register	
0x06	0x9a	DMA3_CTL	DMA3 Control Register	
0x06	0x9b	DMA3_SRCADDRH	DMA3 SRC Address High Register	
0x06	0x9c	DMA3_SRCADDRL	DMA3 SRC Address Low Register	
0x06	0x9d	DMA3_CCNTH	DMA3 Column Higher Counter Register	
0x06	0x9e	DMA3_CCNTL	DMA3 Column Lower Counter Register	
0x06	0x9f	DMA3_RCNT	DMA3 Row Counter Register	
0x06	0xa2	GPIOAOUTEN	General Purpose Input Output Group A Output Enable	GPIO
0x06	0xa3	GPIOAINEN	General Purpose Input Output Group A Input Enable	
0x06	0xa4	GPIOADAT	General Purpose Input Output Group A Data	
0x06	0xa5	GPIOBOUTEN	General Purpose Input Output Group B Output Enable	
0x06	0xa6	GPIOBINEN	General Purpose Input Output Group B Input Enable	
0x06	0xa7	GPIOBDAT	General Purpose Input Output Group B Data	
0x06	0xa9	GPIOCOUTEN	General Purpose Input Output Group C Output Enable	
0x06	0xaa	GPIOCINEN	General Purpose Input Output Group C Input Enable	
0x06	0xab	GPIOCDAT	General Purpose Input Output Group C Data	
0x06	0xac	GPIODOUTEN	General Purpose Input Output Group D Output Enable	
0x06	0xad	GPIODINEN	General Purpose Input Output Group D Input Enable	
0x06	0xae	GPIODDAT	General Purpose Input Output Group D Data	
0x06	0xaf	GPIOEOUTEN	General Purpose Input Output Group E Output Enable	
0x06	0xb0	GPIOEINEN	General Purpose Input Output Group E Input Enable	
0x06	0xb1	GPIOEDAT	General Purpose Input Output Group	

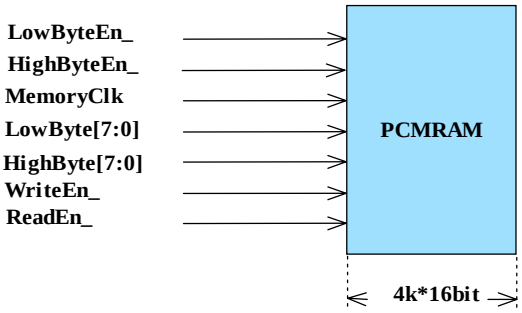
			E Data	
0x06	0xb2	**GPIOFOUTEN**	General Purpose Input Output Group F Output Enable	
0x06	0xb3	**GPIOFINEN**	General Purpose Input Output Group F Input Enable	
0x06	0xb4	**GPIOFDAT**	General Purpose Input Output Group F Data	
0x06	0xc6	**PWMDUTY**	PWM Control Register	
0x06	0xc7	**PWMDIV**	PWM Clock Divide Register	
6,8	0xca	**MFPSEL0**	Multifunction select 0 Register	
6,8	0xcb	**MFPSEL1**	Multifunction select 1 Register	
0x06	0xcc	**MFPSEL2**	Multifunction select 2 Register	
0x06	0xcd	**MFPSEL3**	Multifunction select 3 Register	
0x06	0xce	**MFPSEL4**	Multifunction select 4 Register	
6,8	0xcf	**MFPSEL5**	Multifunction select 5 Register	
0x06	0xd2	**MFPSEL6**	Multifunction select 6 Register	
0x0a	0x99	**SPI_CTL**	SPI Control Register	SPI
0x0a	0x9a	**SPI_DRQ**	SPI DMA/IRQ control Register.	
0x0a	0x9b	**SPI_STA**	SPI Status Register	
0x0a	0x9c	**SPI_CLKDIV**	SPI Clock Divide Control Register	
0x0a	0x9d	**SPI_TXDAT**	SPI TX FIFO register	
0x0a	0x9e	**SPI_RXDAT**	SPI RX FIFO register	
0x0a	0x9f	**SPI_BCL**	SPI Bytes Count Low Register	
0x0a	0xa2	**SPI_BCH**	SPI Bytes Count high Register	
0x0a	0x90	**UART_BR**	UART BAUDRATE Register.	UART
0x0a	0x91	**UART_MODE**	UART mode setup Register.	
0x0a	0x92	**UART_CTL**	UART Control Register.	
0x0a	0x93	**UART_DRQ**	UART DRQ/IRQ register	
0x0a	0x94	**UART_STA**	UART Status Register	
0x0a	0x95	**UART_TXDAT**	UART TX FIFO register	
0x0a	0x97	**UART_RXDAT**	UART RX FIFO register	
0x0a	0xa5	**IR_CTL**	IR Control Register	IR
0x0a	0xa6	**IR_STA**	IR Status Register	
0x0a	0xa7	**IR_LUC**	IR low user code register.	
0x0a	0xa9	**IR_HUC**	IR high user code register.	
0x0a	0xaa	**IR_KDC**	IR key data code register.	
0x01	0x86	**MRCR1**	Module Reset Control Register 1	RMU

all bank	0x87	**PCON**	Power Control	
0x01	0x89	**MRCR2**	Module Reset Control Register 2	
0x01	0x9f	**MRCR3**	Module Reset Control Register 3	

4 On Chip Memory

4.1 Mode of MCU's Access to PCMRAM

PCMRAM is a 16bitX4k single-port synchronous RAM. MCU access PCMRAM in the mode of 8bit.



PCMRAM's Access Interface

4.1.1 MCU's Access to PCMRAM

When accessing PCMRAM in the mode of MCU, LowByteEn_ and HighByteEn_ accessing are enabled at the same time, because MCU's bus is 8bit when it is accessing Memory. If the access address is even, LowByteEn_ is enabled (set as '0'); if odd, HighByteEn_ is enabled (set as '0'). MemoryClk is from the MCU's current working clock.

4.2 Memory Banking Register List

The Base Address of Memory Banking Group

Index	Mnemonic	Description
0xf5	BankMissEntryH	Bank Miss Entry Address High byte
0xf6	BankMissEntryL	Bank Miss Entry Address Low byte
0xf9	MemBankCtl	Memory banking control register
0xfa	NewPageAddr	New page address register
0xfb	PageAddr	Current Page Address register

BankMissEntryH

（Bank Miss Entry Address High byte, sfr address 0xf5, bank :00）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	BankMissEntryH	Bank Miss Entry Address High byte	R/W	00h

BankMissEntryL（Bank Miss Entry Address Low byte, sfr address 0xf6, bank :00）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	BankMissEntryL	Bank Miss Entry Address Low byte	R/W	83h

MemBankCtl（Memory banking control register, sfr address 0xf9, all bank）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:4	Reserved	/	/	/
3	PCMRAM_MURAM2_ADDR	The start address of PCMRAM and MURAM2: 0: FF9000H~FFBFFFH 1: 009000H~00BFFFH	R/W	0
2	InterruptVectorPage	The Interrupt vector's start address is 0fe0000h as a default value. The address 0ff0000h is this bit is set. 0: the interrupt vector start address is 0fe0000h 1: the interrupt vector start address is 0ff0000h	R/W	0
1	Reserved	Be read as zero	-	-
0	MemBankEn	Memory Banking Enable 0: Disable Memory Banking 1: Enable Memory Banking	R/W	0

NewPageAddr（New page address register, sfr address 0xfa, all bank）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	NewPageAddr	New page address register pc[23:16]	R	11111110b

PageAddr（Current Page Address register, sfr address 0xfb, all bank）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	PageAddr	Current Page Address register pc[23:16]	R/W	11111110b

5 PMU

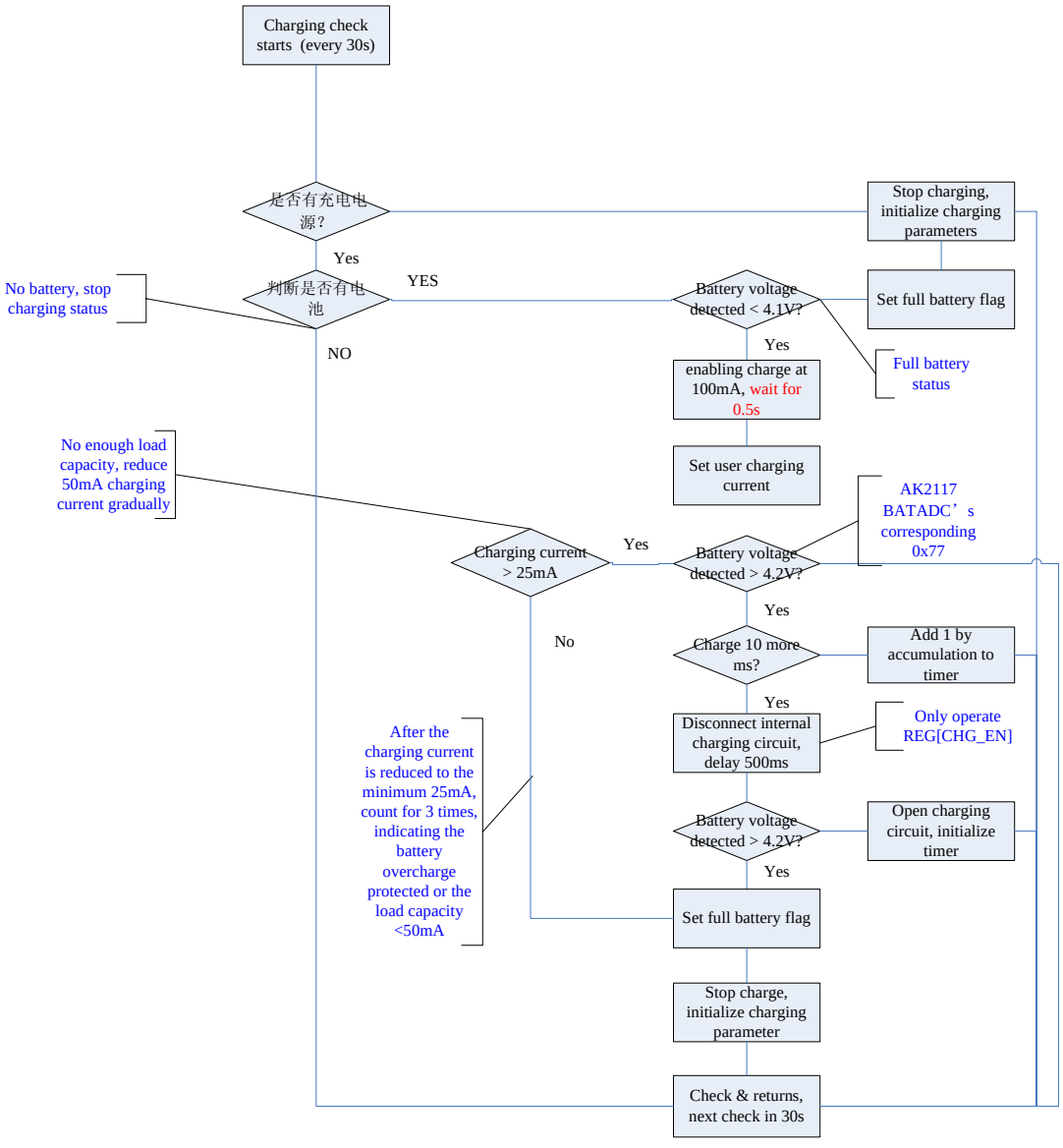
ATS2505 integrates a comprehensive power supply subsystem, including the following features:

- Supports Li-Ion battery power supply
- Five linear regulators supply power directly from DC5V or Li-Ion cell. The outputs are VCC, VDD, AVCC, and FM_VCCOUT. AVCC supply analog power.
- Linear battery charger for Li-Ion cell.
- Low precision A/D converters for Battery voltage monitor, system monitors for temperature and wire-controller.

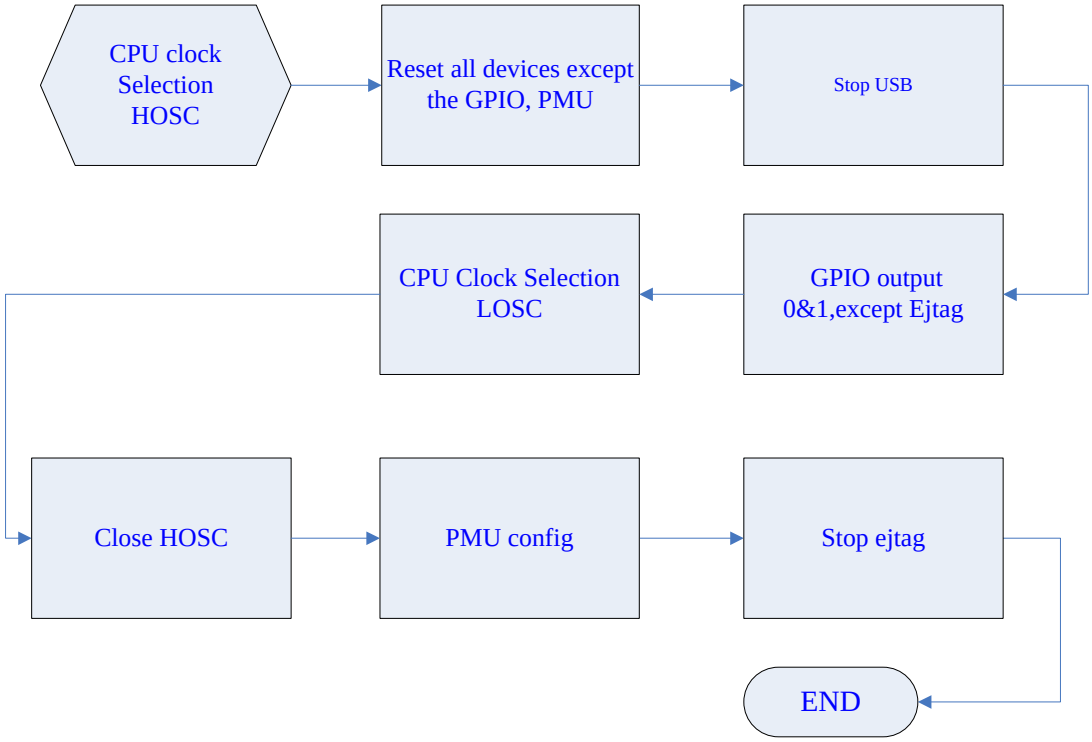
ATS2505 power supply is designed to offer maximum flexibility and performance, while minimizing external component requirements.

5.1 Operation Manual

5.1.1 CHARGER Software Control Flow



5.1.2 Standby Software Control Flow



5.1.3 Power Consumption Management Flow

1. First increase VDD voltage, then MCU/DSP's frequency, first reduce MCU's/DSP's frequency, and then VDD voltage.
2. When entering S3 from S1, it is necessary to check whether long-press status is 1, if long-press status=1, clear long-press status, set REG_ENPMU to 0. Or after clearing long-press status, save some information in the register of RTCVDD, and then set REG_ENPMU as 0.

Note: S1 refers to normal working status, while S3 refers to Soft switch status.

5.2 PMU Register List

The Address of PMU Controller Register Group = SFR:0X90，SFR BANK:0x05.

Index	Mnemonic	Description	Voltage Domain
0x90	VOUT_CTL	VCC/VDD voltage set Register	VDD
0x92	VCC_CURRENT_CTL	VCC LDO current limit set Register	VDD
0x94	CHG_CTL	Charge POWER detect and current set Register	VDD
0x95	CHG_DET	Charge current and status detect Register	VDD
0x97	CHG_ASSISTANT	Charge terminate voltage and temperature set Register	VDD
0x9b	PMUADC_CTL	ADC frequency and enable Register	VDD
0x9c	BATADC_DATA	BATADC data Register	VDD
0x9d	LRADC2_DATA	LRADC2 data Register	VDD
0x9e	LRADC1_DATA	LRADC1 data Register	VDD
0xa4	MULTI_USED	GPIO multi-used set Register	VDD
0xa5	SYSTEM_VOL	System Voltage detect or set Register	VDD
0xa7	SYSTEM_CTL_RTCVDD	System on/off and play/pause time set & LB voltage set Register	RTCVDD
0xa9	PRESS_DISPLAY	SYSON key-press status display Register	VDD

5.3 Register Description

5.3.1 VOUT_CTL

VCC/VDD VOLTAGE SET Register。

（SFR:0x90, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7	-	Reserved	R/W	0
6:4	VCC_SET	VCC voltage level select 000 2.6V 001 2.7V 010 2.8V	R/W	101

		011 2.9V 100 3.0V ***101 3.1V 110 3.2V 111 3.3V		
3:1	VDD_SET	VDD(DC-DC & Regulator) voltage coarse control 000 1.3V 001 1.4V 010 1.5V 011 1.6V **100 1.7V 101 1.8V 110 1.9V 111 2.0V	R/W	100
0	VDD_50 mV	VDD (DC-DC & Regulator) voltage fine control (one control level=50mV); 0: disable; 1: enable	R/W	0

5.3.2 CHG_CTL

Charger Control Register

（SFR:0x94, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7	CHG_POWER	CHG_POWER status: (charging power check and cable in/out check flag bit) 1: has charging power, check cable in. When DC5V's voltage > BAT+0.14V and >3.6V, and the debounce time > 16ms (41us optional), the bit is 1. 0: no charging power, check cable out. When DC5V voltage < BAT+0.07V or < 3.5V, and the debounce time >16ms (41us optional), the bit is 1.	R	x
6	-	Reserved	R/W	0
5	CHG_EN	Enable charge circuit 0: Disable charge circuit.	R/W	0

		1: Enable charge circuit. Charging current grows up as soon as possible, no need to wait. **Must enable USBVDD before using charger.**		
4	TRICKLE_EN	Trickle charging enable: 0: Disable trickle charge. Whether battery voltage is below or up 3.0V, the charging current will be the value setting by CHG_CURRENT 1: Enable trickle charge. When battery voltage is below 3.0V, the charging current is 1/10 of the value setting by CHG_CURRENT	R/W	0
3:0	CHG_CURRENT	Charge current set: **0000 25mA** **0001 25mA** 0010 50mA 0011 100mA 0100 150mA ***0101 200mA 0110 250mA 0111 300mA 1000 350mA 1001 400mA 1010 450mA 1011 500mA Others Reserved Use USB's calibration data of 6.2K resister to adjust charging current.	R/W	101

5.3.3 CHG_DET

Charger detect Register

（SFR:0x95, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7	TEMP_STATUS	Over-temperature display during charging: When the detected temperature of charging pipe > the set value, the bit is set to 1. Decide whether	R	x

		to reduce the charging current or disable charging circuit by this bit.		
6	CHG_TEST	For test only. The bit is for fast test of charge status. When there is charging current, the bit is set to 0 without delay. And for normal application, in order to achieve stable charge status detection, delay shall be made. In this case, this bit cannot be used here, instead, use CHG_STATUS.	R	x
5:4	CHG_PHASE	Charging Phase Status: 0 0: Reserved 0 1: Pre-Charging 1 0: Constant-Current-Charging 1 1 : Constant-Voltage-Charging This two bit will be available Only when bit 7 of this register is set, or will be always read 00. There is 3 phases through all the charging process: Pre-C, CC, CV. These 2bits show which phase the charging at.	R	xx
3:1	CHG_I_DET	Charge Current detect 000....0~30%*I_{chg}, I_{chg} is set by register CHARGER_CTL, indicating that the current charging current is within 30% of the set value. 001....25%~50%I_{chg} 010....50%~75%I_{chg} 011....75%~87%I_{chg} 100.... above 87%I_{chg} Others reserved You can see current charging current by these 3 bits.	R	xxx
0	CHG_STATUS	Charging Status. 0: not charging When current charging current is up to 1/10 of the value which has been set and last for 1 second, this bit will from low to high. 1: charging When current charging current is down to 7.5% of the value which has been set, this bit will from high to low as soon as possible.	R	x

5.3.4 CHG_Assistant

Charge voltage and temperature Control Register

（SFR:0x97, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7:6	–	RESERVED	R/W	01
5:4	CHG_TEM	Charge temperature protection control, set the protection temperature, when the charging circuit's temperation > the set value, issue over-temperature flag, see Charge detect register. 00 100℃ 01 120℃ 10 135℃ 11 150℃ **Mostly influenced by the process.** LQFP-64pin's Theta Ja=49.6℃	R/W	10
3:0	Reserved	Reserved	R/W	1111

5.3.5 PMUADC_CTL

ADC Frequency and enable Control Register

（SFR:0x9b, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7	ADC_FS	AI ADCs Frequency Source Select: All A/D converter's working frequency is 64HZ default; you can raise the working frequency up to 128HZ by setting this bit 0 to consume little power. 0: 64HZ 1: 128HZ	R/W	1
6	BATADC_EN	Temperature sensor/Battery A/D enable. 0: Disable. 1: Enable	R/W	1
5	LRADC1_EN	6bit LRADC1/3/4/5 A/D enable. 0: Disable. 1: Enable	R/W	0
4	LRADC1_IRQ_	Wire-control A/D LRADC1 IRQ Enable.	R/W	0

	EN	0: Disable, shield Wire-control A/D interrupt 1: Enable, enable Wire-control A/D interrupt The interrupt voltage of Wire-control A/D LRADC1 can be lower than AVCC, or lower than 0.9*AVCC, decided by REG[8CH.bit6]. (Realized solely by digital, no Analog)		
3	LRADC1_IRQ_VOL	Wire-Control A/D IRQ threshold Voltage. 0: 0.9*AVCC. When the voltage of LRADC1 pin is lower then 0.9*AVCC, LRADC1 IRQ occur. 1: High, AVCC. When the voltage of LRADC1 pin is lower then AVCC, LRADC1 IRQ occur. (realized together by Analog and digital)	R/W	0
2	LRADC1_PENDING	Wire-control A/D LRADC1 IRQ Pending. Write 1 will clear this bit. When LRADC1's input <IRQ threshold voltage, the pending bit is set to 1. (Realized solely by digital, no Analog)	R/W	0
1:0	–	Reserved	R/W	00

Note: only LRADC1 can send interrupt.

5.3.6 BATADC_DATA

BATADC DATA Register

(SFR:0x9c, SFR bank 0x05)

Bit(s)	Name	Description	R/W	Reset
7	-	Reserved	R	x
6:0	BATADC	Battery 7bit Voltage ADC, used to detect Battery voltage. Input voltage range is: Li-ion: 1.4-4.4V	R	xx

5.3.7 LRADC1_DATA

LRADC1 DATA Register

(SFR:0x9e, SFR bank 0x05)

Bit(s)	Name	Description	R/W	Reset

7:6	–	Reserved	R	xx
5:0	LRADC1	6bit LRADC1's data output LRADC1 input voltage range is from 0 to AVCC.	R	xx

5.3.8 LRADC2_DATA

LRADC2 DATA Register

（SFR:0x9d, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7	–	Reserved	R	x
6:0	LRADC2	7bit LRADC2, used for BAT temperature. Temp sensor's Input voltage range is 0.7-2.2V. 1LSB= (2.2-0.7)V/2^7=11.72mV.	R	xx

5.3.9 LRADC3_DATA

LRADC3 DATA Register

（SFR:0x9f, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7:6	--	RESERVED	R	xx
5:0	LRADC3	6bit LRADC3 data output LRADC3 input voltage range is from 0 to AVCC.	R	xx

5.3.10 LRADC4_DATA

LRADC4 DATA Register

（SFR:0xa2, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7:6	--	RESERVED	R	xx
5:0	LRADC4	6bit LRADC4 data output LRADC4 input voltage range is from 0 to AVCC.	R	xx

5.3.11 LRADC5_DATA

LRADC5 DATA Register

（SFR:0xa3, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7:6	--	RESERVED	R	xx
5:0	LRADC5	6bit LRADC5 data output LRADC5 input voltage range is from 0 to AVCC.	R	xx

5.3.12 MULTI_USED

GPIO multi-used Control Register

（SFR:0Xa4, SFR bank 0x05）

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	R/W	0
6:4	Reserved	Reserved	R/W	100
3	Reserved	Reserved	R/W	0
2	FM_VCCOUT_EN	FM_VCCOUT LDO is used for FM power supply. 0: FM_VCCOUT pin floating, no power out 1: FM_VCCOUT=2.89V. If there is a capacitance at FM_VCCOUT, you should wait a moment after set this bit 1.	R/W	0
1	Reserved	Reserved	R/W	0
0	Reserved	Reserved	R/W	0

5.3.13 SYSTEM_CTL_RTCVDD

System on/off and play/pause time Control Register

（SFR:0xa7, SFR bank 0x05）(RTCVDD)

Bit(s)	Name	Description	R/W	Reset
7:6	SYSON_TIME	SYSON key pressing length set: 00: 60ms < t < 2s, issue Short-press status flag; t >=2s, system starts or issue Long-press status flag.	R/W	01

		01: 60ms < t < 3s, issue Short-press status flag; t >=3s, system starts or issue Long-press status flag. 10: 60ms < t < 4s, issue Short-press status flag; t >=4s, system starts or issue Long-press status flag. 11: 60ms < t < 5s, issue Short-press status flag; t >=5s, system starts or issue Long-press status flag. (note that CLK is not accurate for the first power up) (After Analog gives digital one flag, the time count etc. is realized by digital, cannot give it to Analog)		
5	LB_EN	LB_ enters standby and enable: 0: disable, shield the function of low power standby 1: enable, start the function of low power standby The battery voltage for low power standby can be set by LB_VOL. Note: (UVLO without debounce) =1, low power LB_ function is automatically disabled. Pay attention to the sequence of the comparator of low power detection and UVLO detection. Ensure that UVLO is before the comparator.	R/W	1
4:3	LB_VOL	LB (Low battery) voltage setting Li-ION 00 2.8V (no battery and the short connection between VCC and BAT). ***01 3.0V (Li-Ion battery power supply, 3.0V for protection) 1X 3.3V 8ms debounce, adopt asynchronous detection method, the condition is more critical. In this case, can select 3.0V or 2.8V low power when short connecting between VCC and BAT. If there is great fluctuation in VCC application, then set this bit to 2.8V in the AP. When the battery voltage is lower than the default 3.0V, the system will send low power system off signal, and the power of VCC/VDD will be cut off. Used together with LB_ to standby enable.	R/W	01
2	OC_EN	VCC/VDD LDO over-current protection enable 0: disable, VCC/VDD over-current protection is ineffective.	R/W	1

		1: enable, enable VCC/VDD over-current protection function.		
1	LVPRO_EN	VCC/VDD low voltage protection enable 0: disable, no protection even VCC/VDD voltage is very low. 1: enable.	R/W	1
0	REG_ENPMU	REG_ENPMU: 0: disable VCC/VDD 1: enable VCC/VDD	R/W	1

Note: after the writing operation on the register of RTCVDD, it has to wait for 3 MCUCLK periods + 4 low-frequency periods for the real written-in, and the written value then can be read.

5.3.14 PRESS_DISPLAY

System on/off and play/pause status display Register

（**SFR:0xa9, SFR bank 0x05**）

Bit(s)	Name	Description	R/W	Reset
7	SHORT_PRESS	Short-press status flag: 0: no Short-press status flag, SYSON key has not been pressed in a short time 1: has Short-press status flag, SYSON key has been pressed in a short time, and the pressing time is within the set value. Set this bit only when the key is up. Write 1 to chear this bit. Deisgn note: only as this bit is cleared to 0, and there is a key, the next detection will be carried out and the next status will be send if time and condition are satisfied. The same as the key's interrupt design. Software design note: in hard switch design solution, after running brom, it is necessary to write the bit to 1 and clear to 0 for once in order to avoid error of short-pressing when the hard switch cut off.	R/W	0
6	LONG_PRESS	Long-press status flag: 0: no Long-press status flag. SYSON key has not been pressed for a long time.	R	x

		1: has Long-press status flag. SYSON has been pressed down for a long time, and the pressing time > the set value. If the key is not up, then no time count. Key's one status display, unwritable		
5:3	Reserved	Reserved	R/W	100
2	–	Reserved	R	X
1:0	-	Reserved	R	0

6 System Control

6.1 RMU

6.1.1 Features

The RMU Controller of ATS2505 has following features:

(1) The RMU (Reset Management Unit) can reset all the peripherals.

(2) The MCU can enter power-saving mode by setting the registers of RMU .

6.1.2 Function Description

The RMU (Reset Management Unit) can reset all the peripherals and can force MCU enter IDLE or Power Down Mode. The wait cycles to access the SFR can be set by the PCON register which some of bits is different from the old 8051/80251

6.1.3 RMU Register List

The Address of Reset Manage Controller Group = SFR:0x86, sfr bank 0x01.

Index	Mnemonic	Description
0x86	MRCR1	Module Reset Control Register 1
0x87	PCON	Power Control Register
0x89	MRCR2	Module Reset Control Register 2
0x96	ExWait	External bus access wait cycle

6.1.4 Register Description

6.1.4.1 MRCR1（Module Reset Control Register 1, SFR:0x86, sfr bank 0x01）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:4	Reserved	Reserved	R/W	0000
3	UARTReset	UART Controller Reset	R/W	0

		0: reset 1: normal		
2	IRCReset	IRC Controller Reset 0: reset 1: normal	R/W	0
1	SPIReset	SPI Controller Reset 0: reset 1: normal	R/W	0
0	Reserved	Reserved	R/W	0

6.1.4.2 PCON（Power Control Register, SFR:0x87, all bank）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	SFR_wait*	SFR access wait cycle for USB controller 000: wait 0 cycle 001: wait 1 cycle 010: wait 2 cycle 011: wait 3 cycle 100: wait 4 cycle 101: wait 5 cycle 110: wait 6 cycle 111: wait 7 cycle	R/W	111
4	POF	Power Off flag This bit is the image of the input “poweroff”. It is set by hardware as VCC rises above TBD voltage to indicate that power has been off or VCC had fallen below a TBD voltage and that on-chip volatile memory is indeterminate. It can be set or cleared by software.	R/W	0
3	GF1	General purpose flag 1 Set or cleared by software	R/W	0
2	GF0	General purpose flag 0 Set or cleared by software	R/W	0
1	PD	Powerdown mode bit When set, activates powerdown mode Clear by hardware when an enabled external interrupt or a reset occurs.	W	0
0	IDL	Idle mode bit	W	0

		When set, activates idle mode Clear by hardware when an enabled interrupt or a reset occurs.		

* The wait cycles are used for access USB controller registers in 0x07 page.

6.1.4.3 MRCR2（Module Reset Control Register 2, SFR:0x89, sfr bank 0x01）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	Reserved	Reserved	R/W	000
4	DACReset	DAC Reset 0: reset 1: normal	R/W	0
3	Reserved	Reserved	R/W	0
2	DMA4Reset	DMA4 Reset 0: reset 1: normal	R/W	0
1	DMA3Reset	DMA3 Reset 0: reset 1: normal	R/W	0
0	DMA012Reset	DMA0/1/2 Reset 0: reset 1: normal	R/W	0

6.1.4.4 MRCR3（Module Reset Control Register 3, SFR:0x9f, sfr bank 0x01）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:2	Reserved	Read as zero	-	-
1	Reserved	Reserved	R/W	Reserved
0	B1/B2Reset	B1B2 controller reset 0: reset 1: normal	R/W	0

6.1.4.5 ExWait（External bus access wait cycle register, SFR:0x96, sfr all bank）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	Reserved	Read as ‘000’	–	-
4:0	ExWait	External bus access wait cycle	R/W	01fh

The wait cycles are used for accessing the register EXTMEM_DH (page address 06, sfr address 0xfe) and EXTMEM_DL (page address 06/08, sfr address 0xff).

6.2 INTC

6.2.1 Features

ATS2505 Interrupt Controller has following features:

(1) ATS2505 has the similar interrupt sources as the Intel 8xC251 relative to the Flip80251 specification.

(2) The interrupt sources are handled the same as on the original 8xC251, however the Flip80251 has a shorter interrupt latency period, and can distinguish shorter external interrupt pulses.

(3) Fourteen of interrupts can be enabled or disable by the system designer

(4) 4 levels of interrupt priority

6.2.2 Function Description

The Flip80251, like other control-oriented computer architectures, employs a program interrupt method. This operation branches to a subroutine and performs some service in response to the interrupt. When the subroutine completes, execution resumes at the point where the interrupt occurred. Interrupts may occur as a result of internal Flip80251 activity (e.g., timer overflow) or at the initiation of electrical signals external to the microcontroller (e.g., serial port communication). In all cases, interrupt operation is programmed by the system designer, who determines priority of interrupt service relative to normal code execution and other interrupt service routines. Fourteen of the seventeen interrupts are enabled or disabled by the system designer and may be manipulated dynamically.

A typical interrupt event chain occurs as follows. An internal or external device initiates an interrupt-request signal. This signal, connected to an input pin and periodically sampled by the Flip80251 (see figure 2), latches the event into a flag buffer. The priority of the flag (see figure 3 and 4, Interrupt System Special Function Registers) is compared to the priority of other interrupts by the interrupt handler. A high priority causes the handler to set an interrupt flag. This signals the instruction execution unit to execute a context switch. This context switch breaks the current flow of instruction sequences. The execution unit completes the current instruction prior to a save of the program counter (PC) and reloads the PC with the start address of a software service routine. The software service routine executes assigned tasks and as a final activity performs a RETI (return from interrupt) instruction. This instruction signals completion of the interrupt, resets the interrupt-in-progress priority, and reloads the program counter. Program operation then continues from the original point of interruption.

6.2.2.1 Interrupt Vector

The clock to drive the interrupt controller is identical to the clock that drives the MCU core.

Interrupt Vector of Artek' 80251

Interrupt Number	Interrupt Vector Address	Description
-	fe0000h	reset
0	ff0003/fe0003	int0_n
1	ff000b/fe000b	CTC interrupt
2	ff0013/fe0013	int1_n
3	ff001b/fe001b	RTC interrupt
4	ff0023/fe0023	UART interrupt
5	ff002b/fe002b	I2C / IRC interrupt
6	ff0033/fe0033	SPI interrupt
7	ff003b/ fe003b	NMI interrupt
8	ff0043/ fe0043	USB interrupt
9	ff004b/ fe004b	DMA5 interrupt (flash)
10	ff0053/ fe0053	DMA4 interrupt(card)
11	ff005b/ fe005b	LCD interrupt
12	ff0063/ fe0063	AD interrupt
13	ff006b/ fe006b	audio/video codec interrupt
14	ff0073/ fe0073	DMA012 interrupt
15	ff007b /fe007b	TRAP

6.2.2.2 Interrupt Priorities

Each of the fourteen Actions' 80251 interrupt sources may be individually programmed to one of four priority levels. This is accomplished with the IPH0.x/IPL0.x bit pairs in the interrupt priority high (IPH0) and interrupt priority low (IPL0) registers. Specify the priority level as shown in table below using IPH0.x as the MSB and IPL0.x as the LSB.

Level of Priority

IPH0.x	(MSB)	IPL0.x
0	0	0 Lowest Priority
0	1	1
1	0	2
1	1	3 Highest Priority

A low-priority interrupt is always interrupted by a higher priority interrupt but not by another interrupt of equal or lower priority. The highest priority interrupt is not interrupted by any other interrupt source. Higher priority interrupts are serviced before lower priority interrupts. The response to

simultaneous occurrence of equal priority interrupts (i.e., sampled within the same four state interrupt cycle) is determined by a hardware priority-within-level resolver, see below.

Interrupt Priority within Level

Interrupt number	Priority Number	Interrupt Name
0	15	reset
1	16	TRAP
2	7	NMI interrupt
3	0	int0_n
4	1	CTC interrupt
5	2	int1_n
6	3	RTC interrupt
7	4	UART interrupt
8	5	I2C/IRC interrupt
9	6	SPI interrupt
10	8	USB interrupt
11	9	DMA5 interrupt (flash)
12	10	DMA4 interrupt(card)
13	11	LCD interrupt
14	12	AD interrupt
15	13	audio/video codec interrupt
16 highest	14	DMA012 interrupt

Notes: Actions' 80251 Interrupt Priority within Level table differs from MCS® 51 microcontrollers. Other MCS 251 microcontrollers may have unique interrupt priority within level tables.

6.2.3 Interrupt Control Register List

Register Name	SFR Address	BANK	Description
IE0	0xA8	All bank	Interrupt Enable register 0
AIE	0xE8	All bank	Additional Interrupt Enable register
IPH0	0xB7	0x00	Interrupt Priority High register 0
IPL0	0xB8	0x00	Interrupt Priority Low register 0
AIPH	0xF7	0x00	Additional Interrupt Priority High register
AIPL	0xF8	0x00	Additional Interrupt Priority Low register
IF0	0x88	All bank	Interrupt Flag register 0
AIF	0xC0	All bank	Additional interrupt flag register
EXTINT	0XD8	0x06	External Interrupt Control

6.2.4 Register Description

IE0（Interrupt Enable register, SFR Address 0xA8, all bank）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	EA	Global Interrupt Enable Clear to disable all interrupts, except the TRAP and NMI interrupts, which are always enabled. Set to enable all interrupts that are individually enabled in IE0.	R/W	0
6	ESPI	SPI Interrupt Enable Set to enable SPI Interrupt. Cleared to disable SPI Interrupt	R/W	0
5	EI2C_IRC	I2C/IRC Interrupt Enable Set to enable I2C/IRC Interrupt. Cleared to disable I2C/IRC Interrupt	R/W	0
4	ES	UART Interrupt Enable Set to enable UART Interrupt. Cleared to disable UART Interrupt	R/W	0
3	ERTC	ERTC Interrupt Enable Set to enable ERTC Interrupt. Cleared to disable ERTC Interrupt	R/W	0
2	EX1	External Interrupt 1 enable Set to enable External Interrupt 1. Cleared to disable External Interrupt 1.	R/W	0
1	ECTC	ECTC Interrupt Enable Set to enable ECTC Interrupt. Cleared to disable ECTC Interrupt	R/W	0
0	EX0	External Interrupt 0 enable Set to enable External Interrupt 0. Cleared to disable External Interrupt 0.	R/W	0

AIE（Additional Interrupt Enable register, SFR Address 0xE8, all bank）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	EDMA012	DMA0/DMA1/DMA2 Interrupt Enable Set to enable DMA0, DMA1 and DMA2 interrupt. Cleared to disable DMA0, DMA1 and DMA2 Interrupt	R/W	0
5	ECODEC	Audio/video codec Interrupt Enable Set to enable Audio/video codec Interrupt. Cleared to disable Audio/video codec Interrupt	R/W	0

4	EAD	AIE（Additional Interrupt Enable register, SFR Address 0xE8, all bank） Bit4 EAD AD Interrupt Enable and PA or CLASSD Overcurrent Interrupt Enable: 1. Wire-Control IRQ 2. Audio ADC IRQ 3. PA Overcurrent IRQ 4. CLASSD Overcurrent IRQ Set to enable the Interrupt. Cleared to disable the Interrupt	R/W	0
3	ELCD	LCD Interrupt Enable Set to enable LCD Interrupt. Cleared to disable LCD Interrupt	R/W	0
2	EDMA4	DMA4 Interrupt enable Set to enable DMA4 Interrupt. Cleared to disable DMA4 Interrupt.	R/W	0
1	EDMA5	DMA5 Interrupt Enable Set to enable DMA5 Interrupt. Cleared to disable DMA5 Interrupt	R/W	0
0	EUSB	USB interrupt enable Set to enable USB interrupt. Cleared to disable USB interrupt.	R/W	0

Note:

* These interrupt pending can force MCU exit IDLE mode.

** The external interrupt (EX0 and EX1) used to exit powerdown mode must be configured as level sensitive and must be assigned the highest priority. In addition, the duration of the interrupt must be of sufficient length to allow the oscillator to stabilize.

*** Only Reset, EX0 and EX1 pending can force MCU exit POWDOWN mode.

Special attention:

External interrupts INT0# and INT1# (INTx#) pins may each be programmed to be low level-triggered or edge-triggered, dependent upon bits IT0 and IT1 in the EXTINT register . If ITx = 0, INTx# is triggered by a detected low at the pin. If ITx = 1, INTx# is negative-edge triggered. External interrupts are enabled with bits EX0 and EX1 (EXx) in the IE0 register. Events on the external interrupt pins set the interrupt request flags IEx in EXTINT. These request bits are cleared by hardware vectors to service routines only ifthe interrupt is negative-edge triggered. If the interrupt is level-triggered, the interrupt service routine must clear the request bit. External hardware must de-assert INTx# before the service routine completes, or an additional interrupt is requested. External interrupt pins must be deasserted for at least four state times prior to a request.

External interrupt pins must be de-asserted for at least two clock cycles prior to a request. External interrupt inputs are sampled at each clock cycle. A level-triggered interrupt pin held low or high for

any two clock cycles time period guarantees detection. Edge-triggered external interrupts must hold the request pin low for at least two clock cycles. This ensures edge recognition and sets interrupt request bit IEx_. The CPU clears IEx_ automatically during service routine fetch cycles for edge-triggered interrupts.

External interrupt inputs int0_n and int1_n provide both the capability to exit from Power-down mode on low-level signal while the interrupt priority bits of int0_n and int1_n are set to '1'.

IPH0（Interrupt Priority High register 0, SFR Address 0xB7, bank 0x00）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	IPHSPI	SPI interrupt Priority level most significant bit	R/W	0
5	IPHI2C_IRC	I2C/IRC Interrupt interrupt Priority level most significant bit	R/W	0
4	IPHS	UART interrupt Priority level most significant bit	R/W	0
3	IPHRTC	RTC interrupt Priority level most significant bit	R/W	0
2	IPHX1	External interrupt 1 Priority level most significant bit	R/W	0
1	IPHCTC	CTC interrupt Priority level most significant bit	R/W	0
0	IPHX0	External interrupt 0 Priority level most significant bit	R/W	0

IPL0（Interrupt Priority Low register 0, SFR Address 0xB8, bank 0x00）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	IPLSPI	SPI interrupt Priority level least significant bit	R/W	0
5	IPLI2C_IRC	I2C/IRC Interrupt interrupt Priority level least significant bit	R/W	0
4	IPLS	UART interrupt Priority level least significant bit	R/W	0
3	IPLRTC	RTC interrupt Priority level least significant bit	R/W	0
2	IPLX1	External interrupt 1 Priority level least significant bit	R/W	0
1	IPLCTC	CTC interrupt Priority level least significant bit	R/W	0
0	IPLX0	External interrupt 0 Priority level least significant bit	R/W	0

AIPH（Additional Interrupt Priority High register, SFR Address 0xF7, bank 0x00）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	IPHDMA012	DMA012 interrupt Priority level most significant bit	R/W	0
5	IPHCODEC	AUDIO/VIDEO CODEC interrupt Priority level most significant bit	R/W	0
4	IPHAD	The interrupt Priority level most significant bit	R/W	0
3	IPHLCD	LCD interrupt Priority level most significant bit	R/W	0

2	IPHDMA4	DMA4 interrupt Priority level most significant bit	R/W	0
1	IPHDMA5	DMA5 interrupt Priority level most significant bit	R/W	0
0	IPHUSB	USB interrupt Priority level most significant bit	R/W	0

AIPL（Additional Interrupt Priority Low register, SFR Address 0xF8, bank 0x00）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	IPLDMA012	DMA012 interrupt Priority level least significant bit	R/W	0
5	IPLCODEC	AUDIO/VIDEO CODEC interrupt Priority level least significant bit	R/W	0
4	IPLAD	The interrupt Priority level least significant bit	R/W	0
3	IPLLCD	LCD interrupt Priority level least significant bit	R/W	0
2	IPLDMA4	DMA4 interrupt Priority level least significant bit	R/W	0
1	IPLDMA5	DMA5 interrupt Priority level least significant bit	R/W	0
0	IPLUSB	USB interrupt Priority level least significant bit	R/W	0

IF0（Interrupt Flag register 0, SFR Address 0x88, all bank）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	FSPI	This bit will automatically cleared only when All SPI interrupt pending bits are cleared, otherwise unchanged.	R	0
5	FI2C_IRC	This bit will automatically cleared only when All I2C/IRC interrupt pending bits are cleared, otherwise unchanged	R	0
4	FS	This bit will automatically cleared only when All UART interrupt pending bits are cleared, otherwise unchanged	R	0
3	FRTC	This bit will automatically cleared only when all RTC interrupt pending bits are cleared, otherwise unchanged	R	0
2	FX1	This bit will automatically cleared only when all the pending bit of IE1_ (in 06 BANK, at sfr address 0xd8) is cleared, otherwise unchanged	R	0
1	FCTC	This bit will automatically cleared only when all CTC interrupt pending bits are cleared, otherwise unchanged	R	0
0	FX0	his bit will automatically cleared only when all the pending bit of IE0_ (in 06 BANK, at sfr address 0xd8) is cleared, otherwise unchanged	R	0

AIF（Additional interrupt flag register, SFR Address 0XC0, all bank）

Bit Number	Bit Mnemonic	Function	Access	Reset
7	Reserved	The value read from this bit is 0	-	0
6	FDMA012	This bit will automatically cleared only when all DMA012 interrupt pending bits are cleared, otherwise unchanged	R	0
5	FCODEC	This bit will automatically cleared only when all CODEC interrupt pending bits are cleared, otherwise unchanged	R	0
4	FAD	This bit will automatically cleared only when all the interrupt pending bits are cleared, otherwise unchanged	R	0
3	FLCD	This bit will automatically cleared only when all LCD interrupt pending bits are cleared, otherwise unchanged	R	0
2	FDMA4	This bit will automatically cleared only when all DMA4 interrupt pending bits are cleared, otherwise unchanged	R	0
1	FDMA5	This bit will automatically cleared only when all DMA5 interrupt pending bits are cleared, otherwise unchanged	R	0
0	FUSB	This bit will automatically cleared only when all USB interrupt pending bits are cleared, otherwise unchanged	R	0

EXTINT（External Interrupt Control, SFR Address 0XD8, bank 0x06）

Bit Number	Bit Mnemonic	Function	Access	Reset
7:4	Reserved	Be read as '0000'	–	–
3	IE1_	External interrupt 1 edge flag. Hardware controlled Set when external interrupt 1 is detected. Cleared when interrupt is processed. Write '1' will clear this bit.	R/W	0
2	IT1	External interrupt 1 signal type control bit. Set to specify External interrupt 1 as falling edge triggered. Cleared to specify External interrupt 1 as low level triggered.	R/W	0
1	IE0_	External interrupt 0 edge flag. Hardware controlled Set when external interrupt 0 is detected. Cleared when interrupt is processed Write '1' will clear this bit.	R/W	0
0	IT0	External interrupt 0 signal type control bit. Set to specify External interrupt 0 as falling edge triggered. Cleared to specify External interrupt 0 as low level triggered.	R/W	0

6.3 Register description

RTC_CTL0（RTC Control 0 register. index 0x00） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7	cal_en	Calendar enable 0:disable 1:enable	R/W	0
6	en_almpd	Alarm pending enable. 0: disable. The alarm pending bit is disabled. The pending bit is not set when alarm is occoured 1: enable.	R/W	0
5	test_en	Test enable 0: disable 1: enable. The RTC's LOSC is changed to HOSC	R/W	0
4:3	/	reserved	/	0
2	cal_clk_select	Calendar clock select 0:select ILOSC 1:select ELOSC	R/W	0
1	Leap year	RTC Leap Year bit 1: leap year 0: not leap year	R	1
0	alm_ip	Alarm IRQ pending bit. Writing 1 to this bit will clear it.	R/W	0

NOTE: The cal_en bit must be disabled when The RTC Time register being written. And all RTC Time register must be written before cal_en is enabled when set the time, Or error will occur.

RTCTimeS（RTC Time Second Register, index 0x01） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserve	-	-
5:0	time_sec	Calendar Time Second[5:0]	R/W	0

RTCTimeMin (RTC Time Minute Register, index 0x02） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserve	-	-
5:0	time_min	Calendar Time Minute[5:0]	R/W	0

RTCTimeH (RTC Time Hour Register, index 0x03） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	-	Reserve	-	-
4:0	time_hour	Calendar Time Hour[4:0]	R/W	0

RTCTimeD (RTC Time Day Register, index 0x04） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	-	Reserve	-	-
4:0	time_day	Calendar Time Day[4:0]	R/W	01

RTCTimeMon(RTC Time Month Register, index 0x05） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:4	-	Reserve	-	-
3:0	time_mon	Calendar Time Month[3:0]	R/W	01

RTCTimeYear(RTC Time Year Register, index 0x06） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7	-	Reserve	-	-
6:0	time_year	Calendar Time Year[6:0]	R/W	0

RTCAlmS（RTC Alarm Second Register, index 0x07） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserve	-	-
5:0	alm _sec	Alarm Second[5:0]	R/W	0

RTCALMM（RTC Alarm Minute Register, index 0x08） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:6	-	Reserve	-	-
5:0	alm _min	Alarm Minute [5:0]	R/W	0

RTCALMH（RTC Alarm Hour Register, index 0x09） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	-	Reserve	-	-
4:0	alm _hour	Alarm Hour [4:0]	R/W	0

RTCrdm（RTC Random access Register, index 0x0b） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	random	These bits can be accessed by CPU freely.	R/W	0

RTCrdm_2（RTC Random access Register2, index 0x1f） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	random	These bits can be accessed by CPU freely.	R/W	0

RTCrdm_3（RTC Random access Register3, index 0x20） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	random	These bits can be accessed by CPU freely.	R/W	0

RTCrdm_4（RTC Random access Register4, index 0x21） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	random	These bits can be accessed by CPU freely.	R/W	0

RTCREGUPDATE（RTC Register update control Register, index 0x0c） (RTCVDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	update	The RTCVDD register update control Register. When writing the RTC registers (except RTCREGUPDATE register or bit “alm_ip”), the RTC registers’ values are not update immediately. The value is written to backup registers(in VDD) first. Just when writing RTCREGUPDATE register “A5H”, the RTCVDD registers’ values are update with the backup registers’ value. RTCREGUPDATE register is automatically reset as “5AH” after the RTCVDD register is update. NOTE: Do not write RTCVDD registers when this register value is	R/W	0x5a

		“A5H” NOTE: When writing the bit “alm_ip”, it will take effect immediately. Do not need writing this register.		

RTC_CTL1（RTC Control 1 register. index 0x0d） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7	2hz_en	2hz IRQ enable 0:disable 1:enable	R/W	0
6	timer_en	RTC Timer enable 0:disable 1:enable	R/W	0
5	clk_sel	Watch dog, 2hz,timer ‘s clock select bit: 0: pmu_clk_div 1: ELOSC	R/W	0
	/	reserve		/
1	2hz_ip	2hz IRQ pending bit Writing 1 to this bit will clear it.	R/W	0
0	timer_ip	Timer IRQ pending bit Writing 1 to this bit will clear it.	R/W	0

TimerLB（Timer low Byte, index 0x0e） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	timerlb	Low byte of timer Register Timer is a down counter with LOSC as clock. When the Counter Overflow, timer_ip will occur. Timer_ip = [1/(Time bit[23:0]+1)] *FLOSC	R/W	X

TimerMB（Timer middle Byte, index 0x0f） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	timermb	**Middle** byte of LOSC Divider Register	R/W	X

TimerHB（Timer high Byte, index 0x010） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	timerhb	**High** byte of timer Register	R/W	X

WDCtl（watch dog control register, index 0x11） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7	wd_en	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, either an internal reset (WDRST-) is generated to force the system into reset status and then reboot, or a IRQ is sent to CPU.	R/W	0
6:4	clk_sel	Watch Dog timer clock select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1khz 176 ms 001 512hz 352 ms 010 256hz 703ms 011 128hz 1.4 s 100 64hz 2.8s 101 32hz 5.6 s 110 16hz 11.2s 111 8hz 22.5 s	R/W	010
3	clr	Clear bit, write 1 to clear WD timer, cleared automatically	W	0
2	mode_sel	Watchdog IRQ or Reset- Select. 0: sent reset when Dog timer overflows 1:sent IRQ when Dog timer overflows	R/W	0
1	wd_flag	Watch dog overflow flag 1:means WD reset or irq ever occurred. Writing 1 to this bit clears it. 0:not occurred This bit is reset by powerok signal。	R/W	0

0	-	reserve	/	X

CTCCtl（CTC control register, index 0x12） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7	ctc_en	CTC enable 0: Disable, 1: Enable.	R/W	0
6:3	pre_scale	Pre-scale register. 0000: the CTC clock is /1 of the HOSC. 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 1001: /512 Others are reserve	R/W	0
2:1	-	Reserve	/	X
0	ctc_ip	CTC pending bit Writing 1 to this bit will clear it.	R/W	0

CTCCNTL（CTC counter low register, index 0x13） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	counterl	CTC Counter[7:0] CTC is a down counter using CTC clock. When the counter is overflow , a CTC IRQ is sent to CPU. Overflow time as enable CTC is: (Counter[15:0]+1)/(CTC clock)	R/W	0

CTCCNTH（CTC counter high register, index 0x14） (VDD)

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	counterh	CTC Counter[15:8]	R/W	0

7 Co-processor

7.1.1 DMA0/1/2 Register

The Base Address of DMA0 controller Group = SFR: 0x90, sfr bank 0x01.

DMA0 Register List

Index	Mnemonic	Description
0x0	DMA0CTL0	DMA0 Control Register 0
0x1	DMA0SADDR1	DMA0 Source Address 1 Register
0x2	DMA0SADDR0	DMA0 Source Address 0 Register
0x3	DMA0DADDR1	DMA0 Destination Address 1 Register
0x4	DMA0DADDR0	DMA0 Destination Address 0 Register
0x5	DMA0CTL1	DMA0 Control Register 1
0x7	DMA0SZH	DMA0 Transfer Size High Register
0x8	DMA0SZL	DMA0 Transfer Size Low Register
0x9	DMA0IP	DMA0 Interrupt Pending register

The Base Address of DMA1 controller Group = SFR: 0x90, sfr bank 0x02.

DMA1 Register List

Index	Mnemonic	Description
0x0	DMA1CTL0	DMA1 Control Register 0
0x1	DMA1SADDR1	DMA1 Source Address 1 Register
0x2	DMA1SADDR0	DMA1 Source Address 0 Register
0x3	DMA1DADDR1	DMA1 Destination Address 1 Register
0x4	DMA1DADDR0	DMA1 Destination Address 0 Register
0x5	DMA1CTL1	DMA1 Control Register 1
0x7	DMA1SZH	DMA1 Transfer Size High Register
0x8	DMA1SZL	DMA1 Transfer Size Low Register
0x9	DMA1IP	DMA1 Interrupt Pending register

The Base Address of DMA2 controller Group = SFR: 0x90, sfr bank 0x03.

DMA2 Register List

Index	Mnemonic	Description
0x0	DMA2CTL0	DMA2 Control Register 0
0x1	DMA2SADDR1	DMA2 Source Address 1 Register
0x2	DMA2SADDR0	DMA2 Source Address 0 Register
0x3	DMA2DADDR1	DMA2 Destination Address 1 Register
0x4	DMA2DADDR0	DMA2 Destination Address 0 Register
0x5	DMA2CTL1	DMA2 Control Register 1
0x7	DMA2SZH	DMA2 Transfer Size High Register
0x8	DMA2SZL	DMA2 Transfer Size Low Register
0x9	DMA2IP	DMA2 Interrupt Pending register

7.1.1.1 DMA0 Register

DMA0CTL0（DMA0 Control Register 0, index 0x00）

Bit Number	Bit Mnemonic	Description	Access	Reset
7	reserved	Read as '0'	–	–
6	ABORT	0: DMA transfer enable 1: DMA transfer abort This bit will be cleared automatically by writing 1 to this bit.	R/W	0
5:4	DSTMODE	Destination transfer mode 00: fix address 01: address auto count up 10: address auto count down 11: fix address	R/W	00
3:2	SRCMODE	Source transfer mode 00: fix address 01: address auto count up 10: address auto count down 11: fix address	R/W	00
1	DSTTYPE	Destination type 0: Memory 1: SFR	R/W	0
0	SRCTYPE	Source type 0: Memory 1: SFR	R/W	0

DMA0SADDR1（DMA0 Source Address 1 Register, index 0x01）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA0SADDR0	SRCTYPE is Memory:	R/W	0

		DMA0 Source Address [15:8] SRCTYPE is SFR: SFR BANK register		

DMA0SADDR0（DMA0 Source Address 0 Register, index 0x02）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA0SADDR0	DMA0 Source Address [7:0]	R/W	0

DMA0DADDR1（DMA0 Destination Address 1 Register, index 0x03）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA0DADDR1	SRCTYPE is Memory: DMA0 Destination Address [15:8] SRCTYPE is SFR: SFR BANK register	R/W	0

DMA0DADDR0（DMA0 Destination Address 0 Register, index 0x04）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA0DADDR0	DMA0 Destination Address [7:0]	R/W	0

DMA0CTL1（DMA0 Control Register 1, index 0x05）

Bit Number	Bit Mnemonic	Description	Access	Reset
7	Reserved	Read as ‘0’	–	–
6	TCIRQEN	DMA0 TC IRQ enable bit 0: Disable IRQ. 1: Enable IRQ when DMA0 finishes the whole block transfer.	R/W	0
5	HFIRQEN	DMA0 Half Transfer IRQ enable bit 0: Disable IRQ. 1: Enable IRQ when DMA0 finishes half of the block transfer.	R/W	0
4	Reserved	Read as ‘0’	R	0
3:1	EXTRIG	External Trigger 0 0 0 Audio Codec Input DRQ 0 0 1 SPI TX DRQ 0 1 0 SPI RX DRQ 0 1 1 UART TX DRQ 1 0 0 UART RX DRQ 1 0 1 ADC DRQ 1 1 0 Reserved	R/W	000

		1 1 1 Reserved		
0	STAT	DMA Start. After transfer complete the bit will be cleared. A low-go-high edge of this bit will load SRC start address, DST start address and transfer counter into corresponding working registers.	R/W	0

DMA0SZH（DMA0 Transfer Size High Register, index 0x07）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA0SZH	DMA0 Transfer Size [15:8]	R/W	0

DMA0SZL（DMA0 Transfer Size Low Register, index 0x08）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA0SZL	DMA0 Transfer Size [7:0]	R/W	0

NOTE: The number of transfer bytes is “Transfer Size+1”

DMA0IP（DMA0 Interrupt Pending register, index 0x09）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	PriorityTAB	Priority Index Table * 000: DMA0>DMA1>DMA2 001: DMA0>DMA2>DMA1 010: DMA1>DMA0>DMA2 011: DMA1>DMA2>DMA0 100: DMA2>DMA0>DMA1 101: DMA2>DMA1>DMA0 110: same as 000 111: same as 000	R/W	000
4	DSTTYPE2	Destination type 2 : 0: DATARAM SPACE 1: PROGRAM SPACE	R/W	0
3	SRCTYPE2	Source type 2 : 0: DATARAM SPACE 1: PROGRAM SPACE	R/W	0
2	TCIRQ	DMA0 Transfer Complete IRQ Pending, writing 1 to this bit will clear it.	R/W	0
1	HFIRQ	DMA0 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0

0	ERRORFLAG	DMA0 BUS conflict Pending, writing 1 to this bit will clear it.	R/W	0

7.1.1.2 DMA1 Register

DMA1CTL0（DMA1 Control Register 0, index 0x00）

Bit Number	Bit Mnemonic	Description	Access	Reset
7	Reserved	Read as '0'	–	–
6	ABORT	0: DMA transfer enable 1: DMA transfer abort This bit will be cleared automatically by writing 1 to this bit.	R/W	0
5:4	DSTMODE	Destination transfer mode 00: fix address 01: address auto count up 10: address auto count down 11: fix address	R/W	0
3:2	SRCMODE	Source transfer mode 00: fix address 01: address auto count up 10: address auto count down 11: fix address	R/W	0
1	DSTTYPE	Destination type 0: Memory 1: SFR	R/W	0
0	SRCTYPE	Source type 0: Memory 1: SFR	R/W	0

DMA1SADDR1（DMA1 Source Address 1 Register, index 0x01）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA1SADDR0	SRCTYPE is Memory: DMA1 Source Address [15:8] SRCTYPE is SFR: SFR BANK register	R/W	0

DMA1SADDR0（DMA1 Source Address 0 Register, index 0x02）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA1SADDR0	DMA1 Source Address [7:0]	R/W	0

DMA1DADDR1（DMA1 Destination Address 1 Register, index 0x03）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA1DADDR1	SRCTYPE is Memory: DMA1 Destination Address [15:8] SRCTYPE is SFR: SFR BANK register	R/W	0

DMA1DADDR0（DMA1 Destination Address 0 Register, index 0x04）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA1DADDR0	DMA1 Destination Address [7:0]	R/W	0

DMA1CTL1（DMA1 Control Register 1, index 0x05）

Bit Number	Bit Mnemonic	Description	Access	Reset
7	Reserved	Be read as '0'	–	–
6	TCIRQEN	DMA1 TC IRQ enable bit 0: Disable IRQ. 1: Enable IRQ when DMA1 finishes the whole block transfer.	R/W	0
5	HFIRQEN	DMA1 Half Transfer IRQ enable bit 0: Disable IRQ. 1: Enable IRQ when DMA1 finishes half of the block transfer.	R/W	0
4	Reserved	Read as 0	R	0
3:1	EXTRIG	External Trigger 0 0 0 Audio Codec Input DRQ 0 0 1 SPI TX DRQ 0 1 0 SPI RX DRQ 0 1 1 UART TX DRQ 1 0 0 UART RX DRQ 1 0 1 ADC DRQ 1 1 0 Reserved 1 1 1 Reserved	R/W	000
0	STAT	DMA Start. After transfer complete the bit will be cleared. A low-go-high edge of this bit will load SRC st0art address, DST start address and transfer counter into Corresponding working registers.	R/W	0

DMA1SZH（DMA1 Transfer Size High Register, index 0x07）

Bit Number	Bit Mnemonic	Description	Access	Reset

7:0	DMA1SZH	DMA1 Transfer Size [15:8]	R/W	0

DMA1SZL（DMA1 Transfer Size Low Register, index 0x08）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA1SZL	DMA1 Transfer Size [7:0]	R/W	0

NOTE: The number of transfer bytes is “Transfer Size+1”

DMA1IP（DMA1 Interrupt Pending register, index 0x09）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	PriorityTAB	Priority Index Table * 000: DMA0>DMA1>DMA2 001: DMA0>DMA2>DMA1 010: DMA1>DMA0>DMA2 011: DMA1>DMA2>DMA0 100: DMA2>DMA0>DMA1 101: DMA2>DMA1>DMA0 110: same as 000 111: same as 000	R/W	000
4	DSTTYPE2	Destination type 2 : 0: DATARAM SPACE 1: PROGRAM SPACE	R/W	0
3	SRCTYPE2	Source type 2 : 0: DATARAM SPACE 1: PROGRAM SPACE	R/W	0
2	TCIRQ	DMA1 Transfer Complete IRQ Pending, writing 1 to this bit will clear it.	R/W	0
1	HFIRQ	DMA1 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
0	ERRORFLAG	DMA1 BUS conflict Pending, writing 1 to this bit will clear it.	R/W	0

7.1.1.3 DMA2 Register

DMA2CTL0（DMA2 Control Register 0, index 0x00）

Bit Number	Bit Mnemonic	Description	Access	Reset
7	Reserved	Read as ‘0’	–	–
6	ABORT	0: DMA transfer enable 1: DMA transfer abort This bit will be cleared automatically by writing 1 to this bit.	R/W	0

5:4	DSTMODE	Destination transfer mode 00: fix address 01: address auto count up 10: address auto count down 11: fix address	R/W	0
3:2	SRCMODE	Source transfer mode 00: fix address 01: address auto count up 10: address auto count down 11: fix address	R/W	0
1	DSTTYPE	Destination type 0: Memory 1: SFR	R/W	0
0	SRCTYPE	Source type 0: Memory 1: SFR	R/W	0

DMA2SADDR1（DMA2 Source Address 1 Register, index 0x01）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA2SADDR0	SRCTYPE is Memory: DMA2 Source Address [15:8] SRCTYPE is SFR: SFR BANK register	R/W	0

DMA2SADDR0（DMA2 Source Address 0 Register, index 0x02）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA2SADDR0	DMA2 Source Address [7:0]	R/W	0

DMA2DADDR1（DMA2 Destination Address 1 Register, index 0x03）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA2DADDR1	SRCTYPE is Memory: DMA2 Destination Address [15:8] SRCTYPE is SFR: SFR BANK register	R/W	0

DMA2SADDR0（DMA2 Destination Address 0 Register, index 0x04）

Bit Number	Bit Mnemonic	Description	Access	Reset

7:0	DMA2DADDR0	DMA2 Destination Address [7:0]	R/W	0

DMA2CTL1（DMA2 Control Register 1, index 0x05）

Bit Number	Bit Mnemonic	Description	Access	Reset
7	Reserved	Read as '0'	–	–
6	TCIRQEN	DMA2 TC IRQ enable bit 0: Disable IRQ. 1: Enable IRQ when DMA2 finishes the whole block transfer.	R/W	0
5	HFIRQEN	DMA2 Half Transfer IRQ enable bit 0: Disable IRQ. 1: Enable IRQ when DMA2 finishes half of the block transfer.	R/W	0
4	Reserved	Be read as 0	R	0
3:1	EXTRIG	External Trigger 0 0 0 Audio Codec Input DRQ 0 0 1 SPI TX DRQ 0 1 0 SPI RX DRQ 0 1 1 UART TX DRQ 1 0 0 UART RX DRQ 1 0 1 ADC DRQ 1 1 0 Reserved 1 1 1 Reserved	R/W	000
0	STAT	DMA Start. After transfer complete the bit will be cleared. A low-go-high edge of this bit will load SRC start address, DST start address and transfer counter into Corresponding working registers.	R/W	0

DMA2SZH（DMA2 Transfer Size High Register, index 0x07）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA2SZH	DMA2 Transfer Size [15:8]	R/W	0

DMA2SZL（DMA2 Transfer Size Low Register, index 0x08）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:0	DMA2SZL	DMA2 Transfer Size [7:0]	R/W	0

NOTE: The number of transfer bytes is "Transfer Size+1"

DMA2IP（DMA2 Interrupt Pending register, index 0x09）

Bit Number	Bit Mnemonic	Description	Access	Reset
7:5	PriorityTAB	Priority Index Table * 000: DMA0>DMA1>DMA2 001: DMA0>DMA2>DMA1 010: DMA1>DMA0>DMA2 011: DMA1>DMA2>DMA0 100: DMA2>DMA0>DMA1 101: DMA2>DMA1>DMA0 110: same as 000 111: same as 000	R/W	000
4	DSTTYPE2	Destination type 2 : 0: DATARAM SPACE 1: PROGRAM SPACE	R/W	0
3	SRCTYPE2	Source type 2 : 0: DATARAM SPACE 1: PROGRAM SPACE	R/W	0
2	TCIRQ	DMA2 Transfer Complete IRQ Pending, writing 1 to this bit will clear it.	R/W	0
1	HFIRQ	DMA2 Half Transfer IRQ Pending, writing 1 to this bit will clear it.	R/W	0
0	ERRORFLAG	DMA2 BUS conflict Pending, writing 1 to this bit will clear it.	R/W	0

Note: * when SFR's BANK register is set as 1, 2 and 3, the PriorityTAB visited in fact is a register.

7.1.1.4 DMA0/1/2-related Register

（1）Bit 0 in MRCR2 (Module Reset Control Register 2, 3Dh) , controlling DMA0/1/2's reset.

（2）Bit 1:0 in MCSR3 (Module Clock Select Register 3, 2Ch), controlling DMA0/1/2's clock.

（3）Bit 6 of AIPH and AIPL, controlling DMA0/1/2's interrupt priority.

（4）Bit6 of AIF and AIE, respectively control DMA0/1/2's interrupt flag and priotiry.

（5）In addition, in order to reduce current consumption, each RAM block of ATS2505 has clock enable bit, and the clock of the corresponding RAM shall be opened when using DMA to transmit data.

8 Transfer & Communication

8.1 USB

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports 2 IN endpoint and 1 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup.
- Support Udisk mode high speed DMA panel

8.2 SPI

- Support dual I/O write and read mode
- Support SPI norflash boot mode
- Support IRQ and DMA mode to transmit data

8.2.1 Function Description

The SPI module is designed according to Motorola serial peripheral interface protocols. It can be configured as either a master or slave device. It can generate a large range of SPI clock so as to communicate with different devices supporting SPI protocols. Especially, this module support three operation mode: write & read, write only, read only mode.

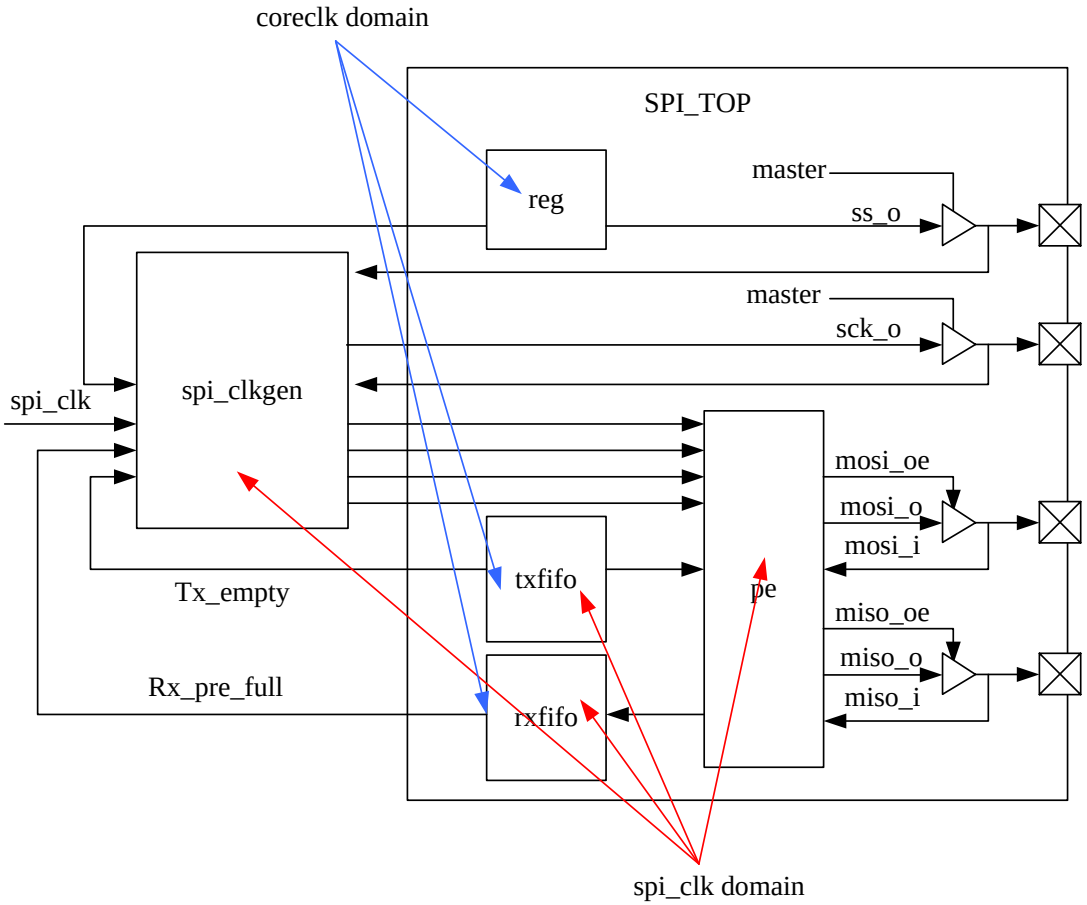
SPI write & read mode use the MOSI pin to serially write instructions, addresses or data to the device. It also uses the MISO pin to read data or status from the device synchronous. This mode is designed to meet normal SPI application.

The write only & read only mode support 1x I/O and 2x I/O mode. The 2x I/O mode allows data to be transfer to or from slave at twice the rate of the 1x I/O mode. This mode is designed to

meet special application.

8.2.2 Module Description

8.2.2.1 Block Diagram



8.2.2.2 Register List

Bank	Offset	Register Name	Description
0x0a	0x99	SPI_CTL	SPI Control Register
	0x9a	SPI_DRQ	SPI DMA/IRQ control Register.
	0x9b	SPI_STA	SPI Status Register
	0x9c	SPI_CLKDIV	SPI Clock Divide Control Register
	0x9d	SPI_TXDAT	SPI tx fifo register
	0x9e	SPI_RXDAT	SPI rx fifo register
	0x9f	SPI_BCL	SPI Bytes Count Low Register
	0xa2	SPI_BCH	SPI Bytes Count high Register

8.2.3 Register Description

8.2.3.1 SPI_CTL

SPI Control Register, This register is used for enabling SPI module, selecting SPI mode and SPI SS output voltage.（SFR address 0x99, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	SPI_EN	**SPI Enable** 0: Disable 1: Enable	R/W	0
6	SPI_MS	**SPI master/slave select** 0: master 1: slave	R/W	0
5	SPI_LM	**LSB/MSB First Select** 0: transmit and receive MSB first 1: transmit and receive LSB first	R/W	0
4	SPI_SS	**SPI SS pin control output,** this bit is valid only in master mode 1: output high 0: output low	R/W	0
3:2	SPI_MODE	**SPI mode select** CPOL CPHA 00: mode 0 01: mode 1 10: mode 2 11: mode 3	R/W	11
1:0	SPI_WR	**SPI write/read select** 00: write and read 01: write and read 10: write only 11: read only	R/W	00

8.2.3.2 SPI_DRQ

SPI DMA/IRQ control Register. This register is used for enabling SPI DRQ/IRQ, and selecting SPI DRQ/IRQ trigger threshold.（SFR address 0x9a, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	SPI_TDRQ_EN	**SPI TX DRQ Enable,** trigger DRQ when SPI TX FIFO is not full. 0: disable	R/W	0

		1: enable		
6	SPI_RDRQ_EN	**SPI RX DRQ Enable,** trigger DRQ when SPI RX FIFO is not empty. 0: disable 1: enable	R/W	0
5:4	-	**Reserved, be read as zero**	-	-
3	SPI_TIRQ_EN	**SPI TX IRQ Enable,** trigger SPI TX IRQ when SPI TX FIFO is empty. 0: disable 1: enable	R/W	0
2	SPI_RIRQ_EN	**SPI RX IRQ Enable,** trigger SPI RX IRQ when SPI RX FIFO is not empty. 0: disable 1: enable	R/W	0
1	SPI_TIRQ_PD	**SPI TX IRQ Pending**, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0
0	SPI_RIRQ_PD	**SPI RX IRQ Pending**, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0

8.2.3.3 SPI_STA

SPI Status Register, This register is used for displaying current SPI FIFO status.

（SFR address 0x9b, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	TXEM	**SPI TX FIFO Empty** 0: not empty 1: empty	R	1
6	TXFU	**SPI TX FIFO Full** 0: not full 1: full	R	0
5	RXEM	**SPI RX FIFO Empty** 0: not empty 1: empty	R	1
4	RXFU	**SPI RX FIFO Full** 0: not full	R	0

		1: full		
3	SPI_BUSY	**SPI transmitting status bit.** The bit is automatically clear when SPI finish transmitted data; and set in transmitting status automatically; 0: SPI idle status 1: SPI transmitting status	R	0
2	TXER	**SPI TX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged. This bit set when SPI TX FIFO is wrote overflow;	R/W	0
1	RXER	**SPI RX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged. This bit set when SPI RX FIFO is wrote or read overflow;	R/W	0
0	-	**Reserved, read as zero**	-	-

8.2.3.4 SPI_CLKDIV

SPI Clock Divide Control Register, This register is used for setting SPI source clock divide factor, and selecting SPI read mode. （SFR address 0x9c, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	-	Reserve, be read as zero	R	0
3:0	SPI_CLKDIV	**SPI Clock Divide Factor [3:0]** 0000 /1 0001 /2 0010 /4 ... 1111 /30 SPI clock = SPI source clock/（SPI_CLKDIV[3:0]*2）	R/W	1111

8.2.3.5 SPI_TXDAT

SPI data register, this register is used for writing data to SPI TX FIFO.
（SFR address 0x9d, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	SPI_TXDAT	**SPI Data[7:0]** Writing this field will send 1 byte to 8bitx8	W	0

		levels depth SPI TX FIFO, be read as zero.		

8.2.3.6 SPI_RXDAT

SPI data register, this register is used for reading data from SPI RX FIFO.

（SFR address 0x9e, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	SPI_RXDAT	**SPI Data[7:0]** Reading this field will fetch 1 byte from 8bitx8 levels depth SPI RX FIFO	R	0

8.2.3.7 SPI_BCL

SPI Bytes Count Low Register, this register is used for setting SPI bytes counter low bits in the SPI read mode.

（SFR address 0x9f, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	SPI_BCL	**Bytes Counter Low bits [7: 0]**	R/W	0

8.2.3.8 SPI_BCH

SPI Bytes Count High Register, This register is used to setting SPI bytes counter high bits, selecting SPI data I/O mode and delay chain. （SFR address 0xa2, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	SPI_IO	**SPI data I/O mode select** (valid when SPI select write or read only mode) 0: 1x I/O mode select 1: 2x I/O mode select	R/W	0
6	SPI_DELAY_EN	**SPI delay chain enable** 0: Disable 1: Enable	R/W	0
5:4	SPI_DELAY	**SPI read clock delay time** (valid when SPI select write/read and read mode) 00: delay 2 ns 01: delay 4 ns 10: delay 8 ns 11: delay 12 ns	R/W	00
3	SPI_RS	**Read Start Control**, write 1 to start read clock, valid when SPI select read only mode. (When transfer is finished, this bit will be auto cleared）	R/W	0
2	-	**Reserved, be read as zero**	-	-

1:0	SPI_BCH	Bytes Counter High bits [1: 0]	R/W	00

8.3 UART

- support BaudRate up to 1.5Mbps;
- support UART auto flow mode;

8.3.1 Function Description

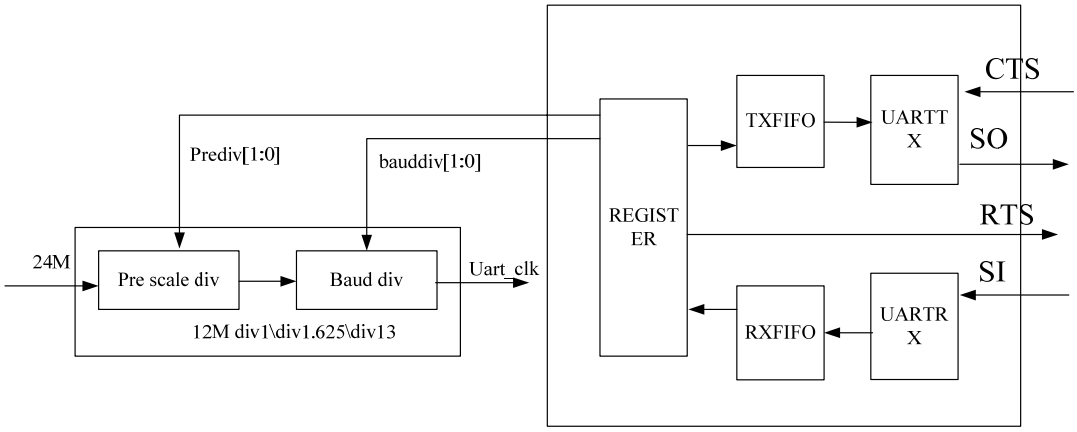
The UART module is designed according to UART protocols. It can generate a large range of standard baud rate so as to communicate with different devices.

UART module support MCU access to UART data. The command instructions, addresses or data you write to UART TX FIFO will be transfer to UART_TX pin immediately. When you read a byte from UART RX FIFO, the RX FIFO pointer will decrease one until it point to the bottom of the RX FIFO.

UART module also supports DMA access to UART data.

Especially, UART module support auto flow mode to control the data transiting sequence.

8.3.2 Module Description



8.3.3 Register List

Bank	Offset	Register Name	Description
0x0a	0x90	UART_BR	UART BAUDRATE Register.

	0x91	UART_MODE	UART mode setup Register.
	0x92	UART_CTL	UART Control Register.
	0x93	UART_DRQ	UART DRQ/IRQ register
	0x94	UART_STA	UART Status Register
	0x95	UART_TXDAT	UART TX FIFO register
	0x97	UART_RXDAT	UART RX FIFO register

8.3.4 Register Description

8.3.4.1 UART_BR

UART BAUDRATE Register.

（SFR address 0x90, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	UART_BR	UART BAUDRATE divider BaudRate = standard BaudRate/(BaudRate diveder +1)	R/W	0

8.3.4.2 UART_MODE

UART mode setup Register.

（SFR address 0x91, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:6	UART_CLK	**UART standard BaudRate select** 0 0 /select 115200 standard BaudRate 0 1 /select 115200 standard BaudRate 1 0 /select 921600 standard BaudRate 1 1 /select 1.5M standard BaudRate	R/W	00
5:4	UART_PA	**UART parity select** 00: no parity 01: no parity 10: odd parity 11: even parity	R/W	00
3	UART_STOP	**UART TX stop bits select** 0: 1 stop bit is generated. 1: 2 stop bit is generated. UART RX always just check 1 stop bit in receiving process.	R/W	0

2	-	**Reserved, be read as zero.**	-	-
1:0	UART_BW	**UART bit width select** 0 0 8 bits 0 1 7 bits 1 0 6 bits 1 1 5 bits	R/W	00

8.3.4.3 UART_CTL

UART Control Register.

（SFR address 0x92, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	UART_TX_EN	**UART TX enable** 0: disable 1: enable	R/W	0
6	UART_RX_EN	**UART RX enable** 0: disable 1: enable	R/W	0
5	U_FLOW_CTL	**UART flow control mode select** 0: normal mode 1: auto flow control mode enable UART TX/RX don't care CTS/RTS pin status in normal mode; RTS will be controlled by hardware and UART TX will be controlled by CTS in auto flow control mode;	R/W	0
4:2	-	**Reserved, read as zero.**	-	-
1	UART_RTS	**UART RTS pin status.** 0: RTS pin low status 1: RTS pin high status	R	0
0	UART_CTS	**UART CTS pin status.** 0: CTS pin low status 1: CTS pin high status	R	0

8.3.4.4 UART_DRQ

UART DRQ/IRQ control Register.

（SFR address 0x93, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	UT_DRQ_EN	**UART TX DRQ enable**, trigger DRQ when UART TX	R/W	0

		FIFO is not full. 0: disable DRQ 1: enable DRQ		
6	UR_DRQ_DN	**UART RX DRQ enable**, trigger DRQ when UART RX FIFO is not empty. 0: disable DRQ 1: enable DRQ	R/W	0
5:4	-	**Reserved**	-	-
3	UT_IRQ_EN	**UART TX IRQ enable,** trigger IRQ when UART TX FIFO is empty. 0: disable 1: enable	R/W	0
2	UR_IRQ_EN	**UART RX IRQ enable,** trigger IRQ when UART RX FIFO is not empty. 0: disable 1: enable	R/W	0
1	UT_IRQ_PD	**UART TX IRQ pending bit.** Write 1 to clear it. 0: not IRQ pending 1: IRQ pending	R/W	0
0	UR_IRQ_PD	**UART RX IRQ pending bit.** Write 1 to clear it. 0: not IRQ pending 1: IRQ pending	R/W	0

8.3.4.5 UART_STA

UART Status Register, This register is used for displaying current UART FIFO status.

（SFR address 0x94, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	TXEM	**UART TX FIFO Empty** 0: not empty 1: empty	R	1
6	TXFU	**UART TX FIFO Full** 0: not full 1: full	R	0
5	RXEM	**UART RX FIFO Empty** 0: not empty 1: empty	R	1
4	RXFU	**UART RX FIFO Full** 0: not full	R	0

		1: full		
3	UART_BUSY	**UART transmitting status bit.** The bit is automatically clear when uart finish transmitted data; and set in transmitting status automatically; 0: uart idle status 1: uart transmitting status	R	0
2	TXER	**UART TX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged. This bit set when SPI TX FIFO is wrote overflow;	R/W	0
1	RXER	**UART RX FIFO error Pending**. Writing 1 to this bit will clear it and reset the RX FIFO, otherwise unchanged. This bit set when SPI RX FIFO is wrote or read overflow;	R/W	0
0	UART_ERR	**UART received error pending bit** This bit set when RX data disobey UART parity checkout. Write 1 to clear it, otherwise unchanged.	R/W	0

8.3.4.6 UART_TXDAT

UART tx fifo register, this register is used for writing data to UART TX FIFO.

（SFR address 0x95, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	UART_TXDAT	**UART Data[7:0]** Writing this field will send 1 byte to 8bitx8 levels depth UART TX FIFO.	W	0

8.3.4.7 UART_RXDAT

UART rx fifo register, this register is used for reading data from UART RX FIFO.

（SFR address 0x97, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	UART_RXDAT	**UART Data[7:0]** Writing this field will send 1 byte to 8bitx8 levels depth UART TX FIFO.	R	0

8.4 IR

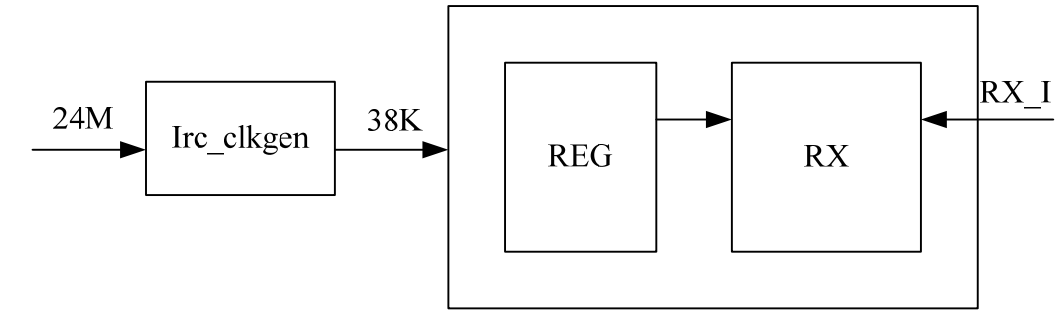
- Infrared remote control hardware decoder.
- Support three infrared remote control decode mode: Toshiba 9012 code、8 bits NEC code、Philips RC5 code.

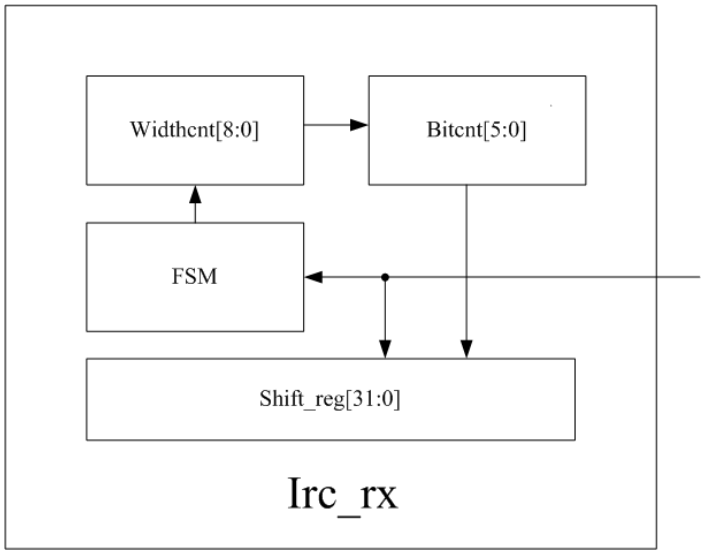
8.4.1 Function Description

IRC interface is designed according to Toshiba 9012 code timing、8 bits NEC code timing、Philips RC5 code timing.

IRC interface support MCU access to IRC data register.

8.4.2 Module Description





8.4.3 Register List

Bank	Offset	Register Name	Description
0x0a	0xa5	IR_CTL	IR Control Register
	0xa6	IR_STA	IR Status Register
	0xa7	IR_LUC	IR low user code register.
	0xa9	IR_HUC	IR high user code register.
	0xaa	IR_KDC	IR key data code register.

8.4.4 Register Description

8.4.4.1 IR_CTL

IR Control Register. This register is used for enabling IR interface, selecting IR coding mode.

（SFR address 0xa5, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	IR_EN	**IR enable** 0: IR disable. 1: IR enable.	R/W	0
6:5	IR_CODE	**IR coding mode select.** 00: 9012 code 01: 8 bits NEC code 10: RC5 code 11: Reserve	R/W	0
4	IR_IRQ	**IR IRQ enable** 0: disable 1: enable	R/W	0
3:0	-	Reserved, be read as zero.	-	-

8.4.4.2 IR_STA

IR Status Register, This register is used for displaying current IR status.

（SFR address 0xa6, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7	IR_FLAG	**IR receiving flag.** This bit is automatically clear when IR module in idle status; and automatically set in receiving status; 0: IR in idle status.	R	0

		1: IR in receiving status.		
6	IR_USER	**User code don't match pending bit.** This bit is set when IR user code don't match. Automatically clear when new user code match, 0: user code match. 1: user code not match.	R	0
5	IR_KEY	**Key data code verify error pending bit.** This bit is set when IR key data code verify error. Automatically clear when new key data code verify ok. 0: key data code verify ok. 1: key data code verify error.	R	0
4	IR_RC_OV	**IR receive overflow pending bit.** Write 1 to this bit will clear it, otherwise don't change. 0: IR receive not overflow. 1: IR receive overflow.	R/W	0
3	IR_IRQ_PD	**IR IRQ pending bit.** Write 1 to this bit will clear it, otherwise don't change. 0: not IRQ pending 1: IRQ pending	R/W	0
2:1	-	Reserved	-	-
0	IR_REP_DET	**IR repeat flag detect bit.** Write 1 to this bit will clear it, otherwise don't change. 0: repeat code is not detected. 1: repeat code is detected.	R/W	0

8.4.4.3 IR_LUC

IR low user code register.

（SFR address 0xa7, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	IR_LUC	IR user code [7:0]	R/W	0

8.4.4.4 IR_HUC

IR high user code register.

（SFR address 0xa9, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	IR_HUC	IR user code [15:8]	R/W	0

8.4.4.5 IR_KDC

IR key data code register.

（SFR address 0xaa, SFR Bank = 0x0a）

Bit(s)	Name	Description	R/W	Reset
7:0	IR_KDC	IR key data code [7:0]	R	0

9 UI

9.1 LCD Controller

- Resolution Maximum to 320x240 QVGA
- Built-in YCbCr420 to RGB conversion
- Support YCbCr420 and RGB source data format
- YCbCr Transfer Mode Via Special DMA3
- 8bit and 16bit RGB565 i8080 Interface

9.1.1 Function Description

9.1.1.1 YCbCr to RGB conversion

The output data format of JPEG Decoder is YCbCr but the LCD panel should be fulfilled with RGB data. A YCbCr to RGB color domain conversion is accomplished in LCD Controller, in the purpose of accelerating Videos and Pictures display.

9.1.1.2 DMA3 Transfer

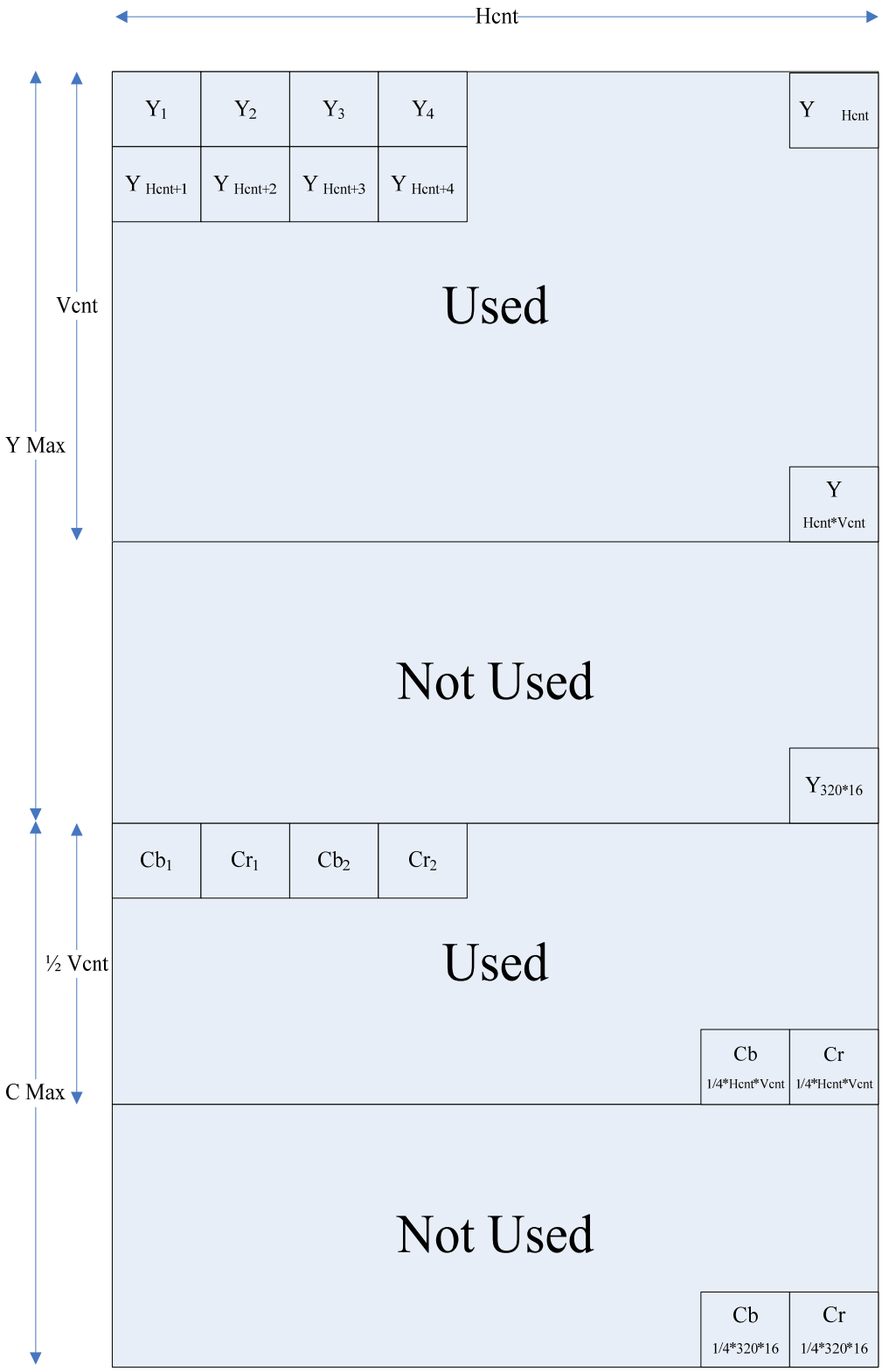
In the YCbCr mode of DMA3, to maximize the utilization of internal memory, the output data format of JPEG Decoder is YCbCr 420. The data sequence in memory before DMA3 transfer is as Figure 11.1.

YCbCr Sequence after DMA3 transfer is as Figure 11.2.

In the normal mode of DMA3, the data in ram is RGB565 format. One pixel contains two bytes RGB565 data. The pixel sequence in ram is as Figure 11.3.

The Hcnt and Vcnt determine the display range in one DMA3 transfer. The Hcnt is corresponding to the width of the image, which means that the image contains Hcnt pixels in one row. The Vcnt is the row quantities that should be transferred in one DMA3 transfer.

The maximum range that DMA3 can transfer in application is determined by the size of internal ram. The maximum size of internal ram is 320x24B=7680B=7.5kB. So when it is in highest resolution 320x240, the DMA3 can only accomplish 16 rows of pixels in one transfer when in YCbCr mode, and 12 rows of pixels when in Normal (RGB565) mode. As the horizontal resolution decreases, the DMA3 can accomplish more rows of pixels in one transfer.



YCbCr In Memory Before DMA3 Transfer

The start address of Y is configured by register DMA3_SRCADDR. The start address of Cb and Cr should be DMA3_SRCADDR+320*16, which is calculated by DMA3.

The 2x2 Y matrix shares one common Cb and Cr. For example, (Y_1, Y_2, Y_{Hcnt+1}, Y_{Hcnt+2}) share Cb_1 and Cr_1. (Y_3, Y_4, Y_{Hcnt+3}, Y_{Hcnt+4}) share Cb_2 and Cr_2. Such YCbCr sequence is so-called YCbCr 411.

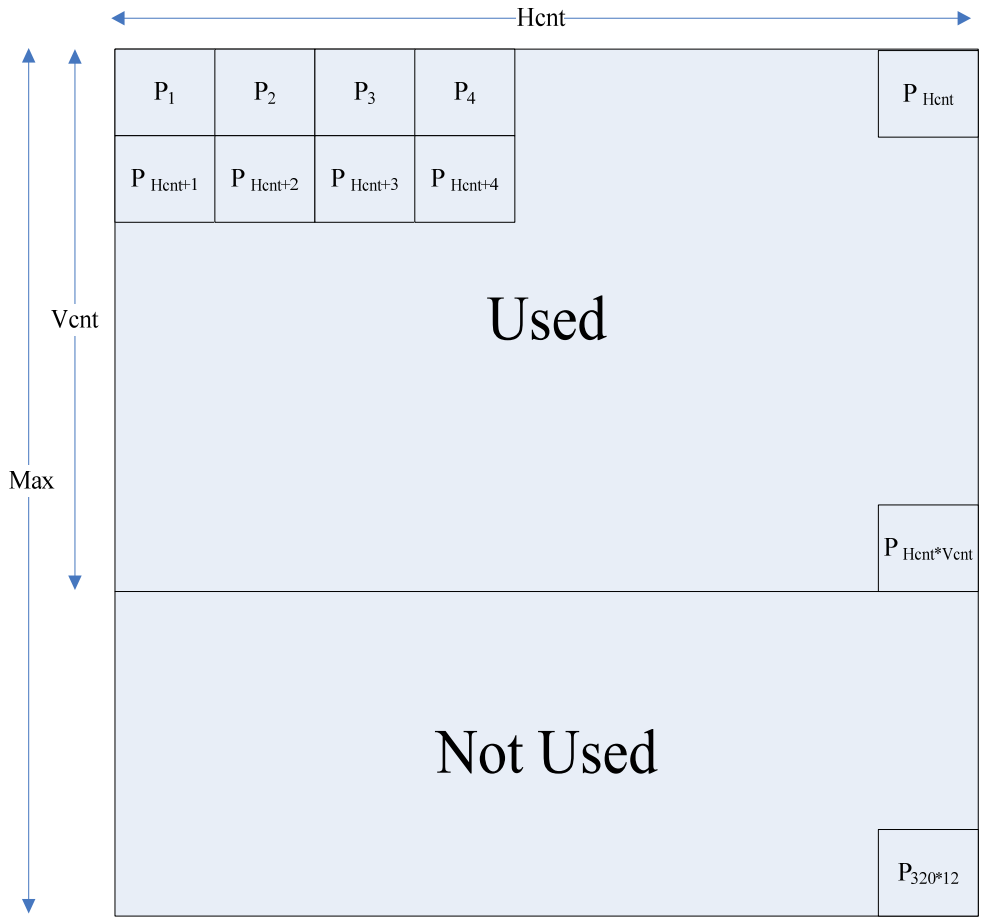
In order to preparing for the YCbCr to RGB conversion, YCbCr420 should be at least transformed to YCbCr422 sequence. This work is done by special DMA3. DMA3 transfers the data from memory to the LCD Controller through a special mode. The data sequence after DMA transfers is as below:

YCbCr 422 Sequence:

Behind----------First

CR2	CB2	Y324	Y323	CR1	CB1	Y322	Y321	.....	CR2	CB2	Y4	Y3	CR1	CB1	Y2	Y1

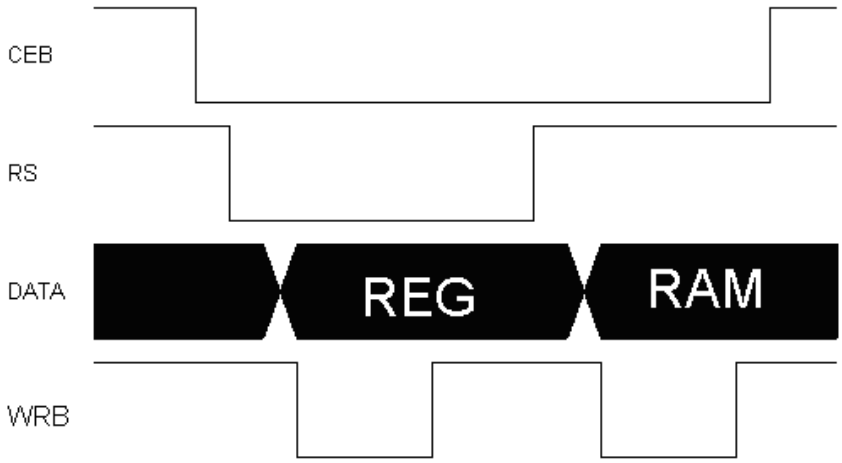
YCbCr Sequence After DMA3 Transfer (320x240 Resolution)



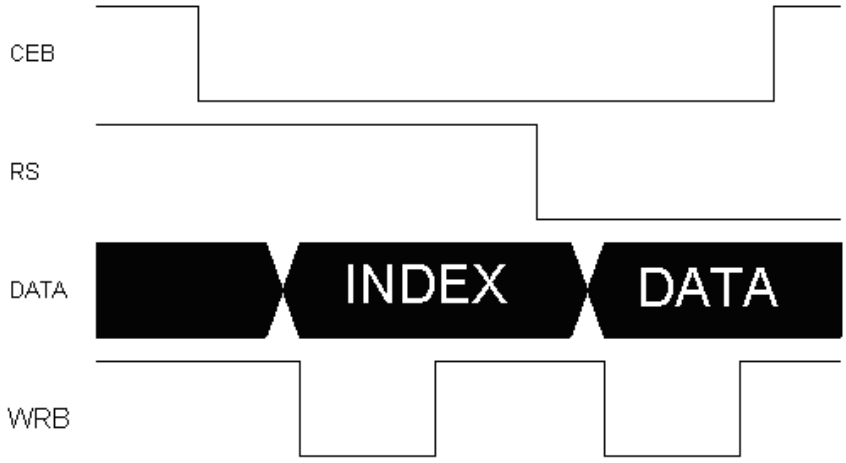
RGB565 In Memory

9.1.1.3 8bit and 16 bit Interface

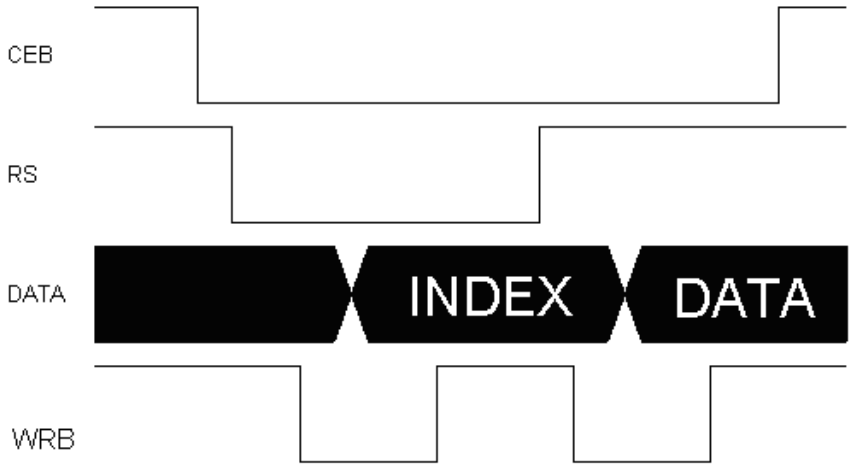
The controller supports 8 bit and 16 bit Intel 8080 interface. In 8bit I/F, one RGB565 data need be transferred in two transfers. In 16bit I/F, one RGB565 data can be transferred in one time. The timing is as below:



Write Timing（Write Register when RS=0;Write ram data when RS=1）



Write Timing（Write Command when RS=1,Write Data when RS=0）

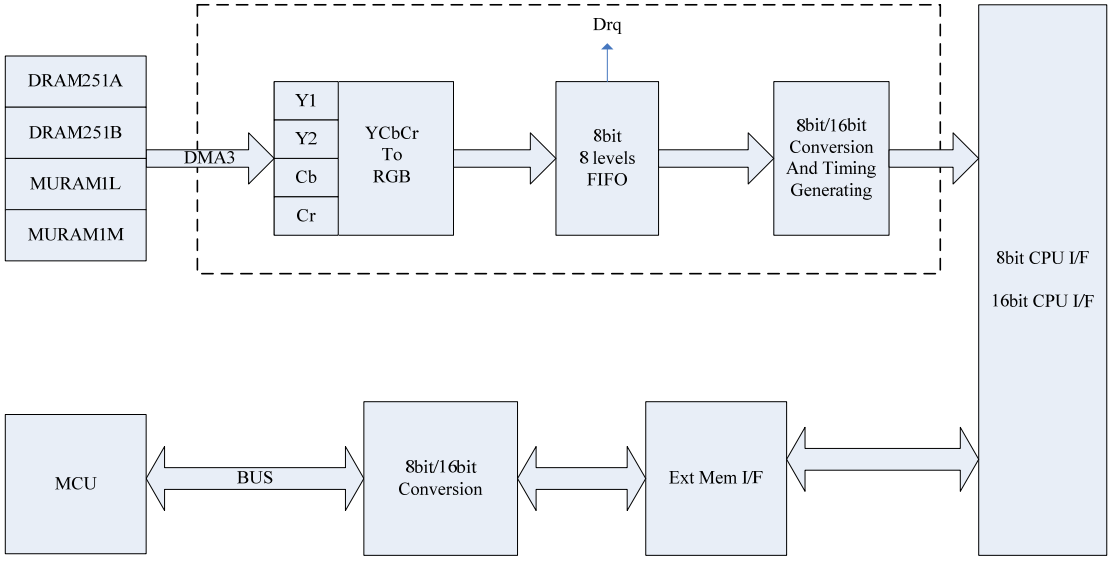


Write Timing（Write Command when RS=0,Write Data when RS=1）

The high level or the low level of the write cycle can be configured to satisfy the hold time and setup time of the LCM timing.

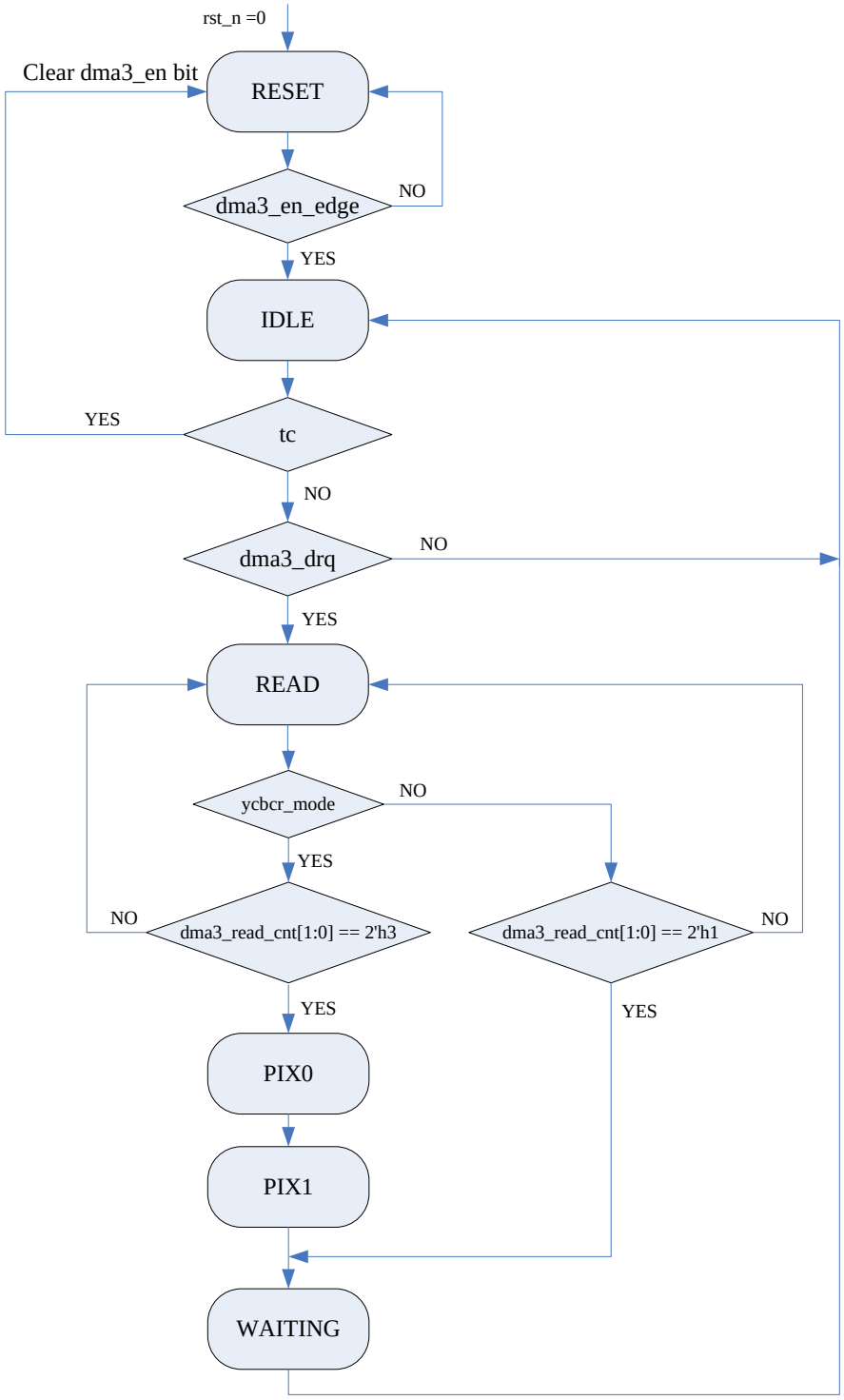
9.1.2 Module Description

9.1.2.1 Block Diagram



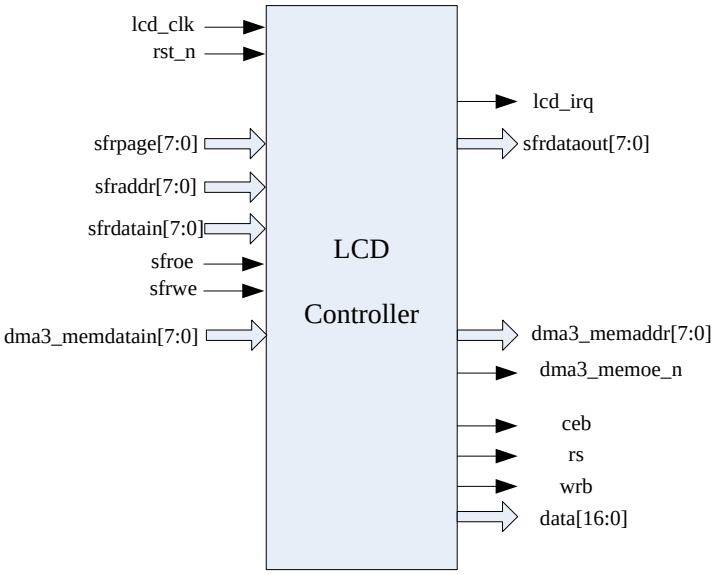
LCD Controller Block Diagram

9.1.2.2 State Machine



DMA3 State Machine

9.1.2.3 Signal List

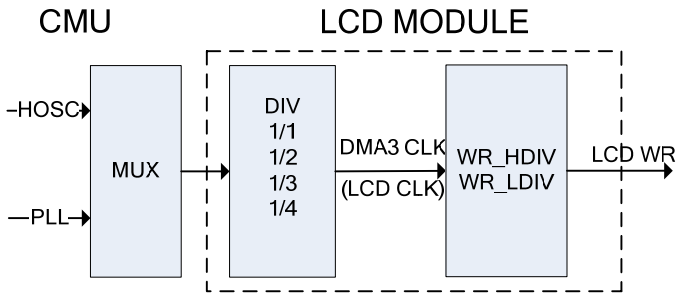


LCD Controller & DMA3 Signal

LCD Controller Interface

Name		I/O	POWER	Short Description
system interface	cpu_clk	I	VDD	CPU Clock
	lcd_clk	I	VDD	LCD Clock
	rst_n	I	VDD	LCD Module Reset
cpu interface	lcd_irq	O	VDD	LCD Interrupt Request
	Sfrpage[7:0]	I	VDD	SFR Page
	Sfraddr[7:0]	I	VDD	SFR Address Bus
	sfroe	I	VDD	SFR Read Enable
	sfrwe	I	VDD	SFR Write Enable
	Sfrdatain[7:0]	I	VDD	SFR Read Data Bus
	Sfrdataout[7:0]	O	VDD	SFR Write Data Bus
Memory interface	dma3_memaddr[15:0]	O	VDD	DMA3 Address Bus
	dma3_memoe_n	O	VDD	DMA3 Read Enable
	dma3_memdatain[7:0]	I	VDD	DMA3 Read Data Bus
Device IO interface	ceb	O	VCC	LCM Chip Select
	rs	O	VCC	LCM Register/Ram select
	wrb	O	VCC	LCM Write Eanble
	Data[15:0]	O	VCC	LCM 16bit Data Bus

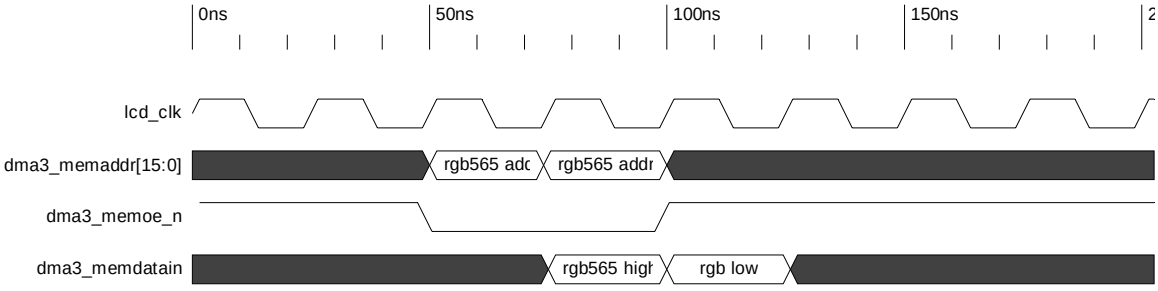
9.1.2.4 Clock Description



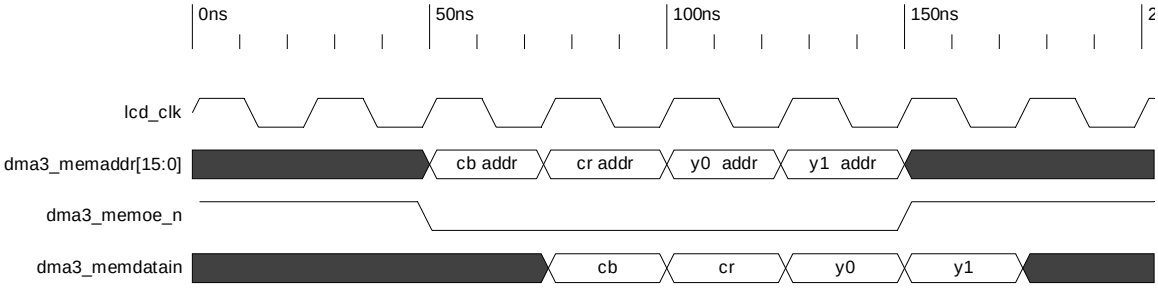
LCD Clock Description

LCD module clock comes from HOSC or PLL. The clock range of LCD module is about 10MHz to 100MHz. The frequency range of LCM interface is about 5MHz to 20MHz.

9.1.2.5 DMA Timing



DMA3 in Normal Mode



DMA3 in ycbcr Mode

9.1.2.6 DMA3

The special DMA3 moves data from RAM to temporary registers.

The DMA3 can run in YCbCr mode and Normal mode. In normal mode, DMA3 transfers the data from ram to FIFO continuously.

In YCbCr mode, YCbCr to RBG module can read YCrCb from temporary register 4 bytes per transfer. While it is in normal mode, YCbCr is bypassed, and the data in temporary registers are transferred directly to FIFO also 4 bytes per transfer.

Once DMA3 had detected the DRQ, it starts to transfer 4 bytes to fulfill the temporary register. After transfer, DMA3 returns to IDLE and detect the DRQ.

9.1.2.7 YCbCr to RGB

After JPEG decoding, the data format in SRAM is YCbCr, and then transferred to LCD through DMA3. The LCM can only support RGB color domain, a YCbCr to RGB conversion should be done by hardware automatically. This function should be optional in the case of transferring RGB565 data format from RAM directly to LCM interface.

The conversion principle is as below:

R=Y+1.402*(Cr-128)

G=Y-0.34414*(Cb-128)-0.71414*(Cr-128)

B=Y+1.772*(Cb-128)

One Y1Y2CB1CR1 data can be transformed into one two RGB888 data. And then RGB888 are shrunk into RGB565 to be suit for the LCM interface.

Y1CB1CR1 is corresponding to the first pixel; Y2CB1CR1 is corresponding to the second pixel, and so on.

The YCbCr to RGB function can be disabled through setting the register bit. When disabled, the data from FIFO goes directly to the 8bit/16bit conversion and then the LCM interface.

9.1.2.8 FIFO

The FIFO width is 8bit, and has 8 levels. The 8-levels-FIFO can be fulfilled with 4 pixels data as buffer when it is full.

When the FIFO is not empty, the timing generator will fetch data from FIFO and generate the corresponding timing and interface continuously.

When the FIFO is half empty, drq request will be sent to DMA3 for data transfer require.

In one DMA3 transfer, there are 4 bytes data corresponding in the FIFO which fulfill the half of it.

As a whole, the LCD controller generates the corresponding timing, and at the same time the DMA3 transfer data to LCD controller while the FIFO is half empty.

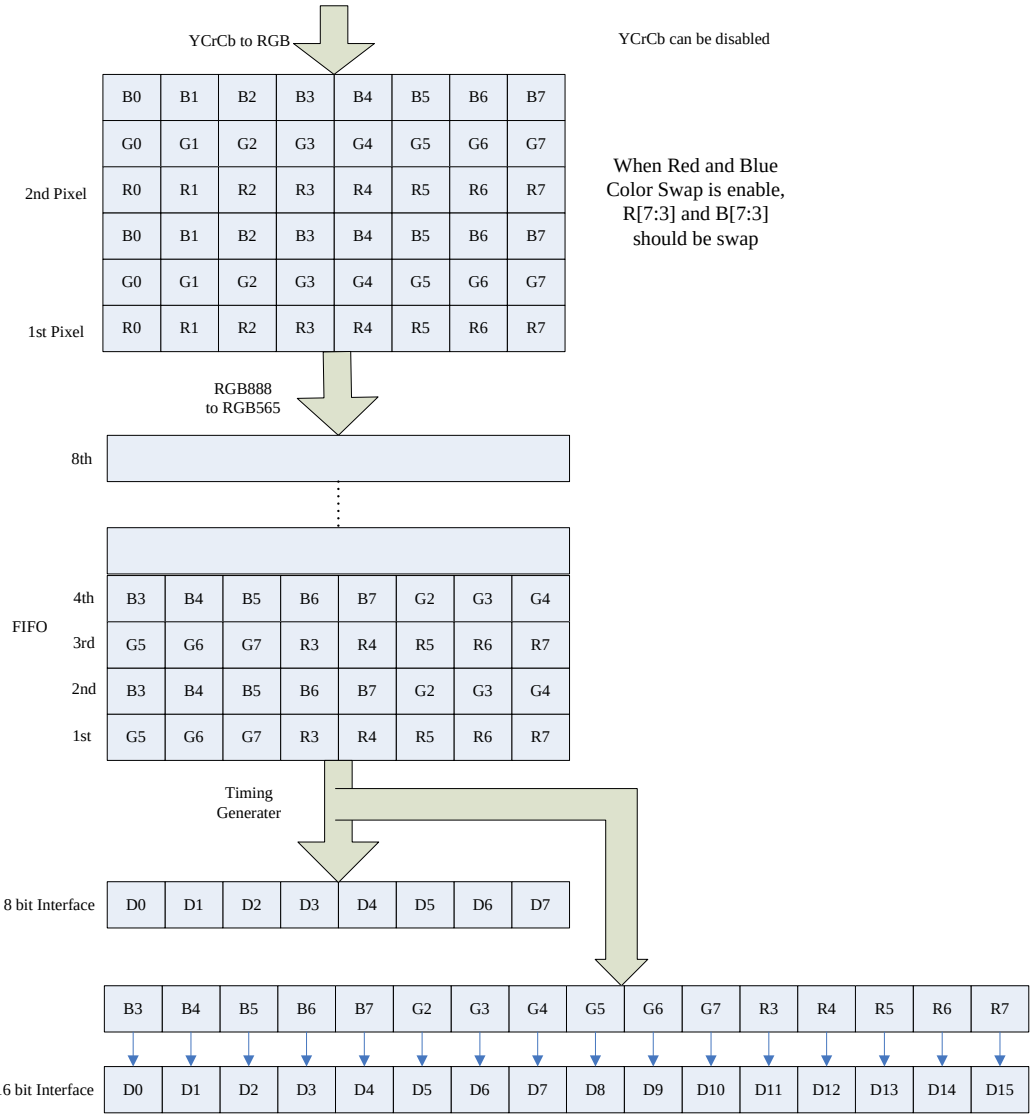
9.1.2.9 8bit/16bit Conversion & Timing Generating

This module will fetch data from the FIFO one byte by one byte.

When the LCM is 8bit interface, the LCD controller should only send the data from YcbCr conversion or directly from FIFO to the interface in one writing cycle.

When the LCM is 16bit interface, the LCD controller should combine every two 8bit data into 16 bit and send it to the interface in one writing cycle.

9.1.2.10 Data Flow and Interface



Data Flow and Interface In LCD Controller

9.1.2.11 The extended CPU bus

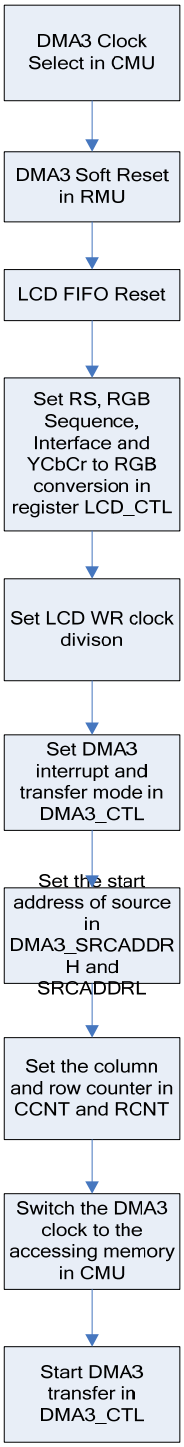
CPU can write or read through two SFR to access the extended bus. If write or read the lower-byte SFR, the bus accesses the lower 8bit data bus. If write the lower-byte SFR first, and then the higher-byte, the bus writes 16bit data bus. If read the higher-byte SFR first，and then the lower-byte, the bus reads 16bits data bus.

9.1.2.12 The LCD Debug Signals

{DebugC[7:2],DebugB[1:0]}={frst_edge,lcd_irq,trans,dma3_drq,dma3_en_edge,dma3_state[2:0]};

9.1.3 Operation Manual

9.1.3.1 Software Operation Flow



9.1.4 Register List

LCD Controller Registers Address

Name	SFR Page	Base Address
LCD_CTL	0x06	0x98

LCD Controller Registers

Address	Register Name	Description
0x98	LCD_CTL	LCD Control Register
0x99	LCD_IF_CLK	LCD Interface Clock Register
0x9a	DMA3_CTL	DMA3 Control Register
0x9b	DMA3_SRCADDRH	DMA3 SRC Address High Register
0x9c	DMA3_SRCADDRL	DMA3 SRC Address Low Register
0x9d	DMA3_CCNTH	DMA3 Column Higher Counter Register
0x9e	DMA3_CCNTL	DMA3 Column Lower Counter Register
0x9f	DMA3_RCNT	DMA3 Row Counter Register

9.1.5 Register Description

9.1.5.1 LCD_CTL

LCD Control Register (0x06: 0x98)

Bit(s)	Name	Description	R/W	Reset
7::6	-	Reserved	R	00
5	DMA3_EN	DMA3 enable bit 0:Disable 1:Start The rise edge of this bit will start the DMA3 transfer, then the DMA3 will load the byte counter and source address.	R/W	0
4	RS_SEL	RS select 0:RS output low voltage level 1:RS output high voltage level RS is low or high voltage in the case of writing INDEX/DATA/REG in different LCM	R/W	0
3	FRST	FIFO Reset	R/W	0

		0: FIFO Normal Operation 1: FIFO Reset		
2	RGB_SEQ	Red and Blue color Swap 0:Swap Disable（RGB） 1:Swap Enable （BGR） The sequence of RGB565 maybe different in sorts of LCM	R/W	0
1	IF_SEL	LCM Interface Select 0:8bit Interface 1:16bit Interface	R/W	0
0	CNV_EN	YcbCr to RGB Conversion Enable 0:Disable 1:Enable When the conversion is disabled, DMA3 can write through FIFO straight to 8bit or 16 bit interface When the DMA3 is in Normal mode (DMA3_CTL_BIT3=0), this bit should be guaranteed to be 0 by software.	R/W	0

9.1.5.2 LCD_IF_CLK

LCD Interface Clock Register (0x06:0x99)

Bit(s)	Name	Description	R/W	Reset
7:4	WR_HDIV	Wr Clock High Level Cycle Division (From LCD Clock) The actual divisor is WR_HDIV+1	R/W	0x0
3:0	WR_LDIV	Wr Clock Low Level Cycle Division (From LCD Clock) The actual divisor is WR_LDIV+1	R/W	0x0

9.1.5.3 DMA3_CTL

DMA3 Control Register (0x06: 0x9a)

Bit(s)	Name	Description	R/W	Reset
7:6	CLKDIV	Clock Divisor for Module Clock division from PLL or HOSC 00: 1/1 01: 1/2 10: 1/3	R/W	0x0

		11: 1/4		
5	HTCPD	DMA3 Half Transfer Complete IRQ pending 0:No IRQ 1:IRQ Write 1 to this bit to clear it	R/W	0x0
4	TCPD	DMA3 Transfer Complete IRQ pending 0:No IRQ 1:IRQ Write 1 to this bit to clear it	R/W	0x0
3	MODE	DMA3 Transfer mode select 0:Normal mode 1:YcbCr mode	R/W	0x0
2	HTC_IRQ	DMA3 Half Transfer Complete IRQ enable 0:Disable 1:Enable	R/W	0x0
1	TC_IRQ	DMA3 Transfer Complete IRQ enable 0:Disable 1:Enable	R/W	0x0
0	TRANS	Transfer Finish Flag 0:Transfer not finish 1:Transfer finish This bit indicates whether the interface on pins, such as Data, Wr, RS and CE, has accomplished the transfer timing. This bit will be cleared to “0” automatically when DMA3_EN is detected rise edge.	R	0x1

P.S. When in RGB565 transfer mode and lcd clock is 3 times (or above) as cpu clock, ([CCNTH,CCNTL]+1)*(RCNT +1) must be more than 2 pixels (4bytes)，or the DMA3 transfer complete pending bit can not be set to 1 and software can not detect the transfer accomplishment.

9.1.5.4 DMA3_SRCADDRH

DMA3 SRC Address High Register (0x06: 0x9b)

Bit(s)	Name	Description	R/W	Reset
7:0	SRCADDRL	DMA3 Source Address High byte	R/W	0x0

9.1.5.5 DMA3_SRCADDRL

DMA3 SRC Address Low Register (0x06:0x9c)

Bit(s)	Name	Description	R/W	Reset

7:0	SRCADDRM	DMA3 Source Address Low byte	R/W	0x0

9.1.5.6 DMA3_CCNTH

DMA3 Column Higher Counter Register (0x06: 0x9d)

Bit(s)	Name	Description	R/W	Reset
7:1	-	Reserved	R	0x0
0	CCNTH	DMA3 Column Higher counter	R/W	0x0

9.1.5.7 DMA3_CCNTL

DMA3 Column Lower Counter Register (0x06: 0x9e)

Bit(s)	Name	Description	R/W	Reset
7:0	CCNTL	DMA3 Column Lower counter	R/W	0x0

P.S. The actual value of column counter is [CCNTH, CCNTL]+1

9.1.5.8 DMA3_RCNT

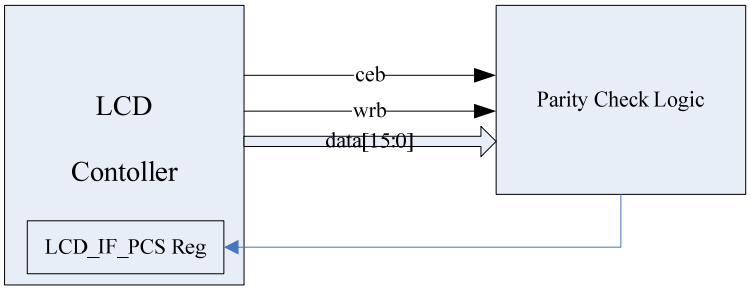
DMA3 Row Counter Register (0x06: 0x9f)

Bit(s)	Name	Description	R/W	Reset
7:0	RCNT	DMA3 Row counter The actual value of Row counter is RCNT+1	R/W	0x0

P.S. All the column and row counters are calculated by pixels. One pixel is corresponding to two bytes.

E.g. the resolution of LCD is 320x240 pixels, and the DMA3 can transfer 320x12 pixels in one time. So the [DMA3_CNTH+DMA3_CNTL+1] should be 319, the DMA3_RCNT should be 11. The transfer amount in byte is (319+1)*(11+1)*2=7.5k bytes.

9.1.5.9 Block Diagram



LCD Controller Test Mode

9.1.5.10 Signal Description

LCD Signal List

Name		I/O	POWER	Short Description
System Interface	lcd_clk	I	VDD	LCD Clock
	rst_n	I	VDD	LCD Module Reset
LCD Controller interface	ceb	I	VDD	LCM Chip Select
	wrb	I	VDD	LCM Write Eanble
	Data[15:0]	I	VDD	LCM 16bit Data Bus

10 GPIO & I/O Multiplexer

- Built-in Pull-up and Pull-low resistance
- Different level of static driving current and dynamic driving capacity control
- Flexible alternation of multifunction
- PWM Available frequency range from 7.8Hz~2KHz and 5.8kHz~1.5MHz
- PWM 16 levels duty occupancy adjusting

10.1 Function Description

In ATS2505, several different kinds of function signals share the common IO pads. The multifunction is used to alternate the function of the IO pads which are driven by different module.

When the pad is used as digital function, the priority of GPIO is higher than other digital functions. Once the OUTEN or INEN is set to “1”, the PAD is used as GPIO output or input function, no matter what the MFPSEL setting is.

10.1.1 Multifunction View

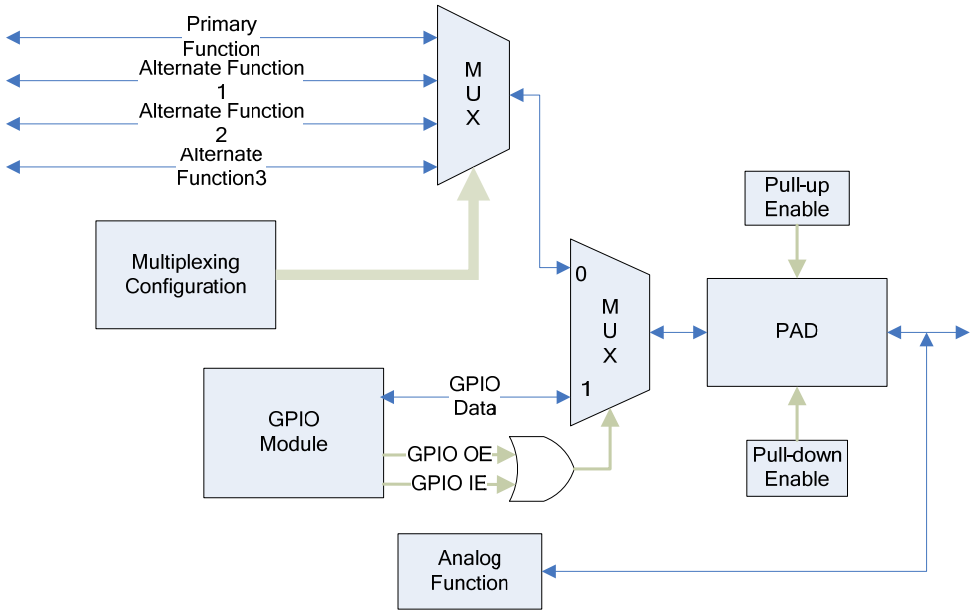
Priority0>Priority1

Mode 1		
Analog	Digital Function	
	Priority0	Priority1
	GPIO_A0	FMCLKOUT
	GPIO_A2	SIRQ0/PWM
	GPIO_A7	EM_CEB5/LCD_CEB
	GPIO_B2	EM_RDB
	GPIO_B3	EM_WRB/LCDWRB
	GPIO_B4	LCD_RS/EM_RS/UART_TX
	GPIO_B5	UART_RX
	GPIO_B7	SIRQ1
	GPIO_C0	I2C_SCL/UART_CTS/IR_RX
	GPIO_C1	I2C_SDA//UART_RTS/EM_RS/LCD_RS/PWM
	GPIO_C4	SPI_SS
	GPIO_C5	SPI_MISO/ EM_CEB2

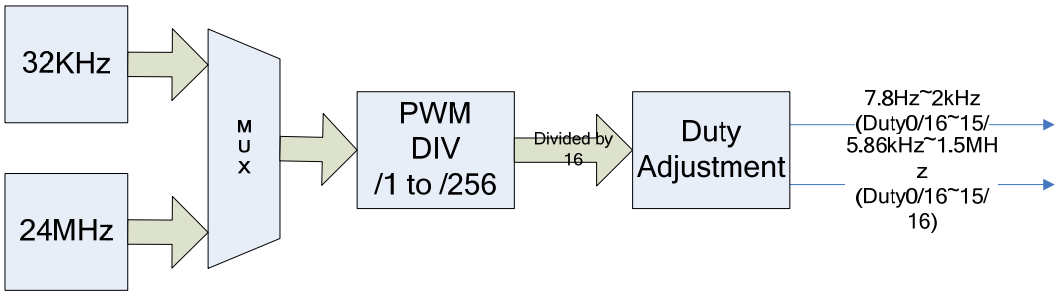
	GPIO_C6	SPI_MOSI/ EM_CEB3/UART_TX/EJ_TCK
	GPIO_C7	SPI_SCLK/ EM_CEB4/UART_RX
	GPIO_D0	EM_D0/LCD_D0
	GPIO_D1	EM_D1/LCD_D1
	GPIO_D2	EM_D2/LCD_D2
	GPIO_D3	EM_D3/LCD_D3
	GPIO_D4	EM_D4/LCD_D4
	GPIO_D5	EM_D5/LCD_D5
	GPIO_D6	EM_D6/LCD_D6
	GPIO_D7	EM_D7/LCD_D7
	GPIO_E1	MMC_CMD/MS_BS
	GPIO_E3	MMC_CLK1/MS_CLK
VCCOUT	GPIO_E4	When P_VS7=1:MS_CLK/IR_RX/FMCLKOUT/ When P_VS7=0, SPI_SS
	GPIO_E7	
	GPIO_F0	MMC_D0/MSD0/EM_D8/LCD_D8/EM_D0/LCD_D0
	GPIO_F1	MMC_D1/MSD1/EM_D9/LCD_D9/EM_D1/LCD_D1
	GPIO_F2	MMC_D2/MSD2/EM_D10/LCD_D10/EM_D2/LCD_D2
	GPIO_F3	MMC_D3/MSD3/EM_D11/LCD_D11/EM_D3/LCD_D3
	GPIO_F5	SD5/LCD_D13/D5 /LRADC3
	GPIO_F6	SD6/LCD_D14/D6 /LRADC4
	GPIO_F7	SD7/LCD_D15/D7 /LRADC5
	GPIO_G1	
	GPIO_G3	
	GPIO_G4	
SDVCCOUT	GPIO_G5	LCM_RST
	GPIO_G6	

10.2 Module Descriptions

10.2.1 Block Diagram



Multifunction Block Diagram



PWM Block Diagram

10.2.2 GPIO

The GPIOs can output high voltage level or low voltage level when OUTEN is enable. When INEN is enable, GPIOs can be used as input for detecting the voltage level through watching the GPIO DAT registers.

The GPIOs are assorted to several driving capacity. Select the proper driving current before using it.

P.S GPIOs have higher priority than other digital functions no matter when they are used as output or input. Once the pad is used as digital function and the Output Enable or Input Enable of GPIOs are set to “1”, the corresponding pad are used as GPIO function.

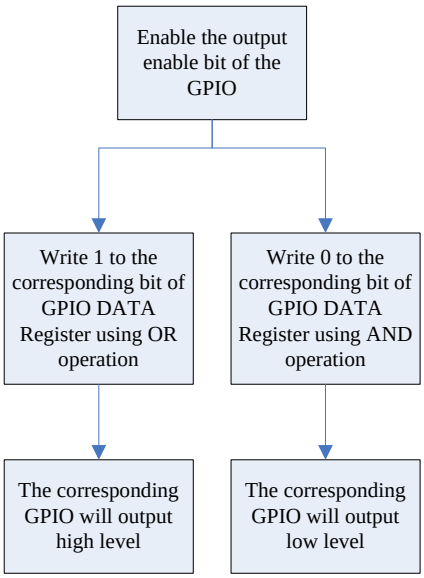
10.2.3 PWM

The PWM module divides the source frequency and adjusst the duty occupancy according to the active polarity (High level active or Low level active)、frequency dividing and duty setting. Note that 16 level duty adjustment needs a 16 times frequency as a reference. E.g. A 2K PWM output with 16 level duty adjustments needs 32Khz as a reference. There are totally 16 adjusting level for each frequency, which can meet most PWM backlight IC application.

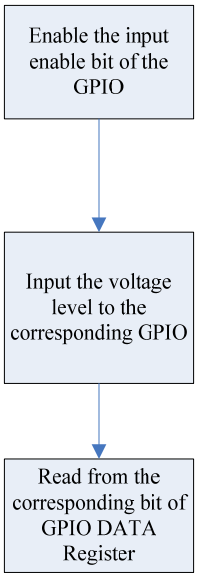
10.3 Operation Manual

10.3.1 Operation Flow for Software

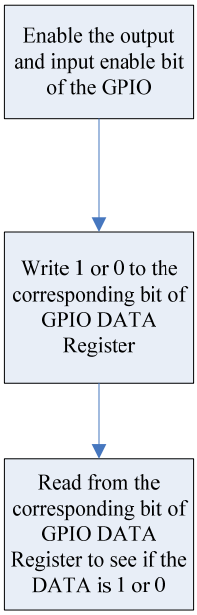
10.3.1.1 GPIO output Voltage Level



10.3.1.2 GPIO Input Voltage Level



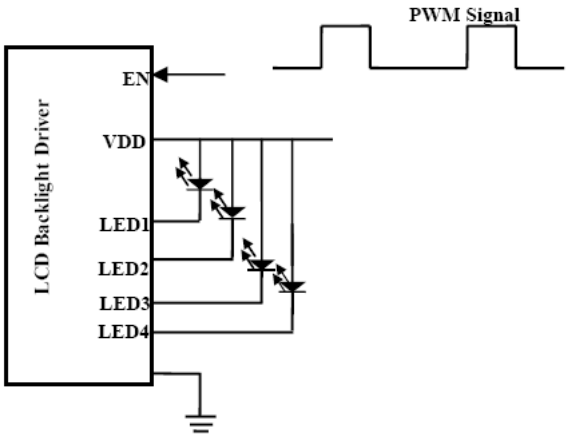
10.3.1.3 GPIO Output/Input Loop Test



10.3.2 Operation Manual for Hardware

10.3.2.1 PWM Back Light Control

The application diagram is as follows:



The PWM signal outputted from ATS2505 controls the Enable signal of LCD backlight driver IC. So the driver IC is modulated by the PWM. The higher the duty occupancy of PWM signal, the

brighter the LCD displays. In other words, changing the PWM duty can change the brightness of the LCD.

The maximum frequency of PWM signal is relevant to the switch speed of the backlight IC and the LED. If the frequency is too high, backlight IC and the LED can not have enough time to switch, so that the change of brightness is not obvious through adjusting of PWM duty occupancy.

10.4 Register List

Bank	Adrress	Register Name	Description
0x06	0xa2	GPIOAOUTEN	General Purpose Input Output Group A Output Enable
0x06	0xa3	GPIOAINEN	General Purpose Input Output Group A Input Enable
0x06	0xa4	GPIOADAT	General Purpose Input Output Group A Data
0x06	0xa5	GPIOBOUTEN	General Purpose Input Output Group B Output Enable
0x06	0xa6	GPIOBINEN	General Purpose Input Output Group B Input Enable
0x06	0xa7	GPIOBDAT	General Purpose Input Output Group B Data
0x06	0xa9	GPIOCOUTEN	General Purpose Input Output Group C Output Enable
0x06	0xaa	GPIOCINEN	General Purpose Input Output Group C Input Enable
0x06	0xab	GPIOCDAT	General Purpose Input Output Group C Data
0x06	0xac	GPIODOUTEN	General Purpose Input Output Group D Output Enable
0x06	0xad	GPIODINEN	General Purpose Input Output Group D Input Enable
0x06	0xae	GPIODDAT	General Purpose Input Output Group D Data
0x06	0xaf	GPIOEOUTEN	General Purpose Input Output Group E Output Enable
0x06	0xb0	GPIOEINEN	General Purpose Input Output Group E Input Enable
0x06	0xb1	GPIOEDAT	General Purpose Input Output Group E Data
0x06	0xb2	GPIOFOUTEN	General Purpose Input Output Group F Output Enable
0x06	0xb3	GPIOFINEN	General Purpose Input Output Group F Input Enable
0x06	0xb4	GPIOFDAT	General Purpose Input Output Group F Data
0x06	0xc6	PWMDUTY	PWM Control Register
0x06	0xc7	PWMDIV	PWM Clock Divide Register
0x06 0x08	0xca	MFPSEL0	Multifunction select 0 Register
0x06 0x08	0xcb	MFPSEL1	Multifunction select 1 Register
0x06	0xcc	MFPSEL2	Multifunction select 2 Register
0x06	0xcd	MFPSEL3	Multifunction select 3 Register
0x06	0xce	MFPSEL4	Multifunction select 4 Register
0x06	0xcf	MFPSEL5	Multifunction select 5 Register

0x08			
0x06	0xd2	MFPSEL6	Multifunction select 6 Register

10.5 Register Description

10.5.1 GPIO_A Output Enable Register

GPIOAOUTEN (0x06:0xA2)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOAOUTEN	GPIO_A[7:0] Output enable 0: Disable, 1: Enable.	R/W	00h

10.5.2 GPIO_A Input Enable Register

GPIOAINEN (0x06:0xA3)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOAINEN	GPIO_A[7:0] Input enable 0: Disable, 1: Enable.	R/W	00h

10.5.3 GPIO_A Data Output/Input Register

GPIOADAT (0x06:0xA4)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOADAT	GPIO_A[7:0] Output/Input Data	R/W	00h

10.5.4 GPIO_B Output Enable Register

GPIOBOUTEN (0x06:0xA5)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOBOUTEN	GPIO_B[7:0] Output enable 0: Disable, 1: Enable.	R/W	00h

10.5.5 GPIO_B Input Enable Register

GPIOBINEN (0x06: 0xA6)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOBINEN	GPIO_B[7:0] Input enable 0: Disable, 1: Enable.	R/W	00h

10.5.6 GPIO_B Data Output/Input Register

GPIOBDAT (0x06:0xA7)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOBDAT	GPIO_B[7:0] Output/Input Data	R/W	00h

10.5.7 GPIO_C Output Enable Register

GPIOCOUTEN (0x06:0xA9)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOCOUTEN	GPIO_C[7:0] Output enable, 0: Disable, 1: Enable.	R/W	00h

10.5.8 GPIO_C Input Enable Register

GPIOCINEN (0x06:0xAA)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOCINEN	GPIO_C[7:0] Input enable 0: Disable, 1: Enable.	R/W	00h

10.5.9 GPIO_C Data Output/Input Register

GPIOCDAT (0x06:0xAB)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOCDAT	GPIO_C[7:0] Output/Input Data	R/W	00h

10.5.10 GPIO_D Output Enable Register

GPIODOUTEN (0x06:0xAC)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIODOUTEN	GPIO_D[7:0] Output enable 0: Disable, 1: Enable.	R/W	00h

10.5.11 GPIO_D Input Enable Register

GPIODINEN (0x06:0xAD)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIODINEN	GPIO_D[7:0] Input enable 0: Disable, 1: Enable.	R/W	00h

10.5.12 GPIO_D Data Output/Input Register

GPIODDAT (0x06:0xAE)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIODDAT	GPIO_D[7:0] Output/Input Data	R/W	00h

10.5.13 GPIO_E[7:0] Output Enable Register

GPIOEOUTEN (0x06:0xAF)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOEOUTEN	GPIO_E[7:0] Output Enable 0: Disable, 1: Enable	R/W	00h

10.5.14 GPIO_E[7:0] Input Enable Register

GPIOEINEN (0x06:0xB0)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOEINEN	GPIO_E[7:0] Input Enable 0: Disable, 1: Enable	R/W	00h

10.5.15 GPIO_E[7:0] Data Output/Input Register

GPIOEDAT (0x06:0xB1)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOEDAT	GPIO_E[7:0] Output/Input Data	R/W	00h

10.5.16 GPIO_F[7:0] Output Enable Register

GPIOFOUTEN (0x06:0xB2)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOFOUTEN	GPIO_F[7:0] Output Enable 0: Disable, 1: Enable	R/W	00h

10.5.17 GPIO_F[7:0] Input Enable Register

GPIOFINEN (0x06:0xB3)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOFINEN	GPIO_F[7:0] Input Enable 0: Disable, 1: Enable	R/W	00h

10.5.18 GPIO_F[7:0] Data Output/Input Register

GPIOFDAT (0x06: 0xB4)

Bit(s)	Name	Description	R/W	Reset
7:0	GPIOFDAT	GPIO_F[7:0] Output/Input Data	R/W	00h

10.5.19 PWM Duty Control Register

PWMDUTY (0x06:0xC6)

Bit(s)	Name	Description	R/W	Reset
7:5	-	Reserved	R/W	000
4	POL	**Active Polarity Select.** 0:The PWM is High level active	R/W	0

		1:The PWM is Low level active		
3:0	DUTY	**Active Duty Occupancy.** 0000: 0/16 0001: 1/16 0010: 2/16 0011: 3/16 0100: 4/16 0101: 5/16 0110: 6/16 0111: 7/16 1000: 8/16 1001: 9/16 1010: 10/16 1011: 11/16 1100: 12/16 1101: 13/16 1110: 14/16 1111: 15/16	R/W	**1000**

10.5.20 PWM Clock Divide Register

PWMDIV (0x06:0xC7)

Bit(s)	Name	Description	R/W	Reset
7:0	DIV	Choose the divisor for PWM clock dividing The PWM Clock is PWM source clock/(DIV+1)	R/W	00h

P.S. The PWM output frequency is PWM source clock/ (DIV+1)/16.

PWM Source clock includes LOSC (32K) and CK24M.

10.5.21 Multifunction Select 0 Register

MFPSEL0 (0x06/0x08: 0xCA)

Bit(s)	Name	Description	R/W	Reset
7	GPIOB2MFP	GPIOB2 Multifunction Select 0:Reserved	R/W	0

		1:EM_RDB (External Memory I/F Read)		
6:5	GPIOB3MFP	GPIOB3 Multifunction Select 00: Reserved 01: EM_WRB (External Memory I/F Write) 10: LCD_WRB (LCD Write) 11: Reserved	R/W	00
4	GPIOB5MFP	GPIOB5 Multifunction Select 0: Reserved 1: UART_RX	R/W	0
3	GPIOB7MFP	GPIOB7 Multifunction Select 0: reserved 1: SIRQ1	R/W	0
2	Reserved	Reserved	Reserved	
1:0	GPIODMFP	GPIOD[7:0] Multifunction Select 00: Reserved 01: EM_D[7:0] (External Memory I/F Data[7:0]) 10: LCD_D[7:0] (LCD Data[7:0]) 11: Reserved	R/W	00

10.5.22 Multifunction Select 1 Register

MFPSEL1 (0x06/0x08: 0xCB)

Bit(s)	Name	Description	R/W	Reset
7:2	Reserved	Reserved	Reserved	000000
1:0	GPIOB4MFP	GPIOB4 Multifunction Select 00: Reserved 01: LCD_RS 10: EM_RS 11: UART_TX	R/W	00

10.5.23 Multifunction Select 2 Register

MFPSEL2 (0x06: 0xCC)

Bit(s)	Name	Description	R/W	Reset
7	GPIOA7MFP	GPIOA7 Multifunction Select 0:EM_CEB5	R/W	0

		1:LCD_CEB		
6:5	GPIOA2MFP	GPIOA2 Multifunction Select 00:SIRQ0 01:MS_BS 10:PWM 11:Reserved	R/W	00
4:3	Reserved	Reserved	R/W	00
2	FMCLKEN	FM clock enable: 0:FMCLKOUT Output Disable（clock gating） 1:FMCLKOUT Output Enable	R/W	0
1:0	FMCLKSEL	FM Clock Output Select 00: FM Clock Output LOSC. 01: FM Clock Output CK24M. 10: FM Clock Output MCUPLL/10.（7.6MHz） 11: FM Clock Output MCUPLL/4. (13MHz)	R/W	00

10.5.24 Multifunction Select 3 Register

MFPSEL3 (0x06: 0xCD)

Bit(s)	Name	Description	R/W	Reset
7	GPIOE1MFP	GPIOE1 Multifunction Select 0:MMC_CMD 1:MS_BS	R/W	0
6	GPIOE3MFP	GPIOE3Multifunction Select 0:MMC_CLK1 1:MS_CLK	R/W	0
5:3	GPIOF03MFP	GPIOF[3:0] Multifunction Select 000:MMC_D[3:0] 001:MSD[3:0] 010:EM_D[11:8] 011:LCD_D[11:8] 100:EM_D[3:0] 101:LCD_D[3:0] Others: Reserved	R/W	000
2:0	GPIOF47MFP	GPIOF[7:4] Multifunction Select 000:MMC_D[7:4] 001:MSD[3:0]	R/W	000

		010:EM_D[15:12] 011:LCD_D[15:12] 100:EM_D[7:4] 101:LCD_D[7:4] 110: Reserved 111: Reserved		

10.5.25 Multifunction Select 4 Register

MFPSEL4 (0x06: 0xCE)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	R/W	1
6	LRADC5	LRADC5 Mapping Enable 0:GPIOF7 is used as digital function, which depends on REG06CDH[1:0] (MFPSEL3_BIT[1:0]) including GPIO function. 1;GPIOF7 is used as LRADC5 (Analog Function)	R/W	0
5	LRADC4	LRADC4 Mapping Enable 0:GPIOF6 is used as digital function, which depends on REG06CDH[1:0] (MFPSEL3_BIT[1:0]) including GPIO function. 1;GPIOF6 is used as LRADC4 (Analog Function)	R/W	0
4	LRADC3	LRADC3 Mapping Enable 0:GPIOF5 is used as digital function, which depends on REG06CDH[1:0] (MFPSEL3_BIT[1:0]) including GPIO function. 1;GPIOF5 is used as LRADC3 (Analog Function)	R/W	0
3	FMVCCMFP	GPIOE4 Multifunction Select 0: Disable digital function. GPIOE4 is used as FMVCCOUT. 1: Enable digital function. GPIOE4 is used as GPIO, EJ_TDO, MS_CLK,IR_RX,FMCLKOUT or SPI_SS, which depends on MFPSEL5_BIT[5:4]	R/W	1
2	SDVCCMFP	GPIOG5 Multifunction Select 0: Disable digital function. GPIOG5 is used as SDVCCOUT. 1: Enable digital function. GPIOG5 is used as	R/W	0

		UART_CTS, IR_RX (depending on MFPSEL4_BIT1) or GPIO.		
1	GPIOG5MFP	GPIOG5 Multifunction Select 0:IR_RX 1:UART_CTS P.S. When GPIOG5 is used as digital function (IR_RX , UART_CTS or GPIO), the analog function must be disable.(REGA405H[1:0]=00), and the digital function must be enable (REG06CEH2=1)	R/W	0
0	Reserved	Reserved	Reserved	0

10.5.26 Multifunction Select 5 Register

MFPSEL5 (0x06/0x08: 0xCF)

Bit(s)	Name	Description	R/W	Reset
7:6	-	Reserved	R/W	00
5:4	GPIOE4MFP	GPIOE4 Multifunction Select 00:MS_CLK 01:IR_RX 10:FMCLKOUT 11:Reserved P.S. When P_VS7=0, GPIOE4 is used as SPI_SS, all the functions above are disable.	R/W	00
3:2	GPIOC5MFP	GPIOC5 Multifunction Select 00:SPI_MISO 01:Reserved 10:EM_CEB2 11:Reserved	R/W	00
1:0	GPIOC67MFP	GPIOC[7:6] Multifunction Select 00: GPIOC6——> SPI_MOSI GPIOC7——> SPI_SCLK 01: GPIOC6——> Reserved GPIOC7——> Reserved 10: GPIOC6——> EM _CEB3 GPIOC7——> EM _CEB4 11: GPIOC6——>UART_TX	R/W	00

		GPIOC7——> UART_RX P.S. When GPIOC[7:6] is used as UART_RX/UART_TX, GPIOC[3:2] can not be used as UART_RX/UART_TX, which is guaranteed by hardware.		

10.5.27 Multifunction Select 6 Register

MFPSEL6(0x06:0xD2)

Bit(s)	Name	Description	R/W	Reset
7	-	Reserved	R/W	1
6:5	-	Reserved	R/W	0
4:2	GPIOC1MFP	GPIOC1 Multifunction Select 000: I2C_SDA 001: UART_RTS 010: EM_RS 011: LCD_RS 100: PWM Others:Reserved	R/W	000
1:0	GPIOC0MFP	GPIOC0 Multifunction Select 00:I2C_SCL 01:UART_CTS 10:IR_RX 11:Reserved	R/W	00

11 Electrical Characteristics

11.1 11.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Ambient Temperature	Tamb	25	-10~+70	℃
Storage Temperature	Tstg	25	-55~+150	℃

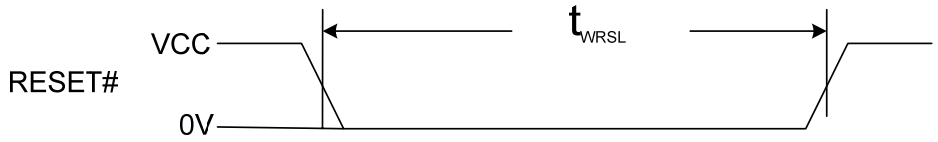
Input Voltage	+3.3V IO	3.1	-0.3~3.6	V
Supply voltage	BAT	3.8	-0.3~5.5	V
	DC5V	5	-0.3~5.5	V
	VCC/AVCC/PAVCC	3.1	-0.3~3.6	V
	VDD	1.7	-0.3~2.0	V
	RTCVDD	1.6	-0.3~2.0	V

Note:

1) Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
2) All voltage values are with respect to GND
3) +3.3V IO/+1.8V IO are defined in the Pin list.
4) According to different application, the VDD voltage can config differently. For optimum CPU perfomance, the VDD should be higher than 1.6V; for reduced the power consumption, the VDD can supply with 1.6V.

11.2 Reset Parameter

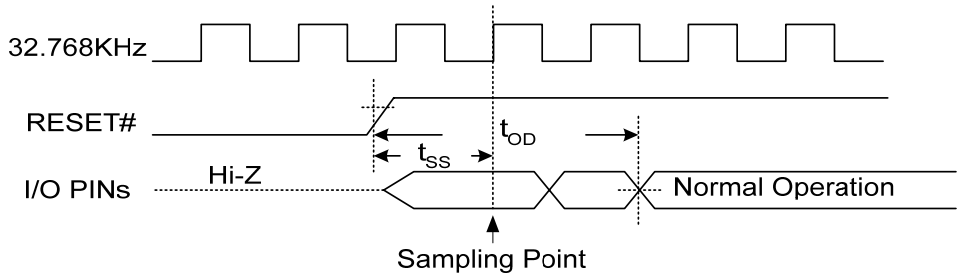
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	50	—	us



Reset Timing

11.3 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data Sampling Time (from RESET#)	t_{SS}		—	61.04	us
Output delay time (from RESET#)	t_{OD}		61.04	—	us



Initialization Timing

11.4 USB DC Electrical Characteristics

Input Level for Low/Full speed：

Parameter	Symbol	Min	Max	Units
HIGH	VIH	2.0		V
LOW	VIL		0.8	V
Differential Input Sensitivity	VDI	0.2		V
Differential Common Mode Range	VCM	0.8	2.5	V

Input Level for High speed

Parameter	Symbol	Min	Max	Units
High-speed squelch detection threshold (differential signal amplitude)	VHSSQ	100	150	mV
High-speed disconnect detection threshold (differential signal amplitude)	VHSDSC	525	625	mV
High-speed data signaling common mode voltage range (guideline for receiver)	VHSCM	-50	500	mV

Output Level for Low/Full speed

Parameter	Symbol	Min	Max	Units
HIGH	VOH	2.8	3.6	V
LOW	VOL	0.0	0.3	V
SE1	VOSE1	0.8		V
Output Signal Crossover	VCRS	0.8	2.5	V

Voltage				

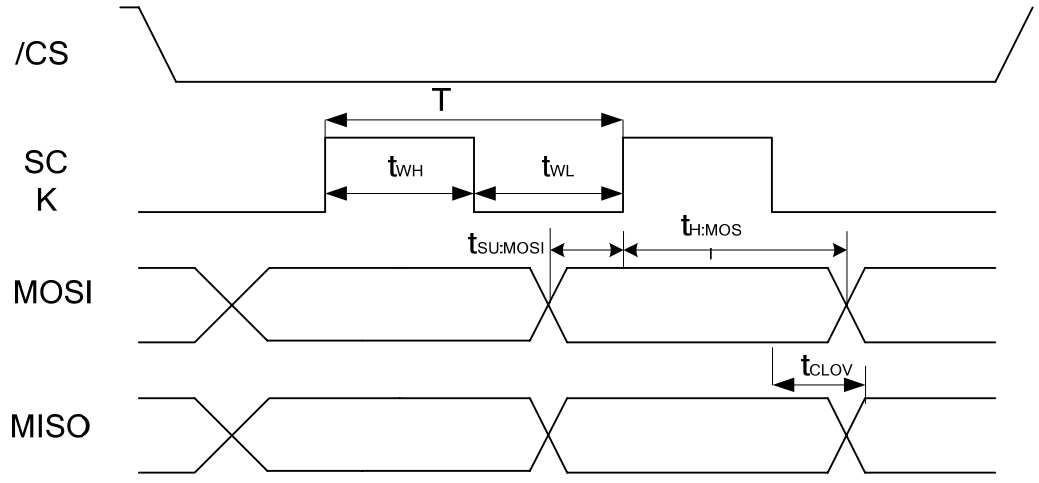
Output Level for High Speed

Parameter	Symbol	Min	Max	Units
High-speed idle level	VHSOI	-10.0	10.0	mV
High-speed data signaling high	VHSOH	360	440	mV
High-speed data signaling low	VHSOL	-10.0	10.0	mV
Chirp J level (differentialvoltage)	VCHIRPJ	700	1100	mV
Chirp K level (differential voltage)	VCHIRPK	-900	-500	mV

Terminations

Parameter	Symbol	Min	Max	Units
Bus Pull-up Resistor on Upstream Facing Port	RPU	1.425	1.575	kΩ
Bus Pull-down Resistor on Downstream Facing Port	RPD	14.25	15.75	kΩ
Input impedance exclusive of pullup/pulldown (for low-/full-speed)	ZINP	300		kΩ
Termination voltage for upstream facing port pullup (RPU)	VTERM	3.0	3.6	V

11.5 SPI Interface Electrical Parameter



SPI timing

Parameter	Symbol	MIN	TYP	MAX	Unit

SCK Clock	fclk	-	24	60	MHz
SCK High time	t_{WH}	8	21	-	ns
SCK Low time	t_{WL}	8	21	-	ns
SCK rise time	t_r	-	0.5	-	ns
SCK fall time	t_f	-	0.6	-	ns
Data output setup time	$t_{SU:MOSI}$	-	2	-	ns
Data output hold time	$t_{H:MOSI}$	-	24	-	ns
Clock low to output valid	t_{CLOV}	-	-	9	ns

11.6 UART Timing Fault-tolerant Parameter

For UART's baud rate of 3 standards, the error rate measurements are as follows:

115200 Standard Baut Rate			
Baut Rate	**Theoretical Bit Width (us)**	**Practical Bit Width (us)**	**Error Rate**
1200	833	832	0.12%
2400	416.67	416	0.16%
3600	277.8	277.5	0.11%
4800	208.33	208	0.15%
7200	138.8	138.8	0
9600	104.17	104	0.16%
14400	69.4	69.3	0.14%
19200	52.08	52	0.15%
28800	34.7	34.65	0.14%
38400	26.04	26	0.15%
57600	17.36	17.35	0.05%
115200	8.68	8.66	0.02%

921600 **Standard Baut Rate**			
Baut Rate	**Theoretical Bit Width (us)**	**Practical Bit Width (us)**	**Error Rate**
3600	277.8	277.5	0.11%
4800	208.33	208	0.16%
7200	138.8	138.8	0
9600	104.17	104	0.16%

14400	69.4	69.3	0.14%
19200	52.08	52	0.15%
28800	34.7	34.7	0
38400	26.04	26	0.15%
57600	17.36	17.32	0.23%
115200	8.68	8.66	0.23%
230400	4.34	4.33	0.23%
460800	2.17	2.165	0.23%
921600	1.085	1.084	0.1%

1.5M Baut Rate			
Baut Rate	**Theoretical Bit Width (us)**	**Practical Bit Width (us)**	**Error Rate**
7200	138.8	138.8	0
9600	104.17	104	0.16%
14400	69.4	69.3	0.14%
19200	52.08	52	0.15%
28800	34.7	34.65	0.14%
38400	26.04	26	0.15%
57600	17.36	17.34	0.12%
115200	8.68	8.68	0
750000	1.33	1.334	0.3%
1500000	0.667	0.666	0.15%

11.7 IR Timing fault-tolerant parameter

	Min	TYP	Max	Unit
Infrared wave carrier frequency	36	38	40	Khz

11.8 MS Card Interface AC Parameter

Table 1 Characteristics of the Serial Interface

Measurement conditions : VCC=2.7~3.6[V],Ta=-5~65[℃]

Signal	Parameter	Symbol	Rating	Unit

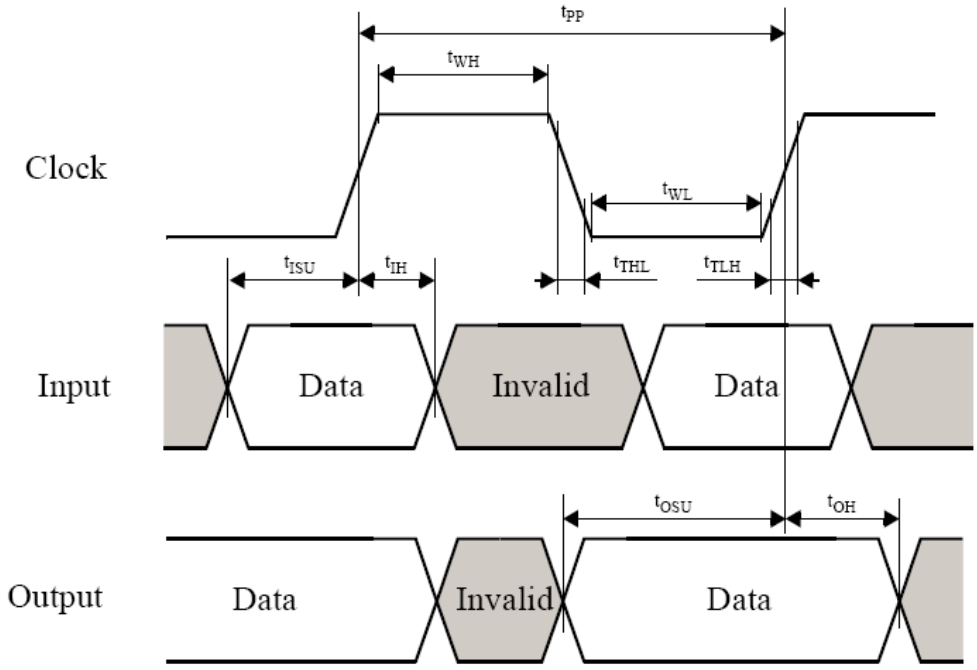
			Min.	Max	
SCLK	Period	tSCLKc	50	-	nsec
	H pulse width	tSCLKwh	15	-	nsec
	L pulse width	tSCLKwl	15	-	nsec
	Rising time	tSCLKr	-	10	nsec
	Falling time	tSCLKf	-	10	nsec
BS	Setup time	tBSsu	5	-	nsec
	Hold time	tBSh	5	-	nsec
	Rising time	tBSr	-	10	nsec
	Falling time	tBSf	-	10	nsec
DATA	Setup time	tDsu	5	-	nsec
	Hold time	tDh	5	-	nsec
	Rising time	tDr	-	10	nsec
	Falling time	tDf	-	10	nsec
	Output delay time	tDd	-	15	nsec

Characteristics of the Parallel Interface

(Measurement conditions : VCC=2.7~3.6[V],Ta=-5~65[℃]

Signal	Parameter	Symbol	Rating		Unit
			Min.	Max	
SCLK	Period	tSCLKc	25	-	nsec
	H pulse width	tSCLKwh	5	-	nsec
	L pulse width	tSCLKwl	5	-	nsec
	Rising time	tSCLKr	-	10	nsec
	Falling time	tSCLKf	-	10	nsec
BS	Setup time	tBSsu	8	-	nsec
	Hold time	tBSh	1	-	nsec
	Rising time	tBSr	-	10	nsec
	Falling time	tBSf	-	10	nsec
DATA	Setup time	tDsu	8	-	nsec
	Hold time	tDh	1	-	nsec
	Rising time	tDr	-	10	nsec
	Falling time	tDf	-	10	nsec
	Output delay time	tDd	-	15	nsec

11.9 SD Card Interface AC Parameter



3.3V Signaling Default Speed Timing

Threshold Level for 3.3V Voltage Range

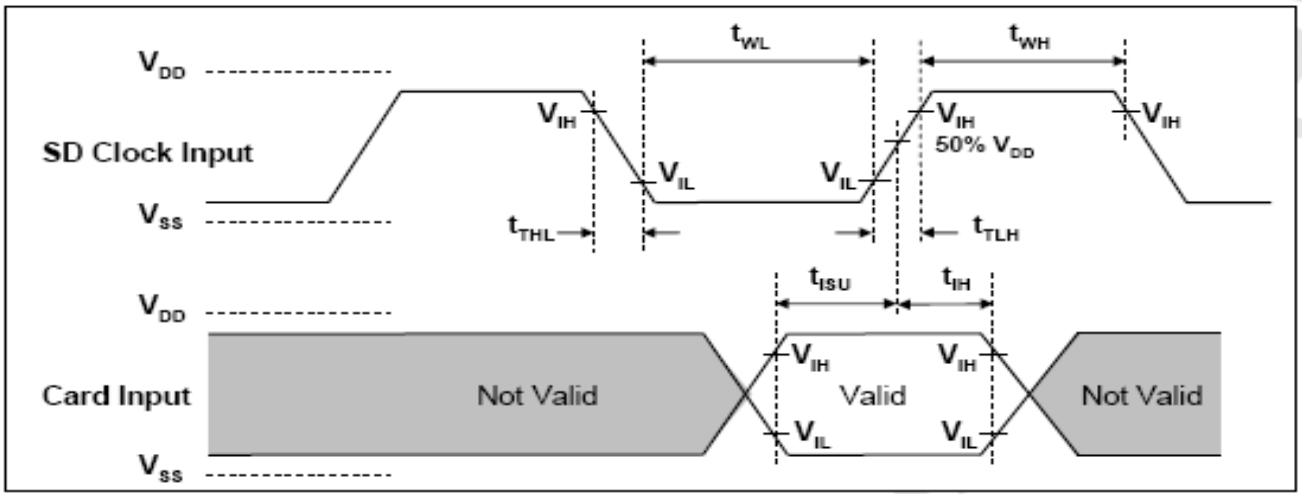
Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	2.7	3.6	V	
Output high voltage	VOH	0.625*VDD	VDD+0.3	V	
Output low voltage	VOL	VSS-0.3	0.25VDD	V	
In put high voltage	VIH	0.75VDD		V	IOH=-2mA
Input low voltage	VIL		0.125VDD	V	IOL=2mA
Power up time			250	ms	From 0 to VDD min

CL=CHost+Cbus+Ccard

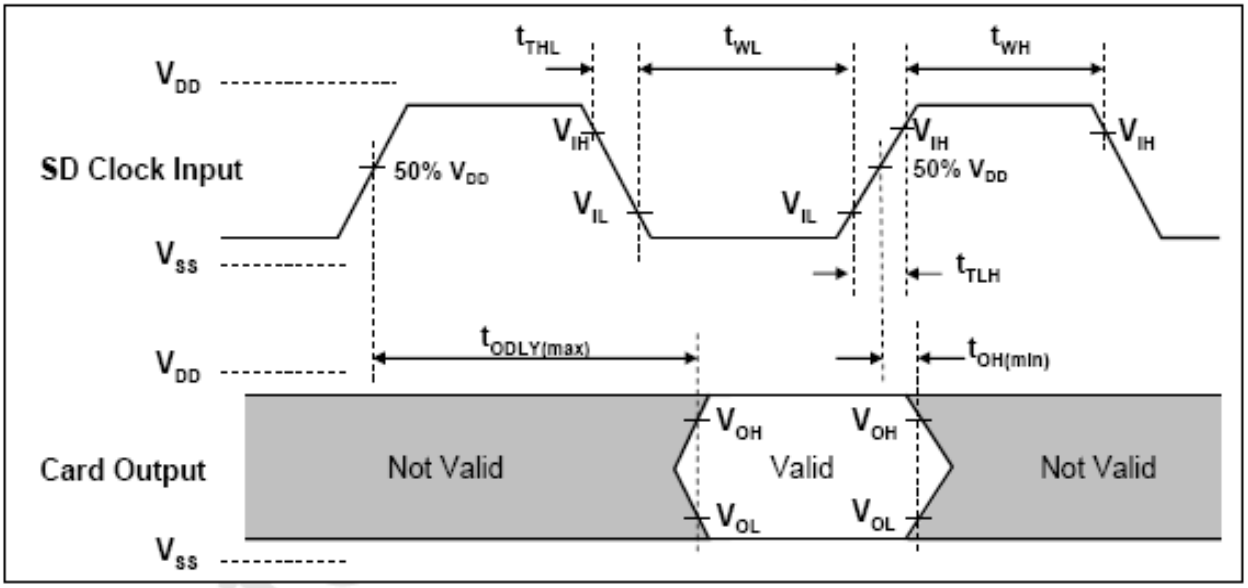
3.3V signals timing Default speed mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	25/26	MHz	CL<=30pF(tolerance +100KHz)
Clock frequency identification Mode(Open	fOD	0	400	KHz	Tolerance:+20KHz

Drain)					
Clock low time	tWL	10		ns	Chost+Cbus<=30pf
Clock low time	tWH	10		ns	Chost+Cbus<=30pf
Clock rise time	tTLH		10	ns	Chost+Cbus<=30pf
Clock fall time	tTHL		10	ns	Chost+Cbus<=30pf
Inputs CMD DAT(reference to CLK)					
Input setup time	tISU	3		ns	CL<=30pF
Input hold time	tIH	3		ns	CL<=30pF
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	5		ns	CL<=30pF
Output hold time	tOH	5		ns	CL<=30pF



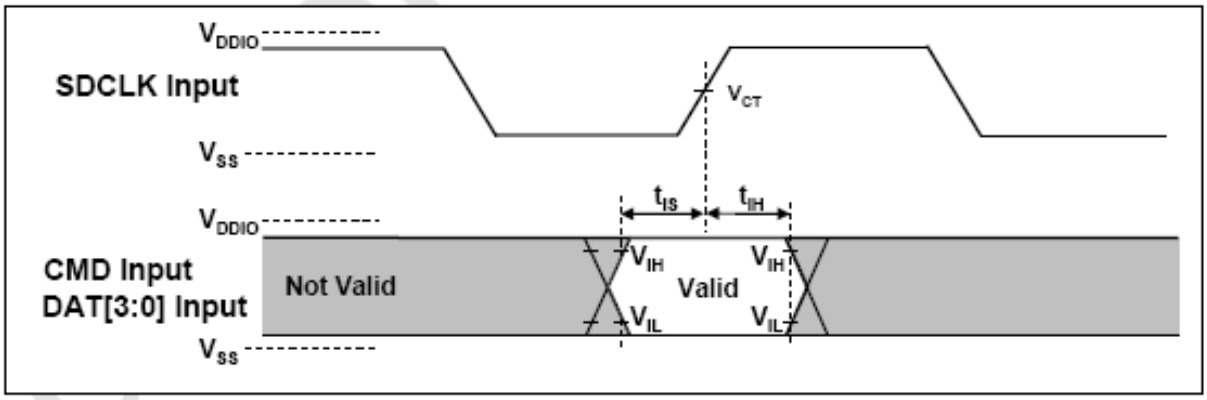
3.3V Signaling High Speed Card Input Timing (SDC Output)



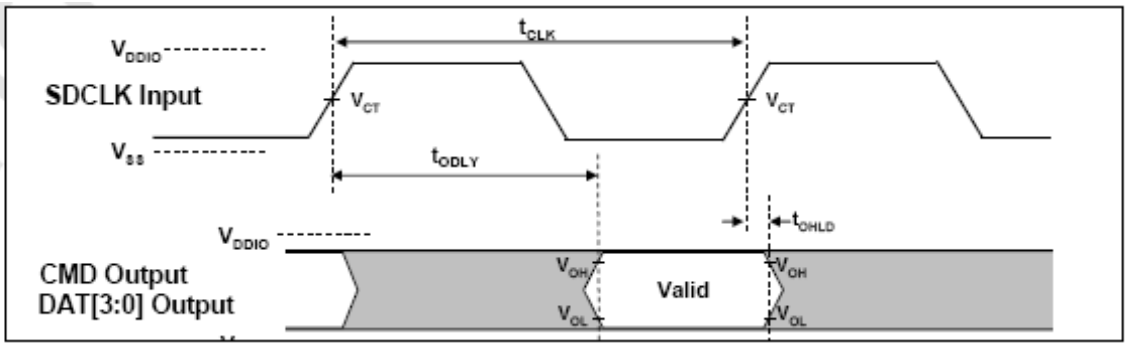
3.3V Signaling High Speed Card Output Timing.(SDC Input)

3.3V Signals Timing High Speed Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	50/52	MHz	CL<=30pF(tolerance +100KHz)
Clock frequency identification Mode(Open Drain)	fOD	0	400	KHz	Tolerance:+20KHz
Clock low time	tWL	7		ns	Chost+Cbus<=30pf
Clock low time	tWH	7		ns	Chost+Cbus<=30pf
Clock rise time	tTLH		3	ns	Chost+Cbus<=30pf
Clock fall time	tTHL		3	ns	Chost+Cbus<=30pf
Peak voltage on all lines		-0.3	0.3	V	
Inputs CMD DAT(reference to CLK)					
Input setup time	tISU	6-delay		ns	CL<=30pF
Input hold time	tIH	2.5		ns	CL<=30pF
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	6		ns	CL<=30pF
Output hold time	tOH	2		ns	CL<=30pF



SRD50 Card Input Timing.(SDC Output)



SRD50 Card Output Timing.(SDC Input)

Threshold Level for 1.8V Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	2.7	3.6	V	
Output high voltage	VOH	1.27	2.0	V	
Output low voltage	VOL	Vss-0.3	0.58	V	
In put high voltage	VIH	1.4		V	IOH=-2mA
Input low voltage	VIL		0.45	V	IOL=2mA

CL=CHost+Cbus+Ccard

1.8V Signals Timing SDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	100	MHz	CL<=30pF(tolerance +100KHz)

Clock duty	tWL	30	70	%	
Clock low time	tWH			ns	
Clock rise time	tTLH		2	ns	Ccard=10pf
Clock fall time	tTHL		2	ns	Ccard=10pf
Inputs CMD DAT(reference to CLK)					
Input setup time	tISU	2.5		ns	CL=30pF,
Input hold time	tIH	0.5		ns	CL=15pf
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	3		ns	Ccard=10pf,Vct=0.975V
Output hold time	tOH	0.8		ns	Ccard=5pf,Vct-0.975V

Bus Signal Line Load

Parameter	Symbol	Min	Normal	Max	Unit	Remark
Pull up resistance for CMD	Rcmd	4.7	50	100	KOhm	To prevent bus floating
Pull up resistance for dat0-7	Rdat	50	50	100	KOhm	To prevent bus floating
Bus signal line capacitance	CL			30	pF	Single card
Signal card capacitance	Ccard			7	pF	
Maximum signal line inductance				16	nH	

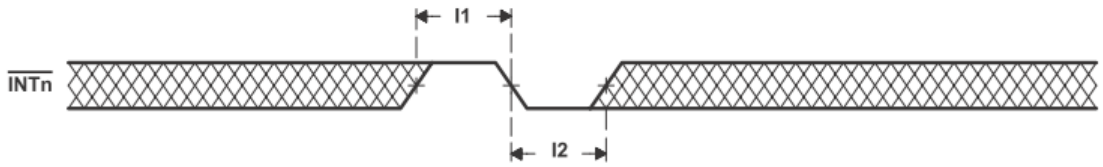
CL=CHost+Cbus+Ccard CHost+Cbus<=30pf

11.10 External Interrupt Timings

The table below assumes testing over recommended operating conditions.

NO.		ATS2505	UNIT
I1	$tW_{(INTH)}$ A Pulse width, interrupt high, CPU active	2P	ns
I2	$tW_{(INTL)}$ A Pulse width, interrupt low, CPU active	2P	ns

NOTE: P = 1/CPU clock frequency in ns. For example, when running parts at 50 MHz, use P = 20 ns.



External Interrupt Timing Requirements

11.11 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T_O = 25℃, VCC = 0 V.

11.12 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -8mA	0.9*VCC			V
Low-level output voltage	V_{OL}	I_{OL} = 8mA			0.1*VCC	V
High-level input voltage	V_{IH}		0.6*VCC		VCC+0.6	V
Low-level input voltage	V_{IL}		-0.3		0.4*VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V		±25		uA
Tri-State leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V		±25		uA
GPIO Drive	Idrive1			8		mA
	Idrive2			12		mA
	Idrive3			16		mA

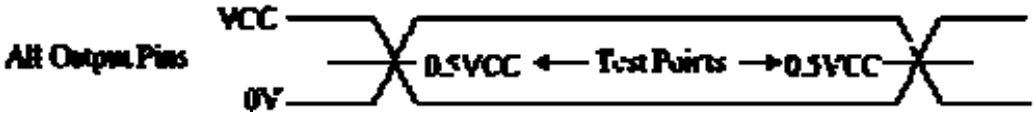
NOTES:
1. T_o = -10 to +70℃, VDD = 1.6 V, VCC = 3.0 V
2. GPIO should not be floating in order to reduce the standby current, refer to the Application Note for the detailed information.
3. There are three types of GPIO drives ranging from 5mA to 15mA, refer to the Section 3.8 for the detailed information.

11.13 AC Characteristics

T_o = -10 to +70℃

11.14 AC Test Input Waveform

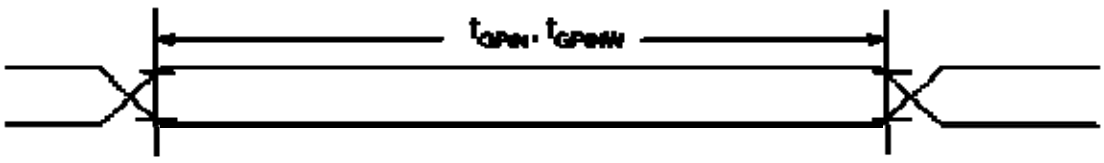
11.15 AC Test Output Measuring Points



11.16 GPIO Interface Parameter

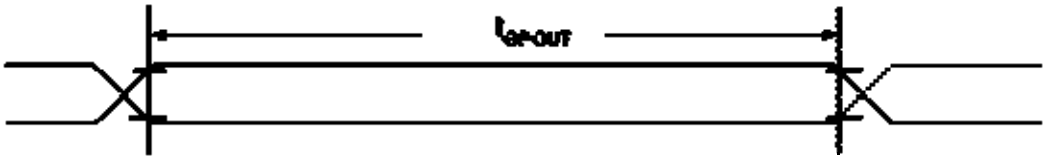
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$8/f_{mcuclk}$		s
GPIO output rise time(@50pf)	t_{GPRISE}		5	20	ns
GPIO output fall time(@50pf)	t_{GPFALL}		5	20	ns
Output level width	t_{GPOUT}		$8/f_{mcuclk}$		s

Notes 1. f_{MCUCLK} is the frequency that MCU is running upon.



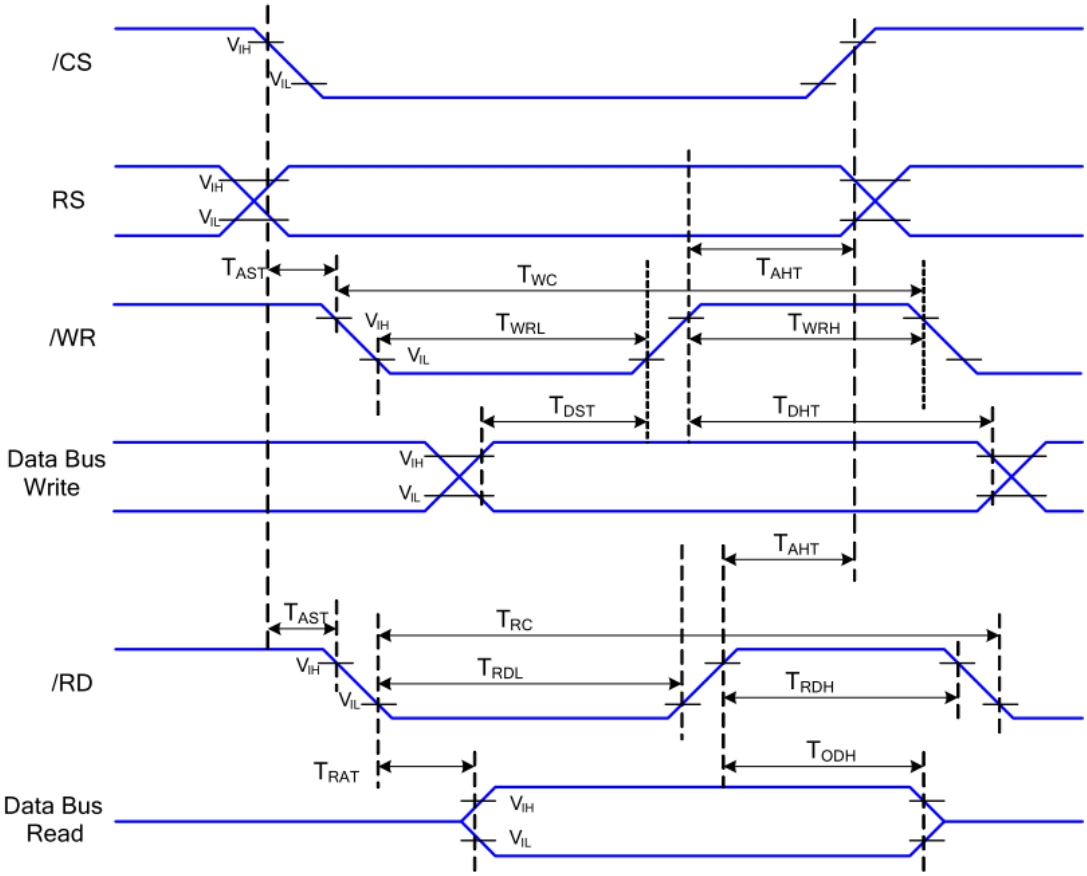
Input Level Width

Output Rise/Fall Time



Output Level Width

11.17 LCM Driver Parameter



LCM Interface Timing

LCM Driver Parameter

Signal	Symbol	Parameter	Condition	Min	Max	Unit
RS	T_{AST}	Address Setup Time	HOSC=24MHZ	50		ns
	T_{AHT}	Address Hold Time(Write/Read)	HOSC=24MHZ	50		ns
/WR	T_{WC}	Write Cycle	HOSC=24MHZ	100	1000	ns
	T_{WRH}	Control Pulse "H" Duration	HOSC=24MHZ	50	500	ns
	T_{WRL}	Control Pulse "L" Duration	HOSC=24MHZ	50	500	ns
/RD	T_{RC}	Read Cycle	HOSC=24MHZ	100	1000	ns
	T_{RDH}	Control Pulse "H" Duration	HOSC=24MHZ	50	500	ns
	T_{RDL}	Control Pulse "L" Duration	HOSC=24MHZ	50	500	ns
DB	T_{DST}	Data Setup Time	HOSC=24MHZ	50	500	ns
	T_{DHT}	Data Hold Time	HOSC=24MHZ	50	500	ns
	T_{RAT}	Read Access Time	HOSC=24MHZ		200	ns
	T_{ODH}	Output Disable Time	HOSC=24MHZ	50		ns

11.18 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 1.6 V, VCC = 3.0V, Sample Rate=48KHz)

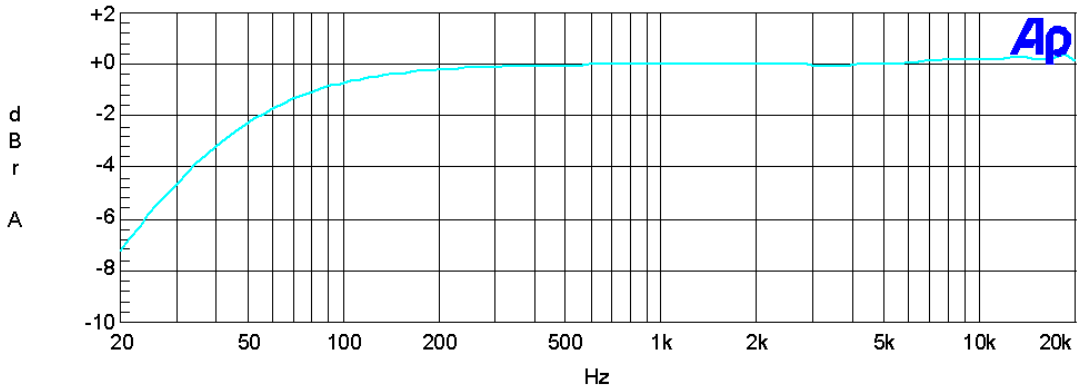
Characteristics	Min	Typ.	Max	Unit
Dynamic range		88.0		dB
Total Harmonic Distortion + Noise		-83.0		dB
Frequency Response (20-20KHz)			±0.98	dB
Full Scale Input Voltage(Gain=0dB)		2.7		Vpp

11.19 Headphone Driver Characteristics Table

(T_o =-10 – to +70℃, VDD = 1.6 V, VCC = 3.0 V, Volume Level=0x28, 16ohm+220uF)

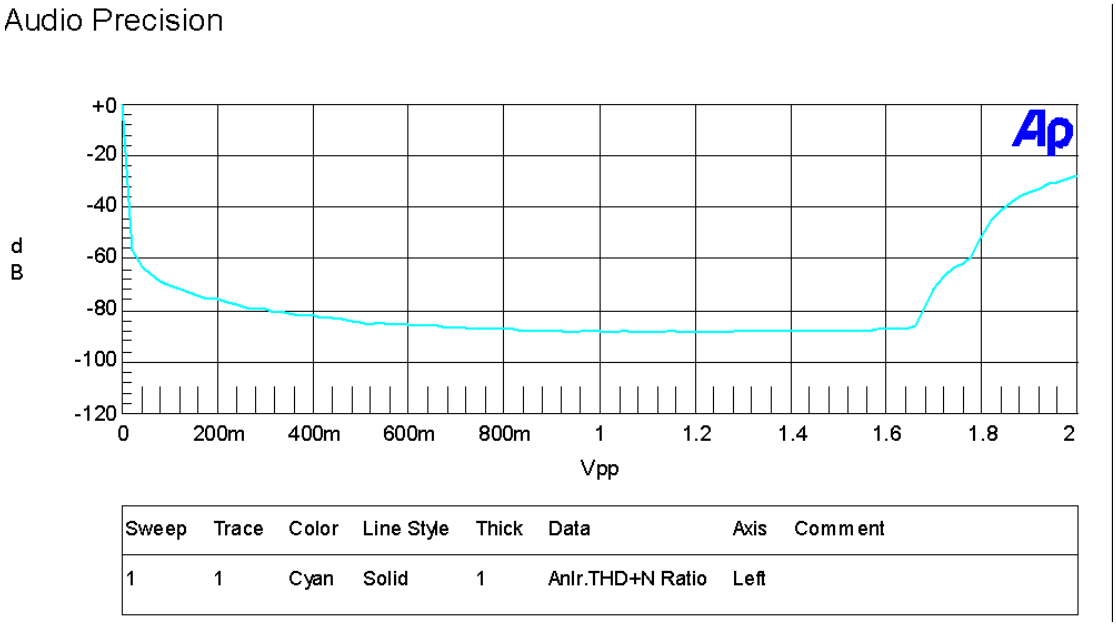
Characteristics	Min	Typ	Max	Unit
Dynamic Range –60 dBFS Input		90		dB
Total Harmonic Distortion + Noise		-85		dB
Frequency Response 20-20KHz	-7.2		+0.3	dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.6		Vpp
Inter channel Gain Mismatch(1KHz)		±0.1		dB

Audio Precision



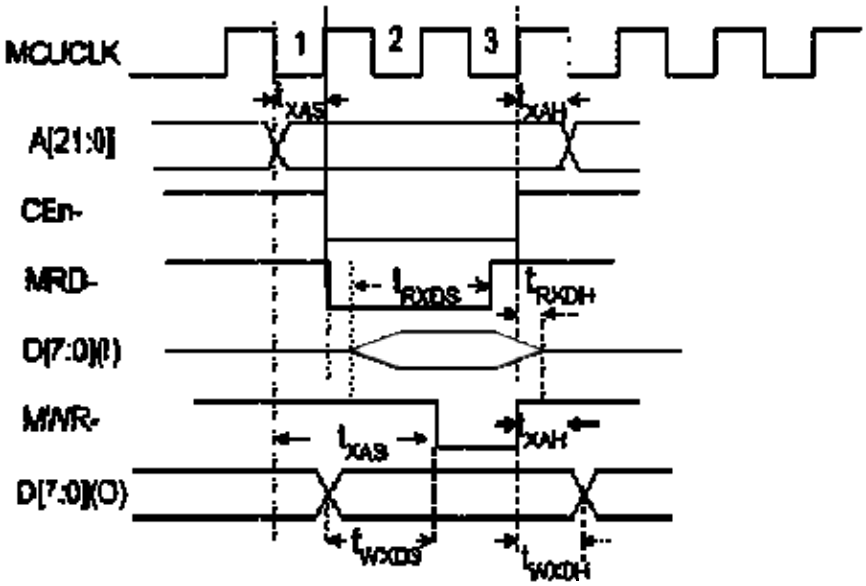
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.Level A	Left	

Frequency Response Diagram of Headphone Driver



THD + N Amplitude Diagram of Headphone Driver

11.20 External System Bus Parameter



External System Bus Parameter

External System Bus Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit

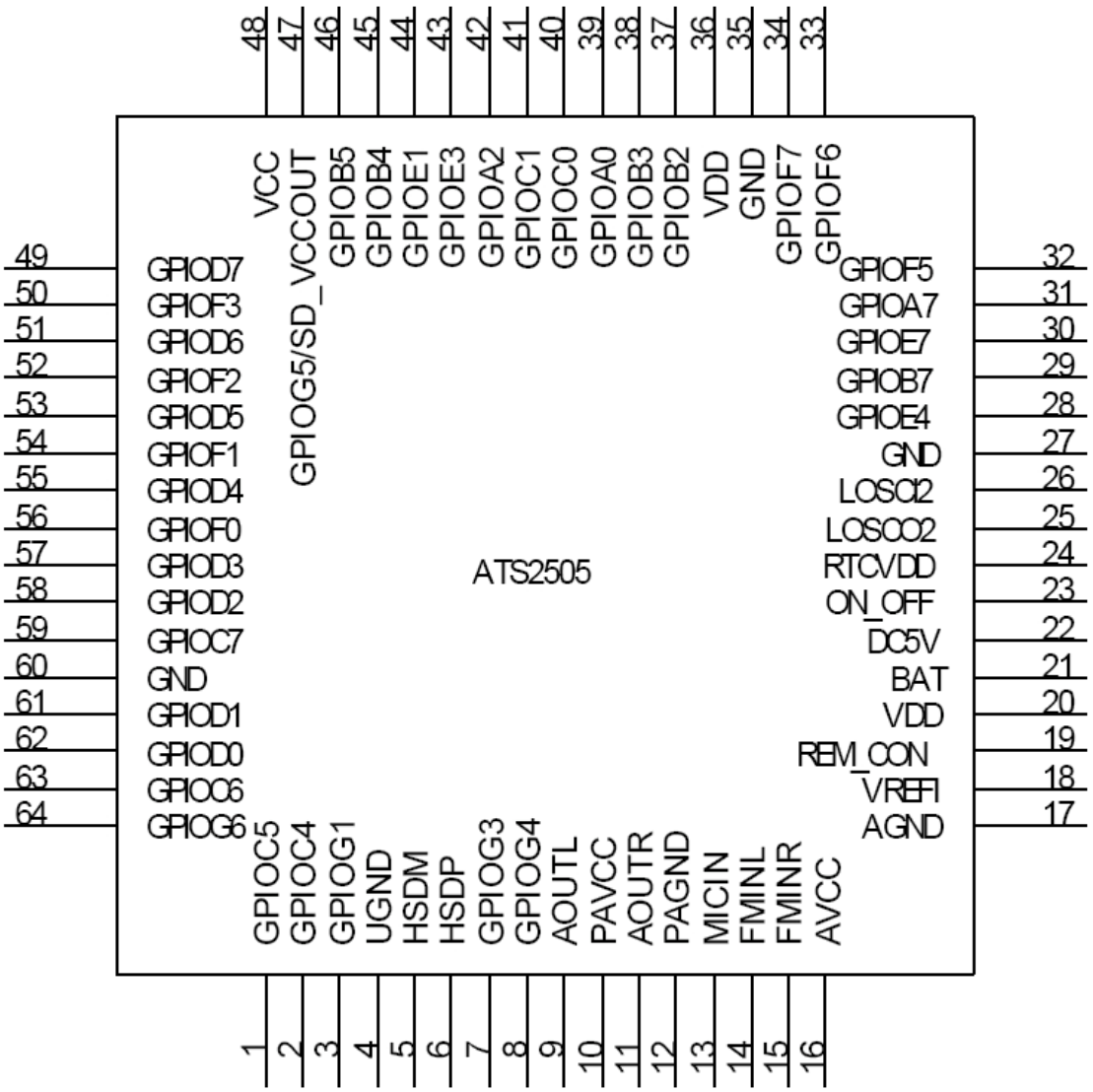
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	10		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

12 Pin Definition

12.1 Pin Sort by Pin Number



12.2 ATS2505 Pin Definition

Pin No.	Pin Name	I/O Type	Driver	Reset Default	Short Description
1	GPIOC5	BI	8/12/16mA	H	Bit5 of General purpose I/O port C
	SPI_MISO	I			Master Input Slave Output of SPI
2	EM_CEB2	O	8/12/16mA	H	Ext. memory chip enable 2
	GPIOC4	BI			Bit4 of General purpose I/O port C
	SPI_SS	O			Chip Enable of SPI
3	GPIOG1	BI	8 mA	H	Bit1 of General purpose I/O port G
	EJ_TMS	I			EJTAG TMS
4	UGND	PWR	/	/	USB ground
5	HSDM	A	/	H	USB data minus
6	HSDP	A	/	H	USB data plus
7	GPIOG3	BI	8 mA	H	Bit3 of General purpose I/O port G
	EJ_TDI	I			EJTAG TDI
8	GPIOG4	BI	8 mA	H	Bit4 of General purpose I/O port G
	EJ_TDO	O			EJTAG TDO
9	AOUTL	AO	/	/	Int. PA left channel analog output
10	PAVCC	PWR	/	/	Power amplifier VCC
11	AOUTR	AO	/	/	Int. PA right channel analog output
12	PAGND	PWR	/	/	Power amplifier ground
13	MICIN	AI	/	/	Microphone pre-amplifier input

14	FMINL	AI	/	/	Left channel of FM line input
15	FMINR	AI	/	/	Right channel of FM line input
16	AVCC	PWR	/	/	Power supply of Analog
17	AGND	PWR	/	/	Analog ground
18	VREFI	AI	/	/	Voltage reference input
19	REM_CON	AI	/	/	Low resolution A/D input 1
20	VDD	PWR	/	/	Digital Core power
21	BAT	I	/	/	Battery Voltage input.
22	DC5V	AI	/	/	5.0V Voltage
23	ON_OFF	AI	/	/	All-purpose hardware switch
24	RTC_VDD	PWR	/	/	Power for RTC
25	LOSCO2	AI	/	/	LOW frequency crystal OSC output
26	LOSCI2	AO	/	/	LOW frequency crystal OSC input
27	GND	PWR	/	/	Ground
28	GPIOE4	BI	8/12/16mA	L	Bit4 of General purpose I/O port E
	MS_CLK	O			Clock for memory stick card
	IR_RX	I			Infrared ray receiver
	FMCLKOUT	O			Clock for FM Module
	FM_VCCOUT	AO	/		Power for FM Module
29	GPIOB7	BI	8mA	H	Bit7 of General purpose I/O port B
	SIRQ1	I			SIRQ1
30	GPIOE7	BI	12 mA	H	Bit7 of General purpose I/O port E
	I2S_LR	O			LR of I2S
31	GPIOA7	BI	8/12mA	H	Bit7 of General purpose I/O port A
	EM_CEB5	O			Ext. memory chip enable 5

	LCD_CEB	O			LCD chip enable
32	GPIOF5	BI	8/12/16mA	Z	Bit5 of General purpose I/O port F
	MMC_D5	BI			Bit5 of MMC/SD Data
	MSD5	BI			Bit5 of MS Data
	EM_D13	BI			Bit13 of Ext. Memory Data
	LCD_D13	O			Bit13 of LCD Data
	EM_D5	BI			Bit5 of Ext. Memory Data
	LCD_D5	O			Bit5 of LCD Data
	LRADC3	AI			Low resolution A/D input 3
	I2S_ BITCLK	O			BITCLK of I2S
33	GPIOF6	BI	8/12/16mA	Z	Bit6 of General purpose I/O port F
	MMC_D6	BI			Bit6 of MMC/SD Data
	MSD6	BI			Bit6 of MS Data
	EM_D14	BI			Bit14 of Ext. Memory Data
	LCD_D14	O			Bit14 of LCD Data
	EM_D6	BI			Bit6 of Ext. Memory Data
	LCD_D6	O			Bit6 of LCD Data
	LRADC4	AI			Low resolution A/D input 4
	I2S_DATA	O			DATA of I2S
34	GPIOF7	BI	8/12/16mA	Z	Bit7 of General purpose I/O port F
	MMC_D7	BI			Bit7 of MMC/SD Data
	MSD7	BI			Bit7 of MS Data
	EM_D15	BI			Bit15 of Ext. Memory Data
	LCD_D15	O			Bit15 of LCD Data
	EM_D7	BI			Bit7 of Ext. Memory Data
	LCD_D7	O			Bit7 of LCD Data
	LRADC5	AI			Low resolution A/D input 5
	I2S_LR	O			LR of I2S

35	GND	PWR	/	/	Ground
36	VDD	PWR	/	/	Digital Core power
37	GPIOB2	BI	8/12/16mA	H	Bit2 of General purpose I/O port B
	EM_RDB	O			Ext. memory read strobe
	GPIOB3	BI			Bit3 of General purpose I/O port B
38	EM_WRB	O	8/12/16mA	H	Ext. memory write strobe
	LCD_WRB	O			LCD write strobe
39	GPIOA0	BI	8/12mA	Z	Bit0 of General purpose I/O port A
	FMCLKOUT	O			Clock for FM Module
40	GPIOC0	BI	8/12mA	Z	Bit0 of General purpose I/O port C
	I2C_SCL	BI			I2C serial clock (Open drain)
	UART_CTS	I			UART Sending Busy Signal
	IR_RX	I			Infrared ray receiver
41	GPIOC1	BI	8/12mA	Z	Bit1 of General purpose I/O port C
	I2C_SDA	BI			I2C serial clock (Open drain)
	UART_RTS	O			UART Receiving Request Signal
	EM_RS	O			Ext. Memory Command/Data select
	LCD_RS	O			LCD Command/Data select
	PWM	O			PWM output
42	GPIOA2	BI	12/16mA	H	Bit2 of General purpose I/O port A
	SIRQ0	I			SIRQ0
	MS_BS	O			Command for MS Card
	PWM	O			PWM output
43	GPIOE3	BI	12/16mA	H	Bit3 of General purpose I/O port E
	MMC_CLK1	O			Clock1 for MMC/SD Card

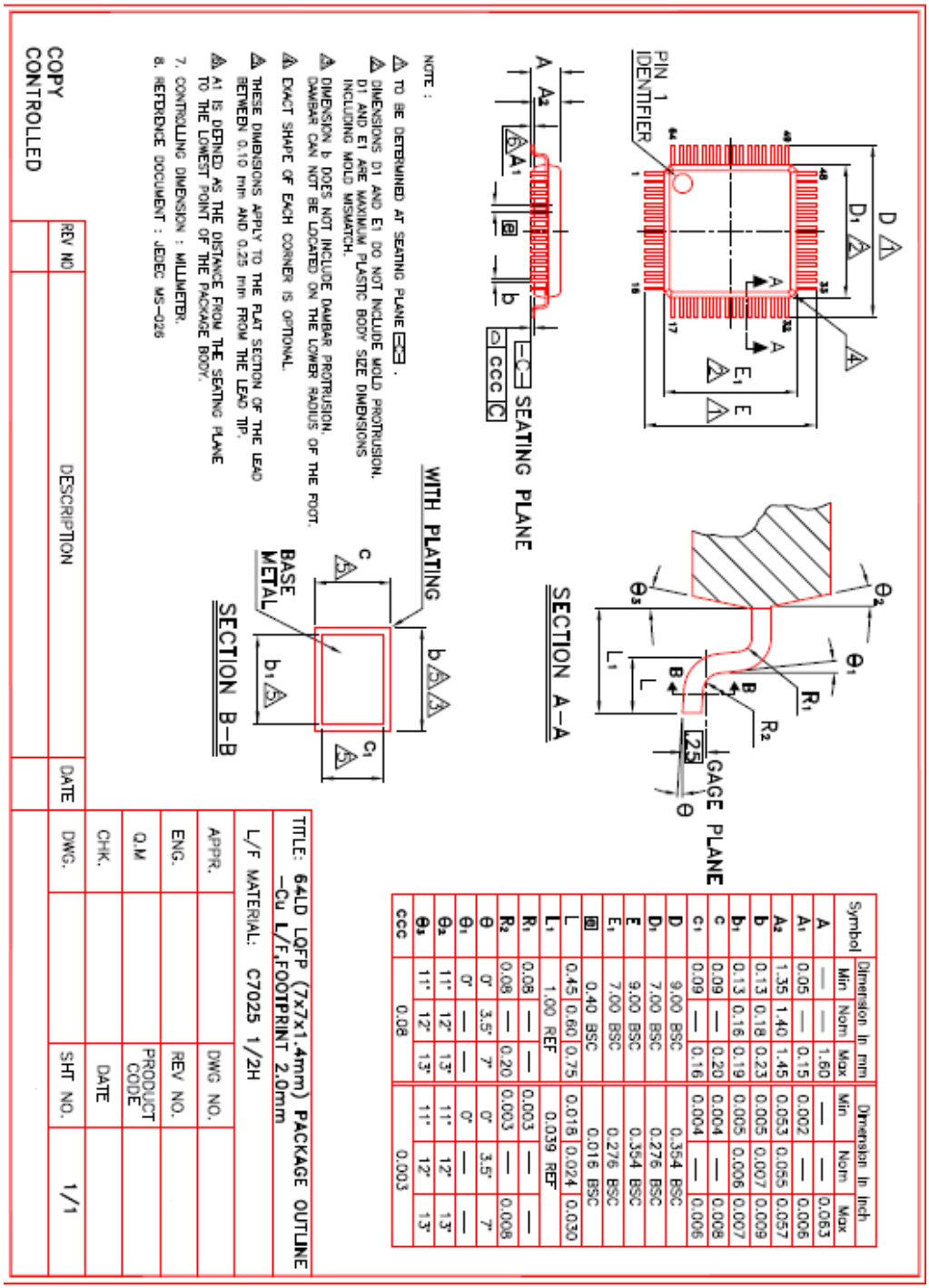
	MS_CLK	O			Clock for MS Card
44	GPIOE1	BI	4/8/12mA	Z	Bit1 of General purpose I/O port E
	MMC_CMD	IO			Command for MMC/SD Card
	MS_BS	O			Command for MS Card
45	GPIOB4	BI	8/12mA	L	Bit4 of General purpose I/O port B
	LCD_RS EM_RS	O O			LCD Command/Data select Ext. Memory Command/Data select
	UART_TX	O			UART TX
46	GPIOB5	BI	8/12mA	L	Bit5 of General purpose I/O port B
	UART_RX	I			UART RX
47	GPIOG5	BI	8mA	Z	Bit5 of General purpose I/O port G
	SD_VCCOUT	PWR	/		Power Supply for SD Card
48	VCC	PWR	/	/	Digital power pin
49	GPIOD7	BI	8/12/16mA	X	Bit7 of General purpose I/O port D
	EM_D7 LCD_D7	BI O			Bit7 of Ext. Memory Data Bit7 of LCD Data
50	GPIOF3	BI	4/8/12mA	Z	Bit3 of General purpose I/O port F
	MMC_D3	BI			Bit3 of MMC/SD Data
	MSD3	BI			Bit3 of MS Data
	EM_D11	BI			Bit11 of Ext. Memory Data
	LCD_D11	O			Bit11 of LCD Data
	EM_D3	BI			Bit3 of Ext. Memory Data
	LCD_D3	O			Bit3 of LCD Data
51	GPIOD6	BI	8/12/16mA	X	Bit6 of General purpose I/O port D

	EM_D6 LCD_D6	BI O			Bit6 of Ext. Memory Data Bit6 of LCD Data
52	GPIOF2	BI	4/8/12mA	Z	Bit2 of General purpose I/O port F
	MMC_D2	BI			Bit2 of MMC/SD Data
	MSD2	BI			Bit2 of MS Data
	EM_D10	BI			Bit10 of Ext. Memory Data
	LCD_D10	O			Bit10 of LCD Data
	EM_D2	BI			Bit2 of Ext. Memory Data
	LCD_D2	O			Bit2 of LCD Data
53	GPIOD5	BI	8/12/16mA	X	Bit5 of General purpose I/O port D
	EM_D5 LCD_D5	BI O			Bit5 of Ext. Memory Data Bit5 of LCD Data
54	GPIOF1	BI	4/8/12mA	Z	Bit1 of General purpose I/O port F
	MMC_D1	BI			Bit1 of MMC/SD Data
	MSD1	BI			Bit1 of MS Data
	EM_D9	BI			Bit9 of Ext. Memory Data
	LCD_D9	O			Bit9 of LCD Data
	EM_D1	BI			Bit1 of Ext. Memory Data
	LCD_D1	O			Bit1 of LCD Data
55	GPIOD4	BI	8/12/16mA	X	Bit4 of General purpose I/O port D
	EM_D4 LCD_D4	BI O			Bit4 of Ext. Memory Data Bit4 of LCD Data
56	GPIOF0	BI	4/8/12mA	Z	Bit0 of General purpose I/O port F
	MMC_D0	BI			Bit0 of MMC/SD Data
	MSD0	BI			Bit0 of MS Data

	EM_D8	BI			Bit8 of Ext. Memory Data
	LCD_D8	O			Bit8 of LCD Data
	EM_D0	BI			Bit0 of Ext. Memory Data
	LCD_D0	O			Bit0 of LCD Data
57	GPIOD3	BI	8/12/16mA	X	Bit3 of General purpose I/O port D
	EM_D3 LCD_D3	BI O			Bit3 of Ext. Memory Data Bit3 of LCD Data
58	GPIOD2	BI	8/12/16mA	X	Bit2 of General purpose I/O port D
	EM_D2 LCD_D2	BI O			Bit2 of Ext. Memory Data Bit2 of LCD Data
59	GPIOC7	BI	8/12/16mA	Z	Bit7 of General purpose I/O port C
	SPI_SCLK	BI			Clock for SPI
	EM_CEB4 UART_RX	O I			Ext. memory chip enable 4 UART RX
60	GND	PWR	/	/	Ground
61	GPIOD1	BI	8/12/16mA	X	Bit1 of General purpose I/O port D
	EM_D1 LCD_D1	BI O			Bit1 of Ext. Memory Data Bit1 of LCD Data
62	GPIOD0	BI	8/12/16mA	X	Bit0 of General purpose I/O port D
	EM_D0 LCD_D0	BI O			Bit0 of Ext. Memory Data Bit0 of LCD Data
63	GPIOC6	BI	8/12/16mA	Z	Bit6 of General purpose I/O port C
	SPI_MOSI	O			Master Output Slave Input of SPI

	EM_CEB3 UART_TX	O O			Ext. memory chip enable 3 UART TX
64	GPIOG6	BI	8 mA	Z	Bit6 of General purpose I/O port G

13 ATS2505 Package Drawing



Symbol	Dimension In mm			Dimension In Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

14 Appendix

14.1 Acronym and Abbreviations

ADC: Analog-to-Digital Converter
ALE: Address-locked Enable
CLE: Command-Locked Enable
CRC: Cyclic Redundancy Check
DAC: Digital-to-analog Converter
dB: Decibel
DC: Direct Current
DSP: Digital Signal Processing
ECC: Error Correct Code
FIR: Fast Infrared
GPIO: General-Purpose Input/Output
I2S: Inter-IC Sound
IR: Infrared
IrDA: Infrared Data Association
IRQ: Interrupt Request
JPEG: Joint Photographic Experts Group
Li-Ion: Lithium Ion (battery type)
LRADC: Low Resolution ADC
MIR: Mid Infrared
MJPEG: Motion JPEG
MMC: Multimedia Card
MMU: Memory Management Unit
MLC: Multi-level Cell
MPEG: Motion Picture Expert Group
MS: Memory stick card
PA: Power Amplifier
PFM: Pulse Frequency Modulation
PLL: Phase-Locked Loop
PMU: Power Management Unit
PWM: Pulse Width Modulation
RTC: Real-Time Clock
SD: Secure Digital memory card
SIR: Slow Infrared

SMC: State Machine Controller
SLC: Single-Level Cell
SOC: System on a Chip
SPEC: Specification
SPI: Serial Peripheral Interface
SW: Software
THD: Total Harmonic Distortion
TLB: Translation Look-aside Buffer
TS: Transport Stream
UART: Universal Asynchronous Receiver Transmitter
WMA: Windows Media Audio
WMV: Windows Media Video