炬芯 Actions

ATS2837 Datasheet

Actions® ATS2837™ QFN68

Bluetooth Audio Solution

Low Power Solution for
Speech Pre-processing
Portable & Wireless Audio Applications
Local MMC/SD Card Audio Playback

CPU + DSP Dual-core Single-chip
Bluetooth V5.0

Version: V1.5

2020-8-25

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Contents

Revision History

Date	Revision	Description
2019-3-29	V1.0	Initial version
2019-7-25	V1.1	Add some information： 1. Reflow soldering profile 2. Moisture sensitivity level 3. Device marking of the chipset 4. Ordering information
2019-12-7	V1.2	Modify the initial state of GPIO16, GPIO17, GPIO23, GPIO28, GPIO29, GPIO30, GPIO31, GPIO42.
2020-3-13	V1.3	1. The initial state of GPIO is divided into boot from NOR Flash and boot from SD Card; 2. Maximum 4.5V battery support in “recommended PWR supply” chapter.
2020-4-21	V1.4	Modify the description of "Bluetooth V5.0 features"
2020-8-25	V1.5	Change the company name to "Actions Technology Co., Ltd."

1 Introduction

1.1 Overview

Actions' ATS2837 is a highly integrated single-chip Bluetooth Audio solution. Positioning at Bluetooth portable stereo speakers, headsets and speakerphones and local MMC/SD Card Audio Playback market, ATS2837 satisfies the market requirements with high performance, low cost and low power consumption.

ATS2837 adopts CPU + DSP dual core architecture. Large capacity RAM is embedded to meet different Bluetooth applications, and support Bluetooth background working while playing high quality music with traditional plug-in card and USB flash disk. ATS2837 supports decoding Bluetooth A2DP audio and loading sound effects simultaneously, support Bluetooth handfree calls with dual MIC AEC and noise reduction.

ATS2837 integrates Bluetooth controller support V5.0 and compliant with 4.2/2.1 Bluetooth specification, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS2837 takes special methods at power optimization, especially for various applications scenarios, including sniff, Bluetooth idle, Bluetooth playing and call modes. Embedded PMU supports power optimization and provide long battery life. The competitive advantages of ATS2837 are high music and call qualities with low power and BOM, which lays the foundation for our goal at high-end market. Above all, ATS2837 provides a true "ALL-IN-ONE" solution, making it the ideal choice for highly integrated and optimized Bluetooth audio products.

1.2 Key Features

System

- 240MHz RISC-32 CPU processor Core
- 400MHz CEVA DSP core
- Internal 304KB RAM for data and program
- Internal 32KB CPU ICache for SPI NorFlash
- Internal 32KB Cache for SPI pSRAM
- Internal 16M bits pSRAM to support rich and flexible software feature
- SPI supporting randomizer
- Supports 24MHz OSC with on-chip PLL
- Operating voltage: I/O 3.1V, Core 1.2V
- Fully configurable PEQ
- Supports for echo cancellation , noise reduction and wind noise reduction
- Supports for packet loss concealment
- Supports for sound effect, such as MDRC, bass enhancement, virtual surround effects
- Symmetric and asymmetric cryptography
- 128bit efuse is used for symmetric key when using symmetric cryptography
- Asymmetric cryptography signature algorithm is SHA256WithRSA Encryption, the public key is 2048bit

Bluetooth

- Supports Bluetooth V5.0
- Compatible with Bluetooth V4.2/V4.2 LE/V4.0/V3.0/V2.1 + EDR systems
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.7
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class2 PA
- Supports Power / Enhanced Power Control

Package

- QFN-68 (8mm*8mm, Pitch 0.4mm)

Audio

- Built-in stereo 24 bit input sigma-delta DAC
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1/48/96kHz
- Built-in stereo 20mW PA for headphone. PA output supports traditional mode and direct drive mode (for earphone)
- Supports differential audio output
- Built-in stereo 24 bit input sigma-delta ADC
- ADC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48/96kHz
- Supports 3 stereo single-ended analog input or 1 stereo fully differential analog input plus 1 stereo single-ended analog input
- Supports Digital microphones
- Supports single-ended Analog microphones and fully differential microphone
- Audio Interfaces: I2S TX and I2S RX*2, sampling rate up to 192KHz
- Audio Interfaces: SPDIF TX and RX, sampling rate up to 96KHz

Power Management

- Supports Li-Ion battery and 5V power supply
- Integrated DC-DC buck converters
- Linear regulators output VCC, SVCC, RTCVDD
- Standby Leakage Current (Include RTC module):<50uA(Whole System)
- Low Power Consumption:
  Typical Sniff Current: 600uA@Vbat=3.8V
  A2DP: 15.5mA@Vbat=3.8V
  HFP: 16.5mA@Vbat=3.8V

Physical Interfaces

- Supports SD/MMC/eMMC card interface
- Supports SDIO interface
- USB 2.0 device and host controllers
- Serial Interface: SPI*2, UART*2, I2C
- Supports Remote Control with internal IRC
- Supports LCM with 8bit CPU Interface, 4COM/5COM/6COM Segment LCD, 7pin LED
- 9 PWM drivers independent of MCU

Applications

- Smart voice front-end system
- Portable stereo speakers and speakerphones
- Bluetooth car audio unit
- Stereo headsets and headphones
- Other Bluetooth audio applications

1.3 Application Diagram

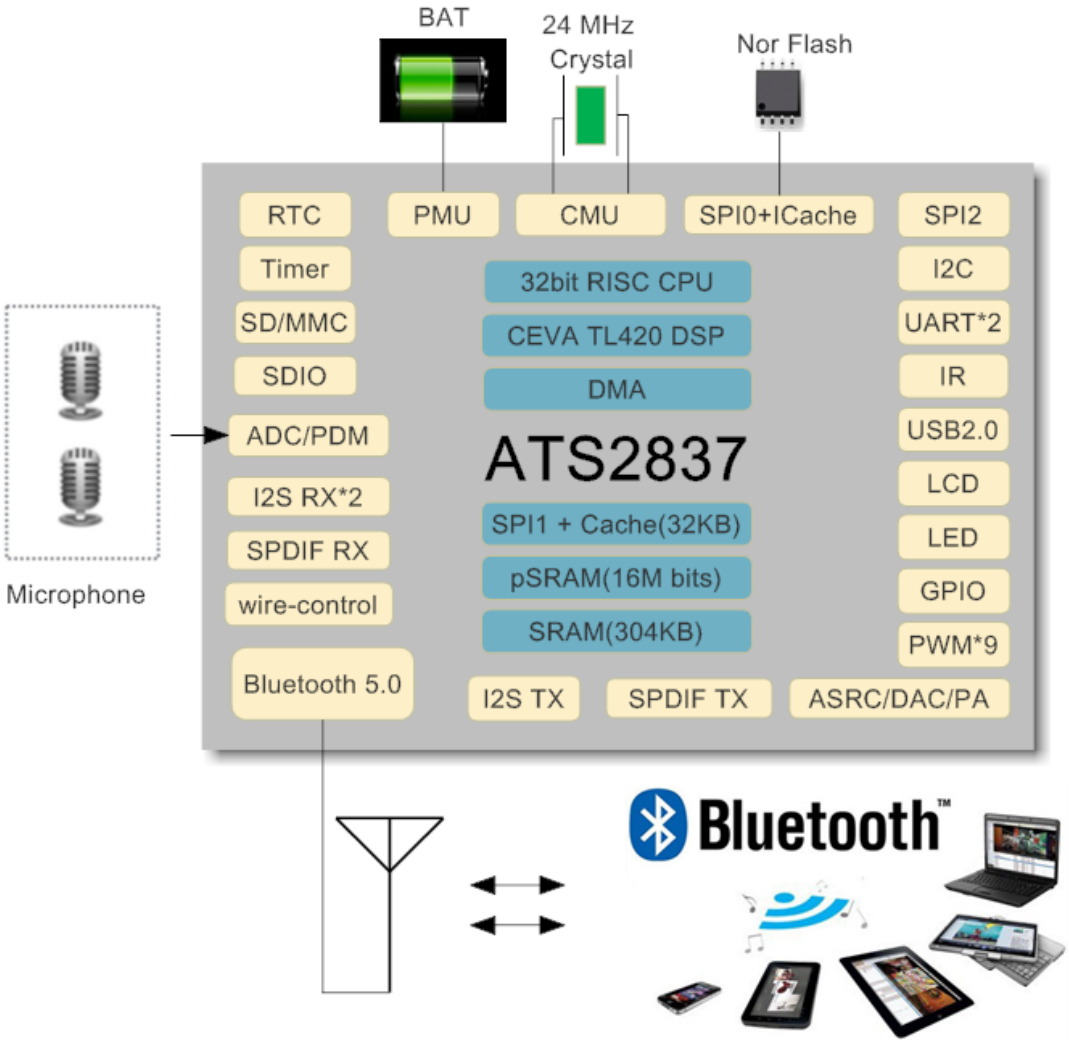
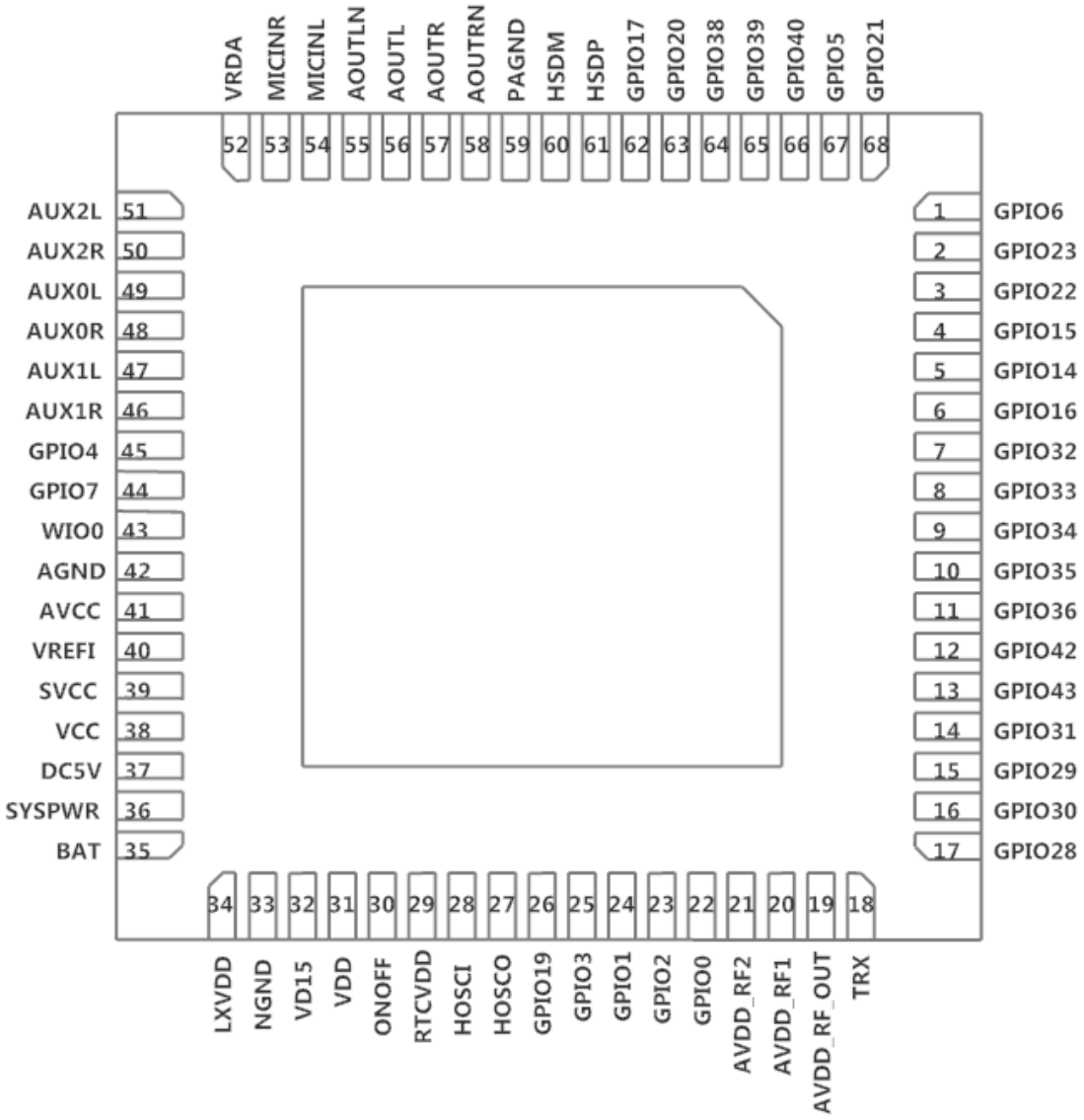


Figure 1-1 ATS2837 Application Diagram

1.4 Pin Assignment and Descriptions

1.4.1 Pin Assignment



1.4.2 Pin Description

Pin No.	Pin Name	Function Multiplex	IO Type	PAD Drive Level	GPIO Initial State		Description
					Boot from NOR Flash	Boot from SD Card	
1	GPIO6	LED_COM6 BT_ACCESS LCD_SEG0 PWM4 I2STX_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK Timer2_cap SD1_DAT0	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit6 of General purpose I/O port

2	GPIO23	LCD_D11 LCD_SEG13 SPDIF_TX PWM2 UART0_TX LRADC3 I2STX_BCLK I2SRX0_BCLK I2SRX1_BCLK Timer3_cap SD1_CMD SD0_DAT3 SD0_DAT0	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	H	Bit23 of General purpose I/O port
3	GPIO22	LCD_D10 LCD_SEG12 IR_RX PWM1 UART0_TX LRADC2 I2STX_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK Timer2_cap SD1_DAT2 UART1_RX SD0_DAT2	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	H	Bit22 of General purpose I/O port
4	GPIO15	LED_SEG7 LCD_D7 LCD_SEG9 PWM4 UART1_RX I2STX_MCLK I2SRX0_MCLK I2SRX1_MCLK Timer3_cap SD1_DAT0 SPI0_IO3	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit15 of General purpose I/O port
5	GPIO14	LED_SEG6 LCD_D6 LCD_SEG8 LRADC11 SPI0_IO2 Timer2_cap	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit14 of General purpose I/O port
6	GPIO16	SD0_CMD UART0_RX LCD_SEG14 SPI2_SS PWM4 Timer2_cap	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	V	Bit16 of General purpose I/O port
7	GPIO32	LCD_SEG22 I2STX_MCLK I2SRX0_MCLK I2SRX1_MCLK	DIO	2/4 /6/8 /10/12 /14/16 mA	PU	PU	Bit32 of General purpose I/O port

8	GPIO33	LCD_SEG23 I2STX_BCLK I2SRX0_BCLK I2SRX1_BCLK	DIO	2/4 /6/8 /10/12 /14/16 mA	PU	PU	Bit33 of General purpose I/O port
9	GPIO34	LCD_SEG24 I2STX_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK	DIO	2/4 /6/8 /10/12 /14/16 mA	PU	PU	Bit34 of General purpose I/O port
10	GPIO35	LCD_SEG25 SPDIFTX I2STX_DOUT I2SRX0_DIN I2SRX1_DIN	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit35 of General purpose I/O port
11	GPIO36	LED_SEG26 I2STX_DOUT I2SRX0_DIN I2SRX1_DIN	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit36 of General purpose I/O port
12	GPIO42	I2C_SCL PWM3 IR_RX SD0_CLK0 PWM5 I2STX_BCLK I2SRX0_BCLK I2SRX1_BCLK UART1_TX SD1_DAT1	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	V	Bit42 of General purpose I/O port
13	GPIO43	I2C_SDA	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit43 of General purpose I/O port
14	GPIO31	SPI0_MOSI SPI0_MISO LCD_SEG20 PWM5 Timer3_cap	DIO	2/4 /6/8 /10/12 /14/16 mA	V	V	Bit31 of General purpose I/O port
15	GPIO29	SPI0_SCLK SPI0_SS SD0_CLK1 I2C_SDA LCD_SEG19 Timer3_cap	DIO	2/4 /6/8 /10/12 /14/16 mA	V	V	Bit29 of General purpose I/O port
16	GPIO30	SPI0_MISO SPI0_SCLK I2C_SCL LCD_SEG21 Timer2_cap	DIO	2/4 /6/8 /10/12 /14/16 mA	V	V	Bit30 of General purpose I/O port
17	GPIO28	SPI0_SS SPI0_MOSI LCD_SEG18	DIO	2/4 /6/8 /10/12	V	V	Bit28 of General purpose I/O port

		Timer2_cap		/14/16 mA			
18	TRX		RF				Bluetooth antenna IO
19	AVDD_RF_OUT		PWR				1.2V Voltage
20	AVDD_RF1		PWR				1.2V Voltage
21	AVDD_RF2		PWR				1.2V Voltage
22	GPIO0	LED_COM0 LCD_WRB LCD_COM0 I2C_SCL PWM1 UART0_RTS I2STX_MCLK I2SRX0_MCLK I2SRX1_MCLK Timer2_cap SPI2_SS	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit0 of General purpose I/O port
23	GPIO2	LED_COM2 LCD_RDB LCD_COM2 PWM2 UART0_RX LRADC4 I2STX_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK Timer2_cap SPI2_MOSI	DIO	2/4 /6/8 /10/12 /14/16 mA	V	V	Bit2 of General purpose I/O port
24	GPIO1	LED_COM1 LCD_RS LCD_COM1 I2C_SDA PWM3 UART0_CTS I2STX_BCLK I2SRX0_BCLK I2SRX1_BCLK Timer3_cap SPI2_MISO	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit1 of General purpose I/O port
25	GPIO3	LED_COM3 LCD_CEB LCD_COM3 UART0_TX I2STX_DOUT I2SRX0_DIN I2SRX1_DIN Timer3_cap SPI2_CLK	DIO	2/4 /6/8 /10/12 /14/16 mA	V	V	Bit3 of General purpose I/O port
26	GPIO19	LCD_SEG17 I2C_SDA Timer3_cap	DIO	2/4 /6/8 /10/12	Z	Z	Bit19 of General purpose I/O port

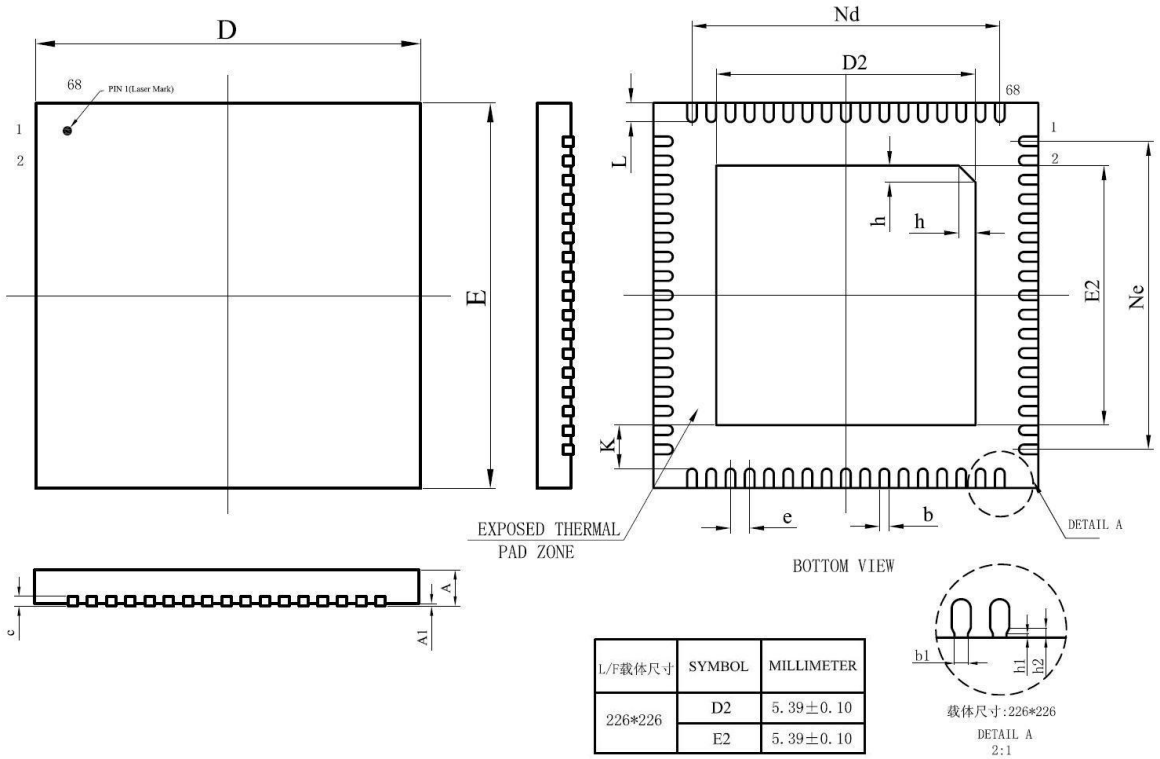
				/14/16 mA			
27	HOSCO		AO				24MHz clock output
28	HOSCI		AI				24MHz clock input
29	RTCVDD		PWR				RTC power
30	ONOFF		AI				ON/OFF reset signal
31	VDD		PWR				Core Logic PWR
32	VD15		PWR				1.5V DCDC feedback
33	NGND		GND				GND
34	LXVDD		PWR				DCDC Output
35	BAT		PWR				Battery Voltage input
36	SYSPWR		PWR				System PWR
37	DC5V		PWR				5.0V Voltage
38	VCC		PWR				Digital IO PWR
39	SVCC		PWR				PWR for standby
40	VREFI		PWR				Reference voltage input
41	AVCC		PWR				Analog IO PWR
42	AGND		GND				Analog GND
43	WIO0	LRADC1	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Wake up I/O port
44	GPIO7	LED_COM7 PTA_GRANT LCD_SEG1 SPDIF_RX PWM0 UART1_TX FMCLKOUT I2STX_DOUT I2SRX0_DIN I2SRX1_DIN Timer3_cap SD1_DAT3	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit7 of General purpose I/O port
45	GPIO4	LED_COM4 LCD_CEB LCD_COM4 PWM1 Timer2_cap IR_RX	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit4 of General purpose I/O port
46	AUX1R/ AUXR	GPIO49	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Linein/FM right channel input1, right channel differential input
47	AUX1L/ AUXR	GPIO48	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Linein/FM left channel input1, right channel differential input
48	AUX0R/ AUXL	GPIO47	AI /DIO	2/4 /6/8			Linein/FM right channel input0, left channel

				/10/12 /14/16 mA			differential input
49	AUX0L/ AUXL	GPIO46	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Linein/FM left channel input0, left channel differential input
50	AUX2R	GPIO55	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Linein/FM right channel input2
51	AUX2L	GPIO54	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Linein/FM left channel input2
52	VRDA		PWR				AUDIO power
53	MICINR/ MICINN	GPIO45 DMIC_DAT	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Microphone right channel input, Differential MICIN Negative Input
54	MICINL/ MICINP	GPIO44 DMIC_CLK	AI /DIO	2/4 /6/8 /10/12 /14/16 mA			Microphone left channel input, Differential MICIN Positive Input
55	AOUTLN /VRO	GPIO51 I2STX_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK PWM3	AO /DIO	2/4 /6/8 /10/12 /14/16 mA			Left channel differential output and direct drive circuit reference voltage
56	AOUTL/ AOUTLP	GPIO50	AO /DIO	2/4 /6/8 /10/12 /14/16 mA			Left channel output and left channel differential output
57	AOUTR/ AOUTRP	GPIO52	AO /DIO	2/4 /6/8 /10/12 /14/16 mA			Right channel output and right channel differential output
58	AOUTRN / VRO_S	GPIO53 I2STX_DOUT I2SRX0_DIN I2SRX1_DIN PWM5	AO /DIO	2/4 /6/8 /10/12 /14/16 mA			Right channel differential output and direct drive circuit reference voltage
59	PAGND		GND				GND for PA
60	HSDM		AIO				USB Data minus
61	HSDP		AIO				USB Data plus
62	GPIO17	SPI2_CLK LCD_SEG15	DIO	2/4 /6/8	Z	V	Bit17 of General purpose I/O port

		UART0_TX Timer3_cap SD0_CLK0		/10/12 /14/16 mA			
63	GPIO20	SPI2_MISO LCD_D8 LCD_SEG10 PWM2 UART1_CTS Timer2_cap SD0_DAT0	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	H	Bit20 of General purpose I/O port
64	GPIO38	SPDIF_RX BT_REQ LCD_SEG28 PWM0 I2STX_DOUT I2SRX0_DIN I2SRX1_DIN	DIO	2/4 /6/8 /10/12 /14/16 mA	PU	PU	Bit38 of General purpose I/O port
65	GPIO39	BT_ACCESS LCD_SEG29 PWM1 I2STX_BCLK I2SRX0_BCLK I2SRX1_BCLK	DIO	2/4 /6/8 /10/12 /14/16 mA	PU	PU	Bit39 of General purpose I/O port
66	GPIO40	PTA_GRANT LCD_SEG30 PWM2 I2STX_MCLK I2SRX0_MCLK I2SRX1_MCLK	DIO	2/4 /6/8 /10/12 /14/16 mA	PU	PU	Bit40 of General purpose I/O port
67	GPIO5	LED_COM5 BT_REQ LCD_COM5 PWM3 Timer3_cap	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	Z	Bit5 of General purpose I/O port
68	GPIO21	SPI2_MOSI LCD_D9 LCD_SEG11 PWM0 UART0_RX TEMPADC I2STX_MCLK I2SRX0_MCLK I2SRX1_MCLK Timer3_cap SD1_CLK UART1_TX SD0_DAT1	DIO	2/4 /6/8 /10/12 /14/16 mA	Z	H	Bit21 of General purpose I/O port
69	EPAD		GND				Exposed pad as ground

Note:
PU: Pull up through 10K resistor inside the chip;
H: High level that is driving ability, but if the external pull-down is strong, it can also be pulled to low level.
Z: High resistance;
V: Variable state.

1.4.3 Package Dimensions



L/F载体尺寸	SYMBOL	MILLIMETER
226*226	D2	5.39±0.10
	E2	5.39±0.10

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	—	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	7.90	8.00	8.10
e	0.40BSC		
Nd	6.40BSC		
E	7.90	8.00	8.10
Ne	6.40BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
h1	0.04REF		
h2	0.10REF		

2 Bluetooth

2.1 Features

- Support Bluetooth V5.0
- Compatible with Bluetooth V4.2/V4.2 LE/V3.0/V2.1 +EDR systems
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Class2 transmit output power supported
- Supports GFSK, π/4 DQPSK and 8DPSK modulation
- Supports Power / Enhanced Power Control

2.2 Bluetooth V5.0 Features

- LE Data Packet Length Extension
- LE 2M PHY
- Channel Selection Algorithm #2

2.3 Bluetooth Performance

- Max transmitting output power: 6dBm
- Bluetooth receiving sensitivity: -93dBm@GFSK, -92dBm@π/4 DQPSK, -86dBm@8DPSK modulation

3 Processor Core

- 240MHz(typical) RISC-32 CPU processor Core
- 32-bit Address and Data Paths
- RISC reduced instruction structure
- 32 bit data, 16/32 bit mixed coding command

4 DSP Core

- 400MHz CEVA TL420 DSP core
- High code compactness
- All instructions can be conditional
  - Conditional execution
  - Reduces cycle count and code size on control and overhead code
- Computational units:
  - One 32-bit x 32-bit Multiply-and-Accumulate (MAC) using 72-bit product
  - One 32-bit x 16-bit MAC using 72-bit product
  - One 32-bit x 32-bit MAC unit with automatic scaling
  - One 32-bit x 16-bit MAC unit with automatic scaling
  - One 36-bit arithmetic unit

- One 36-bit logical unit
- One 36-bit bit-manipulation unit, including a full barrel shifter and an exponent unit
- Four 36-bit accumulators
- Fully programmable product post-shifter for product scaling

- 32-bit Scalar (SC) unit for integer operations
- Unaligned memory access for load and store operations

5 Memory Controller

- Internal 32KB CPU ICache for SPI NorFlash
- Internal 304KB SRAM for data and program
- Internal 32KB Cache for SPI pSRAM, which can be switched to 32K SRAM when Cache is useless.
- It is accessible for all the RAM blocks through DMA
- It is accessible for all the RAM blocks through DSP's data bus and program bus
- It is accessible for all the RAM and ROM block through CPU I/D bus
- The hardware code replace mechanism can fix up to 4 instructions at the same time
- The page miss control mechanism can support 16 different pages at the same time

6 DMA Controller

6.1 Features

- DMA transmission is independent with the CPU and DSP
- Support for memory to memory, memory to peripheral, peripheral to memory, CARD to USB, and USB to CARD transmission.
- 8-channel ordinary DMA, that supports for transmission in burst 8 mode or single mode. Only one of the eight DMA channels can transfer data at the same time.
- DMA0-7 transmission can be triggered on the occurrence of selected events
- Each channel can send two interrupts to the CPU on completion of certain operational events
- Transmission width includes 8-bit, 16-bit, and 32-bit, which is determined by DMA transmission type.

6.2 Memory and Peripheral Access Description

6.2.1 Access memory

（1） Memory is accessed by DMA according to physical address.

（2） The following situations will lead to transfer error:
- Access rom
- Ram has been occupied by other modules
- The clock of ram is disabled

（3） DMA can access PSRAM by CACHE mode or UNCACHE mode. The DMASADDR and DMADADDR must both be PSRAM or Internal RAM when using the AUDIO separated type to transfer.

（4） Memory-to-memory transmission:
- The data in memory should be aligned by word (32-bit) when transferred.
- The transfer width is 64-bit when both the source and destination address are aligned by double-word (64-bit), otherwise the transfer width is 32-bit.

（5） Memory-to-peripheral and peripheral-to-memory transmission:
- The data in memory should be aligned by word (32-bit) when the transfer width is 32-bit or 24-bit.

- The data in memory should be aligned by half-word (16-bit) when the transfer width is 16-bit.
- The data in memory should be aligned by byte (8-bit) when the transfer width is 8-bit.

（6） SRCTYPE/ DSTTYPE/SADDR/DADDR should be set when DMA access the peripherals.

（7） CPU cannot access the peripherals FIFO when the peripherals FIFO is accessed by DMA.

6.2.2 Access Peripheral FIFO

The peripherals that can be accessed by DMA are shown as following:

FIFO Type	FIFO Width	FIFO Depth
SPI0 TX FIFO	8	16
SPI0 RX FIFO	8	16
UART0/1 TX FIFO	8	16
UART0/1 RX FIFO	8	16
USB FIFO	8/32	8
SD/MMC FIFO	32	128
SDIO	32	128
LCD FIFO	16	8
I2S TX/DAC/SPDIF TX FIFO0(DACFIFO0)	16/24(32)	32
I2S TX/DAC/SPDIF TX FIFO1(DACFIFO1)	16/24(32)	32
I2S TX/SPDIF TX FIFO(I2STXFIFO)	16/24(32)	32
I2S RX0/ADC FIFO(ADCFIFO)	16/24(32)	32
I2S RX1/SPDIF RX FIFO(I2SRX1FIFO)	16/24(32)	32
SPI1 TX FIFO	8/32	16
SPI1 RX FIFO	8/32	16
SPI2 TX FIFO	8/32	16
SPI2 RX FIFO	8/32	16

6.2.3 Access Peripheral Mode

Peripheral	Single	Burst8
SPI0	Y	Y
UART0/1	Y	Y
USB	Y	Y
SD/MMC	N	Y
SDIO	N	Y
LCD	N	Y
I2STX/DAC/SPDIFTX	N	Y
I2SRX0/ADC	N	Y
I2SRX1/SPDIFRX	N	Y
SPI1	Y	Y
SPI2	Y	Y

6.2.4 DMA channel priority

Each memory block can be accessed by only one of the three masters at the same time, which are DSP, CPU, and DMA. The 8 channels of DMA share the same bus, so only one of these channels can use the bus to transfer data at the same moment.

While accessing one memory block, DMA submits an access request to the memory controller's arbiter. Meanwhile, DSP or CPU might send another request to access the same memory block. The arbiter grants the bus of this memory block according to the priority scheme. The priority scheme is known as round-robin algorithm. When DMA does not get the bus of this memory block, the memory controller will

hold DMA. See memory controller specification for details.
Once DMA obtains the highest priority among the three masters, one of the 6 channels occupies the DMA bus according to the internal priority. The priority of DMA channel is DMA0 > DMA1 > DMA2 > DMA3 > DMA4 > DMA5 > DMA6 > DMA7.

6.2.5 DMA Access Channel

DMA supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory transmission. Specific access paths are shown as follows:

DST / SRC	RAM	SPI0/1/2 TX FIFO	UART0 UART1 TX FIFO	USB FIFO	SDIO FIFO	SD/ MMC FIFO	LCD FIFO	I2S TX (SPDIFTX/ DAC) FIFO0/1	I2S TX/ SPDIFTX FIFO	PSRAM
RAM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SPI0/1/2 RX FIFO	Y	-	-	-		-	-	-		Y
UART0/1 RX FIFO	Y	-	-	-		-	-	-		Y
USB FIFO	Y	-	-	-		Y	-	-		Y
SDIO	Y									Y
SD/MMC FIFO	Y	-	-	Y		-	-	-		Y
LCD FIFO	Y	-	-	-		-	-	-		Y
I2S RX0 (ADC)FIFO	Y	-	-	-		-	-	-		Y
I2S RX1 SPDIF RX FIFO	Y									Y
PSRAM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

6.3 DMA Register List

Table 6-1 DMA controller base address

Name	Physical Base Address	KSEG1 Base Address
DMA Controller	0xC0040000	0xC0040000

Table 6-2 DMA controller register list

Offset	Register Name	Description
0x00000000	DMAIP	DMA interrupt pending register
0x00000004	DMAIE	DMA interrupt enable register
0x00000008	DMATIMEOUTPD	DMA time out Pending register
0x00000100	DMA0CTL	DMA0 control register
0x00000104	DMA0START	DMA0 start register
0x00000108	DMA0SADDR0	DMA0 source address register 0
0x0000010c	DMA0SADDR1	DMA0 source address register 1
0x00000110	DMA0DADDR0	DMA0 destination address register 0
0x00000114	DMA0DADDR1	DMA0 destination address register 1
0x00000118	DMA0BC	DMA0 byte counter register
0x0000011C	DMA0RC	DMA0 Remain counter Register
0x00000200	DMA1CTL	DMA1 control register
0x00000204	DMA1START	DMA1 start register
0x00000208	DMA1SADDR0	DMA1 source address register 0
0x0000020C	DMA1SADDR1	DMA1 source address register 1
0x00000210	DMA1DADDR0	DMA1 destination address register 0

0x00000214	DMA1DADDR1	DMA1 destination address register 1
0x00000218	DMA1BC	DMA1 byte counter register
0x0000021C	DMA1RC	DMA1 Remain counter Register
0x00000300	DMA2CTL	DMA2 control register
0x00000304	DMA2START	DMA2 start register
0x00000308	DMA2SADDR0	DMA2 source address register 0
0x0000030C	DMA2SADDR1	DMA2 source address register 1
0x00000310	DMA2DADDR0	DMA2 destination address register 0
0x00000314	DMA2DADDR1	DMA2 destination address register 1
0x00000318	DMA2BC	DMA2 byte counter register
0x0000031C	DMA2RC	DMA2 Remain counter Register
0x00000400	DMA3CTL	DMA3 control register
0x00000404	DMA3START	DMA3 start register
0x00000408	DMA3SADDR0	DMA3 source address register 0
0x0000040C	DMA3SADDR1	DMA3 source address register 1
0x00000410	DMA3DADDR0	DMA3 destination address register 0
0x00000414	DMA3DADDR1	DMA3 destination address register 1
0x00000418	DMA3BC	DMA3 byte counter register
0x0000041C	DMA3RC	DMA3 Remain counter Register
0x00000500	DMA4CTL	DMA4 control register
0x00000504	DMA4START	DMA4 start register
0x00000508	DMA4SADDR0	DMA4 source address register 0
0x0000050C	DMA4SADDR1	DMA4 source address register 1
0x00000510	DMA4DADDR0	DMA4 destination address register 0
0x00000514	DMA4DADDR1	DMA4 destination address register 1
0x00000518	DMA4BC	DMA4 byte counter register
0x0000051C	DMA4RC	DMA4 Remain counter Register
0x00000600	DMA5CTL	DMA5 control register
0x00000604	DMA5START	DMA5 start register
0x00000608	DMA5SADDR0	DMA5 source address register 0
0x0000060C	DMA5SADDR1	DMA5 source address register 1
0x00000610	DMA5DADDR0	DMA5 destination address register 0
0x00000614	DMA5DADDR1	DMA5 destination address register 1
0x00000618	DMA5BC	DMA5 byte counter register
0x0000061C	DMA5RC	DMA5 Remain counter Register
0x00000700	DMA6CTL	DMA6 control register
0x00000704	DMA6START	DMA6 start register
0x00000708	DMA6SADDR0	DMA6 source address register 0
0x0000070C	DMA6SADDR1	DMA6 source address register 1
0x00000710	DMA6DADDR0	DMA6 destination address register 0
0x00000714	DMA6DADDR1	DMA6 destination address register 1
0x00000718	DMA6BC	DMA6 byte counter register
0x0000071C	DMA6RC	DMA6 Remain counter Register
0x00000800	DMA7CTL	DMA7 control register
0x00000804	DMA7START	DMA7 start register
0x00000808	DMA7SADDR0	DMA7 source address register 0
0x0000080C	DMA7SADDR1	DMA7 source address register 1
0x00000810	DMA7DADDR0	DMA7 destination address register 0
0x00000814	DMA7DADDR1	DMA7 destination address register 1
0x00000818	DMA7BC	DMA7 byte counter register
0x0000081C	DMA7RC	DMA7 Remain counter Register

6.4 DMA Register Description

6.4.1 DMAIP

DMA Interrupt Pending Register, offset = 0x00000000

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	DMA7HFIP	DMA7 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
14	DMA6HFIP	DMA6 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
13	DMA5HFIP	DMA5 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
12	DMA4HFIP	DMA4 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear.	R/W	0x0
7	DMA7TCIP	DMA7 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
6	DMA6TCIP	DMA6 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
5	DMA5TCIP	DMA5 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
4	DMA4TCIP	DMA4 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0

6.4.2 DMAIE

DMA Interrupt Enable Register, offset = 0x00000004

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	DMA7HFIE	DMA7 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
14	DMA6HFIE	DMA6 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
13	DMA5HFIE	DMA5 Half Transmission Complete IRQ enable	R/W	0x0

		0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt		
12	DMA4HFIE	DMA4 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
7	DMA7TCIE	DMA7 Transmission Complete IRQ Enable 0: disable DMA7 Transmission Complete interrupt 1: enable DMA7 Transmission Complete interrupt	R/W	0x0
6	DMA6TCIE	DMA6 Transmission Complete IRQ Enable 0: disable DMA6 Transmission Complete interrupt 1: enable DMA6 Transmission Complete interrupt	R/W	0x0
5	DMA5TCIE	DMA5 Transmission Complete IRQ Enable 0: disable DMA5 Transmission Complete interrupt 1: enable DMA5 Transmission Complete interrupt	R/W	0x0
4	DMA4TCIE	DMA4 Transmission Complete IRQ Enable 0: disable DMA4 Transmission Complete interrupt 1: enable DMA4 Transmission Complete interrupt	R/W	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	R/W	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	R/W	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	R/W	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	R/W	0x0

6.4.3 DMATIMEOUTPD

DMA Timeout Pending Register, offset = 0x00000008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R/W	0x0
7	DMA7TOPD	DMA7 Tansmission Time out Pending	R/W	0x0
6	DMA6TOPD	DMA6 Tansmission Time out Pending	R/W	0x0
5	DMA5TOPD	DMA5 Tansmission Time out Pending	R/W	0x0
4	DMA4TOPD	DMA4 Tansmission Time out Pending	R/W	0x0
3	DMA3TOPD	DMA3 Tansmission Time out Pending	R/W	0x0
2	DMA2TOPD	DMA2 Tansmission Time out Pending	R/W	0x0

1	DMA1TOPD	DMA1 Tansmission Time out Pending	R/W	0x0
0	DMA0TOPD	DMA0 Tansmission Time out Pending	R/W	0x0

Note: These bits can be written '1' to clear.

6.4.4 DMA0CTL

DMA0 control Register, offset = 0x00000100

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0 (DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1 (DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO	R/W	0x0

		4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved		

6.4.5 DMA0START

DMA0 Start Register 0, offset = 0x00000104

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.6 DMA0SADDR0

DMA0 Source Address Register 0, offset = 0x00000108

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.7 DMA0SADDR1

DMA0 Source Address Register 1, offset = 0x0000010C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.8 DMA0DADDR0

DMA0 Destination Address Register 0, offset = 0x00000110

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.9 DMA0DADDR1

DMA0 Destination Address Register 1, offset = 0x00000114

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.10 DMA0BC

DMA0 Byte Counter Register, offset = 0x00000118

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA0 transmission	R/W	0x0

6.4.11 DMA0RC

DMA0 Remain Byte Counter Register, offset = 0x0000011C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA0 transmission	R/W	0x0

6.4.12 DMA1CTL

DMA1 control Register, offset = 0x00000200

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0 (DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1 (DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO	R/W	0x0

		Others: Reserved		
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO (ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.13 DMA1START

DMA1 Start Register 0, offset = 0x00000204

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.14 DMA1SADDR0

DMA1 Source Address Register 0, offset = 0x00000208

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA1 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.15 DMA1SADDR1

DMA1 Source Address Register 1, offset = 0x0000020C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA1 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.16 DMA1DADDR0

DMA1 Destination Address Register 0, offset = 0x00000210

Bits	Name	Description	Access	Reset

31:0	DMADADDR	The destination address 0 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.17 DMA1DADDR1

DMA1 Destination Address Register 1, offset = 0x00000214

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA1 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.18 DMA1BC

DMA1 Byte Counter Register, offset = 0x00000218

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA1 transmission	R/W	0x0

6.4.19 DMA1RC

DMA1 Remain Byte Counter Register, offset = 0x0000021C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA1 transmission	R/W	0x0

6.4.20 DMA2CTL

DMA2 control Register, offset = 0x00000300

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory	R/W	0x0

		4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved		
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.21 DMA2START

DMA2 Start Register 0, offset = 0x00000304

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.22 DMA2SADDR0

DMA2 Source Address Register 0, offset = 0x00000308

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.23 DMA2SADDR1

DMA2 Source Address Register 1, offset = 0x0000030C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.24 DMA2DADDR0

DMA2 Destination Address Register 0, offset = 0x00000310

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.25 DMA2DADDR1

DMA2 Destination Address Register 1, offset = 0x00000314

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.26 DMA2BC

DMA2 Byte Counter Register, offset = 0x00000318

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA2 transmission	R/W	0x0

6.4.27 DMA2RC

DMA2 Remain Byte Counter Register, offset = 0x0000031C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA2 transmission	R/W	0x0

6.4.28 DMA3CTL

DMA3 control Register, offset = 0x00000400

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is	R/W	0x0

		complete: 0: disable reload mode 1: enable reload mode		
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.29 DMA3START

DMA3 Start Register 0, offset = 0x00000404

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by	R/W	0x0

		the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.		

6.4.30 DMA3SADDR0

DMA3 Source Address Register 0, offset = 0x00000408

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.31 DMA3SADDR1

DMA3 Source Address Register 1, offset = 0x0000040C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.32 DMA3DADDR0

DMA3 Destination Address Register 0, offset = 0x00000410

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.33 DMA3DADDR1

DMA3 Destination Address Register 1, offset = 0x00000414

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.34 DMA3BC

DMA3 Byte Counter Register, offset = 0x00000418

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA3 transmission	R/W	0x0

6.4.35 DMA3RC

DMA3 Remain Byte Counter Register, offset = 0x0000041C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA3 transmission	R/W	0x0

6.4.36 DMA4CTL

DMA4 control Register, offset = 0x00000500

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO	R/W	0x0

		Others: Reserved		

6.4.37 DMA4START

DMA4 Start Register 0, offset = 0x00000504

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.38 DMA4SADDR0

DMA4 Source Address Register 0, offset = 0x00000508

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.39 DMA4SADDR1

DMA4 Source Address Register 1, offset = 0x0000050C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.40 DMA4DADDR0

DMA4 Destination Address Register 0, offset = 0x00000510

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.41 DMA4DADDR1

DMA4 Destination Address Register 1, offset = 0x00000514

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.42 DMA4BC

DMA4 Byte Counter Register, offset = 0x00000518

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA4 transmission	R/W	0x0

6.4.43 DMA4RC

DMA4 Remain Byte Counter Register, offset = 0x0000051C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA4 transmission	R/W	0x0

6.4.44 DMA5CTL

DMA5 control Register, offset = 0x00000600

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory	R/W	0x0

		4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved		

6.4.45 DMA5START

DMA5 Start Register 0, offset = 0x00000604

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.46 DMA5SADDR0

DMA5 Source Address Register 0, offset = 0x00000608

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.47 DMA5SADDR1

DMA5SADDR1 (DMA5 Source Address Register 1, offset = 0x0000060c)

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.48 DMA5DADDR0

DMA5 Destination Address Register 0, offset = 0x00000610

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.49 DMA5DADDR1

DMA5 Destination Address Register 1, offset = 0x00000614

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.50 DMA5BC

DMA5 Byte Counter Register, offset = 0x00000618

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA5 transmission	R/W	0x0

6.4.51 DMA5RC

DMA5 Remain Byte Counter Register, offset = 0x0000061C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA5 transmission	R/W	0x0

6.4.52 DMA6CTL

DMA6 control Register, offset = 0x00000700

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO	R/W	0x0

		4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved		
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.53 DMA6START

DMA6 Start Register 0, offset = 0x00000704

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.54 DMA6SADDR0

DMA6 Source Address Register 0, offset = 0x00000708

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.55 DMA6SADDR1

DMA6 Source Address Register 1, offset = 0x0000070C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.56 DMA6DADDR0

DMA6 Destination Address Register 0, offset = 0x00000710

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.57 DMA6DADDR1

DMA6 Destination Address Register 1, offset = 0x00000714

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.58 DMA6BC

DMA6 Byte Counter Register, offset = 0x00000718

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA6 transmission	R/W	0x0

6.4.59 DMA6RC

DMA6 Remain Byte Counter Register, offset = 0x0000071C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA6 transmission	R/W	0x0

6.4.60 DMA7CTL

DMA7 control Register, offset = 0x00000800

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode	R/W	0x0

		0: increment 1: constant		
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.61 DMA7START

DMA7 Start Register 0, offset = 0x00000804

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.62 DMA7SADDR0

DMA7 Source Address Register 0, offset = 0x00000808

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA7 transmission	R/W	0x0

		The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.		

6.4.63 DMA7SADDR1

DMA7 Source Address Register 1, offset = 0x0000080C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.64 DMA7DADDR0

DMA7 Destination Address Register 0, offset = 0x00000810

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.65 DMA7DADDR1

DMA7 Destination Address Register 1, offset = 0x00000814

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.66 DMA7BC

DMA7 Byte Counter Register, offset = 0x00000818

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA7 transmission	R/W	0x0

6.4.67 DMA7RC

DMA7 Remain Byte Counter Register, offset = 0x0000081C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA7 transmission	R/W	0x0

7 PMU

7.1 Features

The ATS2837 integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery and DC5V power supply
- Integrated DC-DC buck converters output 1.5V
- Linear regulators outputs AVCC from VCC, and VDD from VD15

7.2 Module Description

7.2.1 DC-DC Converter

The DC-DC converter efficiently scales battery voltage to the required supply voltage. It can work in Pulse Frequency Modulation (PFM) or Pulse Width Modulation (PWM) automatically for different load current. The DC-DC converters include several advanced features:

- Input power from SYSPOWER
- Synchronization DC-DC converter architecture
- Programmable output voltages 1.0~1.7V
- Work in Pulse Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) automatically for different load current.
- Support 2.2uH ~ 4.7uH power inductor, support soft start.

7.2.2 Linear Regulators

7.2.2.1 Regulators Accurate and Maximum Output Current

The output voltages are highly precise within ±2%, They provide large currents with a significantly small dropout voltage within ±5%. Table7-1 shows data of maximum output current.

Table 7-1 Regulators Maximum Output Current

Block Name	Output Voltage	Load Capacity
VCC	2.7~3.4V	300 mA
VDD	0.8~1.5V	70 mA@98%
AVCC	VCC-0.15V	50 mA@98%

7.2.2.2 Regulators Power Down

If the system is to operate from an external power supply, then the internal linear regulators are powered down automatically.

7.2.3 Reference Voltage

There is a build-in 1.5V-reference voltage output—VREFI.

7.2.4 A/D Converters

There are 10 bits A/Ds for system monitor, the input voltage range of which is 0V to 3.6V@ LRADC2~11 pin , 1.5V to 4.5V at VBAT pin, 0V to 6.0V at DC5V pin, 0V to SVCC at LRADC1 pin ,-40~120℃ for temp sensor.
For LRADC1~11, 1LSB = 3.6V/(2^10) = 3.52mV;
For BATADC, 1LSB = 3V/(2^10) =2.93mV;
For DC5V, 1LSB = 6V/(2^10) = 5.86mV;
For SENSADC, T=160/1024*data (decimal) - 40℃;
When the input voltage is V, the related ADC data n = V/(3.6/2^10).

7.3 PMU Register List

Table 7-2 PMU block base address

Name	Physical Base Address	KSEG1 Base Address

PMU	0xC0020000	0xC0020000

Table 7-3 PMU Block Configuration Registers List

Offset	Register Name	Description
0x14	WKEN_CTL	Wake up source enable Register
0x18	WAKE_PD	Wake up pending control Register
0x1C	ONOFF_KEY	On/off KEY control Register
0x44	VOUT_CTL	VCC/VDD/AVCC voltage set Register
0x48	MULTI_USED	multi-used set Register
0x50	PMUADC_CTL	PMU ADC frequency and enable Register
0x54	BATADC_DATA	BATADC data Register
0x58	TEMPADC_DATA	TEMPADC data Register
0x5C	DC5VADC_DATA	DC5V ADC data Register
0x60	SENSADC_DATA	Sensor ADC DATA Register
0x64	LRADC1_DATA	LRADC1 data Register
0x68	LRADC2_DATA	LRADC2 data Register
0x6C	LRADC3_DATA	LRADC3 data Register
0x70	LRADC4_DATA	LRADC4 data Register
0x74	LRADC5_DATA	LRADC5 data Register
0x78	LRADC6_DATA	LRADC6 data Register
0x7C	LRADC7_DATA	LRADC7 data Register
0x80	LRADC8_DATA	LRADC8 data Register
0x84	LRADC9_DATA	LRADC9 data Register
0x88	LRADC10_DATA	LRADC10 data Register
0x8C	LRADC11_DATA	LRADC11 data Register
0x90	AVCCADC_DATA	AVCCADC data Register

7.4 PMU Register Description

7.4.1 WKEN_CTL

Wake up source enable Register, offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved	R	0x0
13	IRC_WK_EN	IRC wake-up enable bit 0: Disable 1: Enable	R/W	0x1
12	BAT_WK_EN	battery insertion wake-up enable bit 0: Turn off battery insertion wake-up 1: Open battery insertion detection	R/W	0x1
11	REMOTE_WK_EN	Wire-control wake-up enable bit 0: Turn off wire-control wake-up 1: Open wire-control wake-up	R/W	0x1
10	UVLOWPD_SEL	DC5V wake-up condition 0: DC5V>BAT+0.1V 1: DC5V>BAT+0.02V	R/W	0x1
9	NFC_WK_EN	NFC wake-up enable bit 0: Disable	R/W	0x1

		1: Enable		
8	HDSW_BLOCK	Toggle switch shields long/short press on play key to wakeup enable release bit 0: Toggle switch turn to OFF will shield long/shot press on the play key to wake up 1: Toggle switch do not shield long/short press on the play key to wake up	R/W	0x0
7	HDSWOFF_EN	Toggle switch power off enable bit in sniff status 0: Disable 1: Enable	R/W	0x1
6	BT_WK_EN	Bluetooth wake-up enable bit 0: Disable 1: Enable	R/W	0x1
5	DC5VOFF_WK_EN	DC5V was pulled up wake-up enable bit 0: Disable 1: Enable	R/W	0x0
4	DC5VON_WK_EN	DC5V was pulled in wake-up enable bit 0: Disable 1: Enable	R/W	0x1
3	RESET_WK_EN	RESET wake-up enable bit 0: Disable 1: Enable	R/W	0x1
2	SHORT_WK_EN	ONOFF was short press wake-up enable bit 0: Disable 1: Enable	R/W	0x0
1	LONG_WK_EN	ONOFF was long press wake-up enable bit 0: Disable 1: Enable	R/W	0x1
0	HDSW_WK_EN	HDSW toggle switch wake-up enable bit 0: Disable 1: Enable	R/W	0x1

7.4.2 WAKE_PD

WAKE up pending control Register, offset = 0x18

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R/W	0x0
23	LB_PD	Battery low power protection pending bit 0: Battery low power did not happen 1: The battery is low power Write “1” to clear this bit.	R/W	0x0
22:20	-	Reserved	R/W	0x0
19	DC5VRST_PD	DC5V reset pending 0: no DC5V reset 1: DC5V reset happened Write “1” to clear this bit.	R/W	0x0
18:16	-	Reserved	R/W	0x0
15	ONOFF_L_PD	Long press on ONOFF key pending bit 0: no long press on ONOFF key 1: long press on ONOFF key happened Write “1” to clear this bit.	R/W	0x0
14	ONOFF_S_PD	Short press on ONOFF key pending bit 0: no short press on ONOFF key	R/W	0x0

		1: short press on ONOFF key happened Write “1” to clear this bit.		
13	IRC_WK_PD	IRC wakeup pending bit 0: no IRC wakeup 1: IRC wakeup happened Write “1” to clear this bit.	R/W	0x0
12	BAT_PD	Battery insert wakeup pending bit 0: no battery insert wakeup 1: battery insert wakeup happened Write “1” to clear this bit.	R/W	0x0
11	REMOTE_PD	Drive-by-wire control wakeup pending bit 0: no Drive-by-wire control wakeup 1: Drive-by-wire control wakeup happened Write “1” to clear this bit.	R/W	0x0
10:8	-	Reserved	R/W	0x0
7	HDSWOFF_PD	Toggle switch OFF pending bit 0: no toggle switch operation 1: toggle switch OFF operation happened Write “1” to clear this bit.	R/W	0x0
6	BT_WK_PD	Bluetooth Pending 0: Interrupt source is not active. 1: Interrupt source is active. Writing ‘1’ to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.	R/W	0x0
5	DC5VOFF_PD	DC5V pull out pending bit 0: no DC5V pull out 1: DC5V pull out happened Write “1” to clear this bit.	R/W	0x0
4	DC5VON_PD	DC5V pull in pending bit 0: no DC5V pull in 1: DC5V pull in happened Write “1” to clear this bit.	R/W	0x0
3	-	Reserved	R/W	0x0
2	SHORT_WK_PD	Short press ONOFF wakeup pending bit 0: no short press 1: short press happened Write “1” to clear this bit.	R/W	0x0
1	LONG_WK_PD	Long press ONOFF wakeup pending bit 0: no long press 1: long press happened Write “1” to clear this bit.	R/W	0x0
0	HDSWON_PD	Toggle switch ON pending bit 0: no toggle switch operation 1: toggle switch ON operation happened Write “1” to clear this bit.	R/W	0x0

7.4.3 ONOFF_KEY

ONOFF key control & detect register, offset = 0x1C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R/W	x
10	RESTART_SET	Set up RESET key function	R/W	0x0

		0: reset VDD power domain registers 1: restart, system enters standby after pressing reset (Debounce 16ms), and waked up to active after lifting up the key.		
9:7	ONOFF_PRESS_TIME	Set up ONOFF keystroke duration 000: 50ms < t < 0.125s, short press; t >=0.125s, long press. 001: 50ms < t < 0.25s, short press; t >=0.25s, long press. 010: 50ms < t < 0.5s, short press; t >=0.5s, long press. 011: 50ms < t < 1s, short press; t >=1s, long press. 100: 50ms < t < 1.5s, short press; t >=1.5s, long press. 101: 50ms < t < 2s, short press; t >=2s, long press. 110: 50ms < t < 3s, short press; t >=3s, long press. 111: 50ms < t < 4s, short press; t >=4s, long press.	R/W	0x1
6	ONOFF_RST_EN	Enable long press ONOFF to reset 0: Disable 1: Enable	R/W	0x1
5:4	ONOFF_RST_T_SEL	Long press ONOFF to send reset signal time 00: 8s 01: 12s 10: 16s 11: 24s	R/W	0x0
3	ONOFF_STATE	Toggle switch status machine indicator bit 0: 2/3 status (OFF status) 1: 1/3 status (ON status)	R	0x1
2	HDSWOFF_2_3	ONOFF electrical level 0: Not at this electrical level 1: at 2/3 electrical level	R	0x0
1	HDSWON_1_3	ONOFF electrical level 0: Not at this electrical level 1: at 1/3 electrical level	R	0x0
0	ONOFF_PRESS_0	ONOFF key pressed indicator bit 0: ONOFF key was not pressed 1: ONOFF key was pressed	R	0x0

7.4.4 VOUT_CTL

Voltage set register, offset=0x44

Bit (s)	Name	Description	Access	Reset
31:21	-	Reserved	R/W	0x0
20	SPLL_AVDD_EN	SPLL_AVDD LDO Enable 0: Disable 1: Enable	R/W	0x0
19	SPLL_AVDD_VOL_SET	SPLL_AVDD Voltage Set 0: 1.1V 1: 1.2V	R/W	0x1

18	AVDD_PD	AVDD capacitor-less LDO pull-down 0: no pull-down 1: 1mA pull-down	R/W	0x1
17:16	AVDD_VOL	00: 1.0V 01: 1.1V 10: 1.2V 11: 1.3V	R/W	0x2
15	AVCC_BIASEN	AVCC_BIAS SET 0: small current 1: big current	R/W	0x0
14:13	AVCC_DROP	AVCC LDO margin tuning, voltage drop from VCC ***00: 0.15V 01: 0.20V 10: 0.25V 11: 0.30V	R/W	0x0
12	VCCOC_SET	VCC LDO Current limit 0: 400mA 1: 500mA	R/W	0x0
11	VDDOC_SET	VDD LDO Current limit 0: 200mA 1: 300mA	R/W	0x0
10:8	VCC_SET	VCC voltage level select 000: 2.7V 001: 2.8V 010: 2.9V 011: 3.0V *100: 3.1V 101: 3.2V 110: 3.3V 111: 3.4V	R/W	0x4
7:4	VDD_SET_S1	VDD(Regulator) voltage coarse control (S1) 0000: 0.80V 0001: 0.85V 0010: 0.9V 0011: 0.95V 0100: 1.0V 0101: 1.05V 0110: 1.1V 0111: 1.15V *1000: 1.2V 1001: 1.25V 1010: 1.3V 1011: 1.35V 1100: 1.4V 1101: 1.45V 1111: 1.5V	R/W	0x8
3:0	VDD_SET_S3BT	VDD(Regulator) voltage coarse control (S3BT) 0000 0.80V 0001 0.85V *0010 0.9V 0011 0.95V 0100 1.0V 0101 1.05V 0110 1.1V	R/W	0x2

		0111 1.15V 1000 1.2V 1001 1.25V 1010 1.3V 1011 1.35V 1100 1.4V 1101 1.45V 1111 1.5V		

7.4.5 MULTI_USED

Multi Use register, offset=0x48

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14	UVLO_T	Debounce time selection for UVLO indication 0: 41us 1: 16ms	R/W	0x1
13:10	-	Reserved	R	0x0
9	UVLO	DC5V pull-in detection condition 0: no DC5V pull-in detection 1: DC5V>BAT+0.1V or DC5V>BAT+0.02V	R	x
8	UVDD_EN	USBVDD LDO enable 0: Disable 1: Enable	R/W	0x0
7:5	UVDD_V	USBVDD LDO output voltage control 000: 1.0V 001: 1.05V 010: 1.1V 011: 1.15V 100: 1.2V 101: 1.25V 110: 1.3V 111: reserved	R/W	0x4
4	USBVDD_PD	USBVDD pull-down resistor enable 0: Disable, no pull-down resistor. 1: Enable, pull-down resistor corresponds to 1mA load current.	R/W	0x0
3	USBVDD_PD2	USBVDD pull-down resistor_2 enable 0: Disable, no pull-down resistor_2. 1: Enable, pull-down resistor_2 corresponds to 5mA load current.	R/W	0x0
2	USBVDD_PD3	USBVDD pull-down resistor_3 enable 0: Disable, no pull-down resistor_3. 1: Enable, pull-down resistor_3 corresponds to 10mA load current.	R/W	0x0
1	SEG_DISP_VCC_EN	Segment screen power enable 0: Disable 1: Enable	R/W	0x0
0	SEG_LED_EN	LED constant current source enable 0: Disable 1: Enable	R/W	0x0

7.4.6 PMUADC_CTL

PMUADC Control Register, offset = 0x50

Bit (s)	Name	Description	Access	Reset
31:18	-	Reserved	R/W	0x0
17	I_COMP_SET	ADC COMP current set 0: 0.5uA 1: 1uA	R/W	0x0
16	COMP_TRIM	COMP trim enable 0: Disable 1: Enable	R/W	0x1
15	LRADC11_EN	LRADC11 A/D enable 0: Disable 1: Enable	R/W	0x0
14	LRADC10_EN	LRADC10 A/D enable 0: Disable 1: Enable	R/W	0x0
13	LRADC9_EN	LRADC9 A/D enable 0: Disable 1: Enable	R/W	0x0
12	LRADC8_EN	LRADC8 A/D enable 0: Disable 1: Enable	R/W	0x0
11	LRADC7_EN	LRADC7 A/D enable 0: Disable 1: Enable	R/W	0x0
10	LRADC6_EN	LRADC6 A/D enable 0: Disable 1: Enable	R/W	0x0
9	LRADC5_EN	LRADC5 A/D enable 0: Disable 1: Enable	R/W	0x0
8	LRADC4_EN	LRADC4 A/D enable 0: Disable 1: Enable	R/W	0x0
7	LRADC3_EN	LRADC3 A/D enable 0: Disable 1: Enable	R/W	0x0
6	LRADC2_EN	LRADC2 A/D enable 0: Disable 1: Enable	R/W	0x0
5	LRADC1_EN	LRADC1 A/D enable 0: Disable 1: Enable	R/W	0x1
4	SENSORADC_EN	sensor A/D enable 0: Disable, sensor circuit and output disable 1: Enable, sensor circuit and output enable	R/W	0x0
3	DC5VADC_EN	DC5V A/D enable 0: Disable 1: Enable	R/W	0x1
2	TEMPADC_EN	TEMP A/D enable 0: Disable 1: Enable	R/W	0x1

1	BATADC_EN	Battery A/D enable 0: Disable 1: Enable	R/W	0x1
0	AVCCADC_EN	AVCC A/D enable 0: Disable 1: Enable	R/W	0x1

7.4.7 BATADC_DATA

BATADC DATA Register, offset = 0x54

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	BATADC	10bit Voltage ADC, used to detect Battery voltage. Input Li-ion voltage range is 1.5-4.5V.	R	xx

7.4.8 TEMPADC_DATA

TEMPADC DATA Register, offset = 0x58

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	TEMPADC	10bit Voltage ADC, used to detect TEMPADC voltage. Input voltage range is 0-3.6V.	R	xx

7.4.9 DC5VADC_DATA

DC5V ADC DATA Register, offset = 0x5C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	DC5VADC	10bit Voltage ADC, used to detect DC5V voltage. Input voltage range is 0-6V.	R	xx

7.4.10 SENSADC_DATA

Sensor ADC DATA Register, offset = 0x60

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	SENSADC	10bit Voltage ADC, used to detect TEMPSENSOR voltage.	R	xx

7.4.11 LRADC1_DATA

LRADC1 DATA Register, offset = 0x64

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC1	LRADC1 data output LRADC1 input voltage range is 0 to SVCC.	R	xx

7.4.12 LRADC2_DATA

LRADC2 DATA Register, offset = 0x68

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC2	LRADC2 data output LRADC2 input voltage range is 0 to AVCC.	R	xx

7.4.13 LRADC3_DATA

LRADC3 DATA Register, offset = 0x6C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC3	LRADC3 data output LRADC3 input voltage range is 0 to AVCC.	R	xx

7.4.14 LRADC4_DATA

LRADC4 DATA Register, offset = 0x70

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC4	LRADC4 data output LRADC4 input voltage range is 0 to AVCC.	R	xx

7.4.15 LRADC5_DATA

LRADC5 DATA Register, offset = 0x74

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC5	LRADC5 data output LRADC5 input voltage range is 0 to 3.6V.	R	xx

7.4.16 LRADC6_DATA

LRADC6 DATA Register, offset = 0x78

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC6	LRADC6 data output LRADC6 input voltage range is 0 to 3.6V.	R	xx

7.4.17 LRADC7_DATA

LRADC7 DATA Register, offset = 0x7C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC7	LRADC7 data output LRADC7 input voltage range is 0 to 3.6V.	R	xx

7.4.18 LRADC8_DATA

LRADC8 DATA Register, offset = 0x80

Bit (s)	Name	Description	Access	Reset

31:10	-	Reserved	R	0x0
9:0	LRADC8	LRADC8 data output LRADC8 input voltage range is 0 to 3.6V.	R	xx

7.4.19 LRADC9_DATA

LRADC9 DATA Register, offset = 0x84

Bit (s)	Name	Description	Access	Reset
31:10	-	RESERVED	R	0x0
9:0	LRADC9	LRADC9 data output LRADC9 input voltage range is 0 to 3.6V.	R	xx

7.4.20 LRADC10_DATA

LRADC10 DATA Register, offset = 0x88

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC10	LRADC10 data output LRADC10 input voltage range is 0 to 3.6V.	R	xx

7.4.21 LRADC11_DATA

LRADC11 DATA Register, offset = 0x8C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC11	LRADC11 data output LRADC11 input voltage range is 0 to 3.6V.	R	xx

7.4.22 AVCCADC_DATA

AVCCADC DATA Register, offset = 0x90

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	AVCCADC	AVCCADC data output AVCCADC input voltage range is 0 to 3.6V.	R	xx

8 System Control

8.1 RMU

8.1.1 Features

The RMU Controller of ATS2837 has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU.

8.1.2 RMU Register List

Table 8-1 RMU base address

Name	Physical Base Address	KSEG1 Base Address
RMU	0xC0000000	0xC0000000

Table 8-2 RMU register list

Offset	Register Name	Description
0x0000	MRCR0	Module Reset Control Register0
0x0004	MRCR1	Module Reset Control Register1
0x0008	DSP_VCT_ADDR	DSP_VECTOR_ADDRESS Register

8.1.3 RMU Register Description

8.1.3.1 MRCR0

Module Reset Control Register0, offset = 0x0000

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R/W	0x0
29	SPI2RESET	SPI2 Controller Reset 0: reset 1: normal	R/W	0x0
28:27	-	Reserved	R	0x0
26	IRRESET	IR Controller Reset 0: reset 1: normal	R/W	0x0
25	-	Reserved	R	0x0
24	USBRESET2	This bit should be reset before USBReset bit is reset. 0: reset 1: normal	R/W	0x0
23	USBRESET	USB Reset 0: reset 1: normal	R/W	0x0
22	-	Reserved	R	0x0
21	PWM_RESET	PWM Reset 0: reset 1: normal	R/W	0x0
20	-	Reserved	R	0x0
19	SEGLCDRESET	SEGLCD & SEGLED Controller Reset 0: reset 1: normal	R/W	0x0
18	LCDRESET	LCD controller Reset 0: reset 1: normal	R/W	0x0
17	I2CRESET	I2C Controller Reset 0: reset 1: normal	R/W	0x0
16	UART1RESET	UART1 Controller Reset 0: reset 1: normal	R/W	0x0

15	UART0RESET	UART0 Controller Reset 0: reset 1: normal	R/W	0x0
14	SPI1DCACHERESET	SPI1DCache Controller Reset 0: reset 1: normal	R/W	0x0
13	SPI0CACHERESET	SPICache Controller Reset 0: reset 1: normal	R/W	0x0
12	SPI1RESET	SPI1 Controller Reset 0: reset 1: normal	R/W	0x0
11	SPI0RESET	SPI0 Controller Reset 0: reset 1: normal	R/W	0x0
10	SD1RESET	SD1 Card Controller Reset 0: reset 1: normal	R/W	0x0
9	SD0RESET	SD0/MMC Card Controller Reset 0: reset 1: normal	R/W	0x0
8	AUDIOIORESET	Audio Global Reset 0: reset 1: normal	R/W	0x0
7	-	Reserved	R	0x0
6	SPDIFTXREAST	SPDIFTX Reset 0: reset 1: normal	R/W	0x1
5	SPDIFRXREAST	SPDIFRX Reset 0: reset 1: normal	R/W	0x1
4	I2SRESET	I2S Reset 0: reset 1: normal	R/W	0x1
3	ADCRESET	ADC Reset 0: reset 1: normal	R/W	0x1
2	DACRESET	DAC Reset 0: reset 1: normal	R/W	0x1
1	-	Reserved	R	0x0
0	DMARESET	DMA0 ~ DMA7 Reset 0: reset 1: normal The reset bit of DMA controller is active while it is driven by MCU clock.	R/W	0x0

8.1.3.2 MRCR1

Module Reset Control Register1, offset = 0x0004

Bit (s)	Name	Description	Access	Reset
31	CPURESET	CPU Reset 0: reset	R/W	0x1

		1: normal		
30:29	-	Reserved	R/W	0x0
28	DSP_ALL	All DSP reset 0: reset all dsp 1: depends on DSP_PART	R/W	0x0
27:0	-	Reserved	R/W	0x0

8.1.3.3 DSP_VCT_ADDR

DSP Vector Address Register, offset = 0x0008

Bit (s)	Name	Description	Access	Reset
31:0	DSP_VECTOR_ADDRESS	DSP_VECTOR_ADDRESS	R/W	0x4000

8.2 CMU Analog

8.2.1 Features

- Support only one oscillator inputs: 24MHz
- Supply 4 PLLs and special clocks of all modules. The 4 PLLs are CORE PLL, SPLL, Audio PLL0 and Audio PLL1

8.2.2 CMU Analog Register List

Table 8-3 CMU Analog Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_ANALOG_REGISTER	0xC0000100	0xC0000100

Table 8-4 CMU Analog Controller Registers

Offset	Register Name	Description
0x00	HOSC_CTL	HOSC control register
0x04	CORE_PLL_CTL	CORE_PLL Control Register
0x08	SPLL_CTL	SPLL Control Register
0x0C	AUDIO_PLL0_CTL	AUDIO PLL0 Control Register
0x10	AUDIO_PLL1_CTL	AUDIO PLL1 Control Register

8.2.3 CMU Analog Register Description

8.2.3.1 HOSC_CTL

HOSC control register, offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:27	-	Reserved, be read as zero.	R	0x0
26:24	HOSCI_BC_SEL	HOSCI PAD base cap select 000: 0p 001: 3p 010: 6p 011: 9p 100: 12p	R/W	0x5

		101: 15p** 110: 18p 111: 21p		
23:19	HOSCI_TC_SEL	HOSCI PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCI_TC_SEL	R/W	0x0
18:16	HOSCO_BC_SEL	HOSCO PAD base cap select 000: 0p 001: 3p 010: 6p 011: 9p 100: 12p 101: 15p** 110: 18p 111: 21p	R/W	0x5
15:11	HOSCO_TC_SEL	HOSCO PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCO_TC_SEL	R/W	0x0
10:6	HGMC	High Frequency crystal Oscillator GMMIN select bits	R/W	0x1f
5	BT_HOSC_SEL	BT HOSC clock select 0: BT_HOSC clock select smiths trigger output. 1: BT_HOSC clock select buffer output. This bit is valid for HOSC from the source, not only valid for HOSC to BT.	R/W	0x0
4	VDD_HOSC_SEL	VDD_HOSC clock select 0: select HOSC before GHR 1: select HOSC after GHR Glitch in HOSC low than 3ns will be removed by GHR. The glitch remove clock only provide to VDD power domain;	R/W	0x1
3:1	-	Reserved	R	0x0
0	HOSC_EN	HOSC enable 0: disable 1: enable Only this bit in the register in the VDD domain. When S3 is active by hardware, HOSC will be disabled automatically, insurance lower power consumption in S3 state.	R/W	0x1

8.2.3.2 CORE_PLL_CTL

CORE_PLL Control Register, offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8	CORE_PLL_PMD	CORE PLL phase match detect 0: CORE PLL phase not match 1: CORE PLL phase match	R	X
7	CORE_PLL_EN	CORE PLL Enable 0: Disable 1: Enable	R/W	0x0
6:0	SCORE	CORE PLL Frequency Select: Formula: 6M* SCORE Range:36 ~ 378M Value must be bigger than 6	R/W	0x06

		0-5: reserved 6: 6*6M=36M …… 63: 63*6M=378M Others: reserved.		

8.2.3.3 SPLL_CTL

SPLL Control Register, offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	CK32M_EN	SPLL 32M clock gating 0: disable 1: enable	R/W	0x1
3:2	CK32M_DUTY	SPLL 32M CLOCK duty select 00: 25.0% 01: 37.5% 1x:50%	R/W	0x1
1	SPLL_LOCK	SPLL phase match detect 0: SPLL phase not match 1: SPLL phase match	R	X
0	SPLL_EN	SPLL Enable 0: disable 1: enable	R/W	0x0

8.2.3.4 AUDIO_PLL0_CTL

AUDIO PLL Control Register, offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:6	-	Reserved	R	0x0
5	AUDIO_PLL0_MODE	AUDIO PLL0 Mode selection 0: Mode0 1: Mode1	R/W	0x1
4	AUDPLL0EN	Audio PLL0 Enable 0: Disable 1: Enable	R/W	0x0
3:0	APS0	AUDIO PLL0 Clock Selection	R/W	0x0

8.2.3.5 AUDIO_PLL1_CTL

AUDIO PLL1 Control Register, offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:6	-	Reserved	R	0x0
5	AUDIO_PLL1_MODE	AUDIO PLL1 Mode selection, see Note3 0: Mode0 1: Mode1	R/W	0x1
4	AUDPLL1EN	Audio PLL1 Enable 0: Disable 1: Enable	R/W	0x0
3:0	APS1	AUDIO PLL1 Clock Selection, see Note3	R/W	0x0

8.3 CMU Digital

8.3.1 Features

The CMU (Clock Management Unit) can select HOSC, CORE_PLL, CK3M and CK32K as the clock of each peripheral.

8.3.2 CMU Digital Register List

Table 8-5 CMU Digital Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_DIGITAL_REGISTER	0xC0001000	0xC0001000

Table 8-6 CMU Digital Controller Registers

Offset	Register Name	Description
0x0000	CMU_SYSCLK	SYSCLK Control Register
0x0004	CMU_DEVCLKEN0	DEVCLKEN Control Register0
0x0008	CMU_DEVCLKEN1	DEVCLKEN Control Register1
0x0014	CMU_ADDACLK	ADDACLK Control Register
0x0018	CMU_I2SCLK	I2SCLK Control Register
0x001C	CMU_SPDIFCLK	SPIDIFCLK Control Register
0x0020	CMU_SDCLK	SD0/1 CLK Control Register
0x0024	CMU_SPICLK	SPI0/1 CLK Control Register
0x0028	CMU_IRCLK	IR CLK Control Register
0x002C	CMU_LCDCLK	LCDCLK Control Register
0x0030	CMU_SEGLCDCLK	SEGLCDCLK Control Register
0x0034	CMU_FMCLK	FMCLK Control Register
0x0038	CMU_PWM0CLK	PWMCLK0 Control Register
0x003C	CMU_PWM1CLK	PWMCLK1 Control Register
0x0040	CMU_PWM2CLK	PWMCLK2 Control Register
0x0044	CMU_PWM3CLK	PWMCLK3 Control Register
0x0048	CMU_PWM4CLK	PWMCLK4 Control Register
0x004C	CMU_PWM5CLK	PWMCLK5 Control Register
0x0050	CMU_PWM6CLK	PWMCLK6 Control Register
0x0054	CMU_PWM7CLK	PWMCLK7 Control Register
0x0058	CMU_PWM8CLK	PWMCLK8 Control Register
0x005C	CMU_LRADCCLK	LRADC CLK Control Register
0x0060	CMU_TIMERCLK	TIMER Clock Control Register
0x0080	CMU_MEMCLKEN	MEMCLKEN Control Register
0x0088	CMU_MEMCLKSEL	MEMCLKSEL Control Register
0x00B0	CMU_DSP_WAIT	DSP Wait Control Register
0x00C0	CMU_DSP_AUDIO_VOLCLK_SEL	DSP Audio Volume Control Register

8.3.3 CMU Digital Register Description

8.3.3.1 CMU_SYSCLK

CMU_SYSCLK Control register, offset = 0x00

Bit (s)	Name	Description	Access	Reset

31:22	-	Reserved	R	0x0
21:20	MEMCLKDIV	MEM_CLK divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
19:18	-	Reserved	R	0x0
17:16	DSPAPBCLKDIV	DSP_APB_CLK divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
15:13	-	Reserved	R	0x0
12	AHBCLKDIV	SCLK divisor 0: /2 1: /4	R/W	0x0
11:8	CPUCLKDIV	CPU_CLK coefficient 0x 0: 1/16 0x 1: 2/16 0x 2: 3/16 0x 3: 4/16 0x 4: 5/16 0x 5: 6/16 0x 6: 7/16 0x 7: 8/16 0x 8: 9/16 0x9: 10/16 0xa: 11/16 0xb: 12/16 0xc: 13/16 0xd: 14/16 0xe: 15/16 0xf: 16/16	R/W	0xf
7:6	-	Reserved	R	0x0
5:4	CORECLKDIV	CORE_CLK Divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
3	-	Reserved	R	0x0
2:0	CORE_CLKSEL	CORE_CLK select 000: CK32K 001: CK3M 010: CORE_PLL 011: HOSC 100: CK_64M Others: Reserved	R/W	0x1

8.3.3.2 CMU_DEVCLKEN0

CMU_DEVCLKEN0 Control register, offset = 0x04

Bit (s)	Name	Description	Access	Reset
31	-	Reserved	R/W	0x0

30	EXINTCLKEN	External Interrupt clock enable bit 0: disable 1: enable The source clock of external interrupt is CK3M	R/W	0x1
29	SPI2CLKEN	SPI2 controller clock enable bit 0: disable 1: enable	R/W	0x0
28	I2SSRDCLKEN	I2S Sample Rate Detect Clock Enable 0: disable 1: enable This bit controls the clock gating of I2SSRD_CLK.	R/W	0x0
27	DMICCLKEN	DMIC clock enable bit 0: disable 1: enable	R/W	0x0
26	IRCLKEN	IR clock enable bit 0: disable 1: enable	R/W	0x0
25	TIMERCLKEN	Timer0/1/2/3 controller clock 0: disable 1: enable This bit controls all the clock gatings of TIMERx_CLK.	R/W	0x0
24	-	Reserved	R	0x0
23	USBCLKEN	USB controller clock enable bit 0: disable 1: enable	R/W	0x0
22	LRADCCLKEN	LRADC Controller clock enable bit 0: disable 1: enable	R/W	0x1
21	PWMCLKEN	PWM clock enable bit 0: disable 1: enable This bit controls all the clock gatings of PWMx.	R/W	0x0
20	FMCLKEN	FM clock enable bit 0: disable 1: enable	R/W	0x0
19	SEGLCDCLKEN	Segment LCD clock enable bit 0: disable 1: enable	R/W	0x0
18	LCDCLKEN	LCD controller clock enable bit 0: disable 1: enable	R/W	0x0
17	I2CCLKEN	I2C controller clock enable bit 0: disable 1: enable	R/W	0x0
16	UART1CLKEN	UART1 controller clock enable bit 0: disable 1: enable	R/W	0x0
15	UART0CLKEN	UART0 controller clock enable bit 0: disable 1: enable	R/W	0x0

14	SPI1DCACHECLKEN	SPI1DCACHE Controller clock enable bit 0: disable 1: enable	R/W	0x0
13	SPI0CACHECLKEN	SPICACHE Controller clock enable bit 0: disable 1: enable	R/W	0x0
12	SPI1CLKEN	SPI1 controller clock enable bit 0: disable 1: enable	R/W	0x0
11	SPI0CLKEN	SPI0 controller clock enable bit 0: disable 1: enable	R/W	0x0
10	SD1CLKEN	SD1 card controller clock enable bit 0: disable 1: enable	R/W	0x0
9	SD0CLKEN	SD0 card controller clock enable bit 0: disable 1: enable	R/W	0x0
8	SPDIFRXCLKEN	SPDIF RX clock enable bit 0: disable 1: enable This bit will enable the HOSC Clock which is sent to SPDIFRX module detecting Audio Sample Rate.	R/W	0x0
7	SPDIFTXCLKEN	SPDIF TX clock enable bit 0: disable 1: enable	R/W	0x0
6	I2SRX1MCLKEN	I2S1 RX1 Mclock enable bit 0: disable 1: enable	R/W	0x0
5	I2SRX0MCLKEN	I2S RX0 Mclock enable bit 0: disable 1: enable	R/W	0x0
4	I2STXMCLKEN	I2S TX Mclock enable bit 0: disable 1: enable	R/W	0x0
3	ADCCLKEN	ADC controller clock enable bit 0: disable 1: enable	R/W	0x0
2	DACCLKEN	DAC controller clock enable bit 0: disable 1: enable	R/W	0x0
1	-	Reserved	R	0x0
0	DMACLKEN	DMA clock enable bit 0: disable 1: enable	R/W	0x0

8.3.3.3 CMU_DEVCLKEN1

CMU_DEVCLKEN1 Control register, offset = 0x08

Bit (s)	Name	Description	Access	Reset
31	CPUCLKEN	CPU Clock Enable bit 0: disable	R/W	0x1

		1: enable		
30	-	Reserved	R/W	0x0
29	DSPCLKEN	DSP clock(DSP_CLK, DSP_APB_CLK, DSP_AXI_CLK) enable bit 0: disable 1: enable	R/W	0x0
28	DSPCPUREGCLKEN	DSP and CPU Communication Register Clock enable bit 0: disable 1: enable	R/W	0x0
27:0	-	Reserved	R/W	0x0

8.3.3.4 CMU_ADDACLK

CMU_ADDACLK Control register, offset = 0x0014

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	ADCCLKSRC	ADC_CLK Clock Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
11	ADCCLKPREDIV	ADC_CLK Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
10:8	ADCCLKDIV	ADC_CLK Clock Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0
7:5	-	Reserved	R	0x0
4	DACCLKSRC	DAC_CLK Clock Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
3	DACCLKPREDIV	DAC_CLK Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
2:0	DACCLKDIV	DAC_CLK Clock Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0

8.3.3.5 CMU_I2SCLK

CMU_I2SCLK Control register, offset = 0x0018

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R	0x0
29:28	I2SRDCLKSRC	I2S Sample Rate Detect Clock Source 00: AudioPLL0 01: AudioPLL1 10: reserved 11: HOSC	R/W	0x0
27	-	Reserved	R	0x0
26	I2SRX1MCLKEXTREV	I2SRX1_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
25:24	I2SRX1MCLKSRC	I2SRX1_MCLK Source 00: I2S1_CLK 01: I2STX_MCLK 10: I2SRX0_MCLK 11: I2SRX1_MCLK_EXT	R/W	0x0
23:21	-	Reserved	R	0x0
20	I2S1CLKSRC	I2S1_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
19	I2S1CLKPREDIV	I2S1_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
18:16	I2S1CLKDIV	I2S1_CLK Divisor 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0
15	-	Reserved	R	0x0
14	I2SRX0MCLKEXTREV	I2SRX0_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
13:12	I2SRX0MCLKSRC	I2SRX0_MCLK Source 00: ADC_CLK 01: I2STX_MCLK 10: I2S1_CLK 11: I2SRX0_MCLK_EXT	R/W	0x0
11	I2STXMCLKEXTREV	I2STX_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
10	I2STXMCLKDACSRC	I2STX_MCLK DAC Source 0: DAC_256fs_CLK 1: DAC_128fs_CLK	R/W	0x0
9:8	I2STXMCLKSRC	I2STX_MCLK Source 00: DAC_256fs_128fs_CLK (according to bit10) 01: ADC_CLK 10: I2S0_CLK 11: I2STX_MCLK_EXT	R/W	0x0
7:5	-	Reserved	R	0x0

4	I2S0CLKSRC	I2S0_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
3	I2S0CLKPREDIV	I2S0_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
2:0	I2S0CLKDIV	I2S0_CLK Divisor 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0

8.3.3.6 CMU_SPDIFCLK

CMU_SPDIFCLK Control register, offset = 0x001C

Bit (s)	Name	Description	Access	Reset
31:6	-	Reserved	R	0x0
5:4	SPDIFTXCLKSRC	SPDIFTX_CLK Source 00: DAC_128fs_CLK 01: I2S0_CLK 10: I2S0_CLK/2 11: Reserved	R/W	0x0
3:2	SPDIFRXCLKSRC	SPDIFRX_CLK Source 00: AudioPLL0 01: AudioPLL1 10: CorePLL 11: Reserved	R/W	0x0
1:0	SPDIFRXCLKDIV	SPDIFRX_CLK Divisor 0: /1 1: 2/3 2: /2 3: /3	R/W	0x0

8.3.3.7 CMU_SDCLK

CMU_SDCLK Control register, offset = 0x0020

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14	SD1CLKSRC	SD1 Card Controller Clock Source Select 0: HOSC 1: CORE_PLL	R/W	0x0
13	-	Reserved	R	0x0
12	SD1CLKPOSTDIV	SD1 Card Controller Clock Post-Divisor 0: /1 1: /128	R/W	0x0
11:8	SD1CLKDIV	SD1 Card Controller Clock Divisor 0000: /1 0001: /2	R/W	0x0

		0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16		
7	-	Reserved	R	0x0
6	SD0CLKSRC	SD0 Card Controller Clock Source Select 0: HOSC 1: CORE_PLL	R/W	0x0
5	-	Reserved	R	0x0
4	SD0CLKPOSTDIV	SD0 Card Controller Clock Post-Divisor 0: /1 1: /128	R/W	0x0
3:0	SD0CLKDIV	SD0 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16	R/W	0x0

8.3.3.8 CMU_SPICLK

CMU_SPICLK Control register, offset = 0x0024

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:22	SPI2CLKSRC	SPI2 Controller Clock Source 00: SCLK 01: HOSC 10: CORE_PLL 11: CK_64M	R/W	0x0
21	-	Reserved	R	0x0
20:16	SPI2CLKDIV	SPI2 Clock Divisor 0: /1	R/W	0x0

		1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5		
15:14	SPI1CLKSRC	SPI1 Controller Clock Source 00: SCLK 01: HOSC 10: CORE_PLL 11: CK_64M	R/W	0x0
13	-	Reserved	R	0x0
12:8	SPI1CLKDIV	SPI1 Clock Divisor 0: /1 1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5	R/W	0x0
7:6	SPI0CLKSRC	SPI0 Controller Clock Source 00: SCLK 01: HOSC 10: CORE_PLL 11: CK_64M	R/W	0x0
5	-	Reserved	R	0x0
4:0	SPI0CLKDIV	SPI0 Clock Divisor 0: /1 1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5	R/W	0x0

8.3.3.9 CMU_IRCLK

CMU_IRCLK Control register, offset = 0x0028

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	IRCLKSRC	IR Controller Clock Source 0: HOSC/120 1: CK200K	R/W	0x0

8.3.3.10 CMU_LCDCLK

CMU_LCDCLK Control register, offset = 0x002C

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	LCDCLKSRC	LCD Controller Clock Source 0: HOSC 1: CORE_PLL	R/W	0x0
3	-	Reserved	R	0x0
2:0	LCDCLKDIV	LCD Controller Clock Divisor 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: Reserved	R/W	0x0

8.3.3.11 CMU_SEGLCDCLK

CMU_SEGLCDCLK Control register, offset = 0x0030

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	SEGLCDCLKSRC	SEGLCD Controller Clock Source 0: CK32K 1: HOSC	R/W	0x0
3	SEGLCDCLKPOSTDIV	SEGLCD Controller Clock Post-Divisor 0: /1 1: /512	R/W	0x0
2:0	SEGLCDCLKDIV	SEGLCD Controller Clock Divisor 000: /1 001: /2 010: /3 011: /4 100: /5 101: /8 110: /16 111: /32	R/W	0x0

8.3.3.12 CMU_FMCLK

CMU_FMCLK Control register, offset = 0x0034

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1:0	FMCLKSEL	FM Clock Source 00: HOSC/2 01: HOSC 10: CORE_PLL/10 11: Reserved	R/W	0x0

8.3.3.13 CMU_PWM0CLK

CMU_PWM0CLK Control register, offset = 0x0038

Bit (s)	Name	Description	Access	Reset

31:9	-	Reserved	R	0x0
8:0	PWM0CLKDIV	PWM0 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.14 CMU_PWM1CLK

CMU_PWM1CLK Control register, offset = 0x003C

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8:0	PWM1CLKDIV	PWM1 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.15 CMU_PWM2CLK

CMU_PWM2CLK Control register, offset = 0x0040

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8:0	PWM2CLKDIV	PWM2 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.16 CMU_PWM3CLK

CMU_PWM3CLK Control register, offset = 0x0044

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0

8:0	PWM3CLKDIV	PWM3 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.17 CMU_PWM4CLK

CMU_PWM4CLK Control register, offset = 0x0048

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8:0	PWM4CLKDIV	PWM4 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.18 CMU_PWM5CLK

CMU_PWM5CLK Control register
Offset = 0x004C

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8:0	PWM5CLKDIV	PWM5 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.19 CMU_PWM6CLK

CMU_PWM6CLK Control register, offset = 0x0050

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0

8:0	PWM6CLKDIV	PWM6 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.20 CMU_PWM7CLK

CMU_PWM7CLK Control register, offset = 0x0054

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8:0	PWM7CLKDIV	PWM7 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.21 CMU_PWM8CLK

CMU_PWM8CLK Control register, offset = 0x0058

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8:0	PWM8CLKDIV	PWM8 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.22 CMU_LRADCCLK

CMU_LRADCCLK Control register, offset = 0x005C

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1:0	LRADCCLKSRC	LRADC Clock Source	R/W	0x0

		00: HOSC/94 255KHz 01: HOSC/47 511KHz 10: HOSC/23 1043KHz 11: CK3M/12 250KHz		

8.3.3.23 CMU_TIMERCLK

CMU_TIMERCLK Control register, offset = 0x0060

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:6	TIMER3CLKSRC	Timer3 clock Source 0: HOSC 1: HOSC/24 2: TIMER3_EXT 3: Reserved	R/W	0x0
5:4	TIMER2CLKSRC	Timer2 clock Source 0: HOSC 1: HOSC/24 2: TIMER2_EXT 3: Reserved	R/W	0x0
3:2	TIMER1CLKSRC	Timer1 clock Source 0: HOSC 1: HOSC/24 Others: Reserved	R/W	0x0
1:0	TIMER0CLKSRC	Timer0 clock Source 0: HOSC 1: HOSC/24 Others: Reserved	R/W	0x0

8.3.3.24 CMU_MEMCLKEN

CMU_MEMCLKEN Control register, offset = 0x0080

Bit (s)	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	SPI1DCACHERAMCLKEN	SPI1 cache RAM clock enable bit 0: disable 1: enable	R/W	0x1
27	URAM2CLKEN	URAM2 clock enable bit 0: disable 1: enable	R/W	0x1
26	-	Reserved	R	0x0
25	URAM1CLKEN	URAM1 clock enable bit 0: disable 1: enable	R/W	0x1
24	-	Reserved	R	0x0
23	URAM0CLKEN	URAM0 clock enable bit 0: disable 1: enable	R/W	0x1
22	SD1BUFCLKEN	SD1BUF0/1 clock enable bit 0: disable 1: enable	R/W	0x1
21	SD0BUFCLKEN	SD0BUF0/1 clock enable bit	R/W	0x1

		0: disable 1: enable		
20:19	-	Reserved	R/W	0x1
18	PCMRAM6CLKEN	PCMRAM6 clock enable bit 0: disable 1: enable	R/W	0x1
17	PCMRAM5CLKEN	PCMRAM5 clock enable bit 0: disable 1: enable	R/W	0x1
16	PCMRAM4CLKEN	PCMRAM4 clock enable bit 0: disable 1: enable	R/W	0x1
15	PCMRAM3CLKEN	PCMRAM3 clock enable bit 0: disable 1: enable	R/W	0x1
14	PCMRAM2CLKEN	PCMRAM2 clock enable bit 0: disable 1: enable	R/W	0x1
13	PCMRAM1CLKEN	PCMRAM1 clock enable bit 0: disable 1: enable	R/W	0x1
12	PCMRAM0CLKEN	PCMRAM0 clock enable bit 0: disable 1: enable	R/W	0x1
11	RAMFUNCLKEN	CPU Access RAM Function clock enable bit 0: disable 1: enable Once this bit is cleared, the clock for CPU accessing the above RAM such as PCMRAM0, URAM0, willed be gated, so that the related circuit will turned off to save more power	R/W	0x1
10:9	-	Reserved	R	0x0
8	RAM7CLKEN	RAM7 clock enable bit 0: disable 1: enable	R/W	0x1
7	RAM6CLKEN	RAM6 clock enable bit 0: disable 1: enable	R/W	0x1
6	RAM5CLKEN	RAM5 clock enable bit 0: disable 1: enable	R/W	0x1
5	RAM4CLKEN	RAM4 clock enable bit 0: disable 1: enable	R/W	0x1
4	RAM3CLKEN	RAM3 clock enable bit 0: disable 1: enable	R/W	0x1
3	RAM2CLKEN	RAM2 clock enable bit 0: disable 1: enable	R/W	0x1
2	RAM1CLKEN	RAM1 clock enable bit 0: disable	R/W	0x1

		1: enable		
1	RAM0CLKEN	RAM0 clock enable bit 0: disable 1: enable	R/W	0x1
0	ROMRAMCLKEN	ROM0~5 clock enable bit 0: disable 1: enable	R/W	0x1

8.3.3.25 CMU_MEMCLKSEL

CMU_MEMCLKSEL Control register, offset = 0x0088

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	R	0x0
27	URAM2CLKSEL	URAM1 clock selection bit 0: CPU_CLK 1: USBctl_URAM_CLK	R/W	0x0
26:25	URAM1CLKSEL	URAM1 clock selection bit 00: CPU_CLK 01: USBctl_URAM_CLK Others: Reserved	R/W	0x0
24:23	URAM0CLKSEL	URAM0 clock selection bit 00: CPU_CLK 01: USBctl_URAM_CLK Others: Reserved	R/W	0x0
22	SD1BUFCLKSEL	SD1BUF0/1 clock selection bit 0: CPU_CLK 1: CARD_MEM_CLK0/1	R/W	0x0
21	SD0BUFCLKSEL	SD0BUF0/1 clock selection bit 0: CPU_CLK 1: CARD_MEM_CLK0/1	R/W	0x0
20:0			R/W	0x0

8.3.3.26 CMU_DSP_WAIT

DSP Wait Control Register, offset＝0x00B0

Bit (s)	Name	Description	Access	Reset
31	DSPWEN	DSP Wait enable 0: disable 1: enable	R/W	0x0
30:4	-	Reserved	R	0x0
3	PSU_DSP_IDLE	DSP Status Indication 0: active status 1: idle status Note: after the PSU_DSP_IDLE becomes '1', the user can externally shut down the DSP root clock(gated by CMU).	R	0x0
2	PSU_DSP_COREIDLE	DSP Core Status Indication 0: active status 1: idle status Note: when the PSU_DSP_COREIDLE becomes '1', only the DSP Internal core clock is gated.	R	0x0

1	DSP_WAIT_AFTER_MPU	DSP Wait or not after DSP MPU Interrupt 0: no wait 1: wait	R/W	0x0
0	DSPDEWS	DSP external wait signal 0: no force wait 1: force wait	R/W	0x0

8.3.3.27 CMU_DSP_AUDIO_VOLCLK_SEL

DSP Audio Volume Control Register, offset = 0x00C0

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	R	0x0
2	PAVOL_CLK_SEL	Audio PA_VOLUME register clock select 0: SCLK 1: DSP_CLK	R/W	0x0
1	LCHVOL_CLK_SEL	Audio VOL_LCH register clock select 0: SCLK 1: DSP_CLK	R/W	0x0
0	RCHVOL_CLK_SEL	Audio VOL_RCH register clock select 0: SCLK 1: DSP_CLK	R/W	0x0

8.4 RTC

This part have individual modules: Calendar, Watch Dog (WD) and Timer0/1/2/3.

8.4.1 Features

- Calendar with a alarm IRQ which can wake up the PMU
- Four Timers with IRQS, while two as universal timer and two timer had get capture timer
- A watch dog which can be configured optional as IRQ or Reset

8.4.2 RTC Register List

Table 8-7 RTC block base address

Name	Physical Base Address	KSEG1 Base Address
RTC	0xC0120000	0xC0120000

Table 8-8 RTC Controller Registers

Offset	Register Name	Description
0x0000	RTC_CTL	RTC Control Register
0x0004	RTC_REGUPDATA	RTC Register update Register
0x0008	RTC_DHMSALM	RTC Day Hour Minute and Second Alarm Register
0x000C	RTC_DHMS	RTC Day Hour Minute and Second Register
0x0010	RTC_YMD	RTC Year Month Date Register
0x0014	RTC_ACCESS	RTC freely access Register
0x001C	WD_CTL	Watch Dog Control register

8.4.3 RTC Register Description

8.4.3.1 RTC_CTL

Calendar Control Register, offset=0x0000

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	LEAP	RTC Leap Year bit 0: not leap year 1: leap year	R	0x1
6:5	-	Reserved	R	0x0
4	CAL_EN	Calendar Enable 0: Disable 1: Enable	R/W	0x0
3:2	CALENDAR_CLK_SEL	00: select HCL division 01: Build-in OSC 11: Build-in OSC 10: select HOSC division	R/W	0x0
1	ALIE	Alarm IRQ Enable 0: Disable 1: Enable	R/W	0x0
0	ALIP	Alarm IRQ Pending bit, Writing '1' to this bit will clear it.	R/W	0x0

8.4.3.2 RTC_REGUPDATA

Offset=0x0004

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	UPDATA	The RTCVDD register update control Register When writing the RTC registers (except RTCREGUPDATE register or bit "ALIP"), the RTC registers' values are not update immediately. The value is written to backup registers (in VDD) first. Just when writing RTCREGUPDATE register "A596H", the RTCVDD registers' values are update with the backup registers' value. RTCREGUPDATE register is automatically reset as "5A69H" after the RTCVDD register is update. NOTE: Do not write RTCVDD registers when this register value is "A5C3E283H" NOTE: When writing the bit "alm_ip", it will take effect immediately. Do not need writing this register.	R/W	0x5A69

8.4.3.3 RTC_DHMSALM

Offset=0x0008

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0x0
20:16	HOUEAL	Alarm hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0

13:8	MINAL	Alarm minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0x0

8.4.3.4 RTC_DHMS

Offset=0x000C

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0x0
20:16	HOUR	Time hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0
13:8	MIN	Time minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SEC	Time second setting 00H – 3BH	R/W	0x0

8.4.3.5 RTC_YMD

Offset=0x0010

Bits	Name	Description	Access	Reset
31:23	-	Reserved	R	0x0
22:16	YEAR	Time year setting 00H – 63H	R/W	0x0
15:12	-	Reserved	R	0x0
11:8	MON	Time month setting 01H – 0CH	R/W	0x1
7:5	-	Reserved	R	0x0
4:0	DATE	Time day setting 01H – 1FH	R/W	0x1

8.4.3.6 RTC_ACCESS

Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	ACCESS	These bits can be accessed by CPU freely.	R/W	0x0

8.4.3.7 WD_CTL

Offset=0x001C

Bits	Name	Description	Access	Reset
31	EJTAG_F	CAN READ AND WRITE FREELY	R/W	0x0
30:7	-	reserved	R	0x0
6	IRQP	Watch dog IRQ pending bit; Writing ‘1’ to this bit will clear it.	R/W	0x0
5	SIGS	Watchdog Signal (IRQ or Reset) Select 0: Send Reset signal when watchdog overflow 1: Send IRQ signal when watchdog overflow	R/W	0x0

4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 0: Disable 1: Enable	R/W	0x0
3:1	CLKSEL	Watch Dog timer Clock Select, The watch dog's overflow value is 180. 000 1khz 176ms 001 512hz 352ms 010 256hz 703ms 011 128hz 1.4s 100 64hz 2.8s 101 32hz 5.6s 110 16hz 11.2s 111 10ms	R/W	0x0
0	CLR	Clear bit, Writing '1' to clear WD timer automatically.	R/W	0x0

8.4.4 TIMER Register List

Table 8-9 TIMER block base address

Name	Physical Base Address	KSEG1 Base Address
TIMER_REGISTER	0xC0120100	0xC0120100

Table 8-10 TIMER Controller Registers

Offset	Register Name	Description
0x00	T0_CTL	Timer0 Control register
0x04	T0_VAL	Timer0 Value
0x08	T0_CNT	Timer0 current counter register
0x20	T1_CTL	Timer1 Control register
0x24	T1_VAL	Timer1 Value
0x28	T1_CNT	Timer1 current counter register
0x40	T2_CTL	Timer2 Control register
0x44	T2_VAL	Timer2 Value
0x48	T2_CNT	Timer2 current counter register
0x4c	T2_CAP	Timer2 capture value register
0x60	T3_CTL	Timer3 Control register
0x64	T3_VAL	Timer3 Value
0x68	T3_CNT	Timer3 current counter register
0x6c	T3_CAP	Timer3 capture value register

8.4.5 TIMER Register Description

8.4.5.1 T0_CTL

Timer0 control register, offset=0x0000（VDD）

Bits	Name	Description	Access	Reset
31:6	-	reserved	R	0x0
5	EN	Timer 0 Enable 0: Disable 1: Enable	R/W	0x0

4:3	-	Reserved	R	0x0
2	RELO	Timer 0 Reload 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer0 IRQ Enable When this bit is enabled, Timer0_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	R/W	0x0
0	ZIPD	Timer0 IRQ Pending; Writing '1' to clear this bit.	R/W	0x0

8.4.5.2 T0_VAL

Timer0 value register, offset=0x0004（VDD）

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write Timer/Counter value register Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.3 T0_CNT

Timer0 current counter register, offset=0x0008（VDD）

Bits	Name	Description	Access	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

8.4.5.4 T1_CTL

Timer1 control register, offset=0x0020（VDD）

Bits	Name	Description	Access	Reset
31:6	-	reserved	R	0x0
5	EN	Timer 1 Enable 0: Disable 1: Enable	R/W	0x0
4:3	-	Reserved	R	0x0
2	RELO	Timer 1 Reload 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer1 IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	R/W	0x0
0	ZIPD	Timer1 IRQ Pending; Writing '1' to clear this bit.	R/W	0x0

8.4.5.5 T1_VAL

Timer1 value register, offset=0x0024（VDD）

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write current Timer1 value Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.6 T1_CNT

Timer1 current counter register, offset=0x0028（VDD）

Bits	Name	Description	Access	Reset
31:0	CNT	Read or write current Timer1 value	R	0x0

8.4.5.7 T2_CTL

Timer2 control register, offset=0x0040（VDD）

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	LEVEL	Current input pulse level Using for counter mode and capture mode	R	0x0
11	DIR	Timer Counting direction set 0: down 1: up	R/W	0x0
10:9	MODE_SEL	Timer mode select 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	R/W	0x0
8	CAPTURE_IP	Capture event IRQ pending; Writing ‘1’ to clear this bit. IRQ pending include counter mode and capture mode.	R/W	0x0
7:6	CAPTURE_SE	Capture signal edge select 00: falling edge 01: rising edge 1x: both falling edge and rising edge Edge select include counter mode and capture mode.	R/W	0x0
5	EN	Timer2 Enable 0: Disable 1: Enable	R/W	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer2 Reload enable 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer2 IRQ Enable When this bit is enabled, Timer2_IRQ sent out the IRQ signal until the pending bit was cleared. If DIR=’0’, T2_CNT compare with ZERO. If DIR=’1’, T2_CNT compare with T2_VAL. In input capture mode, every trigger edge would cause a capture IRQ, which pending reference to CAPTURE_IP.	R/W	0x0
0	ZIPD	Timer2 IRQ Pending; Writing ‘1’ to clear this bit. If timer overflow or zero occurs, this pending would be set to ‘1’.	R/W	0x0

8.4.5.8 T2_VAL

Timer2 value register, offset=0x0044（VDD）

Bits	Name	Description	Access	Reset

31:0	VAL	Set timer counter value If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an IRQ. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero. If timer setting in countdown mode, timer would countdown form Tx_VAL to zero. When the current timer counter equal to zero. it would cause an IRQ. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL. In counter mode, Tx_VAL[7:0] was used. Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.9 T2_CNT

Timer2 current counter register, offset=0x0048（VDD）

Bits	Name	Description	Access	Reset
31:0	CNT	Timer current value registers	R	0x0

8.4.5.10 T2_CAP

Timer2 current counter register, offset=0x004C（VDD）

Bits	Name	Description	Access	Reset
31:0	CAP	Capture value register Using in capture mode, when capture IRQ occurred, read this register to get counter of pulse width counter. If would be reload by every trigger edge set in Tx_CTL.	R	0x0

8.4.5.11 T3_CTL

Timer3 control register, offset=0x0060（VDD）

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	LEVEL	Current input pulse level Using for counter mode and capture mode	R	0x0
11	DIR	Timer Counting direction set 0: down 1: up	R/W	0x0
10:9	MODE_SEL	Timer mode select 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	R/W	0x0
8	CAPTURE_IP	Capture event IRQ pending; Writing ‘1’ to clear this bit. IRQ pending include counter mode and capture mode.	R/W	0x0
7:6	CAPTURE_SE	Capture signal edge select 00: falling edge 01: rising edge 1x: both falling edge and rising edge Edge select include counter mode and capture mode.	R/W	0x0
5	EN	Timer3 Enable 0: Disable 1: Enable	R/W	0x0

4:3	-	reserved	R	0x0
2	RELO	Timer3 Reload enable 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer IRQ Enable In timer/counter mode, When this bit is enabled, Timer3_Zero_IRQ sent out the IRQ signal until the pending bit was cleared. If DIR='0', T3_CNT compare with ZERO. If DIR='1', T3_CNT compare with T3_VAL. In input capture mode, every trigger edge would cause a capture IRQ, which pending reference to CAPTURE_IP.	R/W	0x0
0	ZIPD	Timer3 mode IRQ Pending; Writing '1' to clear this bit.	R/W	0x0

8.4.5.12 T3_VAL

Timer3 value register, offset=0x0064（VDD）

Bits	Name	Description	Access	Reset
31:0	VAL	Set timer counter value. If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an IRQ. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero. If timer setting in countdown mode, timer would countdown form Tx_VAL to zero. When the current timer counter equal to zero. it would cause an IRQ. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL. In counter mode, Tx_VAL[7:0] was used. Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.13 T3_CNT

Timer3 current counter register, offset=0x0068（VDD）

Bits	Name	Description	Access	Reset
31:0	CNT	Timer current value registers	R	0x0

8.4.5.14 T3_CAP

Timer3 current counter register, offset=0x006C（VDD）

Bits	Name	Description	Access	Reset
31:0	CAP	Capture value register Using in capture mode, when capture IRQ occurred, read this register to get counter of pulse width counter.	R	0x0

8.5 Exceptions and Interrupts Controller (INTC)

8.5.1 INTC Register List

Table 8-11 Interrupt Controller base address

Name	Physical Base Address	KSEG1 Base Address
Interrupt_Controller	0xC00B0000	0xC00B0000

Table 8-12 Interrupt Controller Registers

Offset	Register Name	Description
0x00000028	REQ_INT_OUT	Request interrupt output register
0x0000002C	REQ_IN	Request input register
0x00000030	REQ_IN_PD	Request input pending register
0x00000034	REQ_OUT	Request output register
0x00000040	CPU_WAKEUP_EN0	Interrupt Source Wakeup CPU enable register 0
0x00000044	CPU_WAKEUP_EN1	Interrupt Source Wakeup CPU enable register 1
0x00000050	CPU_DSP_INT_EN	CPU to DSP Interrupt enable register

8.5.2 INTC Register Description

8.5.2.1 REQ_INT_OUT

Request interrupt output register, offset = 0x00000028

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DSP_INT3	Send interrupt request to DSP	R/W	0x0

8.5.2.2 REQ_IN

Request input register, offset = 0x0000002C

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	OUT_USER4	It is a CPU interrupt controller sampled value of OUT_USER4 signal.	R	0x0
3	OUT_USER3	It is a CPU interrupt controller sampled value of OUT_USER3 signal.	R	0x0
2	OUT_USER2	It is a CPU interrupt controller sampled value of OUT_USER2 signal.	R	0x0
1	OUT_USER1	It is a CPU interrupt controller sampled value of OUT_USER1 signal.	R	0x0
0	OUT_USER0	It is a CPU interrupt controller sampled value of OUT_USER0 signal.	R	0x0

Note: 0: Interrupt is masked. 1: Interrupt is unmasked.

8.5.2.3 REQ_IN_PD

Request input pending register, offset = 0x00000030

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	OUT_USER4_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER4 signal. Writing '1' can clear this bit.	R/W	0x0
3	OUT_USER3_PD	0: interrupt pending is not detected.	R/W	0x0

		1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER3 signal. Writing '1' can clear this bit.		
2	OUT_USER2_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER2 signal. Writing '1' can clear this bit.	R/W	0x0
1	OUT_USER1_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER1 signal. Writing '1' can clear this bit.	R/W	0x0
0	OUT_USER0_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER0 signal. Writing '1' can clear this bit.	R/W	0x0

8.5.2.4 REQ_OUT

Request output register, offset = 0x00000034

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1	IN_USER1	Send information to DSP	R/W	0x0
0	IN_USER0	Send information DSP	R/W	0x0

8.5.2.5 CPU_WAKEUP_EN0

Interrupt Source Wakeup CPU enable register, offset = 0x00000040

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R	0x0
29	DMA7_WAKEUP_EN	DMA7 wake up source enable bit 0: disable 1: enable	R/W	0x0
28	DMA6_WAKEUP_EN	DMA6 wake up source enable bit 0: disable 1: enable	R/W	0x0
27	DMA5_WAKEUP_EN	DMA5 wake up source enable bit 0: disable 1: enable	R/W	0x0
26	DMA4_WAKEUP_EN	DMA4 wake up source enable bit 0: disable 1: enable	R/W	0x0
25	DMA3_WAKEUP_EN	DMA3 wake up source enable bit 0: disable 1: enable	R/W	0x0
24	DMA2_WAKEUP_EN	DMA2 wake up source enable bit 0: disable 1: enable	R/W	0x0
23	DMA1_WAKEUP_EN	DMA1 wake up source enable bit 0: disable 1: enable	R/W	0x0
22	DMA0_WAKEUP_EN	DMA0 wake up source enable bit 0: disable	R/W	0x0

		1: enable		
21	SD1_WAKEUP_EN	SD1 wake up source enable bit 0: disable 1: enable	R/W	0x0
20	SD0_WAKEUP_EN	SD0 wake up source enable bit 0: disable 1: enable	R/W	0x0
19	MPU_WAKEUP_EN	MPU wake up source enable bit 0: disable 1: enable	R/W	0x0
18	I2S1_SPDIF_RX_WAKEUP_EN	I2S1/SPDIF RX wake up source enable bit 0: disable 1: enable	R/W	0x0
17	ADC_I2S_RX_WAKEUP_EN	ADC/I2S RX wake up source enable bit 0: disable 1: enable	R/W	0x0
16	DAC_WAKEUP_EN	DAC wake up source enable bit 0: disable 1: enable	R/W	0x0
15	I2S_SPDIF_TX_WAKEUP_EN	I2S/SPDIF TX wake up source enable bit 0: disable 1: enable	R/W	0x0
14	UART1_WAKEUP_EN	UART1 wake up source enable bit 0: disable 1: enable	R/W	0x0
13	UART0_WAKEUP_EN	UART0 wake up source enable bit 0: disable 1: enable	R/W	0x0
12	I2C_WAKEUP_EN	I2C wake up source enable bit 0: disable 1: enable	R/W	0x0
11	USB_WAKEUP_EN	USB wake up source enable bit 0: disable 1: enable	R/W	0x0
10	SPI1_WAKEUP_EN	SPI1 wake up source enable bit 0: disable 1: enable	R/W	0x0
9	SPI0_WAKEUP_EN	SPI0 wake up source enable bit 0: disable 1: enable	R/W	0x0
8	RTC_WAKEUP_EN	RTC wake up source enable bit 0: disable 1: enable	R/W	0x0
7	GPIO_INT_WAKEUP_EN	GPIO wake up source enable bit 0: disable 1: enable	R/W	0x0
6	TIMER3_WAKEUP_EN	Timer3 wake up source enable bit 0: disable 1: enable	R/W	0x0
5	TIMER2_WAKEUP_EN	Timer2 wake up source enable bit 0: disable 1: enable	R/W	0x0
4	TIMER1_WAKEUP_E	Timer1 wake up source enable bit	R/W	0x0

	N	0: disable 1: enable		
3	TIMER0_WAKEUP_EN	Timer0 wake up source enable bit 0: disable 1: enable	R/W	0x0
2	WD_WAKEUP_EN	Watchdog wake up source enable bit 0: disable 1: enable	R/W	0x0
1	NFC_WAKEUP_EN	NFC wake up source enable bit 0: disable 1: enable	R/W	0x0
0	BT_BB_WAKEUP_EN	0: no interrupt to CPU 1: generate interrupt to CPU BT Baseband set this bit to generate interrupt to CPU. CPU will clear this bit when it handle this interrupt.	R/W	0x0

8.5.2.6 CPU_WAKEUP_EN1

Interrupt Source Wakeup CPU enable register, offset = 0x00000044

Bit (s)	Name	Description	Access	Reset
31	CPUCLK_LOWPOWER_EN	Whether CPU clock needs to be turned off after executing wait instruction 0: disable（do not turn off CPU clock） 1: enable（turn off CPU clock）	R/W	0x0
30:12	-	Reserved	R	0x0
11	SPI2_WAKEUP_EN	SPI2 wake up source enable bit 0: disable 1: enable	R/W	0x0
10:6	-	Reserved	R	0x0
5	IR_WAKEUP_EN	IRC wake up source enable bit 0: disable 1: enable	R/W	0x0
4	OUT_USER4_WAKEUP_EN	0: disable 1: enable	R/W	0x0
3	OUT_USER3_WAKEUP_EN	0: disable 1: enable	R/W	0x0
2	OUT_USER2_WAKEUP_EN	0: disable 1: enable	R/W	0x0
1	OUT_USER1_WAKEUP_EN	0: disable 1: enable	R/W	0x0
0	OUT_USER0_WAKEUP_EN	0: disable 1: enable	R/W	0x0

8.5.2.7 CPU_DSP_INT_EN

CPU to DSP Interrupt enable register, offset = 0x00000050

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	R	0x0
3	I2STXFIFOINT_EN	I2STX FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x0
2	DACFIFOINT_EN	DAC FIFO Interrupt Enable	R/W	0x1

		0: Disable 1: Enable		
1	I2SRX1FIFOINT_EN	I2SRX1 FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x0
0	ADCFIFOINT_EN	ADC FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x1

9 Storage

SD/MMC Card Controller Features

- ATS2837 integrates two SD/MMC controller: SD0 and SD1
- Fully compliant with MMC Specification 4.3
- Fully compliant with SD card Specification 2.0
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for input Signal, Output Delay Chain for output signal.
- Integrated Watchdog timeout Counter to report Exception happening.
- Integrated Pull up resistance (value 50Komh) for Data and CMD Line.
- Integrated CRC calculate and check circuit.
- Send continuous clock to support SDIO card.
- Support 3.1V CLK PAD voltage.
- Support 3.1V CMD PAD voltage.
- Support 3.1V DAT PAD voltage.
- Band Width: 25MByte/S
- Maximal SD interface Clock: 50MHz

10 Transfer and Communication

10.1 USB

10.1.1 Features

- Complies with the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports point-to-point communication with one full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports 3 IN endpoint and 3 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup for device mode.
- Support DMA transfer for endpoint in1 and out2

10.1.2 USB Register List

Table 10-1 USB Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
USB_CONTROLLER_REGISTERS	0xC0080000	0xC0080000

Table 10-2 USB Controller Registers

Offset	Register Name	Description
0x421	DPDMCTRL	DPDM control register
0x422	LINESTATUS	Line status register

10.1.3 USB Register Description

10.1.3.1 DPDMCTRL

DP DM control register
Offset = 0x421

Bit (s)	Name	Description	Access	Reset
7	-	Reserved	R	0B
6	PLUGIN	This bit Indicated the usb connection status when Linedeten is enable. 1: connect 0: disconnect	R	x
5	-	Reserved	R	0B
4	LSDETEN	Line status detect enable 1：enable 0：disable	R/W	1B
3	DMPUEN	500Kohm DM pull up resistor enable. 1：enable 0：disable	R/W	1B
2	DPPUEN	500Kohm DP pull up resistor enable. 1：enable 0：disable	R/W	1B
1	DMPDDIS	DM pull down disable. 1：disable 0：enable	R/W	1B
0	DPPDDIS	DP pull down disable. 1：disable 0：enable	R/W	1B

10.1.3.2 LINESTATUS

Line status register
Offset = 0x422

Bit (s)	Name	Description	Access	Reset
7:5	-	Reserved	R	0H
4:3	LINESTATE	USB linestate[1:0] Linestate0:DP Linestase1:DM	R	0B
2:1	-	Reserved	R	0H
0	OTGRESET	USB OTG reset. If AOTG is in reset state, this bit will be set, else it will be 0.	R/W	0B

10.2 I2C

10.2.1 Features

- Both master and slave functions supported

- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Only 7-bit address mode support
- 8 bit x16 TX FIFO and 8bit x16 RX FIFO
- Supports general call
- Pull-up resistors are required on both of the I2C signal lines as the I2C drivers are open drain. Typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal Pull-Up resistor.

10.2.2 Function Description

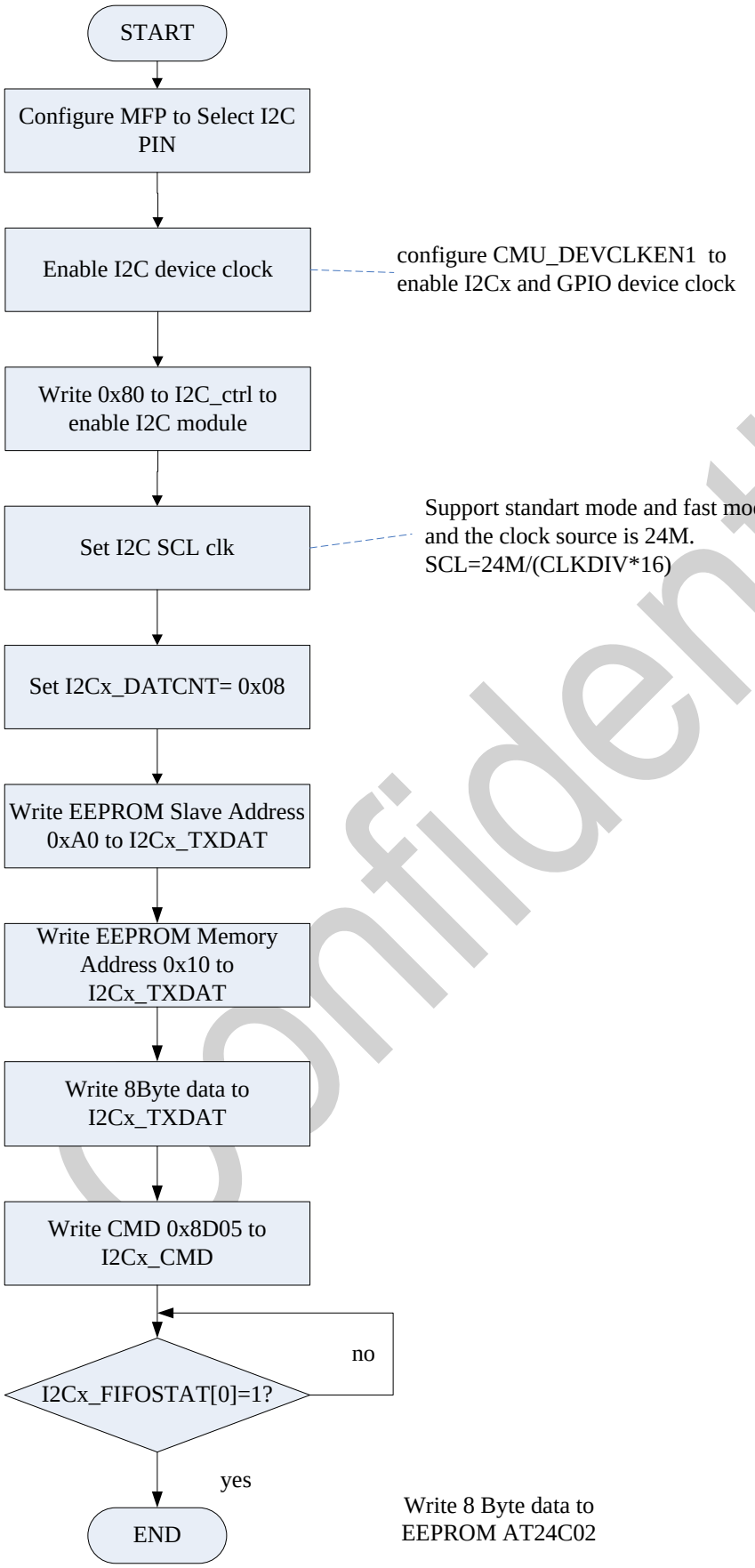
An Inter-IC bus，used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is I2C.
I2C provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available I2C devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. I2C is easy to use to link multiple devices together since it has a built-in addressing scheme.

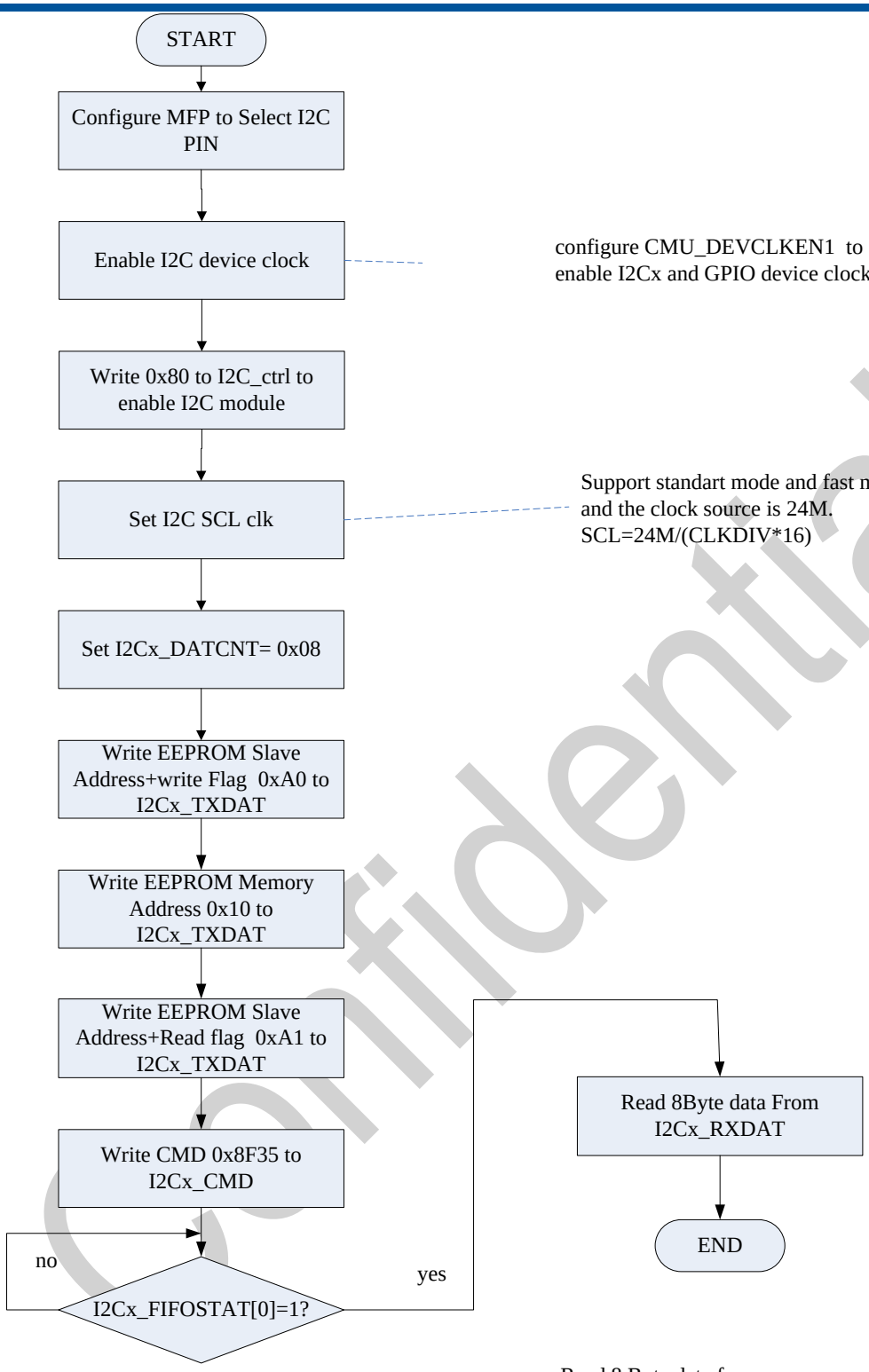
Note:

1. The I2C module is Slave mode when in IDLE status.
2. When write start command, the I2C module change from slave to master mode; and after a stop command change to slave mode.
3. Generate the IRQ while the bus statuses change.
   - transfer complete
   - detect normal stop bit (no bus error)

   If the address received don't match the content of I2C_address , don't generate the IRQ and reset to IDLE when detect the start bit followed the slave address in slave mode.
4. Release the bus by software after receive data or address.
5. In multi-master application, when miss the control of the bus, ignore the bus command before a stop command detected. After a stop command, the device start an arbitration procedure. The arbitration will end with one of the following:
   - The I2C module enters master mode (it won the arbitration)
   - The I2C module enters slave mode (it lost the arbitration or the other master addresses the I2C module)
   - The I2C module enter master-in-waiting mode, when the I2C module is waiting for the other master (that won control) to complete its transaction so that it can once again try to grain the arbitration of the bus.

10.2.3 Operation Manual





Read 8 Byte data from EEPROM AT24C02

10.2.4 I2C Register List

Table 10-3 TWI Register Block Base Address

Name	Physical Base Address	KSEG1 Base Address
TWI	0xC0130000	0xC0130000

Table 10-4 TWI Registers Offset Address

Offset	Register Name	Description
0x0000	I2C_CTL	I2C Control Register
0x0004	I2C_CLKDIV	I2C Clock Divider Register
0x0008	I2C_STAT	I2C Status Register
0x000C	I2C_ADDR	I2C Address Register
0x0010	I2C_TXDAT	I2C TX Data Register
0x0014	I2C_RXDAT	I2C RX Data Register
0x0018	I2C_CMD	I2C Command Register
0x001C	I2C_FIFOCTL	I2C FIFO Control Register
0x0020	I2C_FIFOSTAT	I2C FIFO Status Register
0x0024	I2C_DATCNT	I2C Data Transmit Counter Register
0x0028	I2C_RCNT	I2C Data Transmit Remain Counter Register

10.2.5 I2C Register Description

10.2.5.1 I2C_CTL

I2C Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10	IRQC	I2C IRQ Control 0: set when RX FIFO received 1 bytes data in IRQ mode 1: set when RX FIFO received 4 bytes data in IRQ mode	R/W	0x0
9:7	-	Reserved	R	0x0
6	IRQE	IRQ Enable. 0: Disable 1: Enable	R/W	0x0
5	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	R/W	0x0
4	-	Reserved	R/W	0x0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the I2C_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus.	R/W	0x0
1	RB	Release Bus. Writing '1' to this bit will release the bus.	R/W	0x0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	R/W	0x0

10.2.5.2 I2C_CLKDIV

I2C Control Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	CLKDIV	Clock Divider Factor (only for master mode). I2C clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=24M/(CLKDIV*16)	R/W	0x0

10.2.5.3 I2C_STAT

I2C Status Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10	SRGC	Slave receive general call 0: not receive a general call 1: receive a general call	R	0x0
9	SAMB	Slave address match bit 0: slave address not match 1: slave address match	R	0x0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0x0
7	TCB	Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing '1' to this bit will clear it.	R/W	0x0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0x0
5	STAD	Start detect bit, include restart. The bit is clear when the I2C module is disable or when the STOP condition is detected. Writing '1' to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	R/W	0x0
4	STPD	Stop detect bit The bit is clear when the I2C module is disable or when the START condition is detected. Writing '1' to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	R/W	0x0
3	-	Reserved	R	0x0
2	IRQP	IRQ Pending Bit. 1: IRQ 0: No IRQ Set condition: 1） transfer complete 2） detect normal stop bit (no bus error) 3） arbit fail Clear condition:	R/W	0x0

		Writing '1' to this bit will clear it.		
1	BEB	Bus error bit 0: No error occur 1: Bus error occur Write "1" to clear this bit. The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data.	R/W	0x0
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived	R	0x0

10.2.5.4 I2C_ADDR

I2C Address Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. I2C_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the I2C module is functioning as a master.	R/W	0x0
0	-	Reserved	R	0x0

10.2.5.5 I2C_TXDAT

I2C TX Data Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	DAT	The registers of Data or address to be transfer, or received to. I2CDAT contains the byte to be transmitted on the I2C-bus or a byte that has been received from the I2C-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave I2C device address while the LSB is the Read/Write bit. 8 level FIFO，8 x 8bit	W	0x0

10.2.5.6 I2C_RXDAT

I2C RX Data Register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	DAT	The Receive data Register 8 level FIFO，8 x 8bit	R	0x0

10.2.5.7 I2C_CMD

I2C Command Register
Offset=0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	SECL	Start to execute the command list 0: not execute 1: execute command	R/W	0x0
14:13	-	Reserved	R	0x0
12	WRS	Write or Read select 0: write 1: read This bit only used in Slave mode.	R/W	0x0
11	MSS	Master or slave mode select 0: slave mode 1: Master mode	R/W	0x0
10	SE	Stop enable 0: disable 1: enable	R/W	0x0
9	NS	NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data	R/W	0x0
8	DE	Data enable 0: disable 1: enable The counts of data transmitted depend on the I2Cx_CNT register.	R/W	0x0
7:5	SAS	Second address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address	R/W	0x0
4	RBE	Restart bit enable 0: not send restart bit 1: send restart bit	R/W	0x0
3:1	AS	Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address includes slave address and slave internal memory address.	R/W	0x0

0	SBE	Start bit enable 0: not send start bit 1: send start bit	R/W	0x0

10.2.5.8 I2C_FIFOCTL

I2C FIFO Control Register
Offset=0x001C

Bits	Name	Description	Access	Reset
31:3	-	Reserved	R	0x0
2	TFR	TX FIFO reset bit Writing '1' to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	R/W	0x0
1	RFR	RX FIFO reset bit Writing '1' to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	R/W	0x0
0	NIB	NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute，generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	R/W	0x0

10.2.5.9 I2C_FIFOSTAT

I2C FIFO Status Register
Offset=0x0020

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:12	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0x0
11:8	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0x0
7	-	Reserved	R	0x0
6	WRS	Write or read status bit when acts as slave， used only in FIFO mode 0: master write to slave 1: master read from slave	R	0x0
5	TFF	TX FIFO full bit 0: not full 1: full	R	0x0
4	TFE	TX FIFO empty bit 0: not empty 1: empty	R	0x1
3	RFF	RX FIFO full bit 0: not full 1: full	R	0x0
2	RFE	RX FIFO empty bit 0: not empty 1: empty	R	0x1
1	RNB	Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data	R/W	0x0

		Writing '1' to clear this bit		
0	CECB	Command Execute Complete bit 0: not complete 1: complete	R	0x1

10.2.5.10 I2C_DATCNT

I2C Data Transmit Counter Register
Offset=0x0024

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Data Transmit counter	R/W	0x0

10.2.5.11 I2C_RCNT

I2C Data Transmit Remain Counter Register
Offset=0x0028

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Remain counter Displays the number of data not currently transmitted.	R	0x0

10.3 IRC

10.3.1 Features

- Support IRC receive function, include hardware mode, hardware self-learning mode, hardware awake mode, software decode mode, software awake mode
- Hardware mode support IRC transfer function, which support TC9012/NEC/RC5/RC6 protocol
- Need to connect an IR receiver when use
- Support remote infrared awake function

10.3.2 IRC Register List

Table 10-5 IRC Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
IRC	0xC0150000	0xC0150000

Table 10-6 IRC Registers Offset Address

Offset	Register Name	Description
0x0000	IRC_RX_CTL	Infrared remote control hardware interface control register
0x0004	IRC_RX_STAT	Infrared remote control hardware status register
0x0008	IRC_RX_ICC0	Infrared remote control hardware customer code register0
0x000C	IRC_RX_ICC1	Infrared remote control hardware customer code register1
0x0010	IRC_RX_ICC2	Infrared remote control hardware customer code register2
0x0014	IRC_RX_ICC3	Infrared remote control hardware customer code register3
0x0018	IRC_RX_RCC	Infrared remote control hardware customer data code register
0x001C	IRC_RX_IWKDC0	Infrared remote control hardware customer wake up key code 0 register
0x0020	IRC_RX_IWKDC1	Infrared remote control hardware customer wake up key code 1 register

0x0024	IRC_RX_IWKDC2	Infrared remote control hardware customer wake up key code 2 register
0x0028	IRC_RX_IWKDC3	Infrared remote control hardware customer wake up key code 3 register
0x002C	IRC_RX_KDC	Infrared remote control hardware customer key code register
0x0100	IRC_CTL	Infrared remote control software control register
0x0104	IRC_STAT	Infrared remote control software status register
0x0108	IRC_DAT	Infrared remote control software data register
0x010C	IRC_SCT	Infrared remote control software sample counter register
0x0110	IRC_TC	Infrared remote control software sample tolerance control register
0x0114	IRC_DB	Infrared remote control debounce register

10.3.3 IRC Register Description

10.3.3.1 IRC_RX_CTL

Infrared remote control hardware interface control register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	MODE_SEL	IRC RX mode select 0: hardware mode 1: hardware self-learning mode	R/W	0x0
6	WFE	Wake up function enable bit 0: disable wake up function 1: enable wake up function	R/W	0x0
5	CCCD	customer code compare disable bit 0: enable customer code compare 1: disable customer code compare	R/W	0x0
4	KDCM	Key code compare disable bit 0: enable customer code compare 1: disable customer code compare	R/W	0x0
3	IRCE	IRC hardware enable 0: disable 1: enable	R/W	0x0
2	IIE	IRC hardware IRQ enable 0: disable 1: enable	R/W	0x0
1:0	ICMS	IRC coding mode select 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: RC6 code	R/W	0x0

10.3.3.2 IRC_RX_STAT

Infrared remote control hardware status register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	DET_PRO_PD	Detect Protocol ok pending bit 0: detect protocol not ok 1: detect protocol ok	R/W	0x0

		Writing ‘1’ to this bit will clear it		
14:13	PROTOCOL	Recognized Infrared Protocol 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: RC6 code	R	0x0
12	-	Reserved	R	0x0
11	LDCM	Leader data code mismatch pending bit. Writing ‘1’ to this bit will clear it, or auto clear if receive the correct leader data code the next time 0: leader data code match 1: leader data code mismatch	R/W	0x0
10:9	CCM	Customer code match 00: ICC0 customer match 01: ICC1 customer match 10: ICC2 customer match 11: ICC3 customer match	R	x
8	CCMP	Customer code mismatch pending 0: ICC customer match 1: ICC customer mismatch Writing ‘1’ to this bit will clear it	R/W	0x0
7:6	IWKCDM	Key code match 00: IWKDC0 key match 01: IWKDC1 key match 10: IWKDC2 key match 11: IWKDC3 key match	R	x
5	IWKCDMP	IRC wake up key code mismatch pending bit 0: IWKDC key match 1: IWKDC key mismatch Writing ‘1’ to this bit will clear it	R/W	0x0
4	RCD	Repeated code detected, Writing ‘1’ to this bit will clear it, otherwise don’t change 0: no repeat code 1: detect repeat code	R/W	0x0
3	WUP	Wake up pending bit 0: wake up pulse not generated 1: wake up pulse generated Writing ‘1’ to this bit will clear it	R/W	0x0
2	IIP	IRC IRQ pending bit. Writing ‘1’ to this bit will clear it 0: no IRQ pending 1: IRQ pending	R/W	0x0
1	-	Reserved	R	0x0
0	IREP	IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing ‘1’ to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	R/W	0x0

10.3.3.3 IRC_RX_ICC0

Infrared remote control hardware customer code register0
Offset=0x0008

Bits	Name	Description	Access	Reset

31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.4 IRC_RX_ICC1

Infrared remote control hardware customer code register1
Offset=0x000C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.5 IRC_RX_ICC2

Infrared remote control hardware customer code register2
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.6 IRC_RX_ICC3

Infrared remote control(IRC) hardware customer code register3
Offset=0x0014

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.7 IRC_RX_RCC

Infrared remote control hardware customer data code register
Offset=0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	CCRCV	customer code received In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R	0x0

10.3.3.8 IRC_RX_IWKDC0

Infrared remote control hardware customer wake up key code 0 register
Offset=0x001C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In RC6 mode, Bit 7:0 is the key code.	R/W	0x0

10.3.3.9 IRC_RX_IWKDC1

Infrared remote control hardware customer wake up key code 1 register
Offset=0x0020

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In RC6 mode, Bit 7:0 is the key code.	R/W	0x0

10.3.3.10 IRC_RX_IWKDC2

Infrared remote control hardware customer wake up key code 2 register
Offset=0x0024

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key	R/W	0x0

		anti-code In RC6 mode, Bit 7:0 is the key code.		

10.3.3.11 IRC_RX_IWKDC3

Infrared remote control hardware customer wake up key code 3 register
Offset=0x0028

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In RC6 mode, Bit 7:0 is the key code.	R/W	0x0

10.3.3.12 IRC_RX_KDC

Infrared remote control hardware customer key code register
Offset=0x002C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data In RC6 mode: Bit 7:0 is the Key data;	R	0x0

10.3.3.13 IRC_CTL

Infrared remote control software control register
Offset=0x0100

Bits	Name	Description	Access	Reset
31:12	-	Reserved	R	0x0
11:4	SRL	Soft Select level Received data in ram Set the number of wake-up codes compared with those in RAM when using software wake-up mode.	R/W	0x40
3	SWCS	IRC wake up memory clk select bit 0: Hclk 1: Irc_clk	R/W	0x0
2	SWFE	Soft wake up function enable bit 0: disable wake up function 1: enable software wake up function	R/W	0x0
1	SIRCE	IRC software enable 0:disable 1:enable	R/W	0x0
0	SIIE	IRC software IRQ enable 0: disable 1: enable	R/W	0x0

10.3.3.14 IRC_STAT

Infrared remote software status register
Offset=0x0104

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	BUSY	IRC busy bit 0: busy 1: not busy	R	0x0
11:4	SRLV	IRC level in ram bit Current data IRC Ram received	R	0x0
3	SWUP	Wake up pending bit 0: wake up pulse not generated 1: wake up pulse generated Writing '1' to this bit will clear it	R/W	0x0
2	SIIP	IRC IRQ pending bit, Writing '1' to this bit will clear it. 0: no IRQ pending 1: IRQ pending	R/W	0x0
1	SIREP	IRC receive error pending 0: receive ok 1: receive error Error occurs when IRC ram overflows. Writing '1' to this bit will clear this bit.	R/W	0x0
0	SRST	IRC ram reset bit Writing '1' to reset IRC ram, auto clear to 0 when IRC ram reset complete.	R/W	0x0

10.3.3.15 IRC_DAT

Infrared remote control software data register
Offset=0x0108

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IDAT	IRC data register	R/W	0x0

10.3.3.16 IRC_SCT

Infrared remote control software sample counter register
Offset=0x010C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Receive Counter configure	R/W	0x0

10.3.3.17 IRC_TC

Infrared remote control software sample tolerance control register
Offset=0x0110

Bits	Name	Description	Access	Reset
31:7	-	Reserved	R	0x0
6:0	STC	When comparing the received sample count value with the data	R/W	0x0

		configured in RAM, the register can be used to configure the positive and negative error range in units of 5us.		

10.3.3.18 IRC_DB

Infrared remote control debounce register
Offset=0x0114

Bits	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8	DBEN	Debouncer enable 0: disable 1: enable	R/W	0x0
7:0	DBC	Debouncer counter, 1 counter = 1/200KHz Default counter = 40(200us)	R/W	0x28

10.4 UART0 and UART1

10.4.1 Features

ATS2837 contains two UART interfaces: UART0 and UART1. UART0/1 has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Capable of speeds up to 6Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX Support DMA single mode
- Add UART RX DMA counter for valid data in RAM。
- RX Baud Rate tolerance≤±2%
- UART0 TXFIFO can be accessed by CPU and DSP

10.4.2 UART0 Register List

Table 10-7 UART0 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART0	0xC0190000	0xC0190000

Table 10-8 UART0 Registers Offset Address

Offset	Register Name	Description
0x0000	UART0_CTL	UART0 Control Register
0x0004	UART0_RXDAT	UART0 Receive FIFO Data Register
0x0008	UART0_TXDAT	UART0 Transmit FIFO Data Register
0x000C	UART0_STA	UART0 Status Register
0x0010	UART0_BR	UART0 BAUDRATE divider Register

10.4.3 UART0 Register Description

10.4.3.1 UART0_CTL

UART0 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	RXENABLE	UART RX enable 0:disable 1:normal	R/W	0x0
30	TXENABLE	UART TX enable 0:disable 1:normal	R/W	0x0
29	TX_FIFO_EN	UART TX FIFO enable: 0: Disable 1: Enable	R/W	0x0
28	RX_FIFO_EN	UART RX FIFO enable: 0: Disable 1: Enable	R/W	0x0
27:26	TX_FIFO_SEL	UART TX FIFO Input Select 00: From CPU 01: From DMA 1x: From DSP	R/W	0x0
25:24	RX_FIFO_SEL	UART RX FIFO Input Select 00: From CPU 01: From DMA 1x: Reserved	R/W	0x0
23:21	-	Reserved	R/W	0x0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	R/W	0x0
19	TXIE	UART0 TX IRQ Enable. 0: Disable 1: Enable	R/W	0x0
18	RXIE	UART0 RX IRQ Enable. 0: Disable 1: Enable	R/W	0x0
17	TXDE	UART0 TX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
16	RXDE	UART0 RX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
15	EN	UART0 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable	R/W	0x0
14	-	Reserved	R/W	0x0

13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: no request 1: request to send data	R/W	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	R/W	0x0
11:10	RDIC	UART0 RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00, 01 because at least 8 bytes necessary. In DMA single mode (normal DMA), DO set 00 for 1 Bytes transfer for each DRQ.	R/W	0x0
9:8	TDIC	UART0 TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01 because at least 8 bytes necessary.	R/W	0x0
7	CTSE	CTS Enable If this bit is 1, the transmitter checks CTS-before sending the next data byte. Note: this bit has no effect if autoflow enable bit is set. 0: do not checks CTS-before sending 1: checks CTS-before sending	R/W	0x0
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	R/W	0x0
3	-	Reserved	R/W	0x0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	R/W	0x0

		0: 1 stop bit 1: 2 stop bit		
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	R/W	0x0

10.4.3.2 UART0_RXDAT

UART0 Receive FIFO Data Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	x

10.4.3.3 UART0_TXDAT

UART0 Transmit FIFO Data Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TXDAT	Transmitted Data. The depth of FIFO is 8bit×16 levels	W	0x0

10.4.3.4 UART0_STA

UART0 Status Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23	PAER	Parity Status 0: Parity OK 1: Parity error Writing '1' to the bit will clear the bit. When parity error.	R/W	0x0
22	STER	Stop Status 0: Stop OK 1: Stop error Writing '1' to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART0 TX busy bit 0: not busy, TX FIFO is empty and all data be shift out 1: busy	R	0x0
20:16	TXFL	TX FIFO Level The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0x0
10	TFES	TX FIFO empty Status 0: no empty	R	0x1

		1: empty		
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0x0
8	RTSS	RTS Status The bit reflects the status of the external RTS- pin.	R	0x0
7	CTSS	CTS Status The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full 1: Full 0: No Full	R	0x0
5	RFEM	RX FIFO Empty 1: Empty 0: No Empty	R	0x1
4	RXST	Receive Status 0: receive OK 1: receive error Writing '1' to the bit will clear the bit. When receive bit detect error, which would be parity error or clock error.	R/W	0x0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the TX FIFO.	R/W	0x0
2	RXER	RX FIFO Error 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the RX FIFO.	R/W	0x0
1	TIP	TX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear the bit.	R/W	0x1
0	RIP	RX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear it.	R/W	0x0

10.4.3.5 UART0_BR

UART0 BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	Access	Reset
31:28	-	Reserved	R	0x0
27:16	TXBRDIV	UART0 TX BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28
15:12	-	Reserved	R	0x0
11:0	RXBRDIV	UART0 BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28

10.4.4 UART1 Register List

Table 10-9 UART1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART1	0xC01A0000	0xC01A0000

Table 10-10 UART1 Registers Offset Address

Offset	Register Name	Description
0x0000	UART1_CTL	UART1 Control Register
0x0004	UART1_RXDAT	UART1 Receive FIFO Data Register
0x0008	UART1_TXDAT	UART1 Transmit FIFO Data Register
0x000C	UART1_STA	UART1 Status Register
0x0010	UART1_BR	UART1 BAUDRATE divider Register

10.4.5 UART1 Register Description

10.4.5.1 UART1_CTL

UART1 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	RXENABLE	UART RX enable 0 : disable 1 : normal	R/W	0x0
30	TXENABLE	UART TX enable 0 : disable 1 : normal	R/W	0x0
29	TX_FIFO_EN	UART TX FIFO enable 0: Disable 1: Enable	R/W	0x0
28	RX_FIFO_EN	UART RX FIFO enable 0: Disable 1: Enable	R/W	0x0
27:26	TX_FIFO_SEL	UART TX FIFO Input Select 00: From CPU 01: From DMA 1x: From DSP	R/W	0x0
25:24	RX_FIFO_SEL	UART RX FIFO Input Select 00: From CPU 01: From DMA 1x: Reserved	R/W	0x0
23:21	-	Reserved	R/W	0x0
20	LBEN	Loop Back Enable Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	R/W	0x0
19	TXIE	UART1 TX IRQ Enable 0: Disable 1: Enable	R/W	0x0
18	RXIE	UART1 RX IRQ Enable	R/W	0x0

		0: Disable 1: Enable		
17	TXDE	UART1 TX DRQ Enable 0: Disable 1: Enable	R/W	0x0
16	RXDE	UART1 RX DRQ Enable 0: Disable 1: Enable	R/W	0x0
15	EN	UART1 Enable When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable	R/W	0x0
14	-	Reserved	R/W	0x0
13	RTSE	RTS Enable When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: no request 1: request to send data	R/W	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	R/W	0x0
11:10	RDIC	UART1 RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00, 01 because at least 8 bytes necessary. In DMA single mode (normal DMA), DO set 00 for 1 Bytes transfer for each DRQ.	R/W	0x0
9:8	TDIC	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01 because at least 8 bytes necessary.	R/W	0x0
7	CTSE	CTS Enable If this bit is 1, the transmitter checks CTS-before sending the next data byte. Note: this bit has no effect if autoflow enable bit is set. 0: do not checks CTS-before sending	R/W	0x0

		1: checks CTS-before sending		
6:4	PRS	Parity Select Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	R/W	0x0
3	-	Reserved	R/W	0x0
2	STPS	STOP Select If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0: 1 stop bit 1: 2 stop bit	R/W	0x0
1:0	DWLS	Data Width Length Select 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	R/W	0x0

10.4.5.2 UART1_RXDAT

UART1 Receive FIFO Data Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	RXDAT	Received Data The depth of FIFO is 8bit×16levels.	R	x

10.4.5.3 UART1_TXDAT

UART1 Transmit FIFO Data Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TXDAT	Transmitted Data The depth of FIFO is 8bit×16 levels	W	0x0

10.4.5.4 UART1_STA

UART1 Status Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23	PAER	Parity Status 0: Parity OK 1: Parity error. Writing '1' to the bit will clear the bit.	R/W	0x0

		When parity error.		
22	STER	Stop Status 0: Stop OK 1: Stop error. Writing '1' to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART1 TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0x0
20:16	TXFL	TX FIFO Level The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL	RX FIFO Level The field indicates the current RX FIFO level of valid data.	R	0x0
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	0x1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0x0
8	RTSS	RTS Status The bit reflects the status of the external RTS- pin.	R	0x0
7	CTSS	CTS Status The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full 1: Full 0: No Full	R	0x0
5	RFEM	RX FIFO Empty 1: Empty 0: No Empty	R	0x1
4	RXST	Receive Status 0: receive OK 1: receive error Writing '1' to the bit will clear the bit. When receive bit detect error, which would be parity error or clock error.	R/W	0x0
3	TFER	TX FIFO Error 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the TX FIFO.	R/W	0x0
2	RXER	RX FIFO Error 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the RX FIFO.	R/W	0x0
1	TIP	TX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear the bit.	R/W	0x1
0	RIP	RX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear it.	R/W	0x0

10.4.5.5 UART1_BR

UART1 BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	Access	Reset
31:28	-	Reserved	R	0x0
27:16	TXBRDIV	UART1 TX BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28
15:12	-	Reserved	R	0x0
11:0	RXBRDIV	UART1 BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28

10.5 SPI0

- SPI0 is for serial flash memory and support randomizer
- Internal 32KB CPU ICache for SPI0 serial flash

10.6 SPI2

10.6.1 Features

- Support SPI normal mode: mode 0/1/2/3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data
- Support 16 level delay chain, 1ns/step
- Support slave mode
- Support 100MHz spi_clk as highest speed

10.6.2 SPI2 Register List

Table 10-11 SPI2 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
SPI2	0xC01B0000	0xC01B0000

Table 10-12 SPI2 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI2_CTL	SPI2 Control Register
0x0004	SPI2_STA	SPI2 Status Register
0x0008	SPI2_TXDAT	SPI2 Transmit FIFO Data Register
0x000C	SPI2_RXDAT	SPI2 Receive FIFO Data Register
0x0010	SPI2_BC	SPI2 Byte Counter Register

10.6.3 SPI2 Register Description

10.6.3.1 SPI2_CTL

SPI2 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0x0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27	-	Reserved	R/W	0x0
26	RX_WRITE_SEL	SPI2 Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0
25	DMS	DMA transmit mode select 0: burst8 mode 1: single mode	R/W	0x0
24	TXCEB	TX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
23	RXCEB	RX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0x0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0x0
20	RILS	RX IRQ Level select 0: RX FIFO not empty, generate IRQ 1: RX FIFO at least 8 level data, generate IRQ Note: this bit have no effect when SPI_RIRQ_EN is disable, SPI2_CTL[8].	R/W	0x0
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode)	R/W	0x0

		0000: no delay 0001: delay 1 ns 0010: delay 2 ns 0011: delay 3 ns 0100: delay 4 ns 0101: delay 5 ns 0110: delay 6 ns 0111: delay 7 ns 1000: delay 8 ns 1001: delay 9 ns 1010: delay 10 ns 1011: delay 11 ns 1100: delay 12 ns 1101: delay 13 ns 1110: delay 14 ns 1111: delay 15 ns		
15:10	-	Reserved	R/W	0x0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO at least 8 level empty 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, this trigger of SPI RX IRQ controlled by SPI2_CTL[20]. 0: disable 1: enable	R/W	0x0
7	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 8 level empty; When DMA remain counter < 8, trigger DRQ until all data transfer completely 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 8 level full; When DMA remain counter < 8, trigger DRQ until all data received completely 0: disable 1: enable	R/W	0x0
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	0x1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

10.6.3.2 SPI2_STA

SPI2 Status Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:12	-	Reserved	R	0x0
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
10	-	Reserved	R	0x0
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
7	SPI_RXFU	SPI2 RX FIFO Full 0: not full 1: full	R	0x0
6	SPI_RXEM	SPI2 RX FIFO Empty 0: not empty 1: empty	R	0x1
5	SPI_TXFU	SPI2 TX FIFO Full 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI2 TX FIFO Empty 0: not empty 1: empty	R	0x1
3	SPI_TIRQ_PD	SPI2 TX IRQ Pending, Writing '1' to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	R/W	0x0
2	SPI_RIRQ_PD	SPI2 RX IRQ Pending, Writing '1' to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0x0
1	-	Reserved	R	x
0	SPI_BUSY	SPI2 master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0

10.6.3.3 SPI2_TXDAT

SPI2 Transmit FIFO Data Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:0	SPI2_TXDAT	SPI2 TX FIFO, 32bitx16 levels When SPI2_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI2_CTL[30] select 32bit width, bit[31:0] is valid.	W	0x0

		Be read as zero.		

10.6.3.4 SPI2_RXDAT

SPI2 Receive FIFO Data Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:0	SPI2_RXDAT	SPI RX FIFO, When SPI2_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI2_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx16 levels	R	0x0

10.6.3.5 SPI2_BC

SPI2 Bytes Count Register, this register is used for setting SPI2 bytes counter bits in the SPI read mode only.
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be received, only use in master mode	R	0x0
15:0	SPI2_BC	Bytes Counter [15:0]	R/W	0x0

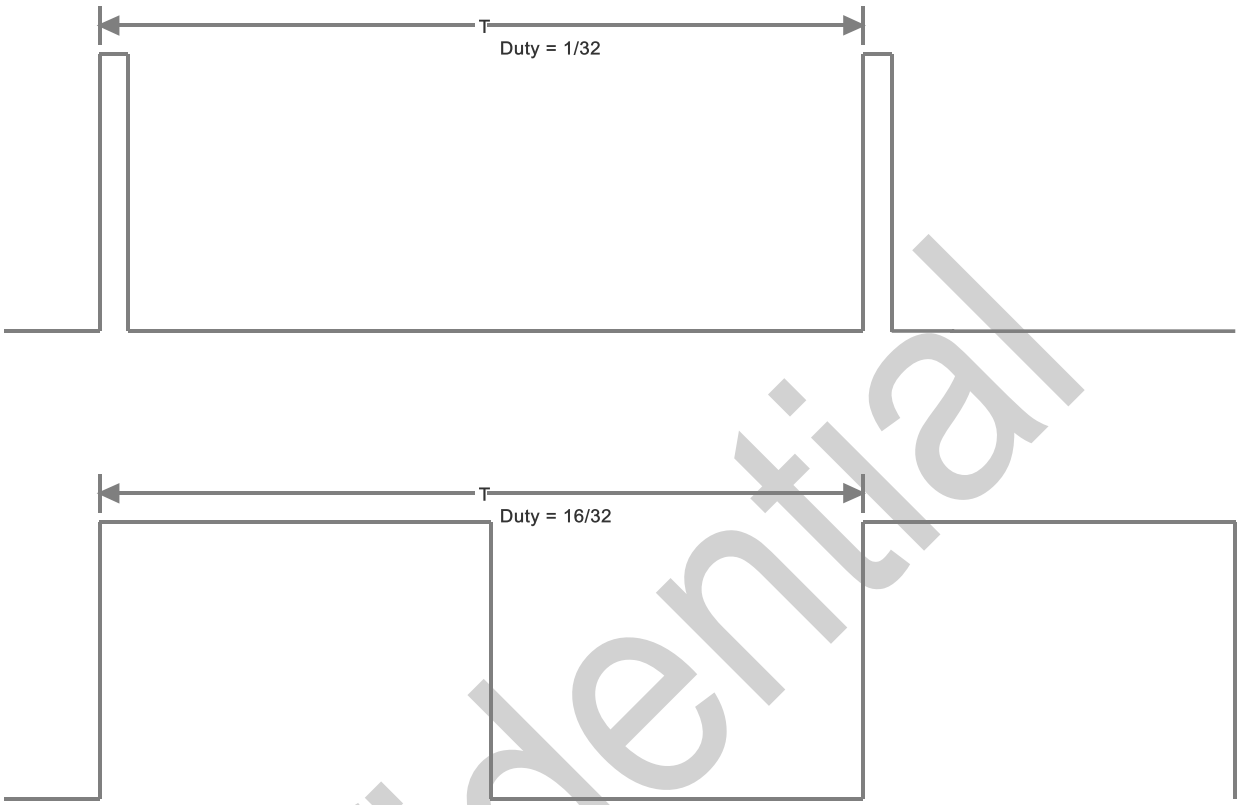
10.7 PWM

10.7.1 Features

- Independent of 9 PWM
- The frequency of PWM comes from the division of 32KHz
- Support normal mode and breath mode
  - Normal mode can output 256 kinds of duty
  - Breath mode supports breathing lights with various flicker frequencies

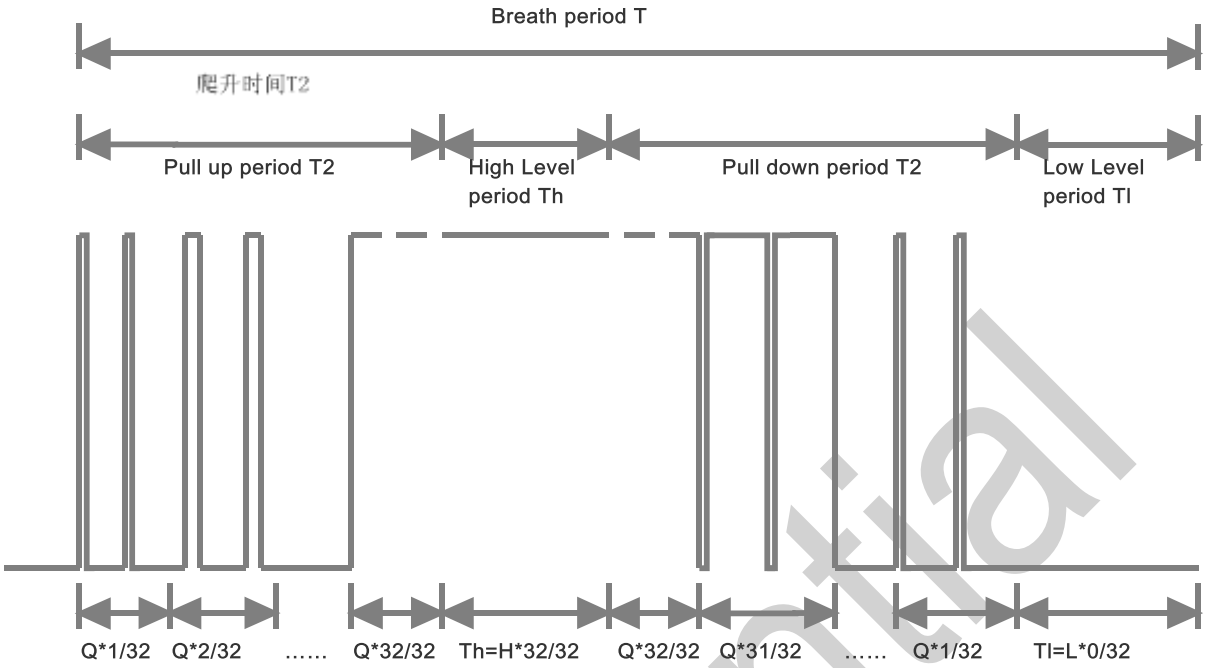
10.7.2 Module Description

10.7.2.1 Normal Mode Timing



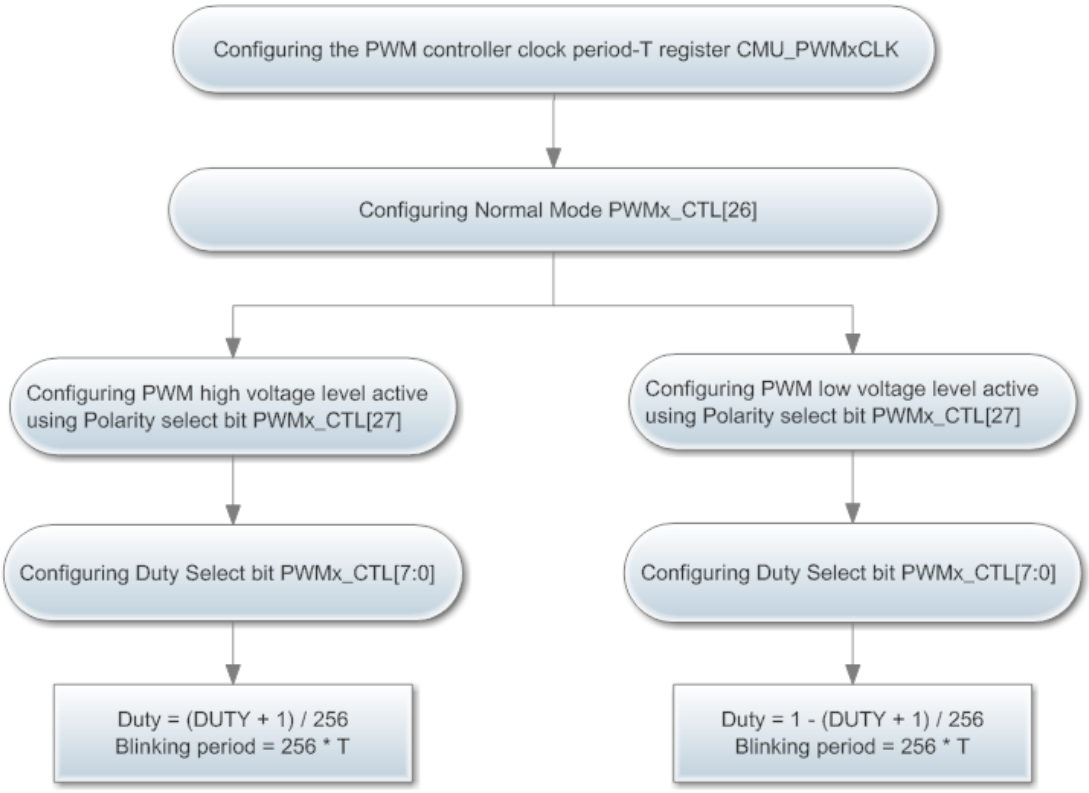
PWM can be used as backlights enable signal of LCD. The brightness of the backlights is decided by the duty cycle of PWM.

10.7.2.2 Breath Mode Timing



The breath mode of PWM can be used for driver of breathing light. For example, if PWM CLK from CMU is f=1/t and we need the time of pull up or pull down to be T2=Q*32*32t=0.5s, and the time of high level Th=H*32T=0.5s and the time of low level Tl=L*32t=2s, when we set Q=2, the f should be 4096 and H is 64, L is 256.

10.7.3 Operation Manual



For example, if Duty =50% and the Blinking period is two seconds, T=2/256, the Frequency of the PWM controller clock is 1/T=128Hz, So CMU_PWMxCLK can be configured as 0xF9, PWMx_CTL can be configured as 0x0800007F.

10.7.4 PWM Register List

Table 10-13 PWM Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
PWM	0xC0180000	0xC0180000

Table 10-14 PWM Registers Offset Address

Offset	Register Name	Description
0x0000	PWM0_CTL	PWM0 Output Control
0x0004	PWM1_CTL	PWM1 Output Control
0x0008	PWM2_CTL	PWM2 Output Control
0x000C	PWM3_CTL	PWM3 Output Control
0x0010	PWM4_CTL	PWM4 Output Control
0x0014	PWM5_CTL	PWM5 Output Control
0x0018	PWM6_CTL	PWM6 Output Control
0x001C	PWM7_CTL	PWM7 Output Control
0x0020	PWM8_CTL	PWM8 Output Control

10.7.5 PWM Register Description

10.7.5.1 PWM0_CTL

PWM0 Output Control Register
Offset=0x00

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256	R/W	0x0

		Only Active in Normal Mode		

10.7.5.2 PWM1_CTL

PWM1 Output Control Register
Offset=0x04

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.3 PWM2_CTL

PWM2 Output Control Register
Offset=0x08

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t	R/W	0x0

		t is the period of CMU_PWM		
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.4 PWM3_CTL

PWM3 Output Control Register
Offset=0x0C

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.5 PWM4_CTL

PWM4 Output Control Register
Offset=0x10

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode	R/W	0x0

		1: Breath Mode		
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.6 PWM5_CTL

PWM5 Output Control Register
Offset=0x14

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.7 PWM6_CTL

PWM6 Output Control Register
Offset=0x18

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0

26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.8 PWM7_CTL

PWM7 Output Control Register
Offset=0x1C

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.9 PWM8_CTL

PWM8 Output Control Register
Offset=0x20

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable	R/W	0x0

		0: Disable 1: Enable		
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select: 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

11 Audio Interface

11.1 DAC

- Build in stereo 24 bit input sigma-delta DAC, SNR>98dB, SNR (A-WEIGHTING)>101dB, THD<-87dB
- DAC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48/96kHz
- Support digital volume of 256 steps with zero cross detection
- Build in stereo 20mW PA (Power Amplifier) for headphone. PA output supports traditional mode and direct drive mode(for earphone)
- An anti-pop circuit for suppressing noise of PA when enable and disable
- Support differential audio output for speaker PA

11.2 ADC

- Build in stereo 24 bit input sigma-delta ADCs, SNR>96dB, SNR (A-WEIGHTING)>98dB, THD<-85dB
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48/96kHz
- A digital high-pass filter can be used to remove dc offsets when ADC use
- Supports single-ended input analog microphones and full difference input microphone
- Supports Digital microphones

11.3 I2S

11.3.1 Features

- Support 3 I2S module: I2SRX0, I2SRX1, and I2STX
- I2SRX0 and I2SRX1 support I2S receiver(RX) with master mode and slave mode
- I2STX support I2S transmission(TX) with master mode and slave mode
- I2S support sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/96k/192kHz

- I2S support 3 transmission modes: left-justified format, right-justified format, and I2S format

11.3.2 I2SRX0 Register List

Table 11-1 I2SRX0 Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
I2SRX0_Register	0xC0052100	0xC0052100

Table 11-2 I2SRX0 Controller Registers

Offset	Register Name	Description
0x0000	I2SRX0_CTL	I2SRX0 Control Register
0x0010	I2SRX0_SRDCTL	I2SRX0 sample rate detect control register
0x0014	I2SRX0_SRDSTA	I2SRX0 sample rate detect status register

11.3.3 I2SRX0 Register Description

11.3.3.1 I2SRX0_CTL

I2SRX0 Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	RX0_RX1_5W_EN	I2S RX0 and I2S RX1 in 5w mode 0 : disable 1 : enable RX1 would share the clock with RX0, when this bit set to '1', and should not set RX1_EN in this case. Master mode used only.	R/W	0x0
11:8	-	Reserved	R	0x0
7	RXMODE	I2SRX0 mode select 0: I2S Master mode 1: I2S Slave mode	R/W	0x0
6	RX_SMCLK	MCLK source when in slave mode 0: from internal module 1: from extern input by pad of MCLK Note: if there was no MCLK supply by master, this bit should be set to '1'.	R/W	0x1
5:4	RXWIDTH	Effective width 00: datas are 16 bit effective 01: datas are 20 bit effective 10: datas are 24 bit effective 11: reserved	R/W	0x2
3	RXBCLKSET	Rate of BCLK with LRCLK 0x0: 64*FS 0x1: 32*FS	R/W	0x0
2:1	RXMODELSEL	I2S transfer format select 00: i2s model 01: left-justified 10: right-justified 11: reserved	R/W	0x0

		Note: in case of 32FS, Lj format should not be configured.		
0	RXEN	I2SRX0 Enable 0: Disable 1: Enable	R/W	0x0

11.3.3.2 I2SRX0_SRDCTL

I2SRX0 sample rate detect control register
Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the RX input as 0. 1: mute 0: not mute Mute would continue until SRC_PD was clear.	R/W	0x0
11:9	-	reserved	R/W	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0: disable 1: enable If sample rate detection module timeout, or detected sample rate changing or detected channel width changing, if would cause interrupt.	R/W	0x0
7:6	-	reserved	R/W	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0: 2 LRCLK cycle 1: 4 LRCLK cycle Other: reserved	R/W	0x0
3:1	SRD_TH	These bits represent the sensitivity of sampling rate detection. SRC_PD interrupt will be triggered when the difference between CNT and previous detection results exceeds the preset value. 0: 8 1: 16 … 6: 56 7: 64 Value=(SRD_TH+1)*8	R/W	0x0
0	SRD_EN	Slave mode sample rate detect enable: 0: disable 1: enable	R/W	0x0

11.3.3.3 I2SRX0_SRDSTA

I2SRX0 sample rate detect status register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0x0

24:12	CNT	CNT of LRCLK which sampling by audiopll. CNT= Freq_Audiopll / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	sample rate detect result timeout interrupt pending 0: no irq 1: irq Write '1' to clean this bit. CNT overflow (0x9c00) would cause this irq.	R/W	0x0
10	SRC_PD	sample rate detect result sample rate change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
9	-	Reserved	R	0x0
8	CHW_PD	sample rate detect result channel width change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
7:2	-	Reserved	R	0x0
1:0	WL	Channel word length(the rate of BCLK to LRCLK)： 00: 16bit (32 rate) 01: 32bit (64 rate) 1x: others	R	0x0

11.3.4 I2SRX1 Register List

Table 11-3 I2SRX1 Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
I2SRX1_Register	0xC0052200	0xC0052200

Table 11-4 I2SRX1 Controller Registers

Offset	Register Name	Description
0x0000	I2SRX1_CTL	I2SRX1 Control Register
0x0004	I2SRX1_FIFOCTL	I2SRX1 FIFO control register
0x0008	I2SRX1_FIFOSTAT	I2SRX1 FIFO status register
0x000C	I2SRX1_DAT	I2SRX1 FIFO data register
0x0010	I2SRX1_SRDCTL	I2SRX1 sample rate detect control register
0x0014	I2SRX1_SRDSTA	I2SRX1 sample rate detect status register

11.3.5 I2SRX1 Register Description

11.3.5.1 I2SRX1_CTL

I2SRX1 Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	RXMODE	I2SRX1 mode select	R/W	0x0

		0: I2S Master mode 1: I2S Slave mode		
6	RX_SMCLK	MCLK source when in slave mode 0: from internal module 1: from extern input by pad of MCLK I2S slave mode used only. Note: if there was no MCLK supply by master, this bit should be set to '1'.	R/W	0x1
5:4	RXWIDTH	Effective width 00: datas are 16 bit effective 01: datas are 20 bit effective 10: datas are 24 bit effective 11: reserved	R/W	0x2
3	RXBCLKSET	Rate of BCLK with LRCLK 0x0:64*FS 0x1:32*FS	R/W	0x0
2:1	RXMODELSEL	I2S transfer format select 0 0:I2S model 01: left-justified 10: right-justified 11: reserved Note: in case of 32FS, Lj format should not be configured.	R/W	0x0
0	RXEN	I2SRX1 Enable 0: Disable 1: Enable	R/W	0x0

11.3.5.2 I2SRX1_FIFOCTL

I2SRX1 FIFO Control Register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	RX1FIFO_DMAWIDTH	I2SRX1FIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . I2SRX1FIFO doesn't support 8bit and 64bit DMA data width.	R/W	0x0
6	-	Reserved	R	0x0
5:4	RXFOS	RX FIFO Output Select 0x00: CPU 0x01: DMA 0x02: Reserved 0x03: DSP	R/W	0x0
3	RXFIS	RX FIFO Input Select 0x0: I2SRX1 0x1: SPDIFRX	R/W	0x0
2	RXFFIE	RX FIFO Half Full IRQ Enable 0: Disable 1: Enable	R/W	0x0

1	RXFFDE	RX FIFO Half Full DRQ Enable 0x0: Disable 0x1: Enable	R/W	0x0
0	RXFRT	RX FIFO Reset 0x0: Reset FIFO 0x1: Enable FIFO	R/W	0x0

11.3.5.3 I2SRX1_FIFOSTAT

RX1 FIFO State Register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	RXFEF	RX FIFO Empty Flag 0x0: Not Empty 0x1: Empty	R	0x1
6	RXFIP	RX FIFO Half Full IRQ Pending Bit 0x0: No IRQ 0x1: IRQ Writing '1' to the bit is clear it.	R/W	0x0
5	-	Reserved	R	0x0
4:0	RXFS	RX FIFO Status These 5 bits shows how many sample pairs fifo filled. For example, when read as 6, means DSP can read 12 samples from fifo. If no I2SRX1_CLK, register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0

11.3.5.4 I2SRX1_DAT

I2S1 RX FIFO DAT
Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:8	RXDAT	RX Data FIFO is 24bit x 32 levels.	R	x
7:0	-	Reserved	R	0x0

11.3.5.5 I2SRX1_SRDCTL

I2SRX1 sample rate detect control register
Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the RX input as 0. 1:mute 0:not mute	R/W	0x0

11:9	-	Reserved	R/W	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0:disable 1:enable	R/W	0x0
7:6	-	reserved	R/W	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0:2 LRCLK cycle 1:4 LRCLK cycle Other: reserved	R/W	0x0
3:1	SRD_TH	These bits represent the sensitivity of sampling rate detection. SRC_PD interrupt will be triggered when the difference between CNT and previous detection results exceeds the preset value. 0: 8 1: 16 … 6: 56 7: 64 Value=(SRD_TH+1)*8	R/W	0x0
0	SRD_EN	Slave mode sample rate detect enable 0: disable 1: enable	R/W	0x0

11.3.5.6 I2SRX1_SRDSTA

I2SRX1 sample rate detect status register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by audiopll. CNT= **Freq_Audiopll /** LRCLK**.** It would clear when module was enabling at first time.	R	0x0
11	TO_PD	Sample rate detect result timeout interrupt pending 0: no irq 1: irq Write ‘1’ to clean this bit. CNT overflow (0x9c00) would cause this irq.	R/W	0x0
10	SRC_PD	Sample rate detect result sample rate change interrupt pending 0: no irq 1: irq Write ‘1’ to clean this bit.	R/W	0x0
9	-	Reserved	R	0x0
8	CHW_PD	Sample rate detect result channel width change interrupt pending 0: no irq 1: irq Write ‘1’ to clean this bit.	R/W	0x0

7:2	-	Reserved	R	0x0
1:0	WL	Channel word length(the rate of BCLK to LRCLK)： 00: 16bit(32 rate) 01: 32bit (64 rate) 1x: others	R	0x0

11.3.6 I2STX Register List

Table 11-5 I2STX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
I2STX_Register	0xC0052000	0xC0052000

Table 11-6 I2STX Controller Registers

Offset	Register Name	Description
0x0000	I2STX_CTL	I2STX Control Register
0x0004	I2STX_FIFOCTL	I2STX FIFO control register
0x0008	I2STX_FIFOSTAT	I2STX FIFO status register
0x000C	I2STX_DAT	I2STX FIFO data register
0x0010	I2STX_SRDCTL	I2STX sample rate detect control register
0x0014	I2STX_SRDSTA	I2STX sample rate detect status register
0x0020	I2STX_FIFO_CNT	I2STX FIFO Sample Counter register

11.3.7 I2STX Register Description

11.3.7.1 I2STX_CTL

I2STX Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:17	-	Reserved	R	0x0
16	MULT_DEVICE	Multi device simultaneous startup selection 0x0: Disable 0x1: I2STX with SPDIFTX	R/W	0x0
15:14	-	Reserved	R	0x0
13	I2SRX1_5W_EN	I2STX & I2SRX1 5wire enable 0:disable 1:enable RX1 would share the clock with TX, when this bit set to '1', and should not set RX1_EN in this case. Master mode used only.	R/W	0x0
12	I2SRX0_5W_EN	I2STX & I2SRX0 5wire enable 0:disable 1:enable RX0 would share the clock with TX, when this bit set to '1', and should not set RX0_EN in this case. Master mode used only.	R/W	0x0
11:10	-	Reserved	R	0x0
9	LPEN1	I2STX and I2SRX1 loopback enable 0：disable 1：enable	R/W	0x0

		When enable, I2STX send CLOCK and data to I2SRX1		
8	LPEN0	I2STX and I2SRX0 loopback enable 0 : disable 1 : enable When enable, I2STX send CLOCK and data to I2SRX0	R/W	0x0
7	TXMODE	I2STX mode select 0: Master mode 1: Slave mode	R/W	0x0
6	TX_SMCLK	MCLK(256FS) source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only. Note: if there was no mclk supply by master, this bit should be set to '1'.	R/W	0x1
5:4	TXWIDTH	Effective width 00:datas are 16 bit effective 01: datas are 20 bit effective 10: datas are 24 bit effective 11: reserved	R/W	0x2
3	TXBCLKSET	Rate of BCLK with LRCLK 0x0:64*FS 0x1:32*FS	R/W	0x0
2:1	TXMODELSEL	I2S transfer format select 00 : I2S format 01 : left-justified format 10 : right-justified format 11 : reserved Note: in case of 32FS, Lj format should not be configured.	R/W	0x0
0	TXEN	I2STX Enable 0: Disable 1: Enable	R/W	0x0

11.3.7.2 I2STX_FIFOCTL

I2STX FIFO control register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	TXFIFO_DMAWIDTH	I2STXFIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . I2STXFIFO doesn't to support 8bit and 64bit DMA data width.	R/W	0x0
6	ASRC_SEL	I2STX FIFO Input select when FIFO_IN_SEL select ASRC OUT 0x0 : ASRC_OUT0 0x1 : ASRC_OUT1 Only use in FIFO_IN_SEL=2b'10	R/W	0x0

5:4	FIFO_IN_SEL	I2STX_FIFO Input Select 0x00: CPU 0x01: DMA 0x02: ASRC OUT 0x03: DSP	R/W	0x0
3	FIFO_SEL	I2STX&SPDIFTX module FIFO select 0 : DAC FIFO0/1 1 : I2STX FIFO	R/W	0x0
2	FIFO_IEN	I2STX_FIFO Half Empty IRQ Enable 0x0: Disable 0x1: Enable	R/W	0x0
1	FIFO_DEN	I2STX_FIFO Half Empty DRQ Enable 0x0: Disable 0x1: Enable	R/W	0x0
0	FIFO_RST	I2STX_FIFO Reset 0x0: Reset FIFO 0x1: Enable FIFO	R/W	0x0

11.3.7.3 I2STX_FIFOSTAT

I2STX FIFO status register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	IP	I2STX_FIFO Half Empty IRQ Pending Bit 0x0: No IRQ 0x1: IRQ Writing '1' to the bit is clear it.	R/W	0x0
6	TFFU	I2STX_FIFO Full Flag 0x0: Not Full 0x1: Full	R	0x0
5	-	Reserved	R	0x0
4:0	STA	I2STX_FIFO Status Indicate how many fifo level can be written into fifo. If no I2STX_CLK register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0

11.3.7.4 I2STX_DAT

I2STX FIFO data register
Offset = 0x0c

Bit (s)	Name	Description	Access	Reset
31:8	DAT	I2STX_FIFO Data FIFO is 24bit x 32 levels.	W	x
7:0	-	Reserved	R	0x0

11.3.7.5 I2STX_SRDCTL

I2STX sample rate detect control register
Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the TX output as 0. 1: mute 0: not mute	R/W	0x0
11:9	-	Reserved	R/W	0x0
8	SRD_IE	Sample rate detect result change interrupt enable 0: disable 1: enable If sample rate detection module timeout, or detected sample rate changing or detected channel width changing, if would cause interrupt.	R/W	0x0
7:6	-	reserved	R/W	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0: 2 LRCLK cycle 1: 4 LRCLK cycle Other: reserved	R/W	0x0
3:1	SRD_TH	These bits represent the sensitivity of sampling rate detection. SRC_PD interrupt will be triggered when the difference between CNT and previous detection results exceeds the preset value. 0: 8 1: 16 … 6: 56 7: 64 Value=(SRD_TH+1)*8	R/W	0x0
0	SRD_EN	Slave mode sample rate detect enable 0: disable 1: enable	R/W	0x0

11.3.7.6 I2STX_RDSTA

I2STX sample rate detect status register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by audiopll. CNT= Freq_Audiopll / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	Sample rate detect result timeout interrupt pending 0: no irq	R/W	0x0

		1: irq Write '1' to clean this bit. CNT overflow (0x9c00) would cause this irq.		
10	SRC_PD	Sample rate detect result sample rate change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
9	-	Reserved	R	0x0
8	CHW_PD	Sample rate detect result channel width change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
7:2	-	Reserved	R	0x0
1:0	WL	Channel word length (the rate of BCLK to LRCLK) 00: 16bit(32 rate) 01: 32bit(64 rate) 1x: Others	R	0x0

11.3.7.7 I2STX_FIFO_CNT

I2STX FIFO counter register
Offset = 0x20

Bit (s)	Name	Description	Access	Reset
31:19	-	Reserved	R	0x0
18	IP	I2STX FIFO sample counter overflow IRQ pending 0: no pending 1: pending Write '1' to clear this bit	R/W	0x0
17	IE	I2STX FIFO sample counter overflow IRQ enable 0: disable 1: enable If CNT overflow, it would cause an interrupt.	R/W	0x0
16	EN	I2STX FIFO counter enable 0:disable 1:enable Disable this function could reset the whole counter.	R/W	0x0
15:0	CNT	I2STX FIFO sample counter If overflow count would be clear to zero and cause an interrupt This counter count the valid data output by FIFO, it means that if FIFO is empty, this counter would not add till FIFO had been written data in again.	R	0x0

11.4 SPDIF TX

11.4.1 Features

SPDIF transmission (TX) supports sample rate 96k/48k/44.1k/32kHz.

11.4.2 SPDIF TX Register List

Table 11-7 SPDIFTX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
SPDIFTX_Control_Register	0xC0053000	0xC0053000

Table 11-8 SPDIFTX Controller Registers

Offset	Register Name	Description
0x00	SPDTX_CTL	SPDIFTX Control Register
0x04	SPDTX_CSL	SPDIFTX Channel State Low Register
0x08	SPDTX_CSH	SPDIFTX Channel State High Register

11.4.3 SPDIF TX Register Description

11.4.3.1 SPDTX_CTL

SPDIFTX Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	R	0x0
2	VALIDITY	Validity flag sent by hardware 0: Disable 0: Enable	R/W	0x0
1	SPD_DIS_CTL	0: Disable SPDIF (write 0 to SPDTX_CTL[0]) will take effect immediately. 1: Disable SPDIF (write 0 to SPDTX_CTL[0]) will take effect after the end of the right channel frame.	R/W	0x0
0	SPDEN	SPDIFTX Enable 0: Disable (will reset TX state machine) 1: Enable	R/W	0x0

11.4.3.2 SPDTX_CSL

SPDIFTX Channel State Low Register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:0	SPDCSL	SPDIFTX Channel State Low (Channel state bit31 to bit0)	R/W	x

11.4.3.3 SPDTX_CSH

SPDIFTX Channel State High Register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	SPDCSH	SPDIFTX Channel State High (Channel state bit47 to bit32)	R/W	x

11.5 SPDIF RX

11.5.1 Features

SPDIF receiver (RX) supports sample rate of 96k/48k/44.1k/32kHz.

11.5.2 SPDIF RX Register List

Table 11-9 SPDIFRX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
SPDIFRX_Control_Register	0xC0054000	0xC0054000

Table 11-10 SPDIFRX Controller Registers

Offset	Register Name	Description
0x0000	SPDIFRX_CTL0	SPDIFRX Control0 Register
0x0004	SPDIFRX_CTL1	SPDIFRX Control1 Register
0x0008	SPDIFRX_CTL2	SPDIFRX Control2 Register
0x000C	SPDIFRX_PD	SPDIFRX IRQ Pending Register
0x0014	SPDIFRX_CNT	SPDIFRX CNT Register
0x0018	SPDIFRX_CSL	SPDIFRX Channel State Register
0x001C	SPDIFRX_CSH	SPDIFRX Channel State Register
0x0020	SPDIFRX_SAMP	SPDIFRX Sample Rate Detect Register
0x0024	SPDIFRX_SRTO_THRES	SPDIFRX Sample Rate Detect Timeout Threshold Register

11.5.3 SPDIF RX Register Description

11.5.3.1 SPDIFRX_CTL0

SPDIFRX Control0 Register
Offset=0x00

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R/W	0x0
14	VBM	Validity bit mask 0: disable 1: enable	R/W	0x0
13	DAMS	Data mask state 0: not mask 1: mask	R/W	0x0
12	DAMEN	If sample rate change the new data mask 0: disable 1: enable	R/W	0x0
11:8	DELTAADD	Delta_t_add Delta to Add on Configured or detected T Width	R/W	0x0
7:4	DELTAMIN	Delta_t_min	R/W	0x0

		Delta to minus from Configured or detected T Width		
3	DELTA_MODE	Setting ±delta for T Width 0: Soft mode, using the DELTAADD and DELTAMIN as ±delta. (The setting values of DELTAAD and DDELTAMIN should be greater than or equal to 3) 1: Hardware mode, The hardware compares 1.5T-1T differenceΔt1 with 2T-1.5T differenceΔt2, chooses half of the smallest Δt as ±delta, and updates it to DELTAADD and DELTAMIN registers. (But when $\frac{1}{2}$ Δt > 15, delta is 15) If BMC Decoder Err appears, the T value and delta will be updated after 256 change edges are received.	R/W	0x1
2	CAL_MODE	Cal_Mode 0: SoftWare Config T Width 1: HardWare Detect T Width	R/W	0x1
1	SPDIF_CKEDG	Select of SPDIF input signal latch clock edge 0: pos_edge 1: nege_edge	R/W	0x0
0	SPDIF_RXEN	SPDIF RX Enable 0: Disable 1: Enable	R/W	0x0

11.5.3.2 SPDIFRX_CTL1

SPDIFRX Control1 Register
Offset=0x04

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	x
24:16	WID2TCFG	2T Width Configure Maximum count 512	R/W	0x0
15:8	WID1P5TCFG	1.5T Width Configure Maximum count 256	R/W	0x0
7:0	WID1TCFG	1T Width = BCM Code Width of Data '1' 1T Width Configure Maximum count 256	R/W	0x0

11.5.3.3 SPDIFRX_CTL2

SPDIFRX Control2 Register
Offset =0x08

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	R	x
27:18	WID4TCFG	4T Width Configure Maximum count 1024	R/W	0x0
17:9	WID3TCFG	3T Width Configure Maximum count 512	R/W	0x0
8:0	WID2P5TCFG	2.5T Width Configure Maximum count 512	R/W	0x0

11.5.3.4 SPDIFRX_PD

SPDIFRX IRQ pending Register
Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:17	-	Reserved	R	0x0
16	BL_HEADPD	Block head detect pending Writing '1' to clear	R/W	0x0
15	-	Reserved	R	0x0
14	SRTOPD	Sample rate detect timeout interrupt pending Writing '1' to clear	R/W	0x0
13	CSSRUPPD	Channel state sample rate change IRQ pending Writing '1' to clear	R/W	0x0
12	CSUPPD	Channel state update irq pending Writing '1' to clear	R/W	0x0
11	SRCPD	Sample rate change pending, Writing '1' to clear	R/W	0x0
10	BMCERPD	BMC Decoder Errror Pending， Writing '1' to clear	R/W	0x0
9	SUBRCVPD	Sub-Frame Receive Error Pending, Writing '1' to clear	R/W	0x0
8	BLKRCVPD	Block Receive Error Pending, Writing '1' to clear	R/W	0x0
7	-	Reserved	R	0x0
6	SRTOEN	Sample rate detect timeout IRQ enable 0: disable 1: enable	R/W	0x0
5	CSSRCIRQEN	Channel state sample rate change IRQ enable 0: disable 1: enable	R/W	0x0
4	CSUPIRQEN	Channel state update IRQ enable 0: disable 1: enable	R/W	0x0
3	SRCIRQEN	SPDIF RX Sample rate change IRQ enable 0: disable 1: enable	R/W	0x0
2	BMCIRQEN	BMC Decoder Error IRQ enable 1: Enable 0: Disable	R/W	0x0
1	SUBIRQEN	Sub-Frame Receive Error IRQ enable 1: Enable 0: Disable	R/W	0x0
0	BLKIRQEN	Block Receive Error IRQ enable 1: Enable 0: Disable	R/W	0x0

11.5.3.5 SPDIFRX_CNT

SPDIFRX CNT Register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0
24:16	HWDMAX	Hardware Detected maximum Width	R	0x0
15:8	HWDMIN	Hardware Detected minimum Width	R	0xff
7:0	FRAMECNT	Audio Frame Counter	R	0x0

		192 Frames in every audio block, range from 0 to 191.		

11.5.3.6 SPDIFRX_CSL

SPDIFRX Channel Status Register
Offset = 0x18

Bit (s)	Name	Description	Access	Reset
31:0	SPDCSL	SPDIFRX Channel State Low (Channel state bit31 to bit0)	R	x

11.5.3.7 SPDIFRX_CSH

SPDIFRX Channel Status Register
Offset = 0x1C

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	SPDCSH	SPDIFRX Channel State High (Channel state bit47 to bit32)	R	x

11.5.3.8 SPDIFRX_SAMP

SPDIFRX Sample Rate Detect Register
Offset = 0x20

Bit (s)	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	SAMP_VALID	Sample rate valid flag 0: no valid 1: valid	R	0x0
27:16	SAMP_CNT	SPDIFRX Sample rate counter detect by 24M clock	R	0x0
15:5	-	Reserved	R	0x0
4:1	SAMP_DELTA	Delta is used by SAMP_CNT to detect sample rate change or not	R/W	0x7
0	SAMP_EN	Sample rate detect enable 1: Enable 0: Disable	R/W	0x0

11.5.3.9 SPDIFRX_ SRTO_THRES

SPDIFRX Sample Rate Detect Timeout Threshold Register
Offset = 0x24

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	SRTO_THRES	The threshold to generate sample rate detect timeout signal.	R/W	0xfa00

12 User Interface (UI)

12.1 LCD Controller (LCDC)

12.1.1 Features

- RGB565 source data format
- Source data Transfer to FIFO by DMA
- Support 8-bit active (TFT) LCD panels with digital CPU input interface
- Support read and write operation

12.1.2 Function Description

12.1.2.1 RGB888 to RGB565 conversion

This module can convert 24bits RBG format to 16bits RGB before translating to LCD Panel.

12.1.2.2 Source DATA transfer channel

Source data is transferred to frame FIFO through DMA.

12.1.2.3 Source DATA

This LCDC can transfer YCbCr444 or RGB565 format data by setting bit SDT of register LCD_CTL.

12.1.2.4 External Memory Interface

The External Memory Interface supports 8-bit or 16-bit CPU LCD. It is used to sent command to CPU LCD and read data back from CUP LCD to LCDC.
CPU can write or read through EXTMEM_DATA to access the extended bus according to IFSEL of EXTMEM_CTL.
When it is set to 8bit interface, CPU writes or reads the lowest 8 bits of EXTMEM_DATA, the bus accesses the lower 8bit data bus. When it is set to 16bit interface, CPU writes or reads the lowest 16 bits of EXTMEM_DATA, the bus accesses the 16 bit data bus.

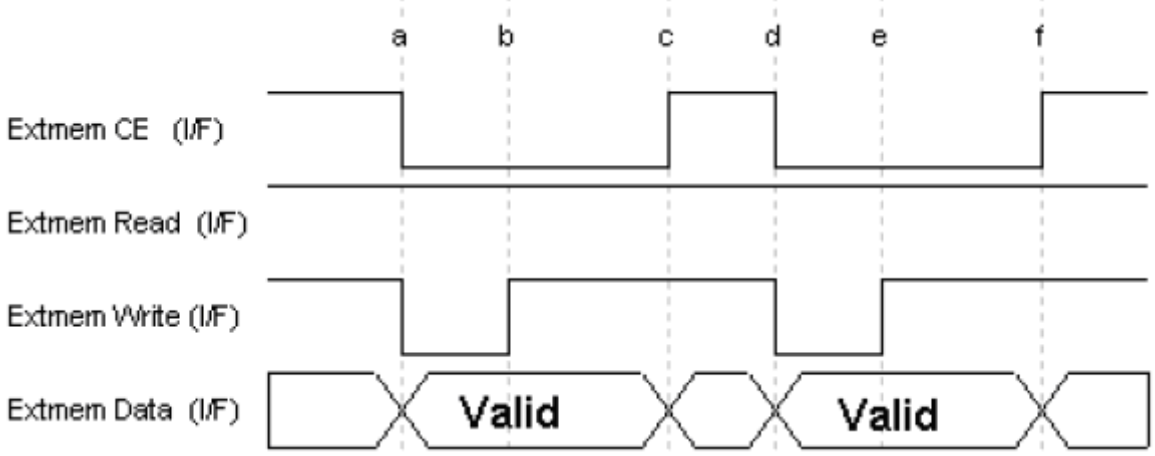


Figure 12-1 LCD Controller Write Timing

Write Timing:

a to b is the low state of writing cycle, the cycles depends on CLKLDU

b to c is the high state of writing cycle, the cycles depends on CLKHDU

a to c is a writing cycle,

When CPU writes EXTMEM_DATA register, the EXTMEM CEB is driven to low level, the host will drive the EXTMEM Data bus until the EXTMEM Write cycle is over. When the EXTMEM CEB is low level, the LCM will be chip selected.

The EXTMEM Write signal will be driven to low level until the low state counter is CLKLDU, then the write signal will be driven to high level until the high state counter is CLKHDU. The device will latch the data at the rise edge of EXTMEM Write.

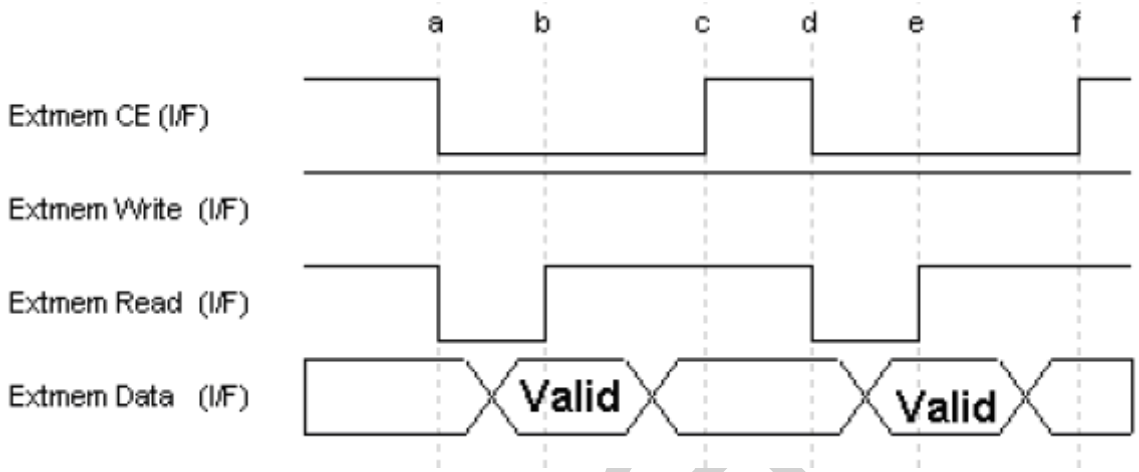


Figure 12-2 LCD Controller Read Timing

Read Timing:

a to b is the low state of reading cycle, the cycles depends on CLKLDU

b to c is the high state of reading cycle, the cycles depends on CLKHDU

a to c is a read cycle

When CPU reads EXTMEM_DATA register, the EXTMEM CEB is driven to low level until the EXTMEM Read cycle is over. When the EXTMEM CEB is low level, the LCM will be chip selected. The EXTMEM Read signal will be driven to low level until the low state counter is CLKLDU, then the read signal will be driven to high level until the high state counter is CLKHDU. When EXTMEM Read is low level, the LCM will drive the EXTMEM Data bus.

12.1.2.5 CPU IF timing

Table 12-1 Control signal define

RS	R/W	Function
0	0	Sets Index Register
0	1	Read Status
1	0	Writes Instruction
1	1	Reads Instruction

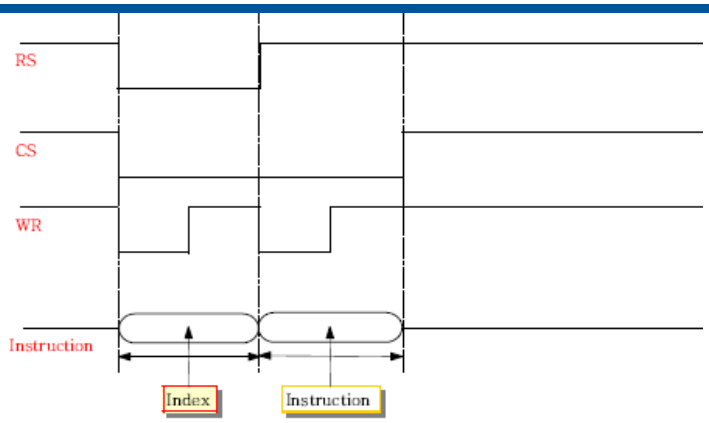


Figure 12-3 CPU LCD Timing

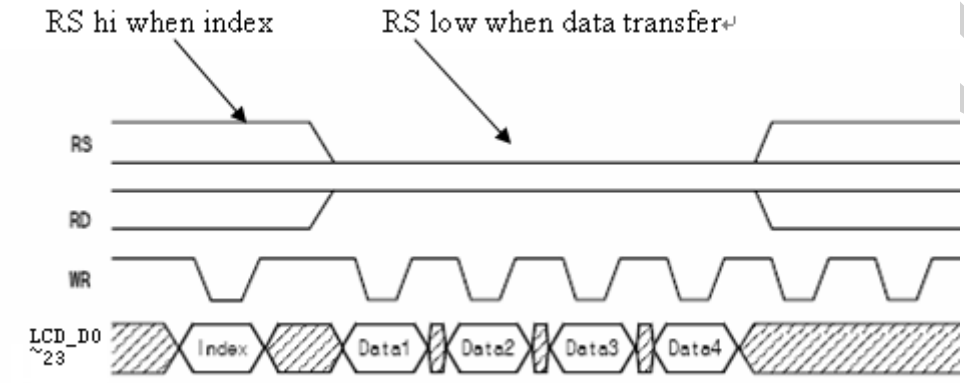


Figure 12-4 LCD Controller 8080 mode bus

12.1.3 LCD Register List

Table 12-2 LCD Controller Registers base address

Name	Physical Base Address	KSEG1 Base Address
LCDC_REGISTER	0xC0030000	0xC0030000

Table 12-3 RTC Controller Registers

Offset	Register Name	Description
0x0000	LCD_CTL	LCD Control Register
0x0004	LCD_CLKCTL	LCD and EXTMEM Clock adjust Register
0x0008	EXTMEM_CTL	Extended Memory Interface Control Register
0x000C	EXTMEM_CLKCTL	Extended Memory Interface Clock adjust Register
0x0010	EXTMEM_DATA	Extended Memory Interface DATA Register
0x0014	LCD_IF_PCS	LCD parity register

12.1.4 LCD Register Description

12.1.4.1 LCD_CTL

LCD controller control register

Offset=0x0000

Bits	Name	Description	Access	Reset
31	LCDFI	LCD Data translate Finish 0: busy 1: finish Writing '1' to clear the bit.	R/W	0x0
30	PC_EN	Parity Check enable bit 0: Disable 1: Enable Just used for TESTMOD, in normal mod this bit should be disable.	R/W	0x0
29:18	-	Reserved	R	0x0
17	FOVF	FIFO Overflow Pending Bit 0: Not overflow 1: overflow Writing '1' to clear this bit and reset the FIFO.	R/W	0x0
16:11	-	Reserved	R	0x0
10	FIFOET	FIFO Empty Status 0: Not Empty 1: Empty	R	0x0
9:8	-	Reserved	R	0x0
7	EMDE	FIFO Empty DRQ Enable 0: Disable 1: Enable This bit should be enabled when DMA is used to transmit the LCD data.	R/W	0x0
6:5	-	Reserved	R	0x0
4	FORMATS	RGB Format Select 0: 8bit (RGB 565 2transfer) 1:16bit (RGB 565 1transfer)	R/W	0x0
3	SEQ	RGB Sequence 0: RGB 1: BGR	R/W	0x0
2	MLS	When LCD_CTL[4](FORMATS) is '0', this bit is used to control LSB or MSB. 0: LSB 1: MSB	R/W	0x0
1	C86	Mode select 0: I8080 Interface 1: M6800 Interface	R/W	0x0
0	EN	LCD controller Enable 0: Disable 1: Enable Note: before setting this bit all other setting of LCDC should be set. This bit would be cleared by hardware after AHB Clock is synchronized with LCD Clock.	R/W	0x0

12.1.4.2 LCD_CLKCTL

LCD and EXTMEM Clock adjust Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:22	-	Reserved	R	0x0

21:16	CLKHDU	Clock High Level Duration (from LCD_CLK) from 1 to 64 (CLKHDU +1)	R/W	0xf
15:14	-	Reserved	R	0x0
13:8	CLKL2DU	Clock Low Level Duration (from LCD_CLK) from 1 to 64 (CLKL2DU +1)	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	CLKLDU	Clock Low Level Duration (from LCD_CLK) from 1 to 64 (CLKLDU +1)	R/W	0xf

12.1.4.3 EXTMEM_CTL

Extended Memory Interface Control Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:29	CESEL	Choose the Chip Select of extended memory Interface 001: CE0 010: CE1 011: CE2 100: CE3 101: CE4 Others: Reserved Note: Write or read from LCDM，must select CE4	R/W	0x5
28:9	-	Reserved	R	0x0
8	IFSEL	Choose the 8bits/16bits bus interface 0: 8 bits interface 1: 16 bits interface	R/W	0x0
7:1	-	Reserved	R	0x0
0	RS	RS select 0: RS output low voltage level 1: RS output high voltage level RS is low or high voltage in the case of writing INDEX/DATA/REG in different LCM.	R/W	0x0

12.1.4.4 EXTMEM_CLKCTL

EM clock control register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:22	-	Reserved	R	0x0
21:16	EXCLKH	Clock High Level Duration (from AHB_CLK) from 1 to 64 (EXCLKH +1)	R/W	0xf
15:14	-	Reserved	R	0x0
13:8	EXCL2KL	Clock Low Level Duration (from AHB_CLK) from 1 to 64 (EXCL2KL +1)	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	EXCLKL	Clock Low Level Duration (from AHB_CLK) from 1 to 64 (EXCLKL +1)	R/W	0xf

NOTE: EXTMEM use clock from AHB_CLK, when use EXTMEM to sent command to LCDM or read data from LCDM, this register should be set to obtain perfect operation clock.

12.1.4.5 EXTMEM_DATA

Extended Memory Interface DATA Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:8	EXT_DATAH	The higher 8bit data bus of extended interface	R/W	0x0
7:0	EXT_DATAL	The lower 8bit data bus of extended interface	R/W	0x0

12.1.4.6 LCD_IF_PCS

LCD parity register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	PCS	Parity Check Sum The Parity Check Sum of the LCD parallel interface (both 8 bit and 16bit).	R	0x0

12.2 SEG_LCD&LED controller

12.2.1 Features

- Support 3com / 4com / 5com / 6com SEG_LCD Driving Timing
- Support 4com or 8com DIG_LED Driving Timing
- Support 7 / 8 pin matrix_LED driving timing
- Support LED segment analog constant current configuration
- Support HOSC / LOSC for SEG_LCD & DIG_LED clock source

12.2.2 SEG_SREEN Register List

Table 12-4 SEG_SREEN Registers base address

Name	Physical Base Address	KSEG1 Base Address
SEG_SREEN	0xC00E0000	0xC00E0000

Table 12-5 SEG_SREEN Registers

Offset	Register Name	Description
0x0000	SEG_SREEN_CTL	Seg LCD Control Register
0x0004	SEG_SREEN_DATA0	Seg LCD Data Register0
0x0008	SEG_SREEN_DATA1	Seg LCD Data Register1
0x000C	SEG_SREEN_DATA2	Seg LCD Data Register2
0x0010	SEG_SREEN_DATA3	Seg LCD Data Register3
0x0014	SEG_SREEN_DATA4	Seg LCD Data Register4
0x0018	SEG_SREEN_DATA5	Seg LCD Data Register5
0x001C	SEG_RC_EN	LED SEG Restrict Current Enable Register
0x0020	SEG_BIAS_EN	LED SEG Bias Current Enable Register

12.2.3 SEG_SREEN Register Description

12.2.3.1 SEG_SREEN_CTL

Seg-screen control register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	LCD_POWER	LCD POWER BACK DOOR 0: SEG0/SEG1 are used as normal function 1: When SEG0/SEG1 are selected as LCD_SEG function，SEG0/SEG1 output 1/3VCC and 2/3VCC Separately.	R/W	0x0
30:11	-	Reserved	R	0x0
10:8	LED_COM_DZ	The com of LED will got a “dead zone”, this register define the width of the dead zone: 000b: no dead zone between LED COM Beats 001b: 1/32 of the LED COM beat will be dead zone 010b: 2/32 of the LED COM beat will be dead zone 011b: 3/32 of the LED COM beat will be dead zone 100b: 4/32 of the LED COM beat will be dead zone 101b: 5/32 of the LED COM beat will be dead zone 110b: 6/32 of the LED COM beat will be dead zone 111b: 7/32 of the LED COM beat will be dead zone	R/W	0x0
7	SEGOFF	Segment Off 0: Segment is always off 1: Segment value is according to LCD_DATA P.S. Only active in COM/SEG or Digit-LED Mode	R/W	0x0
6	-	Reserved	R	0x0
5	LCD_OUT_EN	LCD&LED pad output Enable select 0: the pads of seg_LCD and LED will output “high_Z”. 1: the pads of seg_LCD and LED output signal as it’s timing.	R/W	0x0
4	REFRSH	Refresh LCD/LED Data 0: Hold LCD_DATA Refresh LCD/LED panel according to the LCD_DATA buffer value 1: Update LCD_DATA Refresh the LCD_DATA buffer value from LCD_DATA register P.S. Only active in COM/SEG or Digit-LED Mode; When updating the value of LCD_DATA register, write “1” to this bit, the hardware will clear this bit when the LCD_DATA has been updated.	R/W	0x0

3:0	MODE_SEL	Mode Select 0000b: 3Com,1/3 Bias SEG/COM LCD Frame-Invert 0001b: 3Com,1/3 Bias SEG/COM LCD Row-Invert 0010b: 4Com,1/3 Bias SEG/COM LCD Frame-Invert 0011b: 4Com,1/3 Bias SEG/COM LCD Row-Invert 0100b: 5Com,1/3 Bias SEG/COM LCD Frame-Invert 0101b: 5Com,1/3 Bias SEG/COM LCD Row-Invert 0110b: 6Com,1/3 Bias SEG/COM LCD Frame-Invert 0111b: 6Com,1/3 Bias SEG/COM LCD Row-Invert 1000b: 4Com Digit-LED Common-Cathode Mode 1001b: 4Com Digit-LED Common- Anode Mode 1010b: 8Com Digit-LED Common-Cathode Mode 1011b: 8Com Digit-LED Common- Anode Mode 1100b: 7Pin Matrix_LED Common-Cathode mode 1101b: 7Pin Matrix_LED Common- Anode mode 1110b: 8Pin Matrix_LED Common-Cathode mode 1111b: 8Pin Matrix_LED Common- Anode mode	R/W	0x0

12.2.3.2 SEG_SREEN_DATA0

Seg-screen data register0
Offset=0x0004

Bits	Name	Description	Access	Reset
31:24	COM0_BYTE3	SEG/COM Mode:COM0_SEG[31:24] Digit-LED Mode:COM3_seg[7:0] Matrix_LED: COM3_seg[7:0] When set to “1”, the cross of COM and SEG is ON; Else is OFF.	R/W	0x0
23:16	COM0_BYTE2	SEG/COM Mode:COM0_SEG[23:16] Digit-LED Mode:COM2_seg[7:0] Matrix_LED: COM2_seg[7:0]	R/W	0x0
15:8	COM0_BYTE1	SEG/COM Mode:COM0_SEG[15:8] Digit-LED Mode:COM1_seg[7:0] Matrix_LED: COM1_seg[7:0]	R/W	0x0
7:0	COM0_BYTE0	SEG/COM Mode:COM 0_SEG[7:0] Digit-LED Mode:COM0_seg[7:0] Matrix_LED: COM0_seg[7:0]	R/W	0x0

12.2.3.3 SEG_SREEN_DATA1

Seg-screen data register1
Offset=0x0008

Bits	Name	Description	Access	Reset
31:24	COM1_BYTE3	SEG/COM Mode:COM1_SEG[31:24] Digit-LED Mode:COM7_seg[7:0] Matrix_LED: COM7_seg[7:0]	R/W	0x0
23:16	COM1_BYTE2	SEG/COM Mode:COM1_SEG[23:16] Digit-LED Mode:COM6_seg[7:0] Matrix_LED: COM6_seg[7:0]	R/W	0x0
15:8	COM1_BYTE1	SEG/COM Mode:COM1_SEG[15:8] Digit-LED Mode:COM5_seg[7:0] Matrix_LED:COM5_seg[7:0]	R/W	0x0

7:0	COM1_BYTE0	SEG/COM Mode:COM1_SEG[7:0] Digit-LED Mode:COM4_seg[7:0] Matrix_LED: COM4_seg[7:0]	R/W	0x0

12.2.3.4 SEG_SREEN_DATA2

Seg-screen data register2
Offset=0x000C

Bits	Name	Description	Access	Reset
31:0	COM2_WORD	SEG/COM Mode:COM2_SEG[31:0] if the xTH bit of this register is “1”, Com2_seg-x will on.	R/W	0x0

12.2.3.5 SEG_SREEN_DATA3

Seg-screen data register3
Offset=0x0010

Bits	Name	Description	Access	Reset
31:0	COM3_WORD	SEG/COM Mode:COM3_SEG[31:0] if the xTH bit of this register is “1”, Com3_seg-x will on.	R/W	0x0

12.2.3.6 SEG_SREEN_DATA4

Seg_screen data register4
Offset=0x0014

Bits	Name	Description	Access	Reset
31:0	COM4_WORD	SEG/COM Mode:COM4_SEG[31:0] if the xTH bit of this register is “1”, Com4_seg-x will on.	R/W	0x0

12.2.3.7 SEG_SREEN_DATA5

Seg_screen data register5
Offset=0x0018

Bits	Name	Description	Access	Reset
31:0	COM5_WORD	SEG/COM Mode:COM5_SEG[31:0] if the xTH bit of this register is “1”, Com5_seg-x will on.	R/W	0x0

12.2.3.8 SEG_RC_EN

LED SEG Restrict Current Enable
Offset=0x1C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	LED_SEG7	LED SEG7 Restrict Current Enable	R/W	0x0
6	LED_SEG6	LED SEG6 Restrict Current Enable	R/W	0x0
5	LED_SEG5	LED SEG5 Restrict Current Enable	R/W	0x0
4	LED_SEG4	LED SEG4 Restrict Current Enable	R/W	0x0
3	LED_SEG3	LED SEG3 Restrict Current Enable	R/W	0x0
2	LED_SEG2	LED SEG2 Restrict Current Enable	R/W	0x0
1	LED_SEG1	LED SEG1 Restrict Current Enable	R/W	0x0

0	LED_SEG0	LED SEG0 Restrict Current Enable	R/W	0x0

12.2.3.9 SEG_BIAS_EN

LED SEG Bias Current Enable
Offset=0x20

Bits	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	LED_SEG_ALL_EN	LED SEG Restrict Current ALL Enable 0: Disable 1: Enable	R/W	0x0
3	LED_CATHODE_ANODE_MODE	LED Cathode/Anode Mode 0: Cathode Mode 1: Anode Mode	R	0x0
2:0	LED_SEG_BIAS	LED SEG BIAS 000: 2mA 001: 3mA 010: 6mA 011: 7mA 100: 10 mA 101: 11 mA 110: 14mA 111: 15mA	R/W	0x1

13 GPIO and I/O Multiplexer

13.1 Features

- Supports 32 GPIO and 1 WIO(wake up IO)
- GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers.
- All GPIO and WIO has internal pull down or pull up resistors
- Driving strength can be adjusted, Level (n) corresponds to (2n) mA
- Automatically switching PAD function

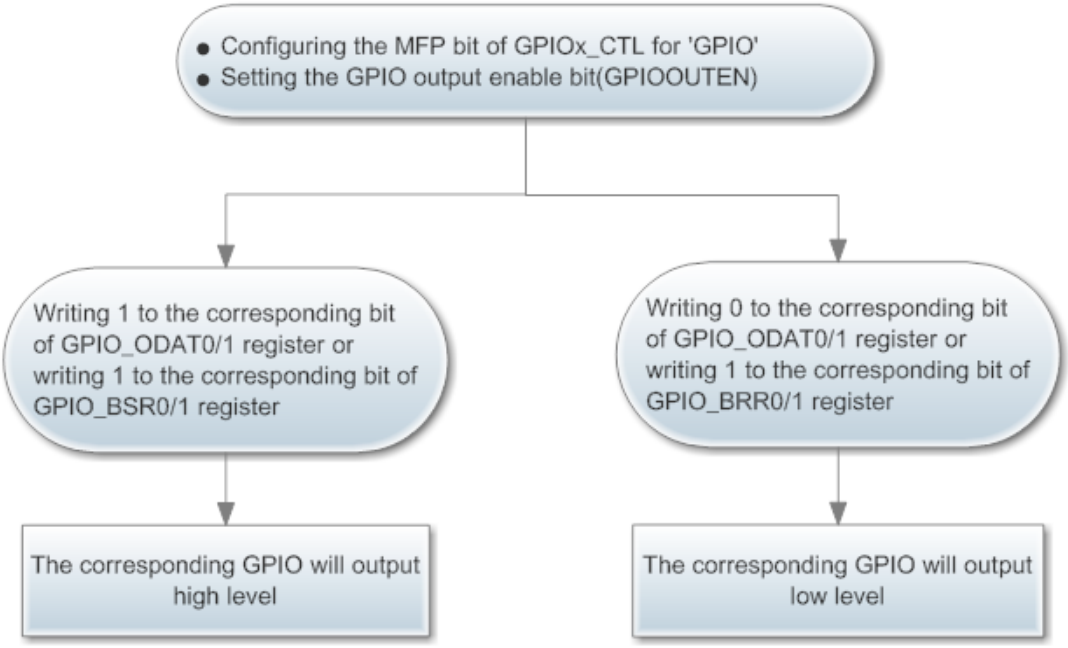
13.2 Operation Manual

13.2.1 Multi-function Switch Operation

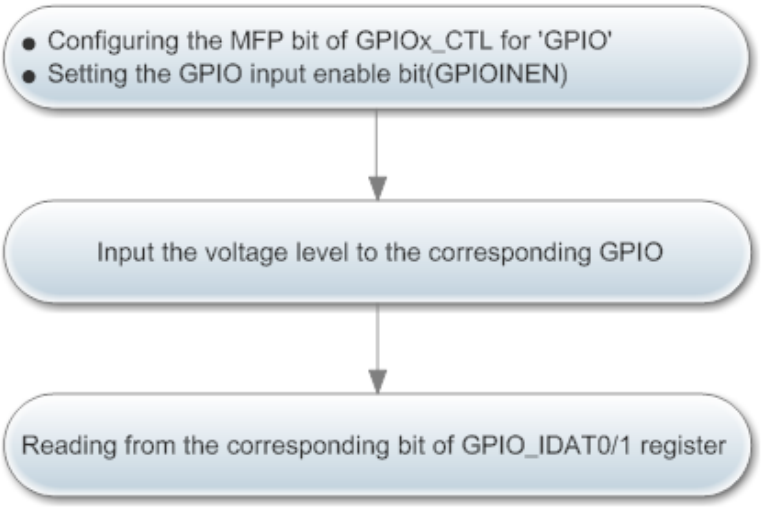
1. Some pin can be multiplexed as three kinds of functions: module function (MFP), GPIO function, Analog function, which can be configured by setting AD_Select bit and MFP bit of GPIOx_CTL registers.
2. GPIO and MFP are digital functions. Once the Analog function is selected, the digital functions will fail. The function priority of some multiplexed pin are Analog function > GPIO function > MFP function.
3. GPIO[44:55] can be multiplexed as analog function and digital function. If the pin is used as digital function, it must be disabled analog function firstly by setting AD_Select register.
4. Some MFP modules have itself pull-up and pull-down resistors, referring the chapter Pad PU control register and Pad PD control register; when the pin is multiplexed as MFP module function, the

modules pull-up/pull-down resistors will be enabled automatically and the pull-up/pull-down resistors of GPIOs must be DISABLED, or the voltage level and functions will be abnormal.

13.2.2 GPIO Output

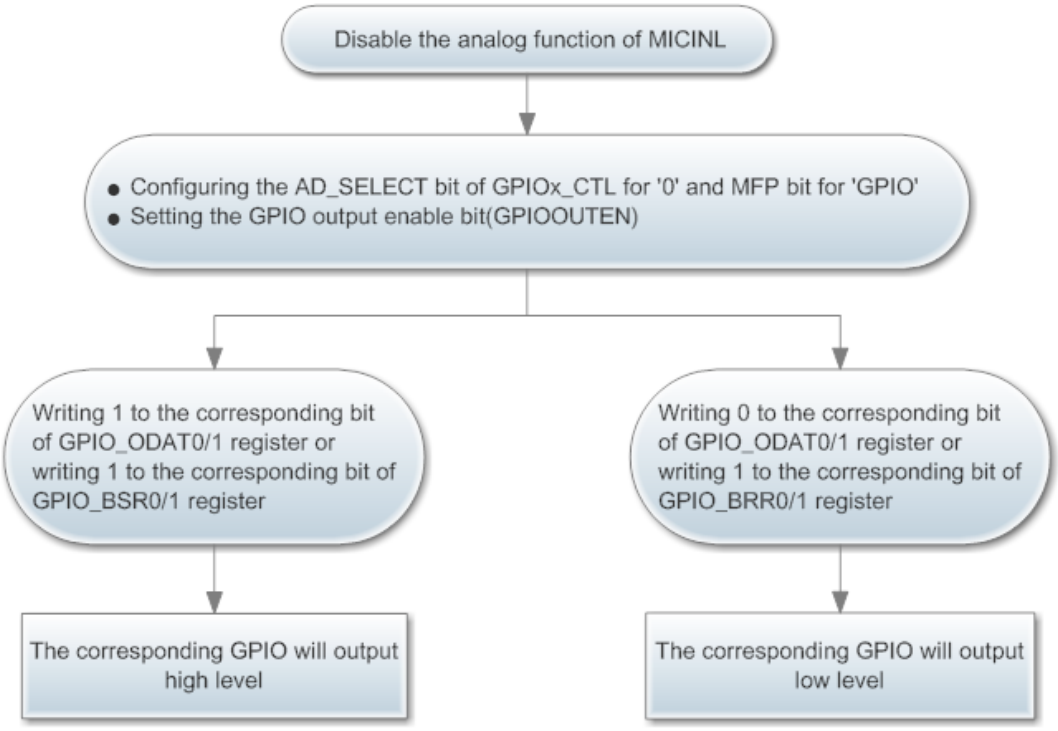


13.2.3 GPIO Input



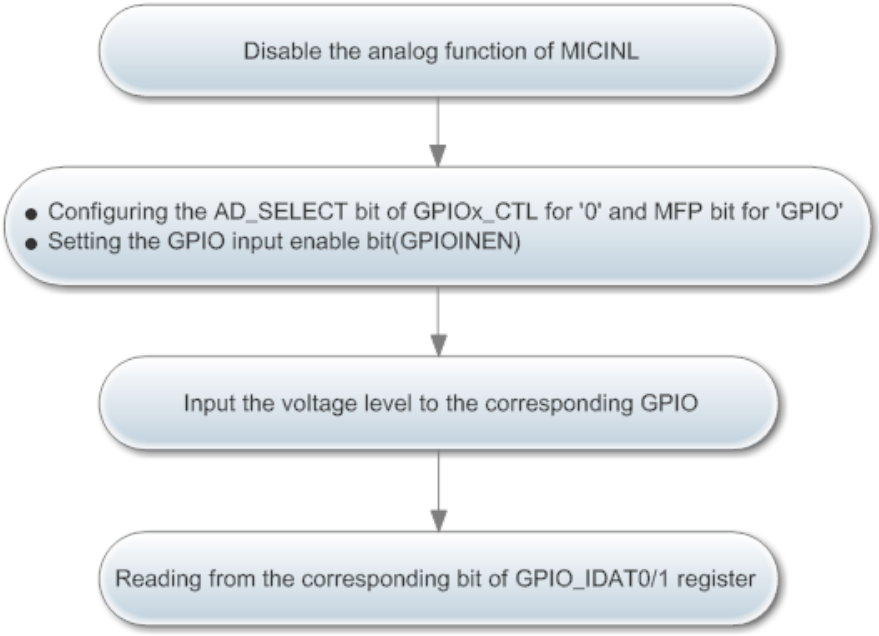
13.2.4 GPIO[44:55] Output

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as GPIO.

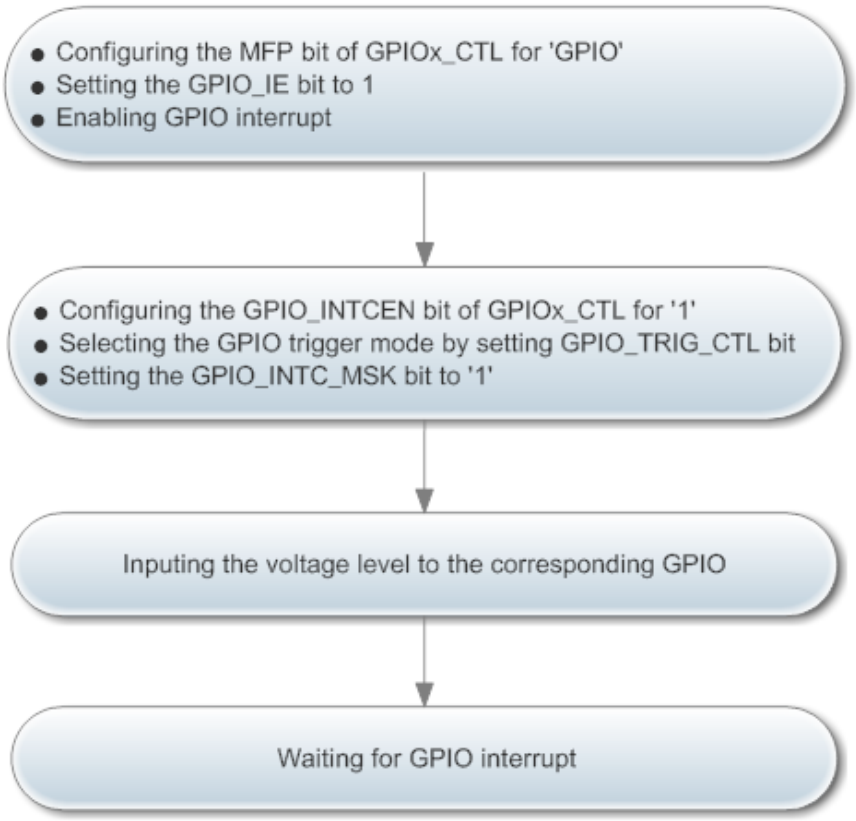


13.2.5 GPIO[44:55] Input

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as GPIO.



13.2.6 GPIO INTC



13.3 GPIO Register List

Table 13-1 GPIO_MFP Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_MFP_REGISTER	0xC0090000	0xC0090000

Table 13-2 GPIO&MFP Controller Registers

Offset	Register Name	Description	Voltage
0x0004	GPIO0_CTL	GPIO0 control Register	VDD
0x0008	GPIO1_CTL	GPIO1 control Register	VDD
0x000C	GPIO2_CTL	GPIO2 control Register	VDD
0x0010	GPIO3_CTL	GPIO3 control Register	VDD
0x0014	GPIO4_CTL	GPIO4 control Register	VDD
0x0018	GPIO5_CTL	GPIO5 control Register	VDD
0x001C	GPIO6_CTL	GPIO6 control Register	VDD
0x0020	GPIO7_CTL	GPIO7 control Register	VDD
0x003C	GPIO14_CTL	GPIO14 control Register	VDD
0x0040	GPIO15_CTL	GPIO15 control Register	VDD
0x0044	GPIO16_CTL	GPIO16 control Register	VDD
0x0048	GPIO17_CTL	GPIO17 control Register	VDD
0x0050	GPIO19_CTL	GPIO19 control Register	VDD
0x0054	GPIO20_CTL	GPIO20 control Register	VDD
0x0058	GPIO21_CTL	GPIO21 control Register	VDD
0x005C	GPIO22_CTL	GPIO22 control Register	VDD
0x0060	GPIO23_CTL	GPIO23 control Register	VDD

0x0074	GPIO28_CTL	GPIO28 control Register	VDD
0x0078	GPIO29_CTL	GPIO29 control Register	VDD
0x007C	GPIO30_CTL	GPIO30 control Register	VDD
0x0080	GPIO31_CTL	GPIO31 control Register	VDD
0x0084	GPIO32_CTL	GPIO32 Control Register	VDD
0x0088	GPIO33_CTL	GPIO33 Control Register	VDD
0x008C	GPIO34_CTL	GPIO34 Control Register	VDD
0x0090	GPIO35_CTL	GPIO35 Control Register	VDD
0x0094	GPIO36_CTL	GPIO36 Control Register	VDD
0x009C	GPIO38_CTL	GPIO38 Control Register	VDD
0x00A0	GPIO39_CTL	GPIO39 Control Register	VDD
0x00A4	GPIO40_CTL	GPIO40 Control Register	VDD
0x00AC	GPIO42_CTL	GPIO42 Control Register	VDD
0x00B0	GPIO43_CTL	GPIO43 Control Register	VDD
0x00B4	GPIO44_CTL	GPIO44 Control Register	VDD
0x00B8	GPIO45_CTL	GPIO45 Control Register	VDD
0x00BC	GPIO46_CTL	GPIO46 Control Register	VDD
0x00C0	GPIO47_CTL	GPIO47 Control Register	VDD
0x00C4	GPIO48_CTL	GPIO48 Control Register	VDD
0x00C8	GPIO49_CTL	GPIO49 Control Register	VDD
0x00CC	GPIO50_CTL	GPIO50 Control Register	VDD
0x00D0	GPIO51_CTL	GPIO51 Control Register	VDD
0x00D4	GPIO52_CTL	GPIO52 Control Register	VDD
0x00D8	GPIO53_CTL	GPIO53 Control Register	VDD
0x00DC	GPIO54_CTL	GPIO54 Control Register	VDD
0x00E0	GPIO55_CTL	GPIO55 Control Register	VDD
0x0100	GPIO_ODAT0	GPIO Output Data Register 0	VDD
0x0104	GPIO_ODAT1	GPIO Output Data Register 1	VDD
0x0108	GPIO_BSR0	GPIO Output Data bit Set Register 0	VDD
0x010C	GPIO_BSR1	GPIO Output Data bit Set Register 1	VDD
0x0110	GPIO_BRR0	GPIO Output Data bit Reset Register 0	VDD
0x0114	GPIO_BRR1	GPIO Output Data bit Reset Register 1	VDD
0x0118	GPIO_IDAT0	GPIO Input Data Register 0	VDD
0x011C	GPIO_IDAT1	GPIO Input Data Register 1	VDD
0x0120	GPIO_PD0	GPIO IRQ Pending Register 0	VDD
0x0124	GPIO_PD1	GPIO IRQ Pending Register 1	VDD
0x0140	WIO0_CTL	WIO0 Control Register	RTCVDD

13.4 GPIO Register Description

13.4.1 GPIO0_CTL

GPIO0 control Register
Offset=0x04

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO	R/W	0x0

		trigger event is detect		
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: Disable 1: Enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM0 0010: EM_WRB 0011: LCD_WRB 0100: LCD_COM0 0101: I2C_SCL	R/W	0x0

		0110: PWM1 0111: UART0_RTS 1001: I2STX_MCLK 1010: I2SRX0_MCLK 1011: I2SRX1_MCLK 1100: TIMER2_CAP 1101: SPI2_SS Others: Reserved		

13.4.2 GPIO1_CTL

GPIO1 control Register
Offset=0x08

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0

8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM1 0010: EM_RS 0011: LCD_RS 0100: LCD_COM1 0101: I2C_SDA 0110: PWM3 0111: UART0_CTS 1001: I2STX_BCLK 1010: I2SRX0_BCLK 1011: I2SRX1_BCLK 1100: TIMER3_CAP 1101:SPI2_MISO Others: Reserved	R/W	0x0

13.4.3 GPIO2_CTL

GPIO2 control Register
Offset=0x0C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable;	R/W	0x0

		Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM2 0010: EM_RDB 0011: LCD_RDB 0100: LCD_COM2 0110: PWM2 0111: UART0_RX 1000: LRADC4 1001: I2STX_LRCLK 1010: I2SRX0_LRCLK 1011: I2SRX1_LRCLK 1100: TIMER2_CAP 1101: SPI2_MOSI Others: Reserved	R/W	0x0

13.4.4 GPIO3_CTL

GPIO3 control Register
Offset=0x10

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0

3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM3 0010: EM_CEB0 0011: LCD_CEB 0100: LCD_COM3 0111: UART0_TX 1001: I2STX_DOUT 1010: I2SRX0_DIN 1011: I2SRX1_DIN 1100: TIMER3_CAP 1101:SPI2_SCLK Others: Reserved	R/W	0x0

13.4.5 GPIO4_CTL

GPIO4 control Register
Offset=0x14

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable	R/W	0x0

		1: Enable		
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM4 0010: EM_CEB1 0011: LCD_CEB 0100: LCD_COM4 0110: PWM1 1100: TIMER2_CAP 1101: IR_RX Others: Reserved	R/W	0x0

13.4.6 GPIO5_CTL

GPIO5 control Register
Offset=0x18

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable;	R/W	0x0

		Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM5 0010: EM_CEB2 0011: BT_REQ 0100: LCD_COM5 0110: PWM3 1100: TIMER3_CAP Others: Reserved	R/W	0x0

13.4.7 GPIO6_CTL

GPIO6 control Register
Offset=0x1C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO	R/W	0x0

		trigger event is detect		
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM6 0010: EM_CEB3 0011: BT_ACCESS 0100: LCD_SEG0 0110: PWM4	R/W	0x0

		1001: I2STX_LRCLK 1010: I2SRX0_LRCLK 1011: I2SRX1_LRCLK 1100: TIMER2_CAP 1101: SD1_DAT0 Others: Reserved		

13.4.8 GPIO7_CTL

GPIO7 control Register
Offset=0x20

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable	R/W	0x0

		1: Enable		
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM7 0010: EM_CEB4 0011: PTA_GRANT 0100: LCD_SEG1 0101: SPDIF_RX 0110: PWM0 0111: UART1_TX 1000: FMCLKOUT 1001: I2STX_DOUT 1010: I2SRX0_DIN 1011: I2SRX1_DIN 1100: TIMER3_CAP 1101: SD1_DAT3 Others: Reserved	R/W	0x0

13.4.9 GPIO14_CTL

GPIO14 control Register
Offset=0x3C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger	R/W	0x0

		event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_SEG6 0010: EM_D6 0011: LCD_D6 0100: LCD_SEG8 1000: LRADC11 1001: SPI0_IO2 1100: TIMER2_CAP Others: Reserved	R/W	0x0

13.4.10 GPIO15_CTL

GPIO15 control Register
Offset=0x40

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO	R/W	0x0

		trigger event is detect		
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_SEG7 0010: EM_D7 0011: LCD_D7 0100: LCD_SEG9 0110: PWM4	R/W	0x0

		0111: UART1_RX 1001: I2STX_MCLK 1010: I2SRX0_MCLK 1011: I2SRX1_MCLK 1100: TIMER3_CAP 1101: SD1_DAT0 1110: SPI0_IO3 1111: Reserved		

13.4.11 GPIO16_CTL

GPIO16 control Register
Offset=0x44

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0

8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: SPI2_SS 0100: LCD_SEG14 0110: PWM4 0111: UART0_RX 1100: TIMER2_CAP 1101: SD0_CMD Others: Reserved	R/W	0x0

13.4.12 GPIO17_CTL

GPIO17 control Register
Offset=0x48

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1	R/W	0x1

		001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: SPI2_SCLK 0100: LCD_SEG15 0111: UART0_TX 1100: TIMER3_CAP 1101: SD0_CLK0 Others: Reserved	R/W	0x0

13.4.13 GPIO19_CTL

GPIO19 control Register
Offset=0x50

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level	R/W	0x0

		100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG17 0101: I2C_SDA 1100: TIMER3_CAP Others: Reserved	R/W	0x0

13.4.14 GPIO20_CTL

GPIO20 control Register
Offset=0x54

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0

25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: SPI2_MISO	R/W	0x0

		0010: EM_D8 0011: LCD_D8 0100: LCD_SEG10 0110: PWM2 0111: UART1_CTS 1100: TIMER2_CAP 1101: SD0_DAT0 Others: Reserved		

13.4.15 GPIO21_CTL

GPIO21 control Register
Offset=0x58

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0

8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: SPI2_MOSI 0010: EM_D9 0011: LCD_D9 0100: LCD_SEG11 0110: PWM0 0111: UART0_RX 1000: TEMPADC 1001: I2STX_MCLK 1010: I2SRX0_MCLK 1011: I2SRX1_MCLK 1100: TIMER3_CAP 1101: SD1_CLK 1110: UART1_TX 1111: SD0_DAT1	R/W	0x0

13.4.16 GPIO22_CTL

GPIO22 control Register
Offset=0x5C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC.	R/W	0x0

		1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable. 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0010: EM_D10 0011: LCD_D10 0100: LCD_SEG12 0101: IR_RX 0110: PWM1 0111: UART0_TX 1000: LRADC2 1001: I2STX_LRCLK 1010: I2SRX0_LRCLK 1011: I2SRX1_LRCLK 1100: TIMER2_CAP 1101: SD1_DAT2 1110: UART1_RX 1111: SD0_DAT2	R/W	0x0

13.4.17 GPIO23_CTL

GPIO23 control Register
Offset=0x60

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0

5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0010: EM_D11 0011: LCD_D11 0100: LCD_SEG13 0101: SPDIFTX 0110: PWM2 0111: UART0_TX 1000: LRADC3 1001: I2STX_BCLK 1010: I2SRX0_BCLK 1011: I2SRX1_BCLK 1100: TIMER3_CAP 1101: SD1_CMD 1110: SD0_DAT3 1111: SD0_DAT0	R/W	0x0

13.4.18 GPIO28_CTL

GPIO28 control Register
Offset=0x74

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3	R/W	0x1

		011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG18 0101: SPI0_SS 0110: SPI0_MOSI 1100: TIMER2_CAP Others: Reserved	R/W	0x0

13.4.19 GPIO29_CTL

GPIO29 control Register
Offset=0x78

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable	R/W	0x0

		0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG19 0101: I2C_SDA 0110: SPI0_SCLK 0111: SPI0_SS 1100: TIMER3_CAP 1101: SD0_CLK1 Others: Reserved	R/W	0x0

13.4.20 GPIO30_CTL

GPIO30 control Register
Offset=0x7C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0

25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG21	R/W	0x0

		0101: I2C_SCL 0110: SPI0_MISO 0111: SPI0_SCLK 1100: TIMER2_CAP Others: Reserved		

13.4.21 GPIO31_CTL

GPIO31 control Register
Offset=0x80

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0

7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0011: SPI0_MOSI 0100: LCD_SEG20 0101: SPI0_MISO 0110: PWM5 1100: TIMER3_CAP Others: Reserved	R/W	0x0

13.4.22 GPIO32_CTL

GPIO32 control Register
Offset=0x84

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5	R/W	0x1

		101: Level 6 110: Level 7 111: Level 8		
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG22 1001: I2STX_MCLK 1010: I2SRX0_MCLK 1011: I2SRX1_MCLK Others: Reserved	R/W	0x0

13.4.23 GPIO33_CTL

GPIO33 control Register
Offset=0x88

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send	R/W	0x0

		IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG23 1001: I2STX_BCLK 1010: I2SRX0_BCLK 1011: I2SRX1_BCLK Others: Reserved	R/W	0x0

13.4.24 GPIO34_CTL

GPIO34 control Register
Offset=0x8C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO	R/W	0x0

		trigger event is detect		
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable. 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable. 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG24 1001: I2STX_LRCLK 1010: I2SRX0_LRCLK 1011: I2SRX1_LRCLK Others: Reserved	R/W	0x0

13.4.25 GPIO35_CTL

GPIO35 control Register
Offset=0x90

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0

5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0010: SPDIFTX 0100: LCD_SEG25 1001: I2STX_DOUT 1010: I2SRX0_DIN 1011: I2SRX1_DIN Others: Reserved	R/W	0x0

13.4.26 GPIO36_CTL

GPIO36 control Register
Offset=0x94

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0

10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0100: LCD_SEG26 1001: I2S0TX_DOUT 1010: I2S0RX_DIN 1011: I2S1RX_DIN Others: Reserved	R/W	0x0

13.4.27 GPIO38_CTL

GPIO38 control Register
Offset=0x9C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0

14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0010: SPDIF_RX 0011: BT_REQ 0100: LCD_SEG28 0110: PWM0 1001: I2STX_DOUT 1010: I2SRX0_DIN 1011: I2SRX1_DIN Others: Reserved	R/W	0x0

13.4.28 GPIO39_CTL

GPIO39 control Register
Offset=0XA0

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode	R/W	0x0

		000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved		
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0011: BT_ACCESS 0100: LCD_SEG29 0110: PWM1 1001: I2STX_BCLK 1010: I2SRX0_BCLK 1011: I2SRX1_BCLK Others: Reserved	R/W	0x0

13.4.29 GPIO40_CTL

GPIO40 control Register
Offset=0XA4

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0

5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0011: PTA_GRANT 0100: LCD_SEG30 0110: PWM2 1001: I2STX_MCLK 1010: I2SRX0_MCLK 1011: I2SRX1_MCLK Others: Reserved	R/W	0x0

13.4.30 GPIO42_CTL

GPIO42 control Register
Offset=0xAC

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable	R/W	0x0

		1: Enable		
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0101: I2C_SCL 0110: PWM3 0111: PWM5 1001: I2STX_BCLK 1010: I2SRX0_BCLK 1011: I2SRX1_BCLK 1100: SD0_CLK0 1101: IR_RX 1110: UART1_TX 1111: SD1_DAT1	R/W	0x0

13.4.31 GPIO43_CTL

GPIO43 control Register
Offset=0xB0

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect.	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable; Do not generate IRQ pending and do not send	R/W	0x0

		IRQ to INTC. 1: Enable; Generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.		
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0101: I2C_SDA Others: Reserved	R/W	0x0

13.4.32 GPIO44_CTL

GPIO44 control Register
Offset=0XB4

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6	R/W	0x1

		110: Level 7 111: Level 8		
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(MICINL/ MICINLP)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: DMICCLK Others: Reserved	R/W	0x0

13.4.33 GPIO45_CTL

GPIO45 control Register
Offset=0XB8

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0

4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(MICINR/MICINLN)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: DMICDAT Others: Reserved	R/W	0x0

13.4.34 GPIO46_CTL

GPIO46 control Register
Offset=0XBC

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AUX0L)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO Others: Reserved	R/W	0x0

13.4.35 GPIO47_CTL

GPIO47 control Register
Offset=0XC0

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1	R/W	0x1

		001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AUX0R)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO Others: Reserved	R/W	0x0

13.4.36 GPIO48_CTL

GPIO48 control Register
Offset=0XC4

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0

6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AUX1L)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO Others: Reserved	R/W	0x0

13.4.37 GPIO49_CTL

GPIO49 control Register
Offset=0XC8

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AUX1R)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO Others: Reserved	R/W	0x0

13.4.38 GPIO50_CTL

GPIO50 control Register
Offset=0XCC

Bit (s)	Name	Description	Access	Reset

31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1: Analog Function(AOUTL/AOUTLP)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO Others: Reserved	R/W	0x0

13.4.39 GPIO51_CTL

GPIO51 control Register
Offset=0XD0

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0

7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(VRO)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: I2STX_LRCLK 0010: I2SRX0_LRCLK 0011: I2SRX1_LRCLK 0100: PWM3 Others: Reserved	R/W	0x0

13.4.40 GPIO52_CTL

GPIO52 control Register
Offset=0XD4

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AOUTR / AOUTRP)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO Others: Reserved	R/W	0x0

13.4.41 GPIO53_CTL

GPIO53 control Register
Offset=0XD8

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(VRO_S)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: I2STX_DOUT 0010: I2SRX0_DIN 0011: I2SRX1_DIN 0100: PWM5 Others: Reserved	R/W	0x0

13.4.42 GPIO54_CTL

GPIO54 control Register
Offset=0XDC

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6	R/W	0x1

		110: Level 7 111: Level 8		
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register 0: Digital Function from MFP 1:Analog Function(AUX2L)	R/W	0x1
3:0	MFP	Multi-Function of GPIO 0000: GPIO54 Others: Reserved	R/W	0x0

13.4.43 GPIO55_CTL

GPIO55 control Register
Offset=0XE0

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11:10	-	Reserved	R/W	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	-	Reserved	R	0x0
4	AD_SELECT	GPIO Analog/Digital Select Register	R/W	0x1

		0: Digital Function from MFP 1:Analog Function(AUX2R)		
3:0	MFP	Multi-Function of GPIO 0000: GPIO55 Others: Reserved	R/W	0x0

13.4.44 GPIO_ODAT0

GPIO Output Data register 0
Offset = 0x100

Bit (s)	Name	Description	Access	Reset
31:0	GPIO_ODAT	GPIO[31:0] Output Data.	R/W	0x0

13.4.45 GPIO_ODAT1

GPIO Output Data register 1
Offset = 0x104

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	GPIO_ODAT	GPIO[55:32] Output Data.	R/W	0x0

13.4.46 GPIO_BSR0

GPIO Output Data bit set register 0
Offset = 0x108

Bit (s)	Name	Description	Access	Reset
31:0	GPIO_BSR	GPIO[31:0] Output Data bit set register 0: The corresponding GPIO_ODAT0 bit has no effect； 1: Set the corresponding GPIO_ODAT0 bit to 1； Writing '1' to clear these bits automatically.	R/W	0x0

13.4.47 GPIO_BSR1

GPIO Output Data bit set register 1
Offset = 0x10C

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	GPIO_BSR	GPIO[55:32] Output Data bit set register 0: The corresponding GPIO_ODAT1 bit has no effect； 1: Set the corresponding GPIO_ODAT1 bit to 1； Writing '1' to clear these bits automatically.	R/W	0x0

13.4.48 GPIO_BRR0

GPIO Output Data bit reset register 0
Offset = 0x110

Bit (s)	Name	Description	Access	Reset
31:0	GPIO_BRR	GPIO[31:0] Output Data bit reset register	R/W	0x0

		0: The corresponding GPIO_ODAT0 bit has no effect; 1: Set the corresponding GPIO_ODAT0 bit to 1; Writing '1' to clear these bits automatically.		

13.4.49 GPIO_BRR1

GPIO Output Data bit reset register 1
Offset = 0x114

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	GPIO_BRR	GPIO[55:32] Output Data bit reset register 0: The corresponding GPIO_ODAT1 bit has no effect; 1: Set the corresponding GPIO_ODAT1 bit to 1; Writing '1' to clear these bits automatically.	R/W	0x0

13.4.50 GPIO_IDAT0

GPIO Input Data register 0
Offset = 0x118

Bit (s)	Name	Description	Access	Reset
31:0	GPIO_IDAT	GPIO[31:0] Input Data	R	0x0

13.4.51 GPIO_IDAT1

GPIO Input Data register 1
Offset = 0x11C

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	GPIO_IDAT	GPIO[55:32] Input Data	R	0x0

13.4.52 GPIO_PD0

GPIO IRQ Pending register 0
Offset = 0x120

Bit (s)	Name	Description	Access	Reset
31:0	GPIO_PD	GPIO[31:0] IRQ Pending register 0: No IRQ 1: IRQ Writing '1' to the bit is clear it.	R/W	0x0

13.4.53 GPIO_PD1

GPIO IRQ Pending register 1
Offset = 0x124

Bit (s)	Name	Description	Access	Reset
31:12	-	Reserved	R	0x0
11:0	GPIO_PD	GPIO[43:32] IRQ Pending register 0: No IRQ	R/W	0x0

		1: IRQ Writing '1' to the bit is clear it.		

13.4.54 WIO0_CTL

WIO0 control Register (RTCVDD)
Offset=0x140

Bit (s)	Name	Description	Access	Reset
31:17	-	Reserved	R	0x0
16	WIODAT	WIO Input/Output Data	R/W	0x0
15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x0
11	GPIO2P2KPUEN	GPIO 2.2K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO100KPUEN	GPIO 100K PU Enable 0: Disable 1: Enable	R/W	0x0
7	WIOINEN	WIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	WIOOUTEN	WIO Output Enable 0: Disable 1: Enable	R/W	0x0
5:4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: PMU_32K_OUT 0010: PMU_3M_OUT 0100: 4Hz_OUT 0101: HOSC 1000: LRADC1 Others: Reserved	R/W	0x0

14 Electrical Characteristics

14.1 Absolute Maximum Ratings

Table 14-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	-25	85	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	4000	-	V
Supply Voltage	DC5V	-0.3	9	V
	BAT	-0.3	5	V
	VCC/SVCC/AVCC	-0.3	3.6	V
	VDD	-0.3	1.32	V
Input Voltage	3.3V IO	-0.3	3.6	V
	1.2V IO	-0.3	1.32	V

Note:
Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

14.2 Recommended PWR Supply

Table 14-2 Recommended PWR Supply

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.4	3.8	4.5	V
DC5V	4.5	5.0	7.0	V
VCC/SVCC/AVCC	2.8	3.1	3.4	V
VDD/RTCVDD	1.08	1.2	1.32	V
VREF	--	1.5	--	V
ONOFF	--	--	1.32	V

14.3 DC Characteristics

Table 14-3 DC Parameters for +3.3V IO Pin with Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.8	V	VCC = 3.1V Tamb = -10 to 70 °C
High-level input voltage	VIH	2.0	-	V	
Low-level output voltage	VOL	-	0.4	V	
High-level output voltage	VOH	2.4	-	V	

Table 14-4 DC Parameter for +3.3V IO Pin with Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition
Schmitt trigger positive-going threshold	VT+	-	1.9	V	VCC=3.1V Tamb = -10 to 70 °C
Schmitt trigger negative-going threshold	VT-	1.2	-	V	

14.4 PWR Consumption

Table 14-5 PWR Consumption Table

VDD = 1.2V @ 25°C unless otherwise specified

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
A2DP	Ct	CPU Clock = 8MHz	-	15.5	-	mA
HFP	Cr	DSP Clock = 64MHz	-	16.5	-	mA
Sniff Mode	Cs	500ms	-	-	600	μA
Standby	Cd	Vbat = 3.8V， with RTC	35	-	50	μA

14.5 Bluetooth Characteristics

14.5.1 Transmitter

Table 14-6 Basic Data Rate of Transmitter

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	4	6	dBm
RF PWR Control Step	-	2	4	8	dB
20dB Bandwidth for Modulated Carrier	-	-	914	1500	KHz
Adjacent Channel Transmit	+2 MHz	-	-52	-20	dBm
	-2 MHz	-	-52	-20	dBm
	+3 MHz	-	-56	-40	dBm
	-3 MHz	-	-55	-40	dBm
Frequency Deviation	Δf1avg Maximum Modulation	140	165	175	KHz
	Δf2max Maximum Modulation	115	142		KHz
	Δf1avg/Δf2avg	0.8	0.88		
Initial Carrier Frequency Tolerance	-	-75	5	75	KHz
Frequency Drift	DH1 Packet	-25	7.5	25	KHz
	DH3 Packet	-40	9.4	40	KHz
	DH5 Packet	-40	9.4	40	KHz
Frequency Drift Rate	-	-20	3	20	KHz/50us
Harmonic Content	-	-	-50	-	dBm

Table 14-7 Enhanced Data Rate of Transmitter

Parameter	Condition	Min.	Typ.	Max.	Unit
Relative Transmit PWR(EDR)	P_{DPSK}-P_{GFSK}	-4	-2.5	1	dB
π/4 DQPSK max carrier frequency stability $\|\omega_0\|$	-	-10	1.2	10	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_i\|$	-	-75	-5	75	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_0+\omega_i\|$	-	-75	-3	75	KHz
8DPSK max carrier frequency stability $\|\omega_0\|$	-	-10	5	10	KHz
8DPSK max carrier frequency stability $\|\omega_i\|$	-	-75	-3	75	KHz
8DPSK max carrier frequency stability $\|\omega_0+\omega_i\|$	-	-75	-3	75	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVIN	-	5	20	%
	99% DEVM	99	100	-	%

	Peak DEVM	-	15	35	%
8DPSK Modulation Accuracy	RMS DEVIN	-	4.9	13	%
	99% DEVM	99	100	-	%
	Peak DEVM	-	12.5	25	%
In-band spurious emissions	F > F0 + 3MHz	-	-55	-40	dBm
	F < F0 - 3MHz	-	-52	-40	dBm
	F = F0 + 3MHz	-	-49	-40	dBm
	F = F0 - 3MHz	-	-48	-40	dBm
	F = F0 + 2MHz	-	-39	-20	dBm
	F = F0 - 2MHz	-	-40	-20	dBm
	F = F0 + 1MHz	-	-40	-26	dB
	F = F0 - 1MHz	-	-40	-26	dB
EDR Differential Phase Encoding	-	99	100	-	%

14.5.2 Receiver

Table 14-8 Basic Data Rate of Receiver

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	2.402GHz	-93	-	-89	dBm
	2.441GHz	-93	-	-89	dBm
	2.480GHz	-93	-	-89	dBm
Maximum Input PWR at 0.1% BER	-	-20	-	-	dBm
Co-Channel Interface	-	-	-70	-60	dB
Adjacent Channel Selectivity C/I	$F = F_0 + 1MHz$	-60	-53	-	dB
	$F = F_0 - 1MHz$	-60	-53	-	dB
	$F = F_0 + 2MHz$	-60	-27	-	dB
	$F = F_0 - 2MHz$	-60	-28	-	dB
	$F = F_0 + 3MHz$	-67	-23	-	dB
	$F = F_{image}$	-67	-40	-	dB

Table 14-9 Enhanced Data Rate of Receiver

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.01% BER	π/4 DQPSK 2.402GHz	-92	-	-89	dBm
	π/4 DQPSK 2.441GHz	-92	-	-89	dBm
	π/4 DQPSK 2.480GHz	-92	-	-89	dBm
	8DPSK 2.402GHz	-86	-	-83	dBm
	8DPSK 2.441GHz	-86	-	-83	dBm
	8DPSK 2.480GHz	-86	-	-83	dBm
Maximum Input PWR at 0.1% BER	π/4 DQPSK	-20	0		dBm
	8DPSK	-20	0		dBm
Co-Channel Interference	π/4 DQPSK		3	13	dB
	8DPSK		5	21	dB

14.6 Audio ADC

Table 14-10 Audio ADC Parameters

Pre-Amplifier					
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Full Scale Input Voltage	THD+N < 1%		-	-	2.8	Vpp
Analogue gain	AUX OP	-	-12	-	7.5	dB
	MIC OP	Single Ended	26	-	39	dB

		Full Differential	32	-	45	
Analogue to Digital Converter						
Resolution	-		-	-	20	Bits
Input Sample Rate	-		8	-	96	kHz
SNR	fin = 1kHz@Full Scale Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	96	-	dB
Dynamic Range	fin = 1kHz@-40dBFS Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	94	-	dB
THD+N	fin = 1kHz(input=1.6Vpp) B/W = 22Hz~22kHz Fs=48kHz		-	-85	-	dB
Digital gain	-		0	-	45	dB

14.7 Stereo DAC

Table 14-11 Stereo DAC Parameters

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	20	Bits
Output Sample Rate	-		8	-	96	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	98	-	dB
		A-Weighting	-	101	-	dBA
Dynamic Range	fin = 1kHz@-48dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	98	-	dB
		A-Weighting	-	101	-	dBA
THD+N	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	-87	-	dB
Digital gain	-		<-98	-	24	dB
Stereo crosstalk	fin = 1kHz@0dBFS input	-	-	-78	-	dB
PWR Amplifier						
Analogue gain	-		-96	-	0	dB
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Single Ended Output	-	-	550	mVrms
			-	-	18.5	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Full Differential Output	-	-	51	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=10KΩ	Full Differential Output	-	-	1.9	Vrms

15 Device Marking of the Chipset

16 Reflow Solder Information

The ATS2837 is constructed with all RoHS compliant material and should be reflowed accordingly. This chip is Moisture Sensitivity Level MSL4 and must be stored and handled accordingly.

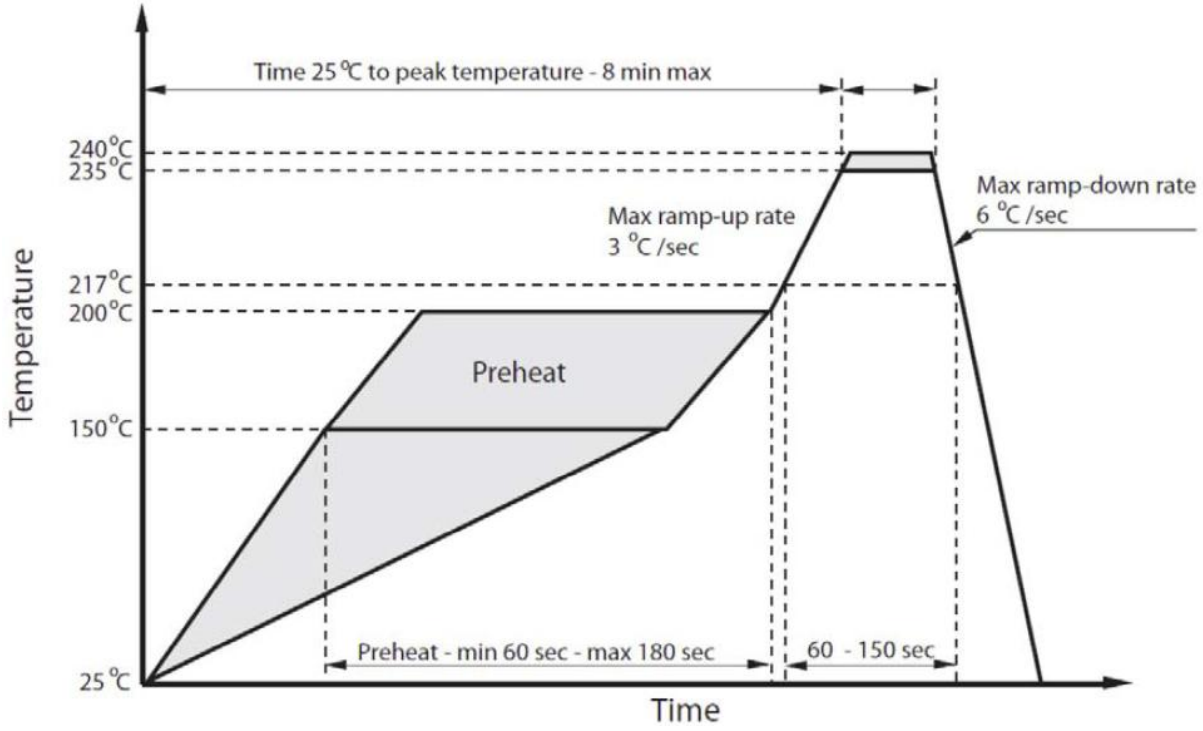


Figure 16-1 Typical Reflow Solder Profile

17 Ordering Information

Part Number	Package	Package Size	Packing Method	MOQ
ATS2837 (MCP 16M bits pSRAM)	QFN68	8mm x 8mm x 0.85mm	Tray	3480

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	acoustic echo cancellers
ADC	Analog-to-Digital-Converter
ALU	Arithmetic Logic Unit
CC	Constant Current
CP0	Control Coprocessor 0
DAC	Digital-to-Analog-Converter
DMA	Direct Memory Access
GPIO	General Purpose Input Output
HOSC	High Frequency OSC
HCL	High Frequency Calibration Low Frequency
INTC	Interrupt Controller
IRQ	Interrupt Request
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LOSC	Internal Low Frequency OSC
Matrix_led	Matrix LED (7-pin LED)
MIC	Microphone
MMU	Memory Management Unit
MFP	Multiple Function PAD
NMI	Nonmaskable Interrupt
OSC	Oscillator
PA	Power Amplifier
Seg-lcd	Segment LCD
UTMI	USB Transceiver Macro Interface

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