## Features

- **Three DSPs and 24-bit Audio Router On-chip**
- **32 kHz to 96 kHz Sampling Rate**
- **16-bit Microcontroller On-chip**
- **Variety of I/Os, including SmartMedia™ and DataFlash®**
- **Embedded RAM for Single Chip Operation (530 Kbits)**
- **Warm Start Power-down**
- **1 µA Typical Deep Power-down, 0.5 mW/MIPS Typical Operating**
- **External Flash/ROM Capability**
- **Available in a 100-lead TQFP Package**
- **Ideal for Real-time Audio Applications**
  - **Wavetable Synthesis (GM-Lite)**
  - **MP3 Decoding**
  - **Effect Processing (Reverb, Echo, Chorus, etc.)**
  - **Filtering, Sampling Rate Conversion**
- **Typical Applications: Cellular Phones, MP3 Player, Musical Instruments, Consumer Electronic, Professional Audio**

## Description

The ATSAM3303 is a member of the new ATSAM3000 family that uses the DSP array technology. The ATSAM3303 includes three 24-bit DSPs, a 24-bit Audio Router and a general-purpose 16-bit on-chip CISC microcontroller. Its high performance and flexibility allow implementation of professional-quality audio applications, such as MP3 decoding, Wavetable synthesis, effect processing and mixing. A variety of I/Os, including external Wave ROM, SmartMedia and DataFlash are provided. Sampling rates up to 96 kHz at 24 bits are supported.

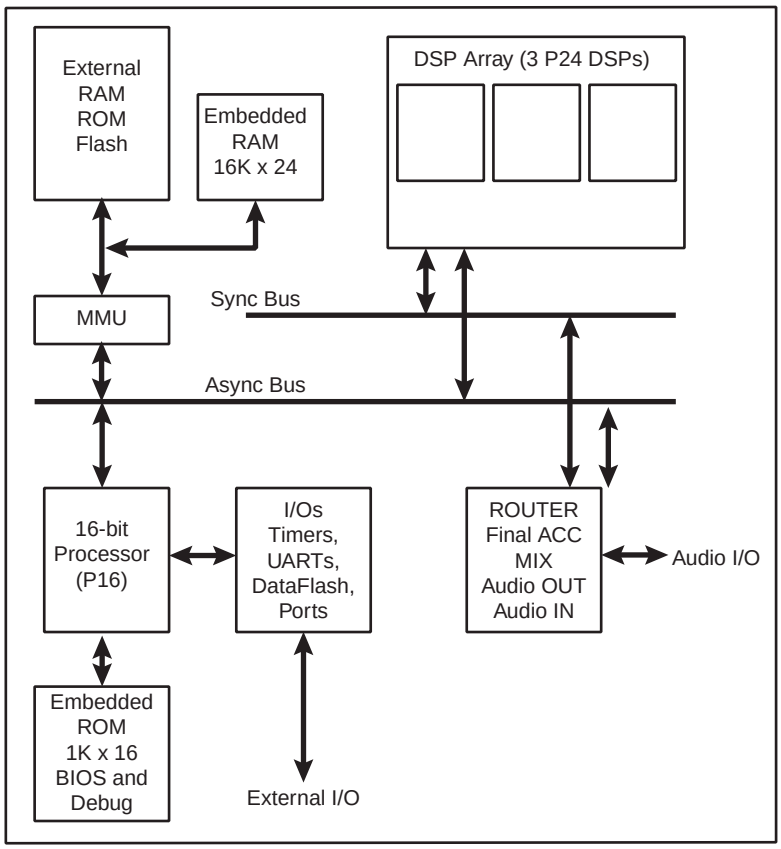
# Audio Processing

# ATSAM3303 GM-Lite Synthesizer/ Professional Effects DSP

6091A–DRMSD–07/04

## DSP Array Block Diagram

**Figure 1.** ATSAM3303 DSP Array Block Diagram




## Functional Description

### DSP Array

The ATSAM3303 includes three on-chip DSPs.

Each DSP (P24) is built around a 2K x 24 RAM and a 1K x 24 ROM. The RAM contains both data and P24 instructions; the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data such as compressed audio through the Async Bus. Each P24 RAM can be accessed through the Async Bus.

Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop.

One P24 is sufficient for processing one channel of MP3, implementing a multi-tap delay line or a multi-tap transversal filter. A single P24 is also capable of generating 12 voices of wavetable sound at 32 kHz sampling rate (8 voices at 48 kHz), including sample cache, pitch control, second-order filter and two envelope generators.

### Sync Bus

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48, 96 kHz. Each frame is divided into 64 time slots. Each slot is divided into 4 bus cycles. Each P24 is assigned a hardwired time slot (8 to 63), during which it may provide 24-bit data to the bus (up to 4 data samples). Each P24 can read data on the bus at any time,

allowing inter P24 communication at the current sampling rate. Slots 0 to 7 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

### Async Bus

The Async Bus is 24-bit data inside the chip and 16-bit outside.

The P16 processor normally masters the Async Bus, it can read/write the P24 memories and the external or embedded ROM/RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX allow to convert fixed point DSP data to floating point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

### 16-bit Processor

The P16 processor is widely used in ATSAM products. Using the P16 allows to keep the large firmware investments from the SAM97xx series. A built-in ROM, connected to the P16, holds basic input/output software (BIOS) for peripherals such as UART, DataFlash®, SmartMedia®, MPU, as well as a debugger using a dedicated asynchronous serial line. The firmware can reside on external parallel ROM/Flash or it can be downloaded at power-up into the built-in 16K x 24 RAM from serial EEPROM, DataFlash, SmartMedia or host.

### MMU (Memory Management Unit)

The MMU handles transfer requests between the external or embedded RAM/ROM, the P16 and the P24s through the Async Bus. The ATSAM3303 includes an on-chip 16K x 24 RAM.

### Router: Final ACC, MIX, Audio Out, Audio In

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. Eight channels of audio in and eight channels of audio out are provided (4 stereo in/out, I2S format). The stereo audio in channels may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

### I/O

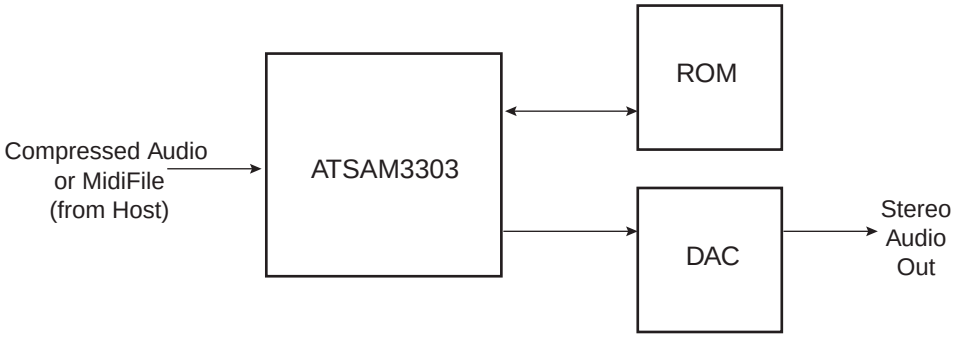
The ATSAM3303 includes versatile I/Os that share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.

The following peripherals are included on-chip:

- 2 x 8-bit timers
- 2 x 16-bit timers
- Parallel slave 8-bit port, MPU401 compatible
- Parallel master 8-bit port, for connection to SmartMedia and/or LCD display, switches, etc.
- 2 x asynchronous bi-directional serial ports
- Synchronous serial slave port (SPI type host connection)
- SPI master bi-directional port for EEPROM or DataFlash connection
- Firmware controlled I/O pins

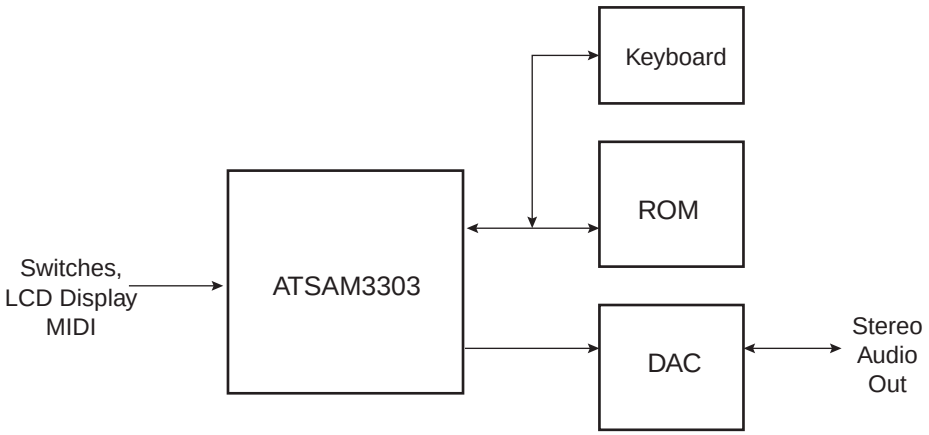
## Typical Application Examples

**Figure 2.** Host-controlled MP3 or Cost-optimized GM-Lite Wavetable Player (Cellular Phone)




- MP3 or Wavetable synthesis (switchable “on the fly”)
- Legendary Dream high-quality wavetable sound
- Typical polyphony
  - 36 voices @ 32 kHz sampling rate
  - 24 voices with effects (reverb, chorus, etc.)
- External wavetable ROM/Flash choice from 4 Mbits to 128 Mbits
- Choice of host communication interfaces
  - 8-bit parallel
  - Asynchronous serial (MIDI)
  - Synchronous serial (SPI)
- Built-in Standard Midi file player (SMF) dramatically reduces host load

**Figure 3.** Ultra Low-cost Musical Keyboard




- 24-voice polyphony with effects @ 32 kHz sampling rate
- Choice of GM+ sampled sounds from 4 Mbits to 64 Mbits
- Maximum external memory addressing range: 128 Mbits

# DSP Capacity and I/O Configuration

## DSP Considerations

The ATSAM3303 includes three P24 DSPs.

Table 1 lists the performance levels achievable by the P24.

**Table 1.** P24 Performance Levels

| Function | P24s Required |
|---|---|
| MP3 decode | 3 |
| 12-voice wavetable synthesis @32kHz | 1 |
| 8-voice wavetable synthesis @48kHz | 1 |
| Stereo reverb and chorus @48kHz | 1 |
| 31-band equalizer @96kHz | 3 |
| Stereo 31-band equalizer @48kHz | 3 |

The ATSAM3303 runs firmware directly from an external ROM/Flash memory. It may also run firmware from local RAM, thus freeing many I/O pins, which can then be used for application-dependent functions. The ATSAM3303 is the ideal choice when wavetable synthesis or many I/O pins are required.

## I/O Selection Considerations

I/Os are organized in groups that can be mutually exclusive because they share the same IC pins (please refer to the pinout to identify the exclusions). The two main types of operation are host controlled and stand-alone.

### Host-controlled Operation

There are three main possible ways of communication with a host processor:

- 8-bit parallel MPU type bi-directional interface signals: D7-D0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, IRQ
- Asynchronous serial, MIDI_IN and, optionally, MIDI_OUT
- Synchronous serial signals: SDIN, SCLK, SYNC, $\overline{INT}$

### Stand-alone Operation

Possible stand-alone modes are:

- Firmware into external ROM or Flash memory
- Firmware into external EEPROM or DataFlash
- Firmware into external SmartMedia. In this case, the firmware should reside in the SmartMedia reserved sectors starting at sector 1.

# Pinout

## Pin Description

- Identical sharing number indicates multifunction pins.
- Pd indicates a pin with built-in pull-down resistor.
- Pu indicates a pin with built-in pull-up resistor.

**Table 2.** Pinout by Pin Name

| Pin Name | Pin Number | Type | Sharing | Description |
|---|---|---|---|---|
| GND | 9, 22, 30, 41, 56, 70, 75, 87, 97 | PWR | - | Digital ground. All these pins should be returned to a ground plane |
| VC18 | 20, 47, 73, 99 | PWR | - | Core power. All these pins should be returned to nominal 1.8V or to PWROUT if the built-in power switch is used. |
| VC33 | 13, 50, 83 | PWR | - | Periphery power. All these pins should be returned to nominal 3.3V. |
| PWRIN | 29 | PWR | - | Power switch input; should be returned to nominal 1.8V even if the power switch is not used |
| PWROUT | 28 | PWR | - | Power switch output; should be connected to all VC18 pins if the power switch is used |
| D7 - D0 | 96, 95, 91, 90, 82, 81, 77, 76 | I/O | 1 | Slave 8-bit interface data. Output if $\overline{CS}$ and $\overline{RD}$ are low (read from chip), input if $\overline{CS}$ and $\overline{WR}$ are low (write to chip). Type of data defined by A0 input. |
| I/O7 - I/O0 | 96, 95, 91, 90, 82, 81, 77, 76 | I/O | 1 | SmartMedia data or other peripheral data |
| P0.7 - P0.0 | 96, 95, 91, 90, 82, 81, 77, 76 | I/O | 1 | General-purpose I/O; can be programmed individually as input or output |
| CLAD3 - 0 | 96, 95, 91, 90 | In | 1 | Optional bit clocks for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif. |
| WSAD3 - 0 | 82, 81, 77, 76 | In | 1 | Optional word selects for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif. |
| A0 | 98 | In | 2 | Slave 8-bit interface address. Indicates data/status or data/ctrl transfer type ($\overline{CS}$/ $\overline{RD}$ low or $\overline{CS}$/$\overline{WR}$ low) |
| SMPD | 98 | In | 2 | SmartMedia presence detect |
| P0.10 | 98 | In | 2 | General-purpose input pin |
| SCLK | 98 | In | 2 | Serial slave synchronous interface input clock |
| $\overline{CS}$ | 100 | In | 3 | Slave 8-bit interface chip select, active low |
| P0.11 | 100 | In | 3 | General-purpose input pin |
| SYNC | 100 | In | 3 | Serial slave synchronous interface input sync signal |
| $\overline{WR}$ | 1 | In | 4 | Slave 8-bit interface write, active low. D7 - D0 data is sampled by chip on $\overline{WR}$ rising edge if $\overline{CS}$ is low |
| $\overline{SMC}$ | 1 | In | 4 | SmartMedia configuration. This pin is sensed after power-up. If found low, it is assumed that a SmartMedia connector is present. The built-in firmware will wait for SmartMedia SMPD. |
| P0.12 | 1 | In | 4 | General-purpose input pin |

**Table 2.** Pinout by Pin Name

| Pin Name | Pin Number | Type | Sharing | Description |
|---|---|---|---|---|
| $\overline{RD}$ | 2 | In | 5 | Slave 8-bit interface read, active low. D7 - D0 data is output when $\overline{RD}$ goes low and $\overline{CS}$ is low |
| $\overline{R\|B}$ | 2 | In | 5 | SmartMedia Ready Busy/ status |
| P0.13 | 2 | In | 5 | General-purpose input pin |
| IRQ | 8 | Out | 6 | Slave 8-bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host ($\overline{CS}$ = 0 and $\overline{RD}$ = 0) |
| $\overline{SMRE}$ | 8 | Out | 6 | SmartMedia read enable ($\overline{RE}$), active low |
| FS0 | 8 | In | 6 | Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1). |
| P0.8 | 8 | I/O | 6 | General-purpose I/O pin |
| $\overline{INT}$ | 8 | Out | 6 | Serial slave synchronous interface data request, active low |
| MIDI_IN | 17 | In | 7 | Serial MIDI in |
| P0.14 | 17 | In | 7 | General-purpose input pin |
| SDIN | 17 | In | 7 | Serial slave synchronous interface input data |
| MIDI_OUT | 18 | Out | 8 | Serial MIDI out |
| FS1 | 18 | In | 8 | Freq sense, sensed at power up. FS1/FS0 allow firmware to know operating frequency of chip as follows:<br>00 6.9552 MHz<br>01 9.6 MHz<br>10 11.2896 MHz<br>11 12.288 MHz |
| P0.9 | 18 | I/O | 8 | General-purpose I/O |
| DABD3 - 0 | 67, 66, 65, 64 | Out | - | Four stereo channels of digital audio output, I2S format |
| CLBD | 6 | Out | - | Audio bit clock for DABD3 - 0. Audio bit clock for DAAD3 - 0 if the corresponding CLAD3 - 0 is not used. |
| WSBD | 7 | Out | - | Audio left/right channel select for DABD3 - 0. Audio left/right channel for DAAD3 - 0 if the corresponding WSAD3 - 0 is not used. |
| CKOUT | 5 | Out | - | External DAC/Codec master clock. Same frequency as X2 pin. Can be programmed to be 128 x Fs, 192 x Fs, 256 x Fs, 384 x Fs, where Fs is the DAC/Codec sampling rate. |
| DAAD0 | 54 | In | 9 | Stereo audio data input, I2S format. Can operate on CLBD master rate or CLAD0 external rate when sampling rate conversion is requested. |
| P0.15 | 54 | In | 9 | General-purpose input pin |
| DAAD3 - 1 | 60, 59, 55 | In<br>Pd | - | Three additional channels of stereo audio input, I2S format. Can individually operate on CLBD master rate or corresponding CLAD3 - 1 when sampling rate conversion is requested.<br>DAAD3 - 1 have built-in pull-downs. They may be left open if not used. |
| MUTE | 19 | I/O | 10 | External DAC/Codec Mute. Sensed at power up. If found high, then MUTE becomes an active high output. If found low, then MUTE becomes an active low output. |
| P1.6 | 19 | I/O | 10 | General-purpose I/O pin |
| WA21 | 45 | Out | 11 | External memory address bit, extension to 64 Mbits |

**Table 2.** Pinout by Pin Name

| Pin Name | Pin Number | Type | Sharing | Description |
|---|---|---|---|---|
| $\overline{\text{SMCE}}$ | 45 | Out | 11 | SmartMedia chip enable ($\overline{\text{CE}}$), active low |
| P1.5 | 45 | I/O | 11 | General-purpose I/O pin |
| WA20 | 44 | Out | 12 | External memory address bit, extension to 32 Mbits |
| SMALE | 44 | Out | 12 | SmartMedia address latch enable (ALE) |
| P1.4 | 44 | I/O | 12 | General-purpose I/O pin |
| WA19 | 43 | Out | 13 | External memory address bit, extension to 16 Mbits |
| $\overline{\text{SMWE}}$ | 43 | Out | 13 | SmartMedia write enable ($\overline{\text{WE}}$), active low |
| P1.3 | 43 | I/O | 13 | General-purpose I/O pin |
| WA18 | 42 | Out | 14 | External memory address bit, extension to 8 Mbits |
| SMCLE | 42 | Out | 14 | SmartMedia command latch enable (CLE) |
| P1.2 | 42 | I/O | 14 | General-purpose I/O pin |
| WA17 - WA16 | 58, 57 | Out | 15 | External memory address bits, extension to 2 and 4 Mbits |
| P1.1 - P1.0 | 58, 57 | I/O | 15 | General-purpose I/O pins |
| WA15 - WA0 | 53, 51, 40, 39, 38, 37, 36, 27, 26, 21, 16, 15, 14, 12, 11, 10 | Out | 16 | External memory address bits, up to 1 MBits (64K x 16) |
| P2.15 - P2.0 | 53, 51, 40, 39, 38, 37, 36, 27, 26, 21, 16, 15, 14, 12, 11, 10 | I/O | 16 | General-purpose I/O pins |
| WD15 - WD0 | 94, 93, 92, 89, 88, 86, 85, 84, 80, 79, 78, 69, 68, 63, 62, 61 | I/O | 17 | External memory data |
| P3.15 - P3.0 | 94, 93, 92, 89, 88, 86, 85, 84, 80, 79, 78, 69, 68, 63, 62, 61 | I/O | 17 | General-purpose I/O pins |
| $\overline{\text{WCS1}}$ | 3 | Out | 18 | External memory chip select 1, active low. Pre-decode for an external RAM/Flash/ROM at address 200:0000H. |
| P1.10 | 3 | I/O | 18 | General-purpose I/O pin |
| $\overline{\text{WCS0}}$ | 4 | Out | 19 | External memory chip select 2, active low. Pre-decode for an external RAM/Flash/ROM at address 000:0000H |
| P1.9 | 4 | I/O | 19 | General-purpose I/O pin |
| $\overline{\text{WOE}}$ | 48 | Out | 20 | External memory output enable, active low |
| P1.8 | 48 | I/O | 20 | General-purpose I/O pin |
| $\overline{\text{WWE}}$ | 49 | Out | 21 | External memory write enable, active low |
| P1.7 | 49 | I/O | 21 | General-purpose I/O pin |
| $\overline{\text{DFCS}}$ | 23 | Out | - | DataFlash chip select |
| DFSI | 25 | Out | - | DataFlash serial input (to DataFlash) |
| DFSO | 32 | In Pd | - | DataFlash serial output (from DataFlash). This pin has a built-in pull-down. It may be left open if not used. |
| DFSCK | 24 | Out | - | DataFlash data clock |

**Table 2.** Pinout by Pin Name

| Pin Name | Pin Number | Type | Sharing | Description |
|---|---|---|---|---|
| P1.15 | 46 | I/O<br>Pu | - | General-purpose I/O pin. This pin has built-in pull-up. It may be left open if not used. |
| X1 - X2 | 72, 71 | - | - | External crystal connection. Standard frequencies are 6.9552 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. $1.8V_{PP}$) can be connected to X1 using AC coupling (22 pF). A built-in PLL multiplies the clock frequency by 4 for internal use. |
| LFT | 74 | - | - | PLL decoupling RCR filter |
| $\overline{\text{RESET}}$ | 33 | In | - | Master reset Schmitt trigger input, active low. $\overline{\text{RESET}}$ should be held low during at least 5ms after power is applied. On the rising edge of $\overline{\text{RESET}}$, the chip enters an initialization routine, which may involve firmware download from an external SmartMedia, DataFlash or host. |
| STIN | 34 | In<br>Pd | - | Serial test input. This is a 57.6 Kbaud asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation. |
| STOUT | 35 | Out | - | Serial test output. 57.6 Kbaud async output used for firmware debugging. |
| $\overline{\text{PDWN}}$ | 31 | In | - | Power down input, active low. High level on this pin is typ. VC18. When $\overline{\text{PDWN}}$ is low, the oscillator and PLL are stopped, the power switch opens, and the chip enters a deep sleep mode (1 µA typ. consumption when power switch is used). To exit from power down, $\overline{\text{PDWN}}$ has to be set high then $\overline{\text{RESET}}$ applied. Alternate programmable power-downs are available which allow warm restart of the chip. |
| TEST | 52 | In<br>Pd | - | Test input. Should be grounded or left open. |

## Pinout by Pin Number

**Table 3.** ATSAM3303 Pinout by Pin Number

| Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{WR}$ $\overline{SMC}$ P0.12 | 26 | WA7 P2.7 | 51 | WA14 P2.14 | 76 | D0 I/O0 P0.0 WSAD0 |
| 2 | $\overline{RD}$ R$\overline{B}$ P0.13 | 27 | WA8 P2.8 | 52 | TEST | 77 | D1 I/O1 P0.1 WSAD1 |
| 3 | $\overline{WCS1}$ P1.10 | 28 | PWROUT | 53 | WA15 P2.15 | 78 | WD5 P3.5 |
| 4 | $\overline{WCS0}$ P1.9 | 29 | PWRIN | 54 | DAAD0 P0.15 | 79 | WD6 P3.6 |
| 5 | CKOUT | 30 | GND | 55 | DAAD1 | 80 | WD7 P3.7 |
| 6 | CLBD | 31 | $\overline{PDWN}$ | 56 | GND | 81 | D2 I/O2 P0.2 WSAD2 |
| 7 | WSBD | 32 | DFSO | 57 | WA16 P1.0 | 82 | D3 I/O3 P0.3 WSAD3 |
| 8 | IRQ | 33 | $\overline{RESET}$ | 58 | WA17 P1.1 | 83 | VC33 |
| 9 | GND | 34 | STIN | 59 | DAAD2 | 84 | WD8 P3.8 |
| 10 | WA0 P2.0 | 35 | STOUT | 60 | DAAD3 | 85 | WD9 P3.9 |
| 11 | WA1 P2.1 | 36 | WA9 P2.9 | 61 | WD0 P3.0 | 86 | WD10 P3.10 |
| 12 | WA2 P2.2 | 37 | WA10 P2.10 | 62 | WD1 P3.1 | 87 | GND |
| 13 | VC3 | 38 | WA11 P2.11 | 63 | WD2 P3.2 | 88 | WD11 P3.11 |
| 14 | WA3 P2.3 | 39 | WA12 P2.12 | 64 | DABD0 | 89 | WD12 P3.12 |
| 15 | WA4 P2.4 | 40 | WA13 P2.13 | 65 | DABD1 | 90 | D4 I/O4 P0.4 CLAD0 |
| 16 | WA5 P2.5 | 41 | GND | 66 | DABD2 | 91 | D5 I/O5 P0.5 CLAD1 |
| 17 | MIDI_IN P0.14 SDIN | 42 | WA18 SMCLE P1.2 | 67 | DABD3 | 92 | WD13 P3.13 |
| 18 | MIDI_OUT FS1 P0.9 | 43 | WA19 $\overline{SMWE}$ P1.3 | 68 | WD3 P3.3 | 93 | WD14 P3.14 |
| 19 | MUTE P1.6 | 44 | WA20 SMALE P1.4 | 69 | WD4 P3.4 | 94 | WD15 P3.15 |
| 20 | VC18 | 45 | WA21 $\overline{SMCE}$ P1.5 | 70 | GND | 95 | D6 I/O6 P0.6 CLAD2 |
| 21 | WA6 P2.6 | 46 | P1.15 | 71 | X2 | 96 | D7 I/O7 P0.7 CLAD3 |
| 22 | GND | 47 | VC18 | 72 | X1 | 97 | GND |
| 23 | $\overline{DFCS}$ | 48 | $\overline{WOE}$ P1.8 | 73 | VC18 | 98 | A0 SMPD P0.10 SCLK |
| 24 | DFSCK | 49 | $\overline{WWE}$ P1.7 | 74 | LFT | 99 | VC18 |
| 25 | DFSI | 50 | VC33 | 75 | GND | 100 | $\overline{CS}$ P0.11 SYNC |

## Mechanical Dimensions

**Figure 4.** Thin Plastic 100-lead Quad Flat Pack (TQFP100B)

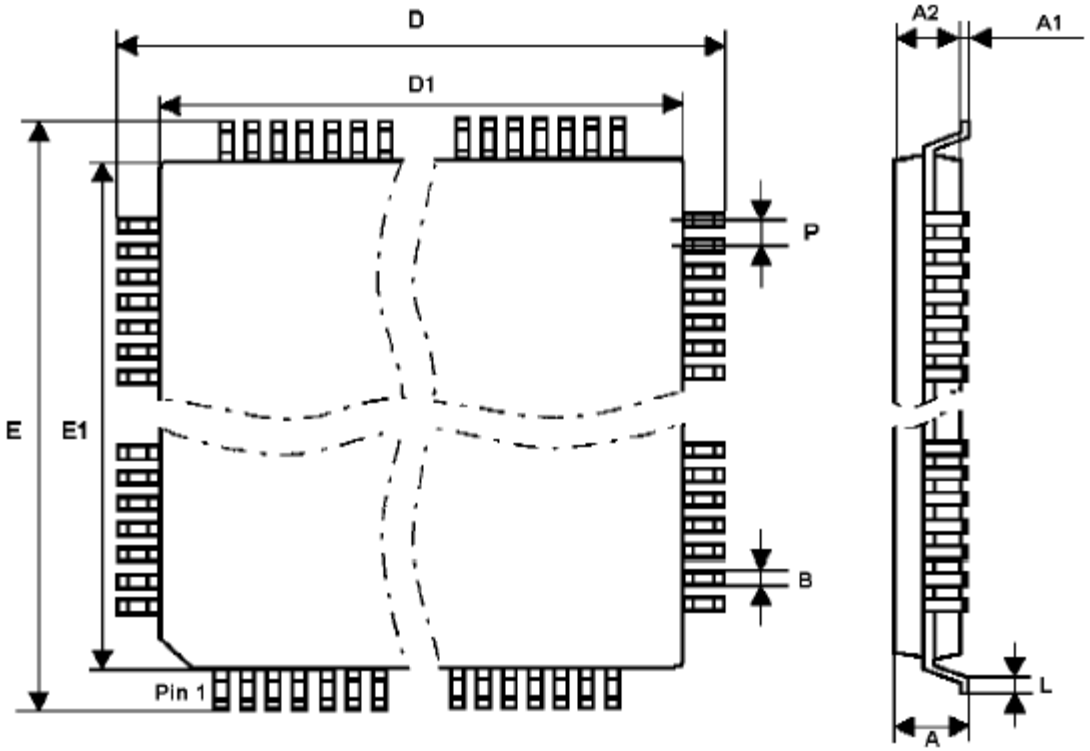



**Table 4.** Package Dimensions in mm

| Denomination | Min | Nom | Max |
|---|---|---|---|
| A | 1.40 | 1.50 | 1.60 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| L | 0.45 | 0.60 | 0.75 |
| D | | 14.00 | |
| D1 | | 12.00 | |
| E | | 14.00 | |
| E1 | | 12.00 | |
| P | | 0.40 | |
| B | 0.13 | 0.18 | 0.23 |

# Electrical Characteristics

## Absolute Maximum Ratings(*)

| | |
|---|---|
| Ambient Temperature (power applied).....-40°C to 85°C<br><br>Storage Temperature.....-65°C to 150°C<br><br>Voltage on any pin<br>X1, LFT..... -0.3 to $V_{C18}$ + 0.3V<br>Others..... -0.3 to $V_{C33}$ + 0.3V<br><br>Supply Voltage.....<br>$V_{C18}$.....-0.3V to 1.95V<br>$V_{C3}$.....-0.3V to 3.6V<br><br>Maximum IOL per I/O pin..... 4 mA | *NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. |

## Recommended Operating Conditions

**Table 5.** Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{C18}$ | Supply voltage | 1.65 | 1.8 | 1.95 | V |
| $V_{C33}$ | Supply voltage(1) | 3 | 3.3 | $V_{C18}$ + 1.5<br>3.6 | V |
| PWRIN | Supply voltage PWRIN pin | 1.75 | 1.9 | 1.95 | V |
| $T_A$ | Operating ambient temperature | 0 | - | 70 | °C |

Note: 1. Operation at lower $V_{C33}$ values down to $V_{C18}$ is possible, however external timing may be impaired. Please contact Atmel if you plan to use these circuits with $V_{C33}$ outside the recommended operating range.

## DC Characteristics

**Table 6.** DC Characteristics ($T_A$ = 25°C, $V_{C18}$ = 1.8V ± 10%, $V_{C33}$ = 3.3V ± 10%)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Low level input voltage | -0.3 | - | 1.0 | V |
| $V_{IH}$ | High level input voltage, except X1, $\overline{PDWN}$ | 2.3 | - | $V_{C33}$ + 0.3 | V |
| $V_{IH}$ | High level input voltage X1, $\overline{PDWN}$ | 1.2 | - | $V_{C18}$ + 0.3 | V |
| $V_{OL}$ | Low level output voltage $I_{OL}$=-2 mA | - | - | 0.4 | V |
| $V_{OH}$ | High level output voltage $I_{OH}$ = 2 mA | 2.9 | - | - | V |
| $I_{CC1}$ | $V_{C18}$ power supply current (crystal freq.=11.2896 MHz, all 3 P24s running) | - | 40 | - | mA |
| $I_{CC2}$ | $V_{C18}$ power supply current (crystal freq. = 11.2896 MHz, all P24s stopped) | - | 22 | - | mA |
| $I_{CC3}$ | $V_{C18}$ power supply current (crystal freq. = 11.2896 MHz, all P24s stopped, warm start power-down active) | - | 4 | - | mA |
| $I_{CC4}$ | $V_{C18}$ deep power down supply current (using power switch) | - | 1 | 10 | µA |
| PU/PD | Built-in pull-up/pull-down resistor | 10 | - | 56 | kOhm |

## Slave 8-bit Parallel Interface

Pins used: D7-D0 (I/O), $\overline{CS}$ (input), A0 (input), $\overline{WR}$ (input), $\overline{RD}$ (input), IRQ (output).

This interface is typically used to connect the chip to a host processor.

**Figure 5.** Host Interface Read Cycle

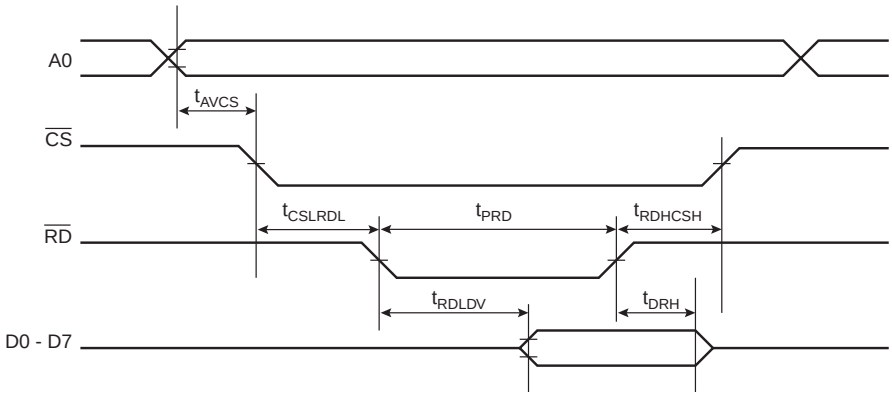



**Figure 6.** Host Interface Write Cycle

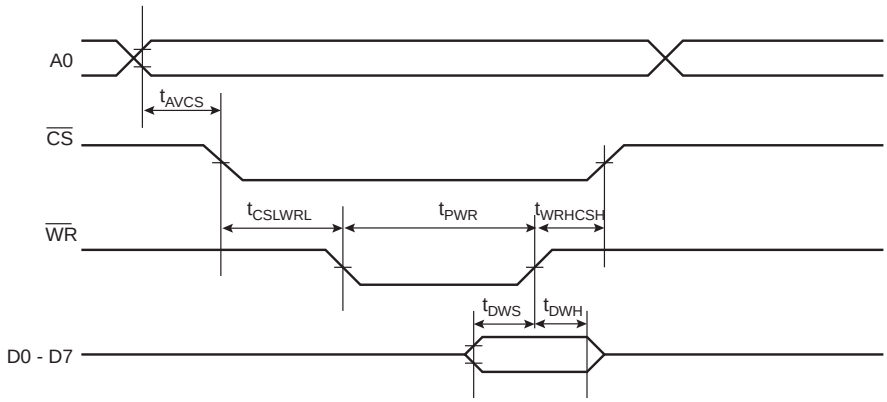



**Table 7.** Timing Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{AVCS}$ | Address valid to chip select low | 0 | - | - | ns |
| $t_{CSLRDL}$ | Chip select low to $\overline{RD}$ low | 5 | - | - | ns |
| $t_{RDHCSH}$ | $\overline{RD}$ high to $\overline{CS}$ high | 5 | - | - | ns |
| $t_{PRD}$ | $\overline{RD}$ pulse width | 50 | - | - | ns |
| $t_{RDLDV}$ | Data out valid from $\overline{RD}$ | - | - | 20 | ns |
| $t_{DRH}$ | Data out hold from $\overline{RD}$ | 5 | - | 10 | ns |
| $t_{CSLRWRL}$ | Chip select low to $\overline{WR}$ low | 5 | - | - | ns |
| $t_{WRHCSH}$ | $\overline{WR}$ high to $\overline{CS}$ high | 5 | - | - | ns |
| $t_{PWR}$ | $\overline{WR}$ pulse width | 50 | - | - | ns |
| $t_{DWS}$ | Write data setup time | 10 | - | - | ns |
| $t_{DWH}$ | Write data hold time | 0 | - | - | ns |

**IO Status Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TE | RF | X | X | X | X | X | X |

Status register is read when A0 = 1, $\overline{RD}$ = 0, $\overline{CS}$ = 0.

- **TE: Transmit empty**

If 0, data from ATSAM3303 to host is pending and IRQ is high. Reading the data at A0 = 0 will set TE to 1 and clear IRQ.

- **RF: Receiver full**

If 0, then ATSAM3303 is ready to accept DATA from host.

Note: If status bit RF is not checked by host, write cycle time should not be lower than 3 µs.

## SmartMedia and Other Peripheral Interfaces

This is a master 8-bit parallel interface, allowing connection to SmartMedia or other peripherals such as LCD screens.

Pins used: I/O7-I/O0 (I/O), SMPD (input), $\overline{SMCE}$, SMALE, SMCLE, $\overline{SMRE}$, $\overline{SMWE}$ (outputs)

All these pins are fully under firmware control, therefore timing compatibility is ensured by firmware only.

## EEPROM/DataFlash Interface

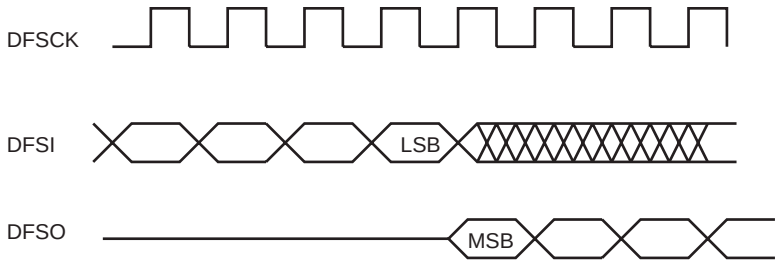
This is a master synchronous serial interface, operating in SPI mode 0.

Pins used: $\overline{DFCS}$, DFSI, DFSCK (outputs), DFSO (input)

The DFSCK frequency is firmware programmable from fck to fck/64, where fck is the crystal frequency. Thus a large variety of EEPROM/DataFlash devices can be accomodated.

Please refer to Atmel DataFlash datasheets for accurate SPI mode 0 timing.

**Figure 7.** Typical DataFlash Interface Timing



## Serial Slave Synchronous Interface

The ATSAM3303 can be controlled by an external host processor through the unidirectional serial interface. However, no firmware can be downloaded at power-up through this interface. Therefore an external ROM/Flash/EEPROM is required.

Pins used: SCLK, SYNC, SDIN (input), $\overline{INT}$ (output)

Data is shifted MSB first. The IC samples an incoming SDIN bit on the rising edge of SCLK, therefore the host should change SDIN on the negative SCLK edge.

SYNC allows initial synchronization. The rising edge of SYNC, which should occur with SCLK low, indicates that SDIN will hold MSB data on the next rising SCLK.

The data is stored internally in a 256-byte FIFO.

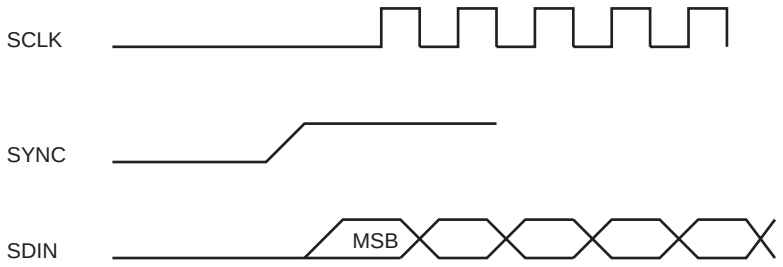
When the FIFO count is below 64, the $\overline{INT}$ output goes low. This allows the host processor to send data in burst mode.

The maximum SCLK frequency is fck (fck being the crystal frequency).

The minimum time between two bytes is 64 fck periods.

The contents of the SDIN data are defined by the firmware.

**Figure 8.** Serial Slave Interface Typical Timing




## Digital Audio

Pins used: CLBD (output), WSBD (output), DABD3 - 0 (outputs), DAAD3 - 0 (inputs)

Optionally: CLAD3 - 0 (inputs), WSAD3 - 0 (inputs)

The ATSAM3303 allows for 8 digital audio output channels and 8 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD3 - 0 inputs can be synchronized with incoming CLAD3 - 0 and WSAD3 - 0 signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S standard, with up to 24 bits per sample

**Figure 9.** Digital Audio

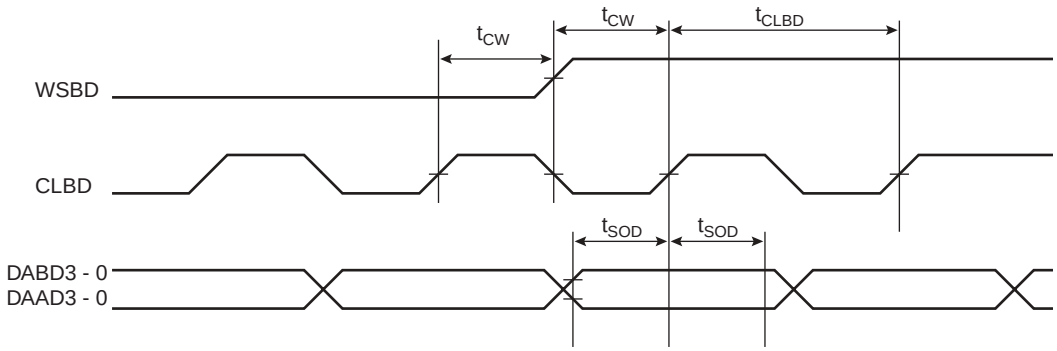



**Table 8.** Digital Audio Timing Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CW}$ | CLBD rising to WSBD change | $t_C$ - 10 | | | ns |
| $t_{SOD}$ | DABD valid prior/after CLBD rising | $t_C$ - 10 | | | ns |
| $t_{CLBD}$ | CLBD cycle time | | 2 * $t_C$ | | ns |

$t_C$ is related to $t_{CK}$, the crystal period at X1 as follows:

**Table 9.** Sample Frequency

| Sample Frequency WSBD | Typical Sample Frequency | $t_C$ | CLBD/WSBD Frequency Ratio |
|---|---|---|---|
| 1/($t_{CK}$ * 128) | 96 kHz | $t_{CK}$ | 64 |
| 1/($t_{CK}$ * 192) | 64 kHz | 2 * $t_{CK}$ | 48 |
| 1/($t_{CK}$ * 256) | 48 kHz | 2 * $t_{CK}$ | 64 |
| 1/($t_{CK}$ * 384) | 32 kHz | 4 * $t_{CK}$ | 48 |

The choice of sample frequency is done by the firmware.

**Figure 10.** Digital Audio Frame Format, 128 x Fs and 256 x Fs Modes

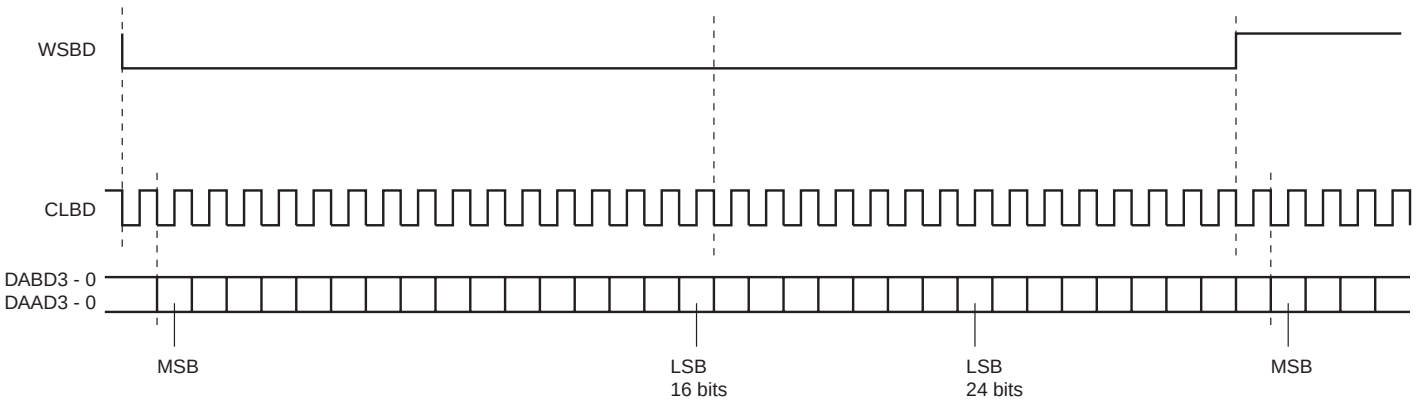
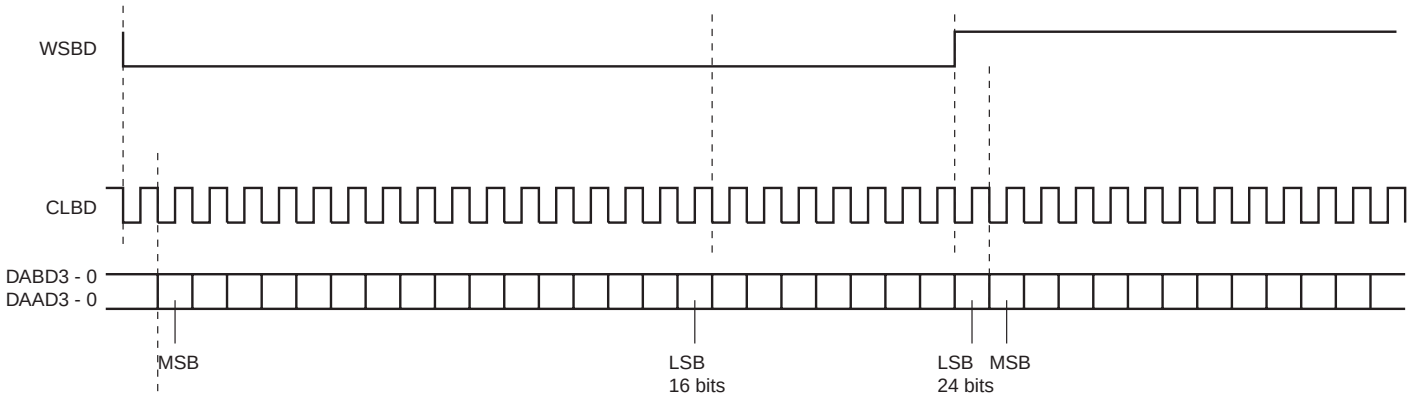


**Figure 11.** Digital Audio Frame Format, 192 x Fs and 384 x Fs Modes




## Serial MIDI_IN and MIDI_OUT

The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

- Baud rate: 31.25 kHz
- Format: start, 8 data bits, 1 stop

## External Memory

Pins used: WA21 - WA0: address out, WD15 - WD0: data bi-directional, $\overline{WCS0}$, $\overline{WCS1}$: pre-decodes out, $\overline{WOE}$: output enable, $\overline{WWE}$: write

When using all address bits, the maximum address range is two pages ($\overline{WCS0}$, $\overline{WCS1}$) of 4M words (total = 16 Mbytes).

**Figure 12.** ROM/Flash Read Cycle

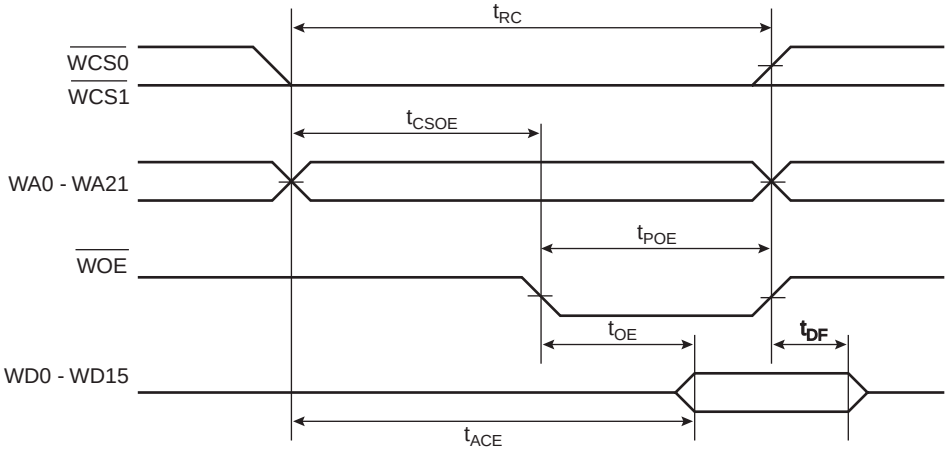



**Table 10.** External Memory Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{RC}$ | Read cycle time | 5 * $p_{LCK}$ | - | 6 * $p_{LCK}$ | ns |
| $t_{CSOE}$ | Chip select low/address valid to $\overline{WOE}$ low | 2 * $p_{LCK}$ - 5 | - | 3 * $p_{LCK}$ + 5 | ns |
| $t_{POE}$ | Output enable pulse width | - | 3 * $p_{LCK}$ | - | ns |
| $t_{ACE}$ | Chip select/address access time | 5 * $p_{LCK}$ - 5 | - | - | ns |
| $t_{OE}$ | Output enable access time | 3 * $p_{LCK}$ - 5 | - | - | ns |
| $t_{DF}$ | Chip select or $\overline{WOE}$ high to input data Hi-Z | 0 | - | 2 * $p_{LCK}$ - 5 | ns |

Notes:
1. A built-in PLL multiplies the crystal clock frequency by 4 for internal use. $p_{LCK}$ is the period of the internal clock generated by PLL. $p_{LCK} = t_{CK}/4$. Typical value with crystal 12.288 MHz is $p_{LCK}$ = 20 ns.
2. Memory access time should be lower than $t_{ACE}$min. Typical value with crystal 12.288 MHz is 90 ns.

**Figure 13.** External RAM/Flash Write Timing

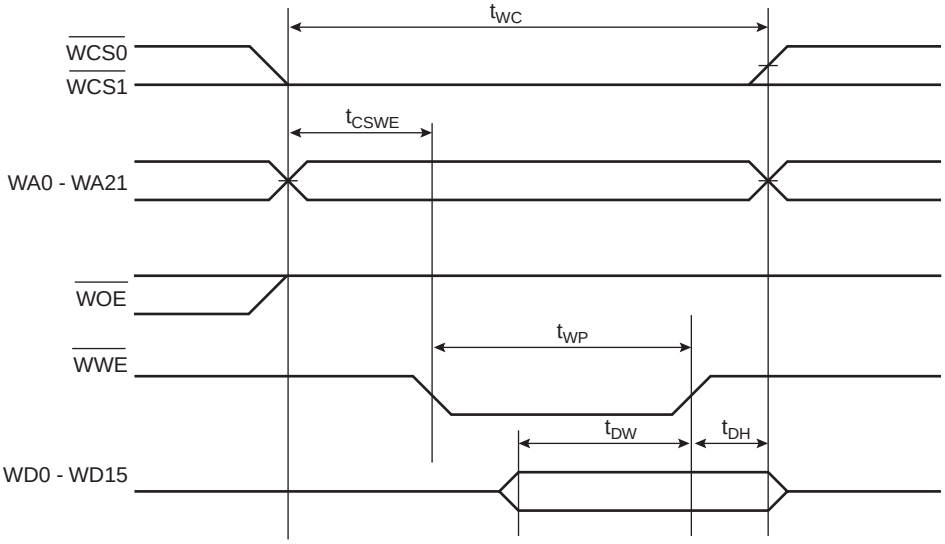



**Table 11.** External Flash Timing Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WC}$ | Write cycle time | 5 * $p_{LCK}$ | - | 6 * $p_{LCK}$ | ns |
| $t_{CSWE}$ | Write enable low from $\overline{CS}$ or Address or $\overline{WOE}$ | 2 * $p_{LCK}$ - 10 | - | - | ns |
| $t_{WP}$ | Write pulse width | - | 4 * $p_{LCK}$ | - | ns |
| $t_{DW}$ | Data out setup time | 4 * $p_{LCK}$ - 10 | - | - | ns |
| $t_{DH}$ | Data out hold time | 10 | - | - | ns |

## Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10ms.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- Addresses 0 & 1 from external ROM are checked. If “DR” is read, then control is transferred to address 400H from external ROM.
- $\overline{\text{SMC}}$ is sensed. If LOW, then the built-in loader waits for SmartMedia presence detect (SMPD). When detected, the firmware is downloaded from SmartMedia reserved sector 1 and started.
- An attempt is done to read the first two bytes of an external EEPROM or DataFlash. If “DR” is read, then the built-in loader loads the firmware from the external EEPROM/DataFlash and starts it.
- Firmware download from a host processor is assumed.

1. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip is ready to accept program download. Higher speed transfer can be reach by polling the parallel interface status ($\overline{\text{CS}}$ = 0, A0 = 1, $\overline{\text{RD}}$ = 0).
2. The host sends the firmware size (in words) on two bytes (Low byte first).
3. The host sends the ATSAM3303 firmware. The firmware should begin with string “DR”.
4. The byte 0ACh is written to the host, this rises IRQ. The host recognizes that the chip has accepted the firmware.
5. ATSAM3303 starts the firmware.

If $\overline{\text{PDWN}}$ is asserted low, then the crystal oscillator and PLL are stopped. If the power switch is used, then the chip enters a deep power-down sleep mode, as power is removed from the core. To exit power down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped.
- The clock frequency can be internally divided by 256.

## Recommended Board Layout

Like all HCMOS high integration ICs, the following simple rules of board layout are mandatory for reliable operation:

- GND, VC33, VC18 Distribution and Decouplings

All GND, VC33, VC18 pins should be connected. A GND plane is strongly recommended. The board GND + VC33 distribution should be in grid form.

Recommended VC18 decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. VC33 requires a single 0.1µF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the ATSAM3033 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from ATSAM3033.

- Buses

Parallel layout between D0 - D7 and WA0 - WA21/WD0 - WD15 should be avoided. The D0 - D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0 - WA21/WD0 - WD15 that can corrupt address and/or data on these buses.

A ground plane should be implemented below the D0 - D7 bus, which is connected to the host and to the ATSAM3033 GND.

A ground plane should be implemented below the WA0 - WA21/WD0 - WD15 bus, which is connected to the ROM/Flash grounds and to the ATSAM3033.

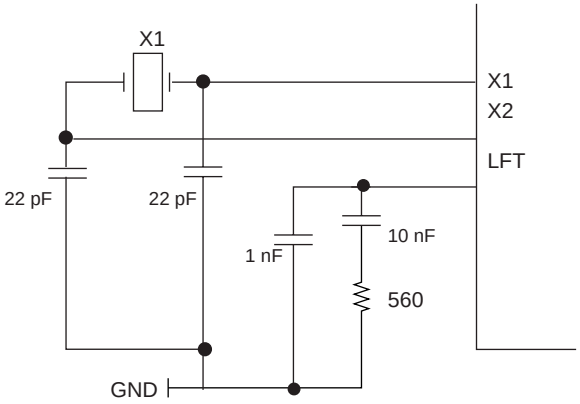
- Analog Section

A specific AGND ground plane should be provided, which is connected to the GND ground by a single trace. No digital signals should cross the AGND plane.

Refer to the Codec vendor recommended layout for correct implementation of the analog section.

## Recommended Crystal Compensation and LFT Filter

**Figure 14.** Recommended Crystal Compensation and LFT Filter



## Product Development and Debugging

Atmel provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (98, ME, 2000, XP). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In-circuit Emulation)
- Program Flash, Dataflash, EEPROM, SmartMedia on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 Kbauds. Thus time-to-market is optimized by testing directly on the final prototype.

A library of frequently used functions is available, such as:

- Wavetable synthesis
- Reverb/Chorus
- MP3 decode
- 31-band equalizer
- Parametric equalizer

Atmel engineers are available to study customer-specific applications.

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