Features

- **Three DSPs and 24-bit Audio Router On-chip**
- **32 kHz to 96 kHz Sampling Rate**
- **Enhanced P16 Processor with C Compiler**
- **New 48-bit Double-precision DSP Instructions**
- **Built-in 16K x 16 Flash Memory**
- **Built-in 8K x 24 RAM**
- **Secure Code - Copy Protected**
- **Direct Connection of LEDs, Switches**
- **Direct Connection of LCD Display**
- **8 Channels for Audio In + Out**
- **DDR-SDRAM/SDRAM Support in Burst Mode**
- **MIDI In/Out**
- **8-bit Parallel Interface**
- **Warm Start Power-down**
- **Deep Power-down (< 5 µA) Using Built-in Power Switch**
- **LQFP80 Package**
- **Typical Applications: Effect Processing (reverb, echo, chorus, etc.), MP3 Decoding, Filtering, Sampling Rate Conversion, Professional Audio, Consumer Electronic, MP3 Player**

1. Description

The ATSAM3703 is a new member of the SAM3000 family of sound synthesis/processing ICs that uses the DSP array technology. It is designed for superior quality sound processing. The 16-bit processor has new instructions and a C compiler for quicker reliable firmware development. Total compatibility is maintained with the other members of the family. Applications written for the ATSAM3703 can be burned into the built-in Flash memory. This memory has specific features to avoid external read of the coded data, thus ensuring very effective copy protection.

The minimum configuration for a product is ATSAM3703 + Codec. An external SDRAM/DDR-SDRAM is needed if the 8K internal RAM is not sufficient for extended delay line buffers, such as high-quality reverb.

Audio Processing

ATSAM3703 High-performance Low-cost Effect Processor

6237A–DRMSD–29-May-06

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2. DSP Array Block Diagram

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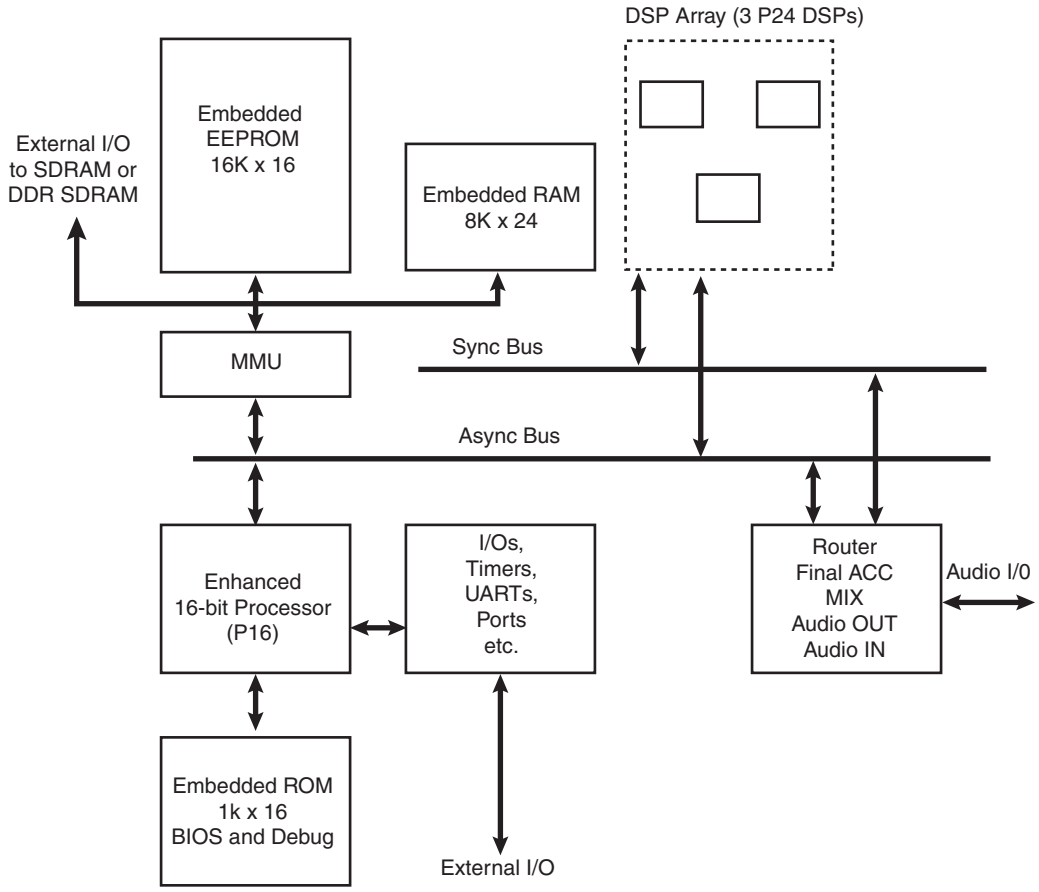
Figure 2-1. DSP Array Block Diagram



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3. Functional Description

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3.1 DSP Array

The ATSAM3703 includes 3 on-chip DSPs.

Each DSP (P24) is built around a 2K x 24 RAM and a 1K x 24 ROM. The RAM contains both data and P24 instructions; the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data, such as compressed audio, through the Async Bus. Each P24 RAM can be accessed through the Async Bus.

Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop. The DSPs have new 48-bit double precision instructions for improved Pro Audio applications.

One P24 is sufficient for processing one channel of MP3, implementing a multi-tap delay line or a multi-tap transversal filter.

3.2 Sync Bus

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48, 96 kHz. Each frame is divided into 64 time slots. Each slot is divided into 4 bus cycles. Each P24 is assigned a hardwired time slot (8 to 63), during which it may provide 24-bit data to the bus (up to 4 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 7 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

3.3 Async Bus

The Async Bus is 24-bit data inside the chip and 16-bit outside.

The P16 processor normally masters the Async Bus, it can read/write the P24 memories and the external or embedded ROM/RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX allow to convert fixed point DSP data to floating point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

3.4 Enhanced 16-bit Processor

This is the new enhanced version of P16 processor with added instructions allowing optimized use of C compiler. Using the P16, widely used in Dream® products, maintains continuity for the large firmware investments from the SAM97xx series. A built-in ROM, connected to the P16 holds basic input/output software (BIOS) for peripherals such as UART, SmartMedia®, MPU as well as a debugger which uses a dedicated asynchronous serial line. The firmware can reside on the built-in 16K x 16 EEPROM or it can be downloaded at power-up into the built-in 8K x 24 RAM from serial SmartMedia or host.

3.5 Memory Management Unit

The MMU handles transfer requests between the external or embedded RAM/ROM, the P16 and the P24s through the Async Bus. The ATSAM3703 includes an on chip 8K x 24 RAM.

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3.6 Router: Final ACC, MIX, Audio Out, Audio In

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This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 8 channels of audio in and 8 channels of audio out are provided (4 stereo in/out, I2S format). The stereo audio in channels may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

3.7 I/O

The ATSAM3703 includes very versatile I/Os that share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.

The following peripherals are included on chip:

- 2 x 8-bit timers
- 2 x 16-bit timers
- Parallel slave 8-bit port, MPU401 compatible
- Parallel master 8-bit port, for connection to SmartMedia and/or LCD display, switches, etc.
- 2 x asynchronous bi-directional serial port (one used as debug interface)
- Synchronous serial slave port (SPI type host connection)
- Firmware controlled I/O pins

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4. Typical Application Examples

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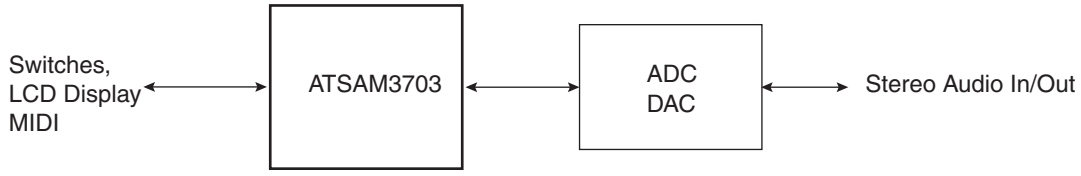
4.1 Low Cost, High Quality Effect

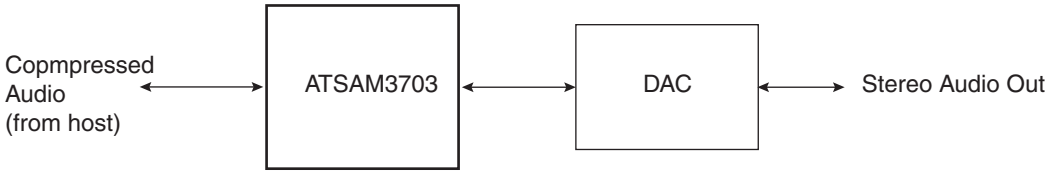
Figure 4-1.



- High quality, full 24-bit multi-effects like reverb, chorus, compressor, etc.
- Stereo 10-band graphic equalizer

4.2 Host-controlled MP3 Player

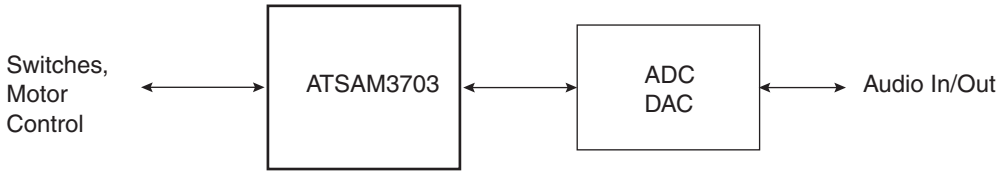
Figure 4-2.



- ATSAM3703 firmware download from host (when using parallel interface)
- Choice of host communication interfaces:
  - 8-bit parallel
  - Asynchronous serial
  - Synchronous serial (SPI
- Full MP3 support including very low bit rates extension (ISO/IEC 13818-3).
- Easily upgradable to other coding standards

4.3 Toys with “Artificial Intelligence”

Figure 4-3.



- Speech recognition
- Learning functions
- ADPCM record / play

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5. DSP Capacity and I/O Configuration

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5.1 DSP Considerations

The ATSAM3703 include 3 x P24 DSPs.

Table 5-1 lists the performance achievable by the P24.

Table 5-1. Performance with P24

Function	P24s required
MP3 decode	3
Stereo reverb and chorus @48 kHz	1
31-band equalizer @96 kHz	3
Stereo 31-band equalizer @48 kHz	3

The ATSAM3703 runs firmware directly from an embedded EEPROM memory. It may also run firmware from local RAM. The ATSAM3703 is the ideal choice when external components count should be minimized and many I/O pins are required.

5.2 I/O Selection Considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (refer to the pinout to identify the exclusions). The two main types of operation are host-controlled and stand-alone.

5.2.1 Host-controlled Operation

There are 3 main ways to communicate with a host processor:

- 8-bit parallel MPU type bi-directional interface
  signals: D7 - D0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, IRQ
- Asynchronous serial, MIDI_IN
- Synchronous serial
  signals: SDIN, SCLK, SYNC, $\overline{INT}$

5.2.2 Stand-alone Operation

Possible stand-alone modes are:

- Firmware into built-in EEPROM memory
- Firmware into external SmartMedia. In this case, the firmware should reside in the SmartMedia reserved sectors starting at sector # 1.

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6. Pinout

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6.1 Pin Description

Identical sharing number indicates multifunction pins.

Pd indicates pin with built-in pull-down resistor.

Pu indicates pin with built-in pull-up resistor.

SSTL indicates a SSTL_2 class 1 compliant I/O pin.

Table 6-1. ATSAM3703 Pin Description

Pin Name	Pin Number	Type	Sharing	Description
GND	1, 13, 24, 32, 40, 45, 49, 54, 61, 70	PWR	-	Digital ground. All these pins should be returned to a ground plane
VC18	28, 46, 62, 77	PWR	-	Core power. All these pins should be returned to nominal 1.8V or to PWROUT if the built-in power switch is used.
VC33	4, 76	PWR	-	Periphery power. All these pins should be returned to nominal 3.3V.
VC25	22, 33, 42, 50, 55	PWR		Memory PAD Power +2.25V to +3.6V. All VC25 pins should be returned to +2.5V (for DDR SDRAM) or 3.3V (for SDRAM)
PWRIN	59	PWR	-	Power switch input, should be returned to nominal 1.8V even if the power switch is not used.
PWROUT	58	PWR	-	Power switch output, should be connected to all VC18 pins if the power switch is used.
VREF	41	In		VC25/2 reference for SSTL_2 pins.
D7 - D0	10, 9, 8, 7, 6, 5, 3, 2	I/O Pd	1	Slave 8-bit interface data. Output if $\overline{CS}$ and $\overline{RD}$ are low (read from chip), input if $\overline{CS}$ and $\overline{WR}$ are low (write to chip). Type of data defined by A0 input.
I/O7 - I/O0	10, 9, 8, 7, 6, 5, 3, 2	I/O Pd	1	SmartMedia data or other peripheral data
P0.7 - P0.0	10, 9, 8, 7, 6, 5, 3, 2	I/O Pd	1	General purpose I/O can individually be programmed as input or output
CLAD3 - 0	10, 9, 8, 7	In Pd	1	Optional bit clocks and word selects for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif.
WSAD3 - 0	6, 5, 3, 2	In Pd	1	
A0	16	In	2	Slave 8-bit interface address. Indicates data/status or data/ctrl transfer type ($\overline{CS}$ $\overline{RD}$ low or $\overline{CS}$ $\overline{WR}$ low)
SMPD	16	In	2	SmartMedia presence detect
P0.10	16	In	2	General purpose input pin
SCLK	16	In	2	Serial slave synchronous interface input clock
$\overline{CS}$	12	In Pu	3	Slave 8-bit interface chip select, active low.
P0.11	12	In Pu	3	General purpose input pin

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Table 6-1. ATSAM3703 Pin Description (Continued)

Pin Name	Pin Number	Type	Sharing	Description
SYNC	12	In Pu	3	Serial slave synchronous interface input sync signal
$\overline{WR}$	17	In Pu	4	Slave 8-bit interface write, active low. D7-D0 data is sampled by chip on $\overline{WR}$ rising edge if $\overline{CS}$ is low
$\overline{SMC}$	17	In Pu	4	SmartMedia configuration. This pin is sensed after power-up. If found low, it is assumed that a SmartMedia connector is present. The built-in firmware waits for SmartMedia SMPD.
P0.12	17	In Pu	4	General purpose input pin
$\overline{RD}$	18	In Pu	5	Slave 8-bit interface read, active low. D7-D0 data is output when $\overline{RD}$ goes low and $\overline{CS}$ is low
$\overline{RIB}$	18	In Pu	5	SmartMedia $\overline{Ready\ Busy}$ status
P0.13	18	In Pu	5	General purpose input pin
MIDI_IN	18	In Pu	5	Serial MIDI in
SDIN	18	In Pu	5	Serial slave synchronous interface input data
IRQ	11	Out	6	Slave 8bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host ($\overline{CS}$ = 0 and $\overline{RD}$ = 0)
$\overline{SMRE}$	11	Out	6	SmartMedia read enable ($\overline{RE}$), active low
FS0	11	In	6	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1)
P0.8	11	I/O	6	General purpose I/O pin
$\overline{INT}$	11	Out	6	Serial slave synchronous interface data request, active low.
DABD0	73	Out		Stereo channel 0 of digital audio output, I2S format
DABD1	74	Out	7	Stereo channel 1 of digital audio output, I2S format
P0.14	74	Out	7	General purpose output pin
DABD2	75	Out	8	Stereo channel 2 of digital audio output, I2S format
P0.15	75	Out	8	General purpose output pin
DABD3	78	Out	9	Stereo channel 3 of digital audio output, I2S format
MIDI_OUT	78	Out	9	Serial MIDI out
DAAD0	66	In Pd	-	Stereo audio data input, I2S format. Can operate on CLBD master rate or CLAD0 or CLAD01 external rate when sampling rate conversion is requested. DAAD0 has built-in pull-down. It may be left open if not used.
DAAD1	67	In Pd	-	Additional channel of stereo audio input, I2S format. Can operate on CLBD master rate or CLAD1 or CLAD01 external rate when sampling rate conversion is requested. DAAD1 has built-in pull-down. It may be left open if not used.

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Table 6-1. ATSAM3703 Pin Description (Continued)

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Pin Name	Pin Number	Type	Sharing	Description
DAAD2	68	In Pd	10	Additional channel of stereo audio input, I2S format. Can operate on CLBD master rate or CLAD2 external rate when sampling rate conversion is requested. DAAD2 has built-in pull-down. It may be left open if not used.
CLAD01	68	In Pd	10	Optional bit clock for digital audio inputs DAAD1-0. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif.
DAAD3	69	In Pd	11	Additional channel of stereo audio input, I2S format. Can operate on CLBD master rate or CLAD3 external rate when sampling rate conversion is requested. DAAD3 has built-in pull-down. It may be left open if not used.
WSAD01	69	In Pd	11	Optional word select for digital audio inputs DAAD1-0. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif.
FS1	69	In Pd	11	Freq sense, sensed at power up. FS1|FS0 allow firmware to know operating freq of chip as follows (optional):00- 6.9552 MHz 01- 9.6 MHz 10- 11.2896 MHz 11- 12.288 MHz
P0.9	69	In Pd	11	General purpose Input pin
CLBD	72	Out	-	Audio bit clock for DABD3-0. Audio bit clock for DAAD3-0 if the corresponding CLAD3-0 is not used.
WSBD	80	Out	-	Audio left/right channel select for DABD3-0. Audio left/right channel for DAAD3-0 if the corresponding WSAD3-0 is not used.
CKOUT	71	Out	-	External DAC/Codec master clock. Same or double frequency as X2 pin. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, 512xFs, Fs being the DAC/Codec sampling rate.
WA11 - WA0	35, 34, 31, 30, 29, 27, 26, 25, 23, 21, 20, 19	Out SSTL	12	Multiplexed addresses for external SDRAM or DDR SDRAM memory
P2.11 - P2.0	35, 34, 31, 30, 29, 27, 26, 25, 23, 21, 20, 19	I/O SSTL	12	General purpose I/O pins
WCKE	57	Out SSTL	13	Clock Enable for external SDRAM or DDR SDRAM memory
P2.12	57	I/O SSTL	13	General purpose I/O pin
WBA1 - WBA0	37, 36	Out SSTL	14	Bank selects for external SDRAM or DDR SDRAM memory
P2.14 - P2.13	37, 36	I/O SSTL	14	General purpose I/O pins
WDQ3	52	I/O SSTL	15	External memory SDRAM or DDR SDRAM data bit 3
P1.3	52	I/O SSTL	15	General purpose I/O pins

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Table 6-1. ATSAM3703 Pin Description (Continued)

Pin Name	Pin Number	Type	Sharing	Description
$\overline{\text{SMCE}}$	52	Out SSTL	15	SmartMedia chip enable ($\overline{\text{CE}}$), active low
WDQ2	51	I/O SSTL	16	External memory SDRAM or DDR SDRAM data bit 2
P1.2	51	I/O SSTL	16	General purpose I/O pin
SMALE	51	Out SSTL	16	SmartMedia address latch enable (ALE)
WDQ1	48	I/O SSTL	17	External memory SDRAM or DDR SDRAM data bit 1
P1.1	48	I/O SSTL	17	General purpose I/O pin
$\overline{\text{SMWE}}$	48	Out SSTL	17	SmartMedia write enable ($\overline{\text{WE}}$), active low
WDQ0	47	I/O SSTL	18	External memory SDRAM or DDR SDRAM data bit 0
P1.0	47	I/O SSTL	18	General purpose I/O pin
SMCLE	47	Out	18	SmartMedia command latch enable (CLE)
WDQS	53	I/O SSTL	19	Data Strobe for external DDR SDRAM memory
P1.4	53	I/O SSTL	19	General purpose I/O pin
WCK	44	Out	20	Positive clock for external SDRAM or DDR SDRAM memory
P1.5	44	I/O	20	General purpose I/O pin
$\overline{\text{WCK}}$	43	Out	21	Negative clock for external DDR SDRAM memory
P1.6	43	I/O	21	General purpose I/O pin
$\overline{\text{WRAS}}$	39	Out SSTL	22	Row address strobe for external SDRAM or DDR SDRAM memory
P1.7	39	I/O	22	General purpose I/O pin
$\overline{\text{WCAS}}$	38	Out SSTL	23	Column address strobe for external SDRAM or DDR SDRAM memory
P1.8	38	I/O	23	General purpose I/O pin
$\overline{\text{WWE}}$	56	Out SSTL	24	Write enable for external SDRAM or DDR SDRAM memory
P2.15	56	I/O SSTL	24	General purpose I/O pin

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Table 6-1. ATSAM3703 Pin Description (Continued)

Pin Name	Pin Number	Type	Sharing	Description
X1 - X2	64, 63	-	-	External crystal connection. Standard frequencies are 6.9552 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. 1.8Vpp) can be connected to X1 using AC coupling (22pF). A built-in PLL multiplies the clock frequency by 4 for internal use.
$\overline{\text{RESET}}$	14	In	-	Master reset Schmitt trigger input, active low. $\overline{\text{RESET}}$ should be held low during at least 10ms after power is applied. On the rising edge of $\overline{\text{RESET}}$, the chip enters an initialization routine, which may involve firmware download from an external SmartMedia, or host.
STIN	65	In Pd	-	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.
STOUT	79	Out	-	Serial test output. 57.6 kbauds async output used for firmware debugging.
$\overline{\text{PDWN}}$	60	In	-	Power down input, active low. High level on this pin is typ. VC18. When $\overline{\text{PDWN}}$ is low, the oscillator and PLL are stopped, the power switch opens, and the chip enters a deep sleep mode (1µA typ. consumption when power switch is used). To exit from power down, $\overline{\text{PDWN}}$ has to be set high then $\overline{\text{RESET}}$ applied. Alternate programmable power-downs are available which allow warm restart of the chip.
TEST	15	In Pd	-	Test input. Should be grounded or left open.

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6.2 Pinout by Pin Number

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Table 6-2. ATSAM3703 Pinout by Pin Number

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	GND	12	$\overline{CS}$ P0.11 SYNC	23	WA3 P2.3	34	WA10 P2.10	45	GND
2	D0 I/O0 P0.0 WSAD0	13	GND	24	GND	35	WA11 P2.11	46	VC18
3	D1 I/O1 P0.1 WSAD1	14	$\overline{RESET}$	25	WA4 P2.4	36	WBA0 P2.13	47	WDQ0 SMCLE P1.0
4	VC33	15	TEST	26	WA5 P2.5	37	WBA1 P2.14	48	WDQ1 $\overline{SMWE}$ P1.1
5	D2 I/O2 P0.2 WSAD2	16	A0 SMPD P0.10 SCLK	27	WA6 P2.6	38	$\overline{WCAS}$ P1.8	49	GND
6	D3 I/O3 P0.3 WSAD3	17	$\overline{WR}$ $\overline{SMC}$ P0.12	28	VC18	39	$\overline{WRAS}$ P1.7	50	VC25
7	D4 I/O4 P0.4 CLAD0	18	$\overline{RD}$ $\overline{RIB}$ P0.13 MIDI_IN SDIN	29	WA7 P2.7	40	GND	51	WDQ2 SMALE P1.2
8	D5 I/O5 P0.5 CLAD1	19	WA0 P2.0	30	WA8 P2.8	41	VREF	52	WDQ3 $\overline{SMCE}$ P1.3
9	D6 I/O6 P0.6 CLAD2	20	WA1 P2.1	31	WA9 P2.9	42	VC25	53	WDQS P1.4
10	D7 I/O7 P0.7 CLAD3	21	WA2 P2.2	32	GND	43	$\overline{WCK}$ P1.6	54	GND
11	IRQ $\overline{INT}$ $\overline{SMRE}$ FS0 P0.8	22	VC25	33	VC25	44	WCK P1.5	55	VC25

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Table 6-2. ATSAM3703 Pinout by Pin Number (Continued)

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
56	$\overline{\text{WWE}}$ P2.15	61	GND	66	DAAD0	71	CKOUT	76	VC33
57	WCKE P2.12	62	VC18	67	DAAD1	72	CLBD	77	VC18
58	PWROUT	63	X2	68	DAAD2 CLAD01	73	DABD0	78	DABD3 MIDI_OUT
59	PWRIN	64	X1	69	DAAD3 WSAD01 FS1 P0.9	74	DABD1 P0.14	79	STOUT
60	$\overline{\text{PDWN}}$	65	STIN	70	GND	75	DABD2 P0.15	80	WSBD

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7. Mechanical Dimensions

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Figure 7-1. Thin 80-lead Quad Flat Pack (LQFP80)

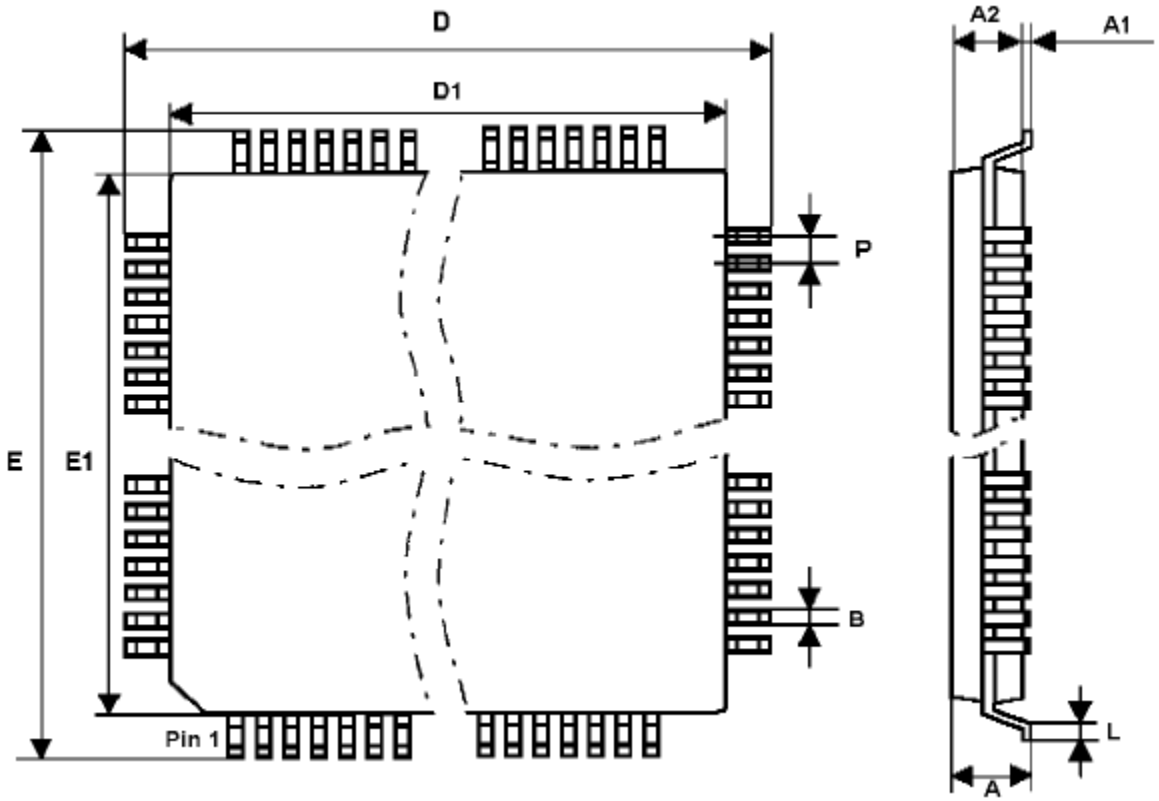

Table 7-1. LQFP Dimensions (mm)

Parameter	Min	Nominal	Max
A	-	1.40	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
L	0.45	0.60	0.75
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
P		0.40	
B	0.13	0.16	0.23

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8. Electrical Characteristics

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8.1 Absolute Maximum Ratings

Temperature under bias ..... -55° C to 125° C Storage Temperature ..... -65° C to 150° C Voltage on any pin X1, PWDN ..... -0.3 to V_{C18} + 0.3V Others ..... -0.3 to V_{C33} + 0.3V Supply Voltage ..... V_{C18} .....-0.3V to 1.95V V_{C25} .....-0.3V to 3.6V V_{C33} .....-0.3V to 3.6V Maximum IOL per I/O pin..... 4 mA (except SSTL pins) Maximum IOH per I/O pin (except SSTL pins) ..... 4 mA Maximum IOL per SSTL pin ..... 8 mA -VOUT = VTT - 0.405 Maximum IOH per I/O pin -VOUT = VTT + 0.405..... 8 mA	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 Recommended Operating Conditions

Table 8-1. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{C18}	Supply voltage	1.65	1.8	1.95	V
V_{C33}	Supply voltage[1]	3	3.3	3.6	V
PWRIN	Supply voltage PWRIN pin	1.75	1.9	1.95	V
T_A	Operating ambient temperature	0	-	70	°C

Note: 1. Operation at lower V_{C33} values down to V_{C18} is possible, however external timing may be impaired. Contact Atmel if you plan to use these circuits with V_{C33} outside the recommended operating range.

8.2.1 SSTL_2 Pads

Memory pads of ATSAM3703 are SSTL_2 compliant. This feature allows direct interfacing with DDR SDRAM devices.

8.2.1.1 DDR SDRAM Operation

When using DDR SDRAM memory, it is recommended to use the schematic in Figure 8-1 for Address, Data and Data Strobe.

In power-down mode, the command lines ($\overline{WRAS}$, $\overline{WCAS}$, $\overline{WWE}$, WCKE) have a fixed level, in contrast with address and data lines which are floating. To avoid consumption in power-down, RT can be not implemented on command lines.

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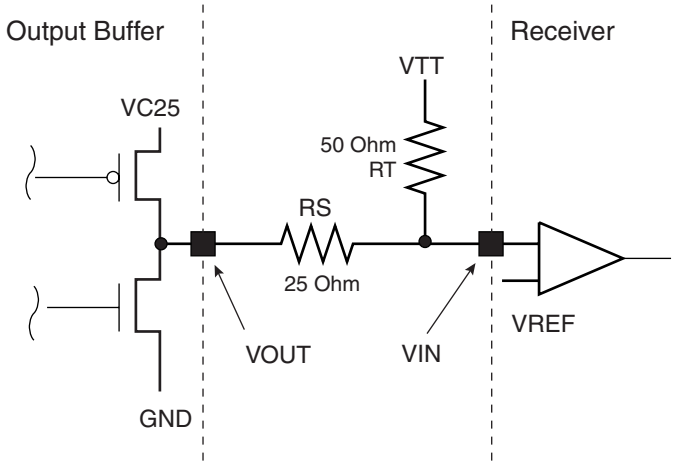
Figure 8-1. Typical SSTL_2 Input/Output Environment



Notes: 1. VC25 = 2.5V
2. VREF = 1.25 V
3. VTT = 1.25V (sink / source capability)

Table 8-2. Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VC25	Supply voltage	2.3	2.5	2.75	V
VREF	Reference voltage	VC25/2 - 0.04	1.25	VC25/2 + 0.04	V
RS	Serial resistor	22.5	25	27.5	Ohm
RT	Termination resistor	45	50	55	Ohm

For more details on SSTL_2, refer to the EIA/JEDEC standard EIA/JESD8-9.

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8.2.1.2 SDRAM OR GPIO OPERATION

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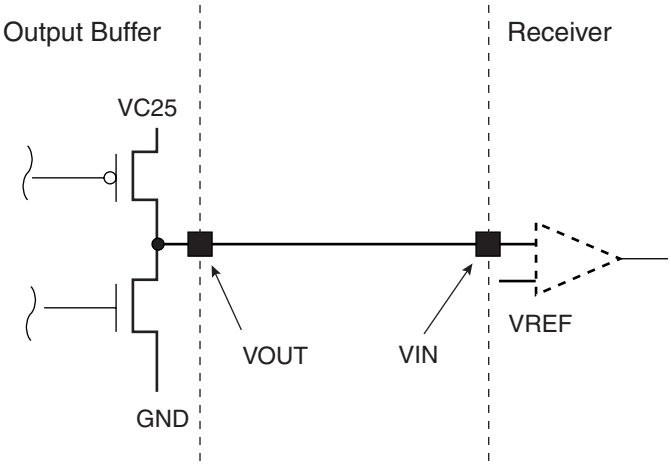
When using the SSTL_2 pad as SDRAM or GPIO signals, it is recommended to use the schematic in Figure 8-2.

Figure 8-2. SSTL_2 in SDRAM or GPIO Operation Schematic



Notes: 1. VC25 = 3.3V
2. VREF = 1.75V

Table 8-3. Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VC25	Supply voltage	3	3.3	3.6	V
VREF	Reference voltage	VC25/2 - 0.04	1.75	VC25/2 + 0.04	V

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8.3 DC Characteristics

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Table 8-4. DC Characteristics (TA= 25°C, VC18 = 1.8V±10%, VC33 = 3.3V±10%, VC25 = 2.5V±10%

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Low level input voltage, except X1, $\overline{\text{PDWN}}$ and SSTL pads	-0.3	-	0.8	V
VIH	High level input voltage, except X1, $\overline{\text{PDWN}}$ and SSTL pads	2	-	3.6	V
VIL	Low level input voltage SSTL pads	-	-	VREF-0.31	V
VIH	High level input voltage SSTL pads	VREF+0.31	-	-	V
VIL	Low level input voltage X1, $\overline{\text{PDWN}}$	-0.3	-	0.605	V
VIH	High level input voltage X1, $\overline{\text{PDWN}}$	1.235	-	VC18+0.3	V
VOL	Low level output voltage IOL = -2mA (Memory pads excepted)	-	-	0.4	V
VOH	High level output voltage IOH = 2mA (SSTL pads excepted)	VC33-0.4	-	-	V
VOL	Low level output voltage IOL = -2mA (SSTL pads only)	-	-	0.4	V
VOH	High level output voltage IOH = 2mA (SSTL pads only)	VC25-0.4	-	-	V
IC18	VC18 power supply current (crystal freq. = 12.288 MHz, all 3 P24 running)	-	46	-	mA
IC18	VC18 power supply current (crystal freq. = 12.288 MHz, all P24 stopped, warm start power-down active)	-	4	-	mA
IC18	VC18 deep power down supply current (using power switch)	-	1	10	µA
IC33	VC33 power supply current (crystal freq.= 12.288 MHz)	-	1	-	mA
IC25	VC25 power supply current (crystal freq.= 12.288 MHz, RS = 25, RT = 50)	-	75	-	mA
PU/PD	Built-in pull-up / pull-down resistor	10	-	56	kOhm

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9. Peripherals and Timings

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9.1 Slave 8-bit Parallel Interface

Pins used: D7-D0 (I/O), $\overline{CS}$ (input), A0 (input), $\overline{WR}$ (input), $\overline{RD}$ (input), IRQ (output)

This interface is typically used to connect the chip to a host processor.

9.1.1 Timings

Figure 9-1. Host Interface Read Cycle

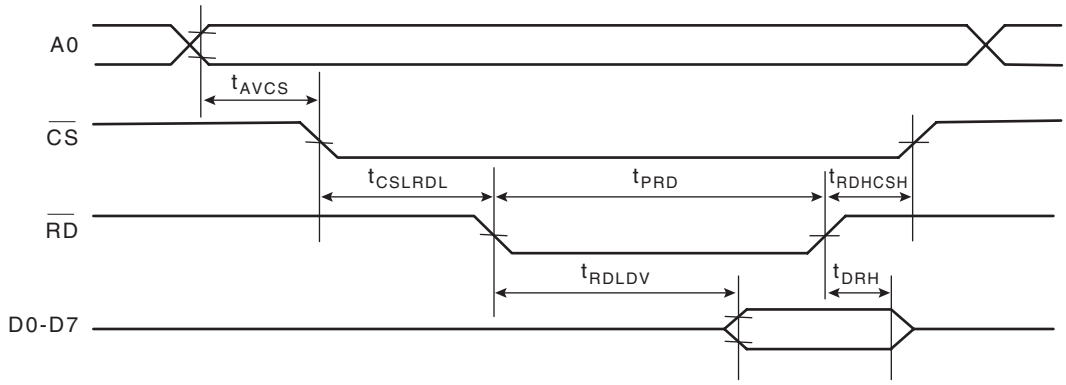

Figure 9-2. Host Interface Write Cycle

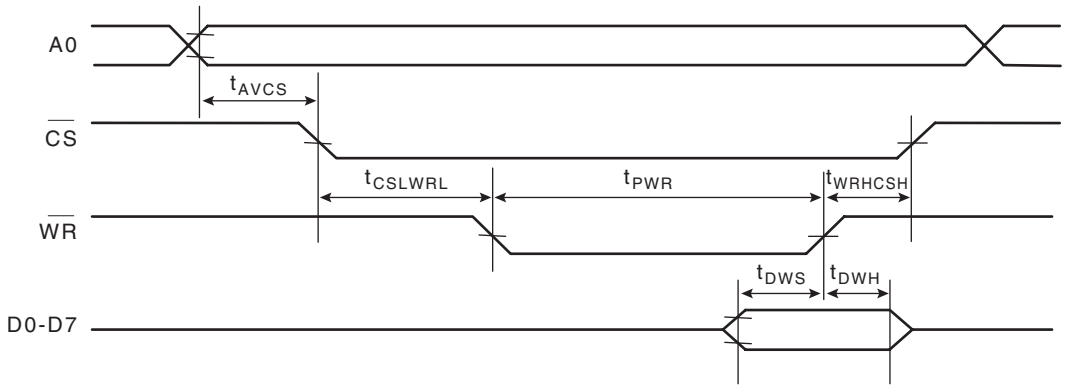

Table 9-1. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address valid to chip select low	0	-	-	ns
t_{CSLRDL}	Chip select low to $\overline{RD}$ low	5	-	-	ns
t_{RDHCSH}	$\overline{RD}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PRD}	$\overline{RD}$ pulse width	50	-	-	ns
t_{RDLDV}	Data out valid from $\overline{RD}$	-	-	20	ns
t_{DRH}	Data out hold from $\overline{RD}$	1.7	-	10	ns
t_{CSLWRL}	Chip select low to $\overline{WR}$ low	5	-	-	ns
t_{WRHCSH}	$\overline{WR}$ high to $\overline{CS}$ high	5	-	-	ns

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Table 9-1. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{PWR}	$\overline{WR}$ pulse width	50	-	-	ns
t_{DWS}	Write data setup time	10	-	-	ns
t_{DWH}	Write data hold time	0.9	-	-	ns

9.1.2 IO Status Register

TE	RF	X	X	X	X	X	X	Status register is read when A0 = 1, $\overline{RD}$ = 0, $\overline{CS}$ = 0

- **TE: Transmit empty**

If 0, data from ATSAM3703 to host is pending and IRQ is high. Reading the data at A0 = 0 sets TE to 1 and clear IRQ.

- **RF: Receiver full**

If 0, then ATSAM3703 is ready to accept DATA from host.

Note: If status bit RF is not checked by host, write cycle time should not be lower than 3 µs.

9.2 SmartMedia and Other Peripheral Interfaces

This is a master 8-bit parallel interface, allowing connection to SmartMedia or other peripherals such as LCD screens.

Pins used:

- I/O7 - I/O0 (I/O)
- SMPD (input)
- $\overline{SMCE}$, SMALE, SMCLE, $\overline{SMRE}$, $\overline{SMWE}$ (outputs)

All these pins are fully under firmware control, therefore timing compatibility is ensured by firmware only.

9.3 Serial Slave Synchronous Interface

The SAM3303 can be controlled by an external host processor through the unidirectional serial interface. However, no firmware can be downloaded at power-up through this interface. Therefore an external ROM/Flash/EEPROM is required.

Pins used:

- SCLK, SYNC, SDIN (input)
- $\overline{INT}$ (output)

Data is shifted MSB first. The IC samples an incoming SDIN bit on the rising edge of SCLK, therefore the host should change SDIN on the negative SCLK edge.

SYNC allows initial synchronization. The rising edge of SYNC, which should occur with SCLK low, indicates that SDIN holds MSB data on the next rising SCLK.

The data is stored internally into a 256 bytes FIFO.

When the FIFO count is below 64, the $\overline{INT}$ output goes low. This allows the host processor to send data in burst mode.

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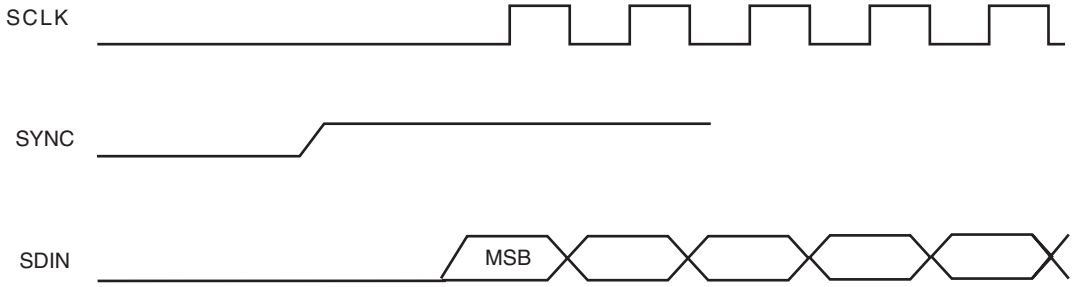
The maximum SCLK frequency is f_{CK} (f_{CK} is the crystal frequency).

The minimum time between two bytes is 64 f_{CK} periods.

The contents of the SDIN data are defined by the firmware.

Figure 9-3. Typical Interface Timing for Serial Slave



9.4 External DDR SDRAM and SDRAM Memories

9.4.1 Overview

The ATSAM3703 supports the DDR SDRAM components compatible with JEDEC standard (JESD79D).

Following memories can be connected to the ATSAM3703:

- DDR SDRAM, 4 bits wide
- SDRAM, 4 bits wide

DDR SDRAM and SDRAM cannot be connected at the same time. The type of connection is SSTL_2 for DDR SDRAM and LVTTL for SDRAM.

DDR SDRAM and SDRAM use time multiplexed addressing with a ROW/COL scheme (banks WBA0 to WBA1 and address lines WA0 to WA11).

9.4.2 Double Data Rate SDRAM

9.4.2.1 Memory Size

The data bus is 4 bits wide. Due to the 12-bit address bus, the maximum accessible address space is 128 Mbits (32M x 4). Larger components are supported, but only a part of the address space is used.

Table 9-2. DDR SDRAM Memory Size

DDR Size	Bank Address	Row Address	Column Address	Remark
64 Mbits (16 M x 4)	2 bits	12 bits	10 bits	
128 Mbits (32 M x 4)	2 bits	12 bits	11 bits	
256 Mbits (64 M x 4)	2 bits	13 bits	11 bits	Only 12-bit rows are used (only 128 Mbits are accessible).
512 Mbits (128 M x 4)	2 bits	13 bits	12 bits	
1 Gbits (256 M x4)	2 bits	14 bits	12 bits	Only 12-bit rows are used (only 128 Mbits are accessible). Self-refresh might not be supported (depending on to t_{XSNR} value; see below)

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9.4.2.2 Pinning

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Table 9-3. DDR SDRAM Pinning

ATSAM3703 Pin	DDR Pin	Description
-	A13, A12	Unused address bits (for larger device). Must be tied to zero.
WA11..WA0	A11..A0	Address
WBA1, WBA0	BA1, BA0	Bank address
WD3..WD0	DQ3..DQ0	Data
WDQS	DQS	Data strobe
	DM	Data mask. Must be tied to zero.
WCK, $\overline{\text{WCK}}$	CK, $\overline{\text{CK}}$	Differential clock
WCKE	CKE	Clock enable
-	$\overline{\text{CS}}$	Chip select. Must be tied to zero.
$\overline{\text{WCAS}}$	$\overline{\text{CAS}}$	Command
$\overline{\text{WRAS}}$	$\overline{\text{RAS}}$	
$\overline{\text{WWE}}$	$\overline{\text{WE}}$	
VREF	VREF	SSTL_2 reference voltage. Must be connected to 1.25 V.

9.4.2.3 Timing

General Parameters

The DDR SDRAM is used with parameters defined in Table 9-4.

Table 9-4. DDR SDRAM General Parameters

Symbol	Parameter		Value
t_{CK}	Clock cycle time		10 ns
CL	Mode Register	CAS Latency	2 cycles
		Burst length	4 data
		Burst type	sequential
		Operating mode	normal
	Extended mode register	DLL	enabled
		Output drive strength	normal

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Command Sequencing

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The ATSAM3703 supports DDR200 and faster DDR devices, and thus the DDR device must support parameters defined in Table 9-5.

Table 9-5. Supported Parameters

Symbol	Parameter	Value
t_{MRD}	MODE REGISTER SET command cycle time	min 20 ns
t_{RAS}	ACTIVE to PRECHARGE command	min 50 ns max 70 us
t_{RC}	ACTIVE to ACTIVE/AUTO REFRESH command period	min 70 ns
t_{RFC}	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	min 120 ns
t_{RCD}	ACTIVE to READ or WRITE delay	min 20 ns
t_{RP}	PRECHARGE command period	min 20 ns
t_{RRD}	ACTIVE bank a to ACTIVE bank b command	min 20 ns
t_{WR}	WRITE recovery time	min 20 ns
t_{WTR}	Internal WRITE to READ command delay	min 10 ns
t_{XSNR}	Exit self refresh to non-READ command	min 80 ns
t_{XSRD}	Exit self refresh to READ command	min 2 us
t_{REFI}	Average periodic REFRESH interval	7.8 us

ATSAM3703 to DDR

Table 9-6. Parameters

Symbol	Parameter	Value
t_{IH}	Address and control hold time	min 3.6 ns
t_{IS}	Address and control setup time	min 3.2 ns
t_{DSS}	DQS falling edge to CK setup time	min 4.3 ns
t_{DSH}	DQS falling edge hold time from CK	min 4.3 ns
t_{DS}	DQ and DM setup time	min 1.7 ns
t_{DH}	DQ and DM hold time	min 0.8 ns

DDR to ATSAM3703

The data from DDR to ATSAM3703 must meet timing requirements defined in Table 9-7. These parameters are applicable at input of ATSAM3703, and must include effects of DDR device and effects of board layout.

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Table 9-7. Timing Requirements

Symbol	Parameter	Value
t_{DQSQ}	Skew between WDQS, WD3, WD2, WD1 and WD0	max 1.6 ns
t_{DQSCK}	Delay from WCK, $\overline{WCK}$ to WDQS (excluding CAS latency)	max 5 ns

9.4.3 Single Data Rate SDRAM

9.4.3.1 Memory Size

The data bus is 4 bits wide. Due to the 12-bit address bus, the maximum accessible address space is 128 Mbits (32M x 4). Larger components are supported, but only a part of the address space is used.

Table 9-8. SDR SDRAM Memory Size

DDR Size	Bank Address	Row Address	Column Address	Remark
64 Mbits (16M x 4)	2 bits	12 bits	10 bits	
128 Mbits (32M x 4)	2 bits	12 bits	11 bits	
256 Mbits (64M x 4)	2 bits	13 bits	11 bits	Only 12-bit rows are used (only 128 Mbits are accessible)
512 Mbits (128M x 4)	2 bits	13 bits	12 bits	

9.4.3.2 Pinning

Table 9-9. SDR Pinning

ATSAM3703 Pin	SDR Pin	Description
-	A13, A12	Unused address bits (for larger device). Must be tied to zero.
WA11..WA0	A11..A0	Address
WBA1, WBA0	BA1, BA0	Bank address
WD3..WD0	DQ3..DQ0	Data
WDQS	-	Not used. Must be left unconnected.
	DM	Data mask. Must be tied to zero.
WCK	CK	Clock
$\overline{WCK}$	-	Not used. Must be left unconnected.
WCKE	CKE	Clock enable
-	$\overline{CS}$	Chip select. Must be tied to zero.
$\overline{WCAS}$	$\overline{CAS}$	Command
$\overline{WRAS}$	$\overline{RAS}$	
$\overline{WWE}$	$\overline{WE}$	
VREF	-	Must be connected to VC25/2.

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9.4.3.3 Timing

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General Parameters

The SDR is used with parameters as in Table 9-10.

Table 9-10. SDR General Parameters

Symbol	Parameter		Value (50 MHz)	Value (100 MHz)
t_{CK}	Clock cycle time		20 ns	10 ns
CL	Mode Register	CAS Latency	2 cycles	2 cycles
		Burst length	4 data	4 data
		Burst type	sequential	sequential
		Operating mode	normal	normal
		Output drive strength	normal	normal

Command Sequencing

The SDRAM device must support following parameters.

Table 9-11. Supported Parameters

Symbol	Parameter	Value (50 MHz)	Value (100 MHz)
t_{MRD}	MODE REGISTER SET command cycle time	min 40 ns	min 20 ns
t_{RAS}	ACTIVE to PRECHARGE command	min 60 ns max 70 us	min 50 ns max 70 us
t_{RC}	ACTIVE to ACTIVE/AUTO REFRESH command period	min 80 ns	min 70 ns
t_{RFC}	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	min 80 ns	min 70 ns
t_{RCD}	ACTIVE to READ or WRITE delay	min 20 ns	min 20 ns
t_{RP}	PRECHARGE command period	min 20 ns	min 20 ns
t_{RRD}	ACTIVE bank a to ACTIVE bank b command	min 20 ns	min 20 ns
t_{WR}	WRITE recovery time	min 20 ns	min 20 ns
t_{XSNR}	Exit self refresh to non-READ command	min 80 ns	min 80 ns
t_{XSRD}	Exit self refresh to READ command	min 4 us	min 2 us
t_{REFI}	Average periodic REFRESH interval	7.8 us	7.8 us

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ATSAM3703 to SDRAM

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The outputs of ATSAM3703 meet constraints as in Table 9-12.

Table 9-12. ATSAM9703 Output Constraints

Symbol	Parameter	Value(50 MHz)	Value(100 MHz)
t_{IH}	Address and control hold time	min 8.8 ns	min 3.8 ns
t_{IS}	Address and control setup time	min 8.3 ns	min 3.3 ns
t_{DS}	DQ and DM setup time	min 14.3 ns	min 6.8 ns
t_{DH}	DQ and DM hold time	min 3.8 ns	min 1.4 ns

SDR to ATSAM3703

The data from SDR to ATSAM3703 must meet following timing requirements. These parameters are applicable at input of ATSAM3703, and must include effects of SDR device and effects of board layout.

Table 9-13. Timing Requirements

Parameter	Value
DQ setup time	min 2.0 ns
DQ hold time	min 1.8 ns

9.4.4 Address Mapping

For information, the mapping in Table 9-14 is applied from the internal async bus address AAD[22:0] to the SDRAM address.

Table 9-14. Address Mapping

ATSAM3703 Address Bus	Value at RAS time	Value at CAS time
WBA0	AAD0	AAD0
WBA1	AAD1	AAD1
WA0	AAD10	0 (see note)
WA1	AAD11	0 (see note)
WA2	AAD12	AAD2
WA3	AAD13	AAD3
WA4	AAD14	AAD4
WA5	AAD15	AAD5
WA6	AAD16	AAD6
WA7	AAD17	AAD7
WA8	AAD18	AAD8
WA9	AAD19	AAD9
WA10	AAD20	Auto-Precharge
WA11	AAD21	AAD22

Note: WA[1:0] = 00 at CAS time means that for each read or write operation at a specified address, four nibbles are read or write in the burst sequential order (0,1, 2, 3). Other sequential orders are not allowed.

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9.5 Digital Audio

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Pins used:

- CLBD, WSBD (outputs)
- DABD3 - 0 (outputs)
- DAAD3 - 0 (inputs)

And optionally

- CLAD3 - 0, WSAD3 - 0 (inputs)

The ATSAM3703 allows for 8 digital audio output channels and 8 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD3 - 0 inputs can be synchronized with incoming CLAD3 - 0 and WSAD3 - 0 signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S standard, with up to 24 bits per sample.

Figure 9-4. Digital Audio Timing

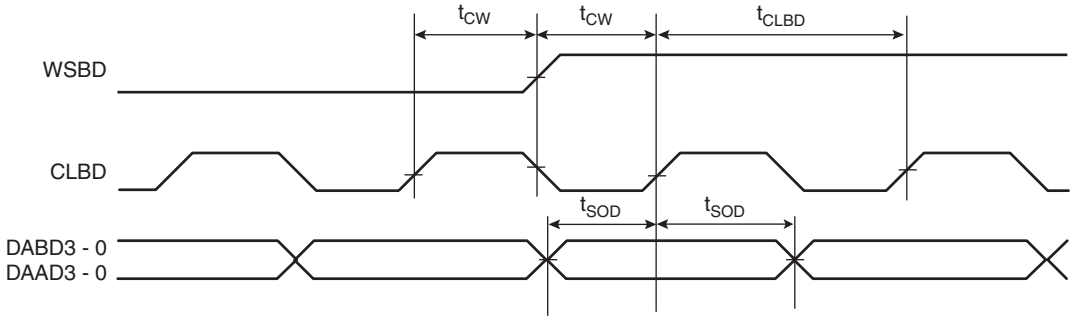

Table 9-15. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD rising to WSBD change	t_C - 10	-	-	ns
t_{SOD}	DABD valid prior/after CLBD rising	t_C - 10	-	-	ns
t_{CLBD}	CLBD cycle time	-	2*tc	-	ns

t_C is related to t_{CK}, the crystal period at X1, as shown in Table 9-16.

Table 9-16. Sample Frequency

Sample Frequency WSBD	Typical Sample Frequency	t_C	CLBD/WSBD Freq Ratio
$1/(t_{CK} * 128)$	96 kHz	t_{CK}	64
$1/(t_{CK} * 192)$	64 kHz	$2 * t_{CK}$	48
$1/(t_{CK} * 256)$	48 kHz	$2 * t_{CK}$	64
$1/(t_{CK} * 384)$	32 kHz	$4 * t_{CK}$	48

The choice of sample frequency is done by the firmware.

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9.5.1 Digital Audio Frame Format

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ATSAM3703 can generate I2S or MSB left justified digital audio format. Master Clock CLBD can be 128 x Fs, 256 x Fs, 512 x Fs, 192 x Fs, 384 x FS or 768 x Fs. Format and clock ratio are selected by firmware.

Figure 9-5. I2S Digital Audio Frame Format,128 x Fs, 256 x Fs and 512 x Fs Modes

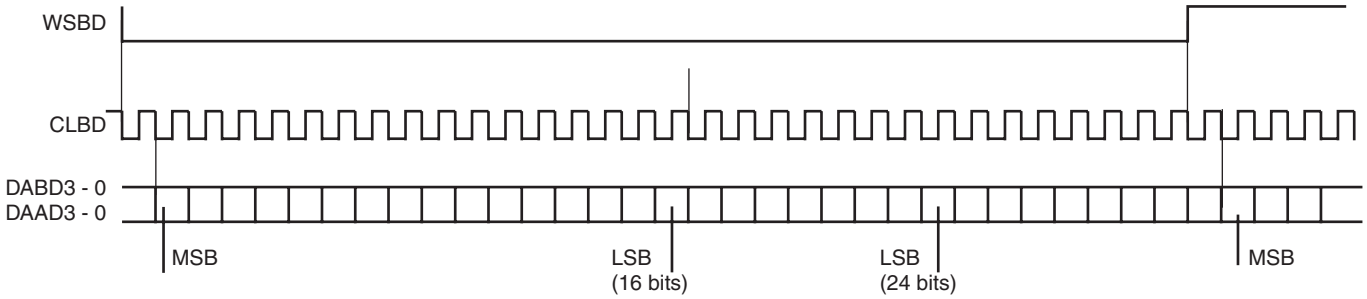


Figure 9-6. I2S Digital Audio Frame Format,192 x Fs, 384 x Fs and 768 x Fs Modes

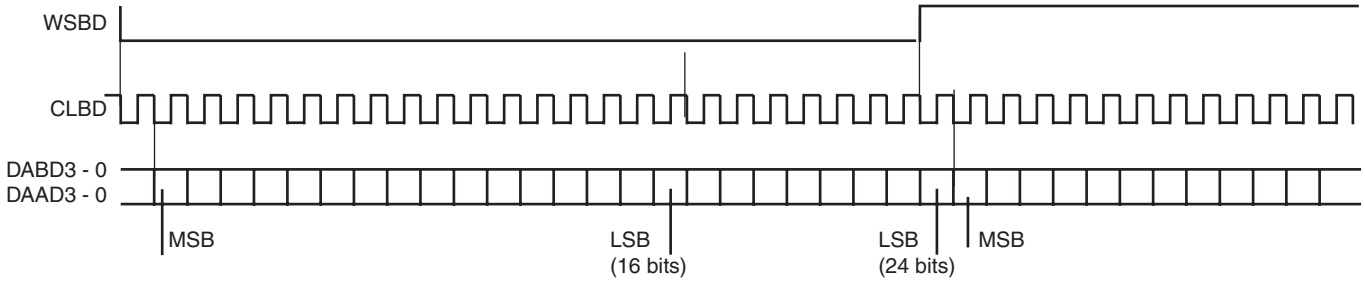


Figure 9-7. MSB Left Justified Digital Audio Frame Format,128 x Fs, 256 x Fs and 512 x Fs Modes

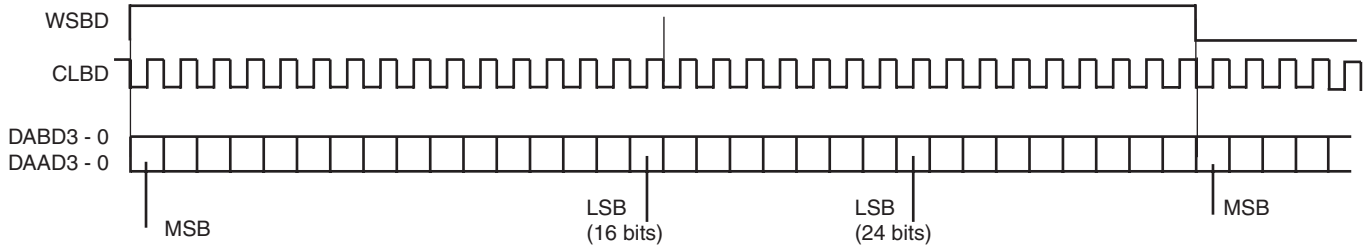
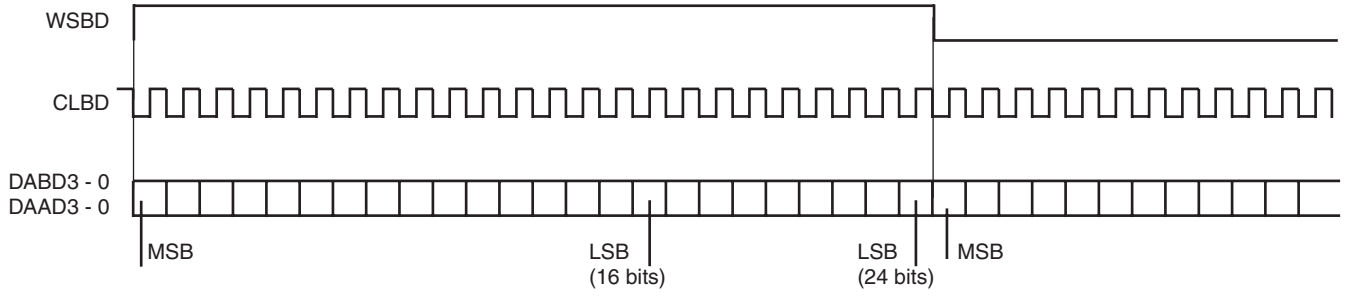


Figure 9-8. MSB Left Justified Digital Audio Frame Format,192 x Fs, 384 x Fs and 768 x Fs Modes



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9.6 Serial MIDI_IN and MIDI_OUT

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The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

- Baud rate: 31.25 kHz
- Format: start bit(0), 8 data bits, stop bit(1)

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10. Reset and Power Down

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During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10ms.

After the low to high transition of $\overline{\text{RESET}}$, the following occurs:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- Addresses 0 &1 from internal EEPROM are checked. If “DR” is read, then control is transferred to address 400H from internal EEPROM.
- $\overline{\text{SMC}}$ is sensed. If LOW, then the built-in loader waits for SmartMedia presence detect (SMPD). When detected, the firmware is downloaded from SmartMedia reserved sector 1 and started.
- Firmware download from an host processor is assumed. (Download in 8K x 24 internal RAM)

1. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip is ready to accept program download. Higher speed transfer can be reach by polling the parallel interface status ($\overline{\text{CS}}$=0, A0=1, $\overline{\text{RD}}$=0).
2. The host sends the firmware size (in words) on two bytes (low byte first).
3. The host sends the ATSAM3703 firmware. The firmware should begin with string “DR”.
4. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip has accepted the firmware.
5. ATSAM3703 starts the firmware.

If $\overline{\text{PDWN}}$ is asserted low, then the crystal oscillator and PLL are stopped. If the power switch is used, then the chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped.
- The clock frequency can be internally divided by 256.

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11. Recommended Board Layout

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Like all HCMOS high integration ICs, the following rules for board layout are mandatory for reliable operations.

11.1 GND, VC33, VC25, VC18 Distribution, Decoupling

All GND, VC33, VC25, VC18 pins should be connected. A GND plane is strongly recommended. The board GND, VC33, VC25 and VC18 distribution should be in grid form.

Recommended VC18 decoupling is 0.1µF at each VC18 pin of the IC with an additional 10µFT decoupling close to the crystal. Minimum recommended VC25 decoupling is 0.1µF at pin 22, 42 and 55. VC33 requires a single 0.1µF decoupling.

11.2 Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

11.3 Buses

Parallel layout from D0-D7 and WA0-WA11/WDQ0-WDQ3 should be avoided. The D0-D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA11/WDQ0-WDQ3 which can corrupt address and/or data on these buses.

A ground plane should be implemented below the D0-D7 bus, which connects both to the host and to the IC GND.

A ground plane should be implemented below the WA0-WA11/WDQ0-WDQ3 bus, which connects both to the SDRAM or DDR SDRAM grounds and to the IC.

11.4 DDR SDRAM and SDRAM

The routing of all signals must be as symmetric as possible. This applies particularly to WDQS, WDQ3, WDQ2, WDQ1 and WDQ0 signals.

The routing of all signals should be kept as short as possible.

VREF must be equal to VC25/2, generated with a resistive divider. Both resistors must have the same value (1% precision). Suggested range is 50 - 150 Ohm. Proper decoupling at each VREF pin (controller, VREF source and RAM device) is recommended.

The SSTL2 signals (DDR) must use a parallel termination (47 Ohm, for example). This termination must be connected to VTT (VC25/2). This VTT is generated from a special component (able to source or to sink current) using VREF as reference. This termination must be placed just after DDR device.

11.5 Analog Section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

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12. Recommended Crystal Compensation

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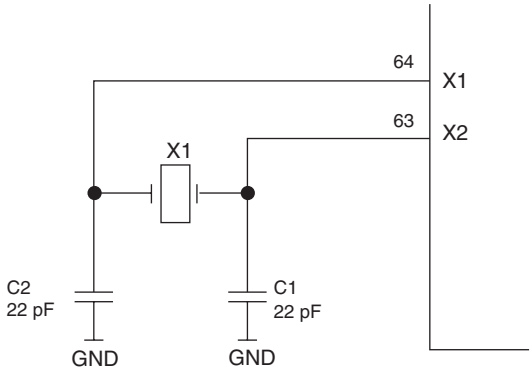
Figure 12-1. Recommended Crystal Compensation



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13. Product Development and Debugging

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Atmel provides an integrated product development and debugging tool SamVS. SamVS runs under Windows® (98, ME, 2000, XP). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program internal EEPROM, SmartMedia on target.

Two dedicated IC pins, STIN and STOUT, permit running the firmware directly into the target using standard PC COM port communication at 57.6 Kbauds. Thus time to market is optimized by testing directly on the final prototype.

A library of frequently used functions is available:

- Reverb
- Chorus
- Delay
- Compressor
- Pitch shifter
- Distortion
- Flanger
- Phaser
- Vocoder
- Feedback canceller
- MP3 decode
- 31 band equalizer
- Parametric equalizer

Atmel engineers are available to study customer specific applications.

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14. Ordering Information

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Table 14-1. Ordering Information

Ordering Code	Package	Package Type
ATSAM3703	LQFP80	Green

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15. Revision History

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Table 15-1. Revision History

Document Ref.	Comments	Change Request Ref.
6237A	First issue	

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