



ATSHA206A

ATSHA206A Summary Data Sheet

Overview

The ATSHA206A is a Microchip CryptoAuthentication™ device primarily dedicated to consumable applications and ecosystem control. The device has five slots and a preassigned configuration that reduces development time and the time to market for specific use cases. The ATSHA206A is a true two-wire device that is powered parasitically through the single-wire interface signal. The device comes in a number of custom packaging solutions and has a built-in decoupling capacitor providing an attractive solution for a wide variety of applications where the accessory may or may not require an actual PCB and space is limited.

Features

- Consumable Authentication Device
- Superior SHA-256 Hash Algorithm with 256-bit Keys
- 248-byte EEPROM for Configuration, Keys and Data:
 - Data zone: 5 slots of 32 bytes each
 - Configuration zone: 88 bytes for counting, locks and serial number
- Data Zone Features:
 - ParentKey slot
 - DerivedKey slot
 - Three dedicated storage slots
- High-Speed, Single-Wire Interface with Parasitic Power
- On-Die Integrated Bypass Capacitor to Allow for Parasitic Power Operation
- 1,024 Maximum Uses (Device Can Be Configured for a Lesser Amount)
- 2.0V to 4.5V Supply Voltage Range
- <150 nA Sleep Current
- Packaging Solutions:
 - 2-Pad VSFN contact package for mechanical attachment without PCB
 - 8-Pad UDFN for prototyping and early development
 - 4-Ball WLCSP, 2 x 2 Grid with a 0.4 mm ball pitch (contact Microchip Sales for more information)

Applications

- Ecosystem Control
- Disposables Authentication
- Anti-cloning

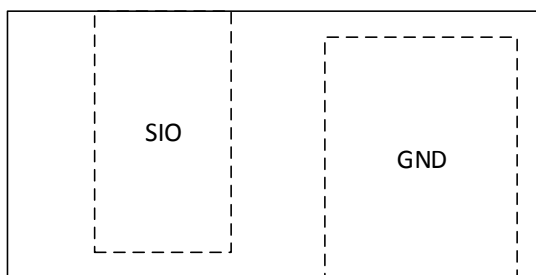
Pin Configuration

Table 1. Pin Descriptions

Pin Name	Pin Type	Description
GND	Supply	Ground Supply
SIO	I/O	Open Drain Serial I/O and Parasitic Power Connection

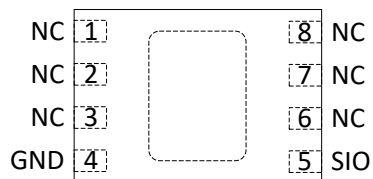
VSFN Package

2 Pad VSFN Package
(Top View)



UDFN Package

UDFN-8 (Top View)



Note: The exposed backside paddle of the UDFN package should be connected to GND.

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1. Introduction

The ATSHA206A device supports a standard challenge-response protocol to authenticate a component or an accessory attached to a system. In use, the host system sends a challenge (i.e. a 32-byte number) to the ATSHA206A device in the client subsystem via the `Message Authentication Code (MAC)` command. The device generates a SHA-256 hash by combining the challenge, the `DerivedKey` and some additional information and returns the result as the response to the host system. The use of a hash algorithm prevents an observer on the bus from deriving the value of the secret key while allowing the system to verify that the response is correct.

The `DeriveKey` command implements a key derivation scheme. Each time the command is used, the current value of the `ParentKey` slot is cryptographically combined with certain fixed values and that result is then written into the `DerivedKey` slot.

All security functions are implemented using the industry-standard SHA-256 secure hash algorithm, using full-sized 256-bit secret keys to prevent any kind of exhaustive attack.

The ATSHA206A is designed to be compatible with the ATSHA204A for a subset of memory and commands as documented in this data sheet. For a comparison, see the *Compatibility with ATSHA204A* section.

1.1 EEPROM Organization

The EEPROM contains a total of 248 bytes (1984 bits) and is divided into the following zones:

Configuration Zone

An 88-byte (704-bit) zone contains a serial number, counter information, slot read/write and lock words. Within this document, the nomenclature `SN[a:b]` indicates a range of bytes within a field of the configuration section. The 88 bytes are accessible from within a three-block address space.

Data Zone

A 160-byte (1280-bit) zone splits into five general purpose, read-only, or read/write memory slots of 32 bytes (256 bits) each, that can be used to store keys or other information related to the item to which the ATSHA206A is attached.

Data Sheet Nomenclature

Within this document, the terms “slot” and “block” are used interchangeably to mean a single, 256-bit (32-byte) area of a particular memory zone. Industry SHA-256 documentation uses the term “block” to indicate a 512-bit section of the message input. In addition, the I/O section of this document uses the term “block” to indicate a variable-length aggregate element transferred between the system and the device.

- In this document, the nomenclature `mode[b]` indicates bit b of the parameter mode.
- Byte ranges are represented as `[LSB:MSB]`
- Slot indicators are represented by `slot[#]`

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to + 150°C
Maximum Applied Voltage	5.5V
DC Output Current	5.0 mA
ESD Ratings:	
Human Body Model (HBM) ESD	> 8 kV
Charge Device Model (CDM) ESD	> 1 kV

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Reliability

The ATSHA206A is fabricated with the high reliability Microchip CMOS EEPROM manufacturing technology.

Table 2-1. EEPROM Reliability

Parameter	Min.	Typ.	Max.	Units
Write Endurance (each byte at +25°C)	100,000	—	—	Write Cycles
Data Retention (at +55°C)	10	—	—	Years
Data Retention (at +35°C)	30	50	—	Years
Read Endurance	Unlimited			Read Cycles

2.3 AC Parameters

Figure 2-1. AC Timing Diagram

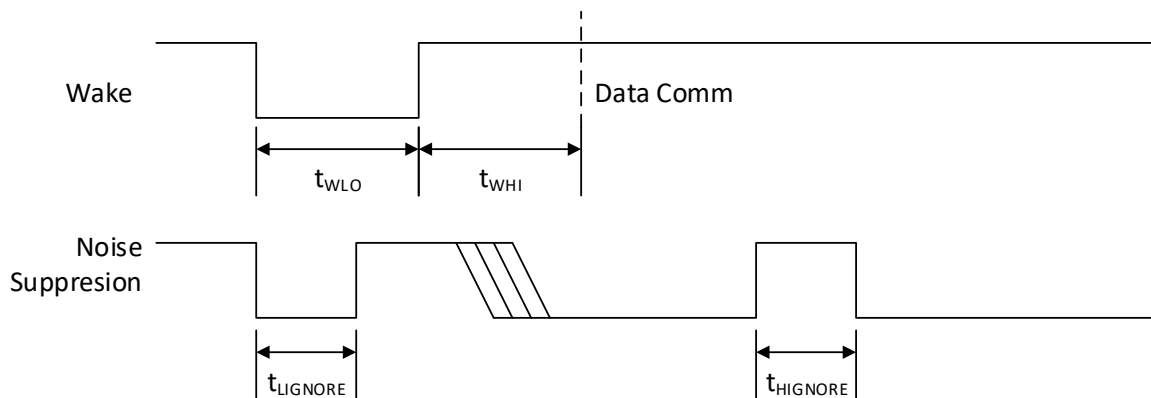


Table 2-2. AC Parameters⁽³⁾

Parameter	Symbol	Direction	Min.	Typ.	Max.	Unit	Notes
Wake Low Duration ⁽⁴⁾	t_{WLO}	To ATSHA206A	60	—	—	μs	Minimum time to guarantee wake under all conditions.
Wake High Delay to Data Comm.	t_{WHI}	To ATSHA206A	2.5	—	—	ms	SIO should be stable and $> V_{SIO}$ for this entire duration.
High-Side Glitch Filter at Active ⁽²⁾	$t_{HIGNORE_IO}$	To ATSHA206A	45	—	—	ns	Pulses shorter than this in width will be ignored by the device when in Active mode.
Low-Side Glitch Filter at Active ⁽²⁾	$t_{LIGNORE_IO}$	To ATSHA206A	45	—	—	ns	Pulses shorter than this in width will be ignored by the device when in Active mode.
High-Side Glitch Filter at Sleep	$t_{HIGNORE_S}$	To ATSHA206A	15	—	—	μs	Pulses shorter than this in width will be ignored by the device when in Sleep mode.
Low-Side Glitch Filter at Sleep	$t_{LIGNORE_S}$	To ATSHA206A	15	—	—	μs	Pulses shorter than this in width will be ignored by the device when in Sleep mode.
Watchdog Reset ⁽¹⁾	$t_{WATCHDOG}$	To ATSHA206A	0.7	1.3	1.7	s	Maximum time from wake until the device is forced into Sleep mode.

Notes:

1. These parameters are ensured through characterization but not tested in production.
2. “Active” refers to either I/O mode or Compute mode, as opposed to Sleep mode.
3. V_{SIO} means the high level to which SIO is driven during the I/O mode. The driver could be either the totem pole driver on the MCU or the resistor when the ATSHA206A returns data.
4. When the device is in Sleep mode, pulses $\leq t_{WLO}$ but $\geq t_{LIGNORE_S}$ may cause the device to wake up and transition to the I/O mode. When in the I/O mode, the device is designed to ensure that no legal t_{START} or t_{ZLO} low pulse will cause the device to reset.

Figure 2-2. AC Data Transfer Timing Diagram

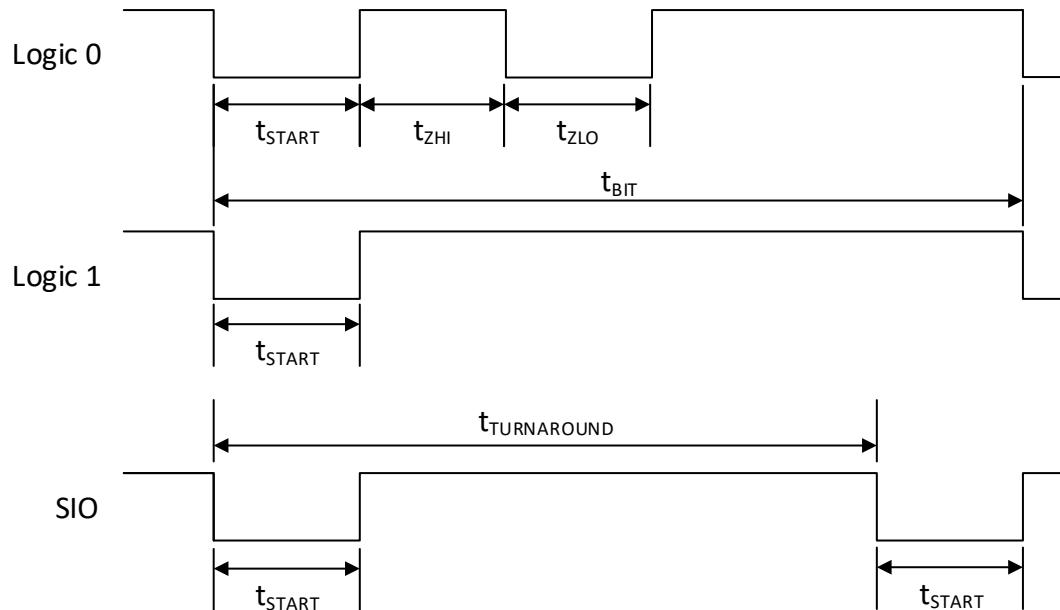


Table 2-3. AC Data Transfer Parameters

Applicable from $T_A = -5^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SIO} = +2.0\text{V}$ to $+4.2\text{V}$, $C_L = 100\text{ pF}^{(2)}$ (unless otherwise noted).

Parameter	Symbol	Direction	Min.	Typ.	Max.	Unit	Notes
Start Pulse Duration	t_{START}	To ATSHA206A	4.10	4.34	4.56	μs	Note 1
		From ATSHA206A	4.60	6.00	8.60	μs	Note 1
Zero Transmission High Pulse	t_{ZHI}	To ATSHA206A	4.10	4.34	4.56	μs	Note 1
		From ATSHA206A	4.60	6.00	8.60	μs	Note 1
Zero Transmission Low Pulse	t_{ZLO}	To ATSHA206A	4.10	4.34	4.56	μs	Note 1
		From ATSHA206A	4.60	6.00	8.60	μs	Note 1
Bit Time	t_{BIT}	To ATSHA206A	37	39	—	μs	Note 1
		From ATSHA206A	41	54	78	μs	Note 1
Turnaround Delay	$t_{TURNAROUND}$	From ATSHA206A	64	80	131	μs	The ATSHA206A initiates the first low-going transition after this time interval following the start of the last bit (t_{BIT}) of the Transmit flag.
		To ATSHA206A	93	—	—	μs	After the ATSHA206A transmits the last bit of a block, the system must wait this interval before sending the first bit of a flag.

Notes:

1. t_{START} , t_{ZLO} , t_{ZHI} , and t_{BIT} are designed to be compatible with a standard UART running at 230.4 Kbaud for both transmit and receive. The UART should be set to seven data bits, no parity, and one Stop bit.
2. All performance parameters assume $C_L \leq 100$ pF. Bus capacitance exceeding 100 pF will reduce performance, both of AC and DC parameters.

2.4 DC Parameters

Table 2-4. DC Parameters⁽¹⁾

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Operating Temperature	T_A	-40	—	+85	°C	—
Supply Voltage ⁽²⁾	V_{SIO}	2.0	—	4.5	V	Voltage on SIO pin during computation and when high during transmission to ATSHA206A
Current Consumption during Computation	$I_{COMPUTE}$	—	500	2000	μA	-40°C → +85°C, $V_{SIO} = 4.5V$
Current Consumption during I/O Mode	I_{IO}	—	125	250	μA	-40°C → +85°C, $V_{SIO} = 4.5V$
Sleep Current ⁽³⁾	I_{SLEEP}	—	50	200	nA	When the device is in Sleep mode, $V_{SIO}^{(1)} \leq 4.5V$, $T_A \leq +85^\circ C$
Output Low Voltage	V_{OL}	—	—	0.4	V	When the device is in I/O mode, $V_{SIO}^{(1)} = 3.0$ to $4.5V$
Output Low Current	I_{OL}	—	—	4	mA	When the device is in I/O mode, $V_{SIO}^{(1)} = 3.0$ to $4.5V$, $V_{OL} = 0.4V$
Input Low Voltage	V_{IL}	GND - 0.3	—	$V_{SIO} \times 0.3$	V	—
Input High Voltage	V_{IH}	$V_{SIO} \times 0.7$	—	4.5	V	—

Notes:

1. V_{SIO} is the high level to which SIO is driven during I/O mode. The driver could be either (or both) the totem pole driver on the MCU or the resistor when the ATSHA206A returns data. This is also the value that should be connected to the pull-up resistor on the SIO signal.
2. During power-up from sleep, or from a prolonged low period on SIO, the ATSHA206A will self-configure and may consume up to 500 μA for t_{WHI} . The V_{SIO} high level must be maintained during this phase.
3. I_{SLEEP} varies exponentially with temperature. The highest sleep current occurs at +85°C.

3. Compatibility with ATSHA204A

The ATSHA206A is designed specifically to implement use cases associated with the authentication of disposable units, ecosystem control and anti-cloning. The commands of the ATSHA206A follow the same structure as other Microchip CryptoAuthentication products, but the number of commands and the flexibility of those commands have been significantly reduced from that of the ATSHA204A, due to the reduced application space. This simplifies the use of the ATSHA206A relative to that of the ATSHA204A.

3.1 ATSHA206A Configuration Zone

- 88-byte configuration zone, the same size as the SHA204A.
- Nothing in the configuration zone can be directly written by the customer using the `Write` command.
- The former I²C Address byte `Config[16]` is not used and set to 0x00.
- All former slot configuration bytes `Config[20:51]` are set to 0x00 as default. These bytes do not affect the operation of the chip.
- The serial number is unique for each device. This is set at the time of the initial test, the same as the SHA204A.
- `Config[4:8]` is used to indicate whether DataStore Slots 1 and 2 are unlocked or locked. They are unique to ATSHA206A.
- Update Count and Use flags have been eliminated for Slots[0:6], `Config[52:65]`. Slot 7 (DerivedKey slot) Use flag and Update Count bytes remain, but have been renamed `DeriveKeyFlag` and `DeriveKeyCount`.
- ParentKey use operation remains the same and is associated with Slot 15.
- `ConfigLock` byte has been eliminated. `DataLock` is now 2 bytes, `Config[87:88]`.
- The device is locked at time of the test. Devices are always shipped locked.

3.2 ATSHA206A Data and OTP Zones

- Slots 0-6, 11-14 have been eliminated.
- Slot 7 has been renamed `DerivedKey` and is configured for key storage. It is the target of the `DeriveKey` command.
- Slots 8-10 have been renamed DataStore. Slots 0, 1 and 2 are set for clear text writes and can be written after the Data zone is locked.
- Slots 9-10 (DataStore Slots 1 and 2) can be individually locked via the `Write` command when `Write.Mode[5] = 1`. This was not available for the SHA204A.
- Slot 15 is configured as the ParentKey slot to hold the Secret Key.
- The OTP zone has been eliminated.

3.3 ATSHA206A Command Differences

- `CheckMac`, `GenDig`, `HMAC`, `Lock`, `Nonce`, `Pause`, `Random`, `SHA`, and `UpdateExtra` commands have been removed.
- The `DeriveKey` command uses the key in Slot 15 (ParentKey slot) and various constants to derive a key and store it in Slot 7 (DerivedKey slot). `Param1` and `Param2` have no effect on the operation of the command. There is no flexibility in source and target locations.
- The `MAC` command computes a digest of Slot 7 and outputs the digest. `Param1` and `Param2` values have no effect on operation.
- The `Nonce` command is a null operation and does not generate an output.
- The `Read` command operates the same as the SHA204A but the slots in which it can be read are limited. All the configuration zones can be read.
- The `Write` command is limited to writing Slots 8-10 (DataStore Slots 0, 1 and 2), once the part has been locked and/or shipped.

4. Package Marking Information

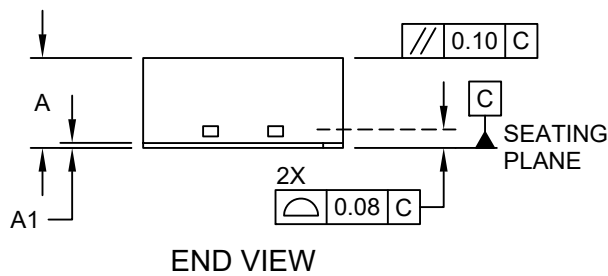
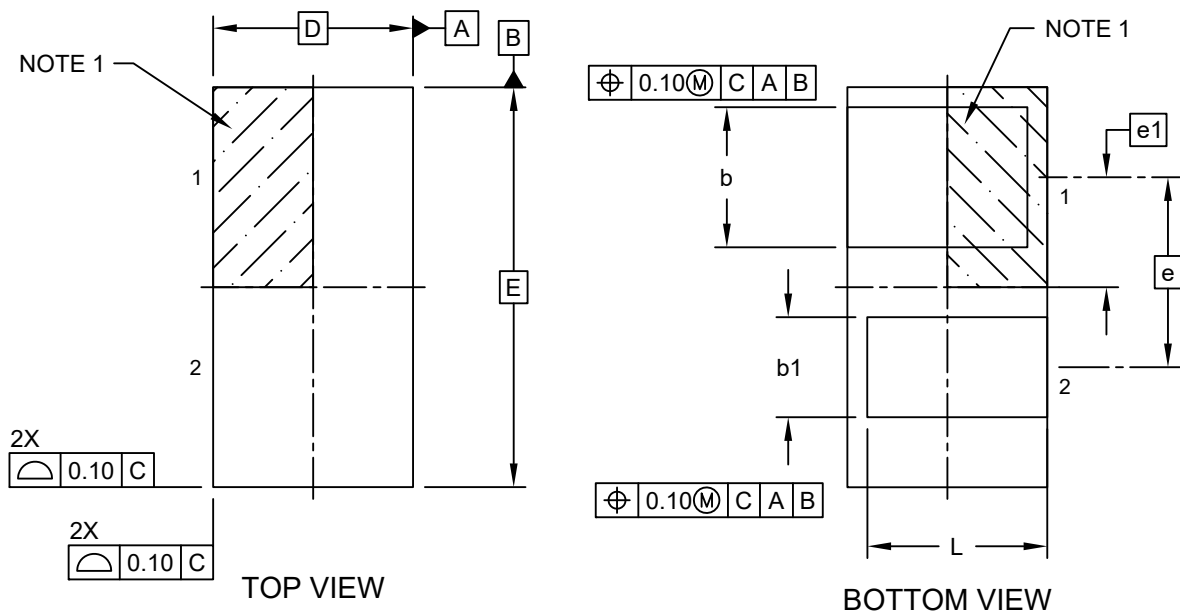
As part of Microchip's overall security features the part mark for all crypto devices is intentionally vague. The marking on the top of the package does not provide any information as to the actual device type or the manufacturer of the device. The alphanumeric code on the package provides manufacturing information and will vary with assembly lot. The packaging mark should not be used as part of any incoming inspection procedure.

5. Package Drawings

5.1 2-Lead VSFN Package

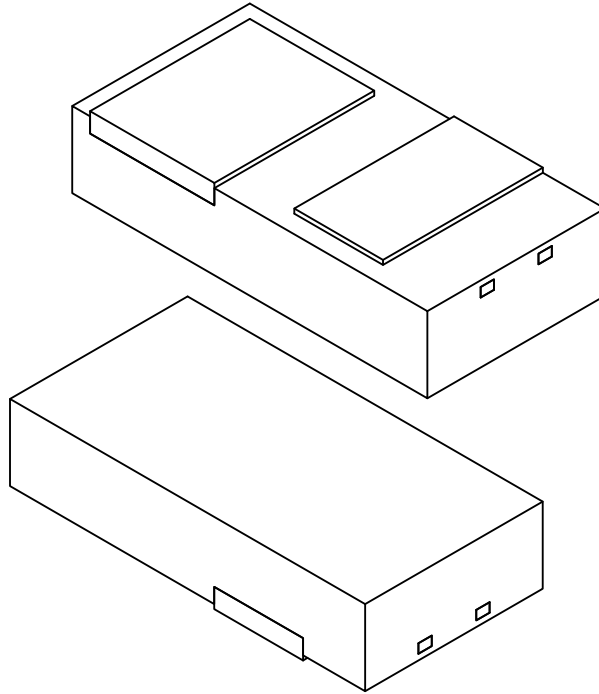
**2-Lead Very Thin Single Flat, No Lead Package (LYB) - 2x4 mm Body [VSFN]
 Atmel Legacy Global Package Code RWX**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



2-Lead Very Thin Single Flat, No Lead Package (LYB) - 2x4 mm Body [VSFN] Atmel Legacy Global Package Code RWX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	2		
Pitch	e	1.90 BSC		
Terminal 1 Center to Body Center	e1	1.10 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	-	-	0.05
Overall Length	D	2.00 BSC		
Overall Width	E	4.00 BSC		
Terminal 1 Width	b	1.35	1.40	1.45
Terminal 2 Width	b1	0.95	1.00	1.05
Terminal Length	L	1.75	1.80	1.85

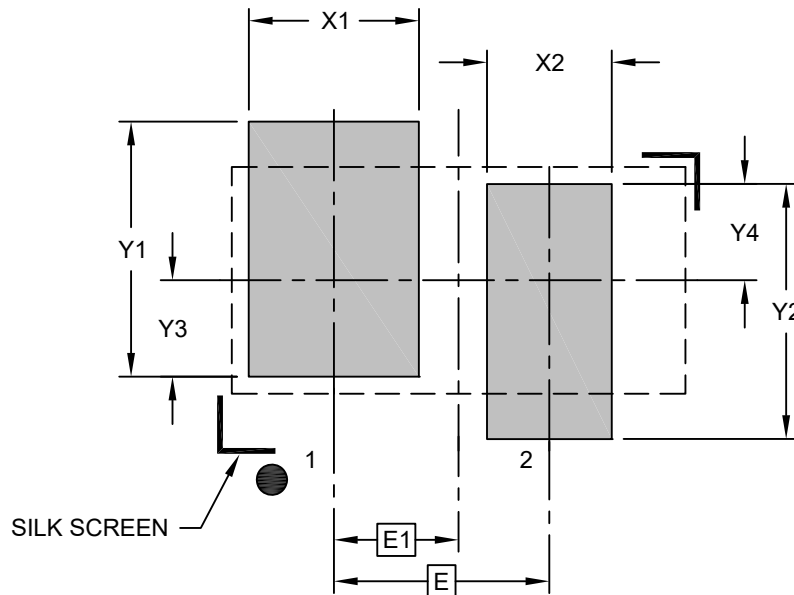
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21315-LYB Rev D Sheet 2 of 2

2-Lead Very Thin Single Flat, No Lead Package (LYB) - 2x4 mm Body [VSFN]
Atmel Legacy Global Package Code RWX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.90 BSC		
Contact Pitch	E1	1.10 BSC		
Contact Pad Width	X1			1.50
Contact Pad Width	X2			1.10
Contact Pad Length	Y1			2.25
Contact Pad Length	Y2			2.25
Package Center to Contact Pad Edge	Y3			0.85
Package Center to Contact Pad Edge	Y4			0.85

Notes:

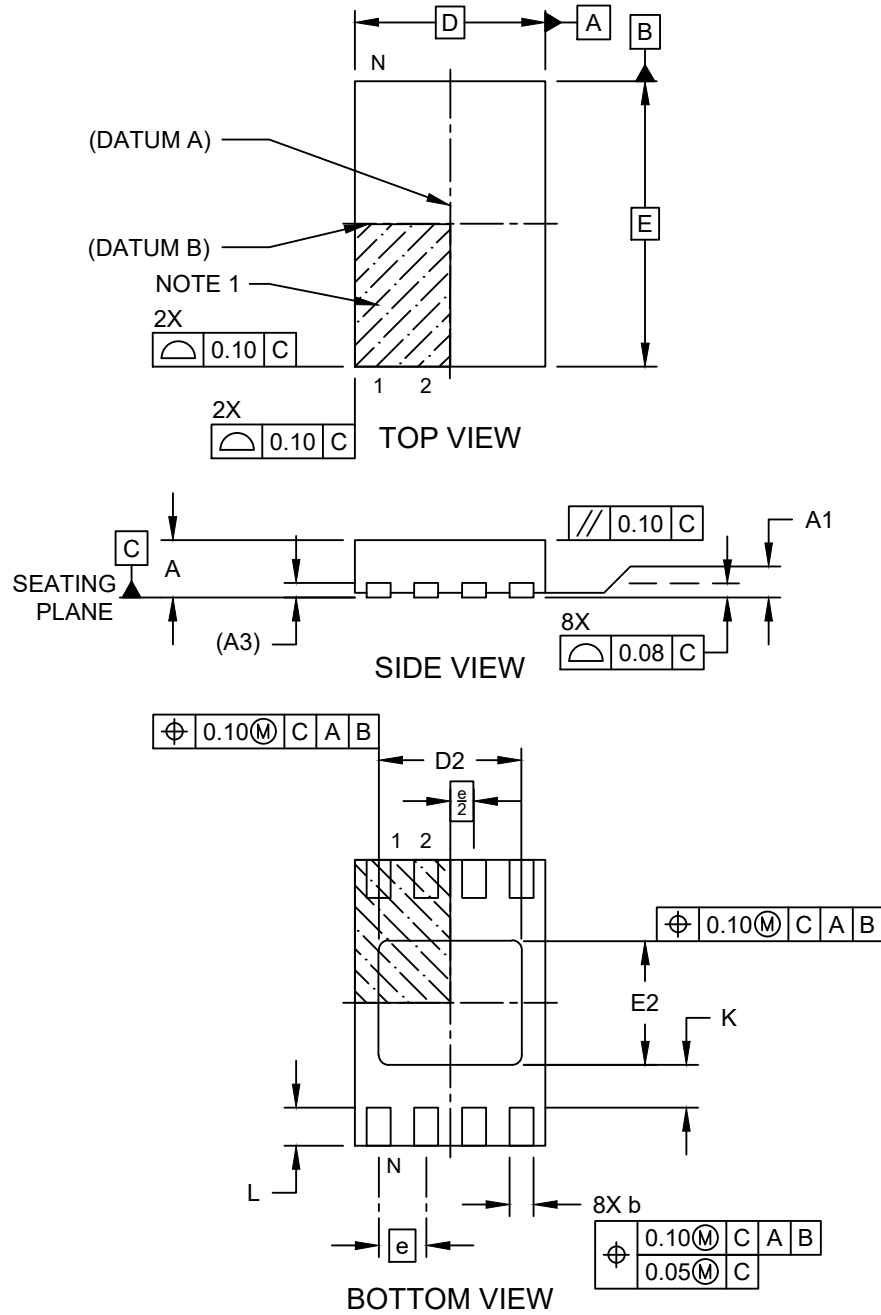
1. Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23315-LYB Rev D

5.2 8-pad UDFN

**8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
 Atmel Legacy Global Package Code YNZ**

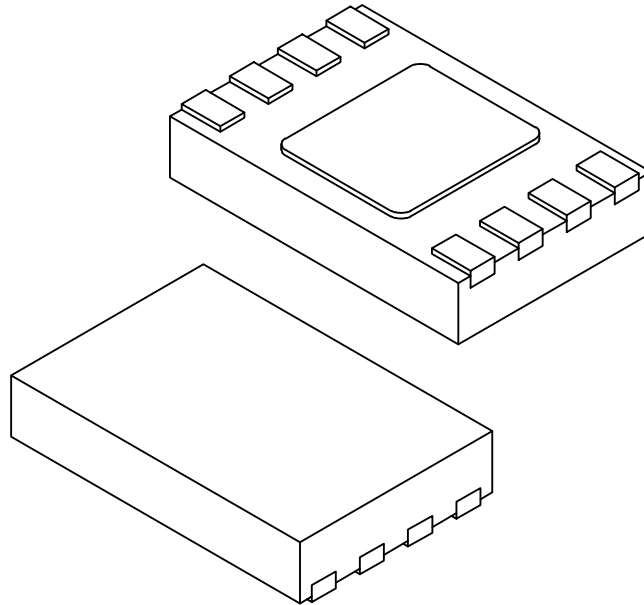
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21355-Q4B Rev B Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

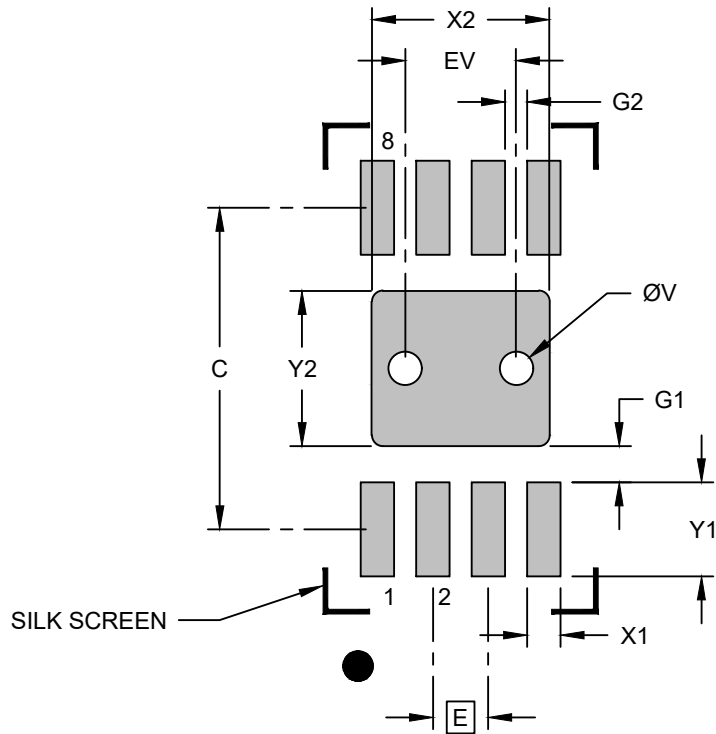
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev B Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev B

6. Revision History

Revision C (March 2021)

- Removed the TSB (MGH) package
- Updated the UDFN package option

Revision B (April 2020)

- Removed WLCSP Packaging Outline Drawing
- Added ESD information to Absolute Maximum Ratings
- Updated VSFN Package Diagram

Revision A (December 2019)

Original release of this document

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XXX	XX	-X
Device	Package	Customer Code	Tape and Reel

Device:	ATSHA206A: Cryptographic Co-Processor with Secure Hardware-Based Key Storage	
Package Options	MBH	2RC-2, 2-Pad, 4.0 x 2.00 mm Body, 0.90 mm Maximum Thickness, Very Thin Single Flat No Lead Package (VSFN)
	MAH	8-Pad, 2.0 x 3.0 mm Body with Exposed Paddle UDFN
	—	4-Ball Wafer Level CSP ⁽³⁾
Customer Code	<xx>	Unique two digit alphanumeric code for each customer. This will be assigned by Microchip.
Delivery Options	B	Bulk
	S	Sample Devices in Tape and Reel

Examples:

- ATSHA206A-MAH1X-S: 8-PAD 2.0 x 3.0 mm UDFN Package. Sample Devices Sold in Tape and Reel Format. NOT FOR PRODUCTION.
- ATSHA206A-MBH1X-B: 2-Pad 4.0 x 2.00 mm body VSFN Package. Sample Devices Sold in Bulk Only. NOT FOR PRODUCTION.
- ATSHA206A-MBH<xx>-B: 2-Pad 4.0 x 2.00 mm body VSFN Package. Customer Specific Ordering Code Format. Sold in Bulk.

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability with the Tape and Reel option.
2. Sample units and customer units are only provided in Bulk format. Tape and Reel options are not currently available.
3. Contact your Microchip sales office if interested in the WLCSP package.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
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