



ATXP3

Jumper Free Over Clock Controller

Datasheet

Release Date: Jan. 2005

Revision: 2.2

Revision History

Version	Date	Changes from Last Version
1.0	Aug/30/2001	
1.01	Oct/18/2001	1. Modified pin names as followed: VCORE LEVEL
2.0	Oct/29/2001	1. Specification Change: Eliminate Level pin and add one GPIO pin 2. Pin assignment change See page 2 for details
2.1	June/9/2003	1. Modify Package Information: → From "E=> Dimension in mm: 0.635 BASIC; Dimension in inch: 0.025 BASIC" to "e => Dimension in mm: 0.635 BASIC; Dimension in inch: 0.025 BASIC"
2.2	Jan/25/2005	Add "Ordering Information" about green device description



Table of Contents

1. General Description.....	1
2. Features.....	1
3. Package Configuration.....	2
4. Pin Description.....	3
5. Package Information.....	5



Figures

Figures 1. ATXP3 Pin Diagram (Top View)..... 2

Tables

Table 1. Pin Description Table..... 3

1. General Description

ATXP3 is a full feature of over clocking device for Intel[®] CPU. It integrates all functions that are possible to be utilized for over-clocking purpose.

2. Features

- Provide Five VID Input (VIDIN0-4) and Five VID Output (VIDOUT0-4) Pins
- Support Auto-Recover
 - Build-in Watch Dog Timer & Reset Output Signal Pin
- Provide Ten GPIO Pins
- SM Bus Interface
- Provide CPU Changing Detect Pin (SLOT0CC#)
- Package: SSOP 28-Pin

3. Pin Configuration

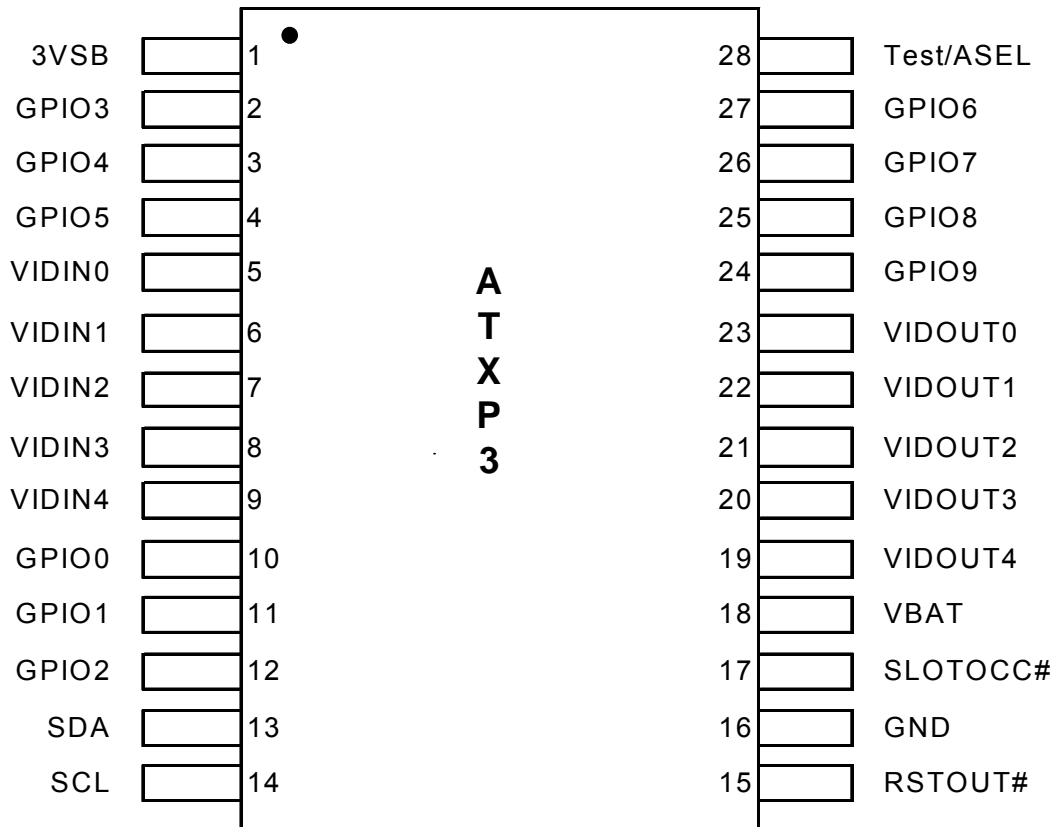


Figure 1. ATXP3 Pin Diagram (Top View)

Ordering Information

ATXP3- Commercial Standard

ATXP3G- Green Device with Commercial Standard

4. Pin Description

I/O Type Description

IN _{tx}	---- Special level input.
IN _t	---- TTL level input.
IN _{ts}	---- TTL level input with Schmitt-tigger.
OD ₁₂	---- Open-drain with 12mA sink current.
O ₁₂	---- Output buffer with 12mA drive/sink current
I/OD ₁₂	---- TTL level bi-directional pin, and open-drain output with 12mA sink current.
I/O ₁₂	---- TTL level bi-directional pin, and output with 12mA drive/sink current.
I/O _{12-10k-up}	---- TTL level bi-directional pin, and output with 12mA drive/sink current and 10K ohm pull-up resistor.

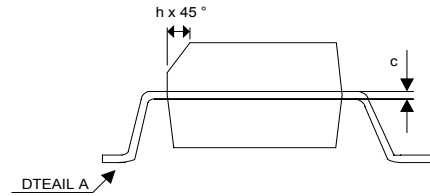
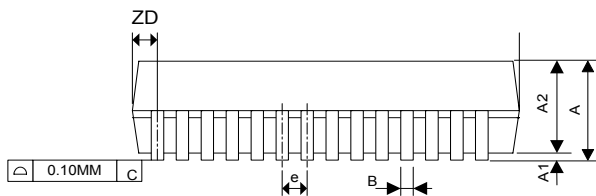
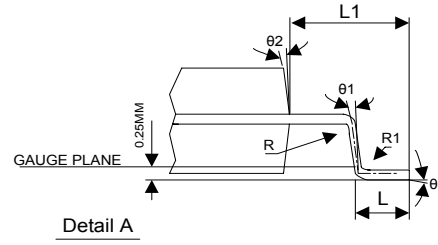
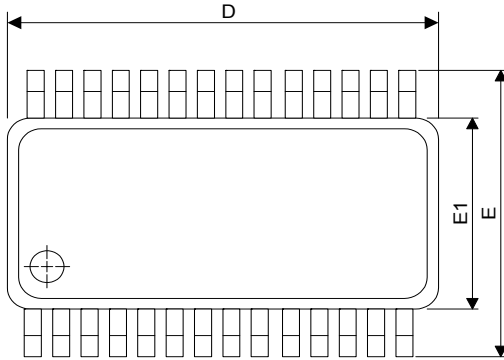
Pin No.	Pin name	I/O Type	Function
1	3VSB	POWER	Power Pin
2	GPIO3	I/O ₁₂	General Purpose I/O Pin
3	GPIO4	I/O ₁₂	General Purpose I/O Pin
4	GPIO5	I/O ₁₂	General Purpose I/O Pin
5	VIDIN0	IN _{tx}	Receive VID0 Signal from CPU
6	VIDIN1	IN _{tx}	Receive VID1 Signal from CPU
7	VIDIN2	IN _{tx}	Receive VID2 Signal from CPU
8	VIDIN3	IN _{tx}	Receive VID3 Signal from CPU
9	VIDIN4	IN _{tx}	Receive VID4 Signal from CPU
10	GPIO0	I/O ₁₂	General Purpose I/O Pin
11	GPIO1	I/O ₁₂	General Purpose I/O Pin
12	GPIO2	I/O ₁₂	General Purpose I/O Pin
13	SDA	I/OD ₁₂	SMB Data Signal
14	SCL	IN _{ts}	SMB Clock Signal
15	RSTOUT#	OD ₁₂	
16	GND		GROUND Pin
17	SLOT0CC#	IN _{ts}	Receive SLOT0CC# From CPU
18	VBAT		Power Pin
19	VIDOUT4	OD ₁₂	VID4 Signal Output Pin to PWM
20	VIDOUT3	OD ₁₂	VID3 Signal Output Pin to PWM
21	VIDOUT2	OD ₁₂	VID2 Signal Output Pin to PWM
22	VIDOUT1	OD ₁₂	VID1 Signal Output Pin to PWM
23	VIDOUT0	OD ₁₂	VID0 Signal Output Pin to PWM
24	GPIO9	I/O ₁₂	General Purpose I/O Pin
25	GPIO8	I/O ₁₂	General Purpose I/O Pin



26	GPIO7	I/O ₁₂	General Purpose I/O Pin
27	GPIO6	I/O ₁₂	General Purpose I/O Pin
28	Test/ASEL	POWER	Power Pin

Table1. Pin Description Table

5. Package Information SSOP-28 Outline Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			0.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
H	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
	0°		8°	0°		8°
1	0°			0°		
2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AF)					



Technology Corporation

Copyright © 2000 Attansic Technology Corp.

The materials contained in this document replace all previous documentation issued for the related products included herein. Please contact Attansic Technology Corp. for the latest documents.

Attansic is the trademark of Attansic Technology Corp.

All specifications are subject to change without notice.

Additional copies of this document or other Attansic literatures may be obtained from:

**3FL., No.147, Hsien Cheng 9th Rd,
Chu-Pei, Hsin-Chu Hsien, Taiwan**

Tel: 886-3-5545660

Fax: 886-3-5545661

To find out more about Attansic, visit our World Wide Web address at:

<http://www.attansic.com.tw/>