Features

- **High-performance, Low-power AVR® 8-bit Microcontroller**
- **RISC Architecture**
  - **90 Powerful Instructions - Most Single Clock Cycle Execution**
  - **32 x 8 General Purpose Working Registers**
  - **Fully Static Operation**
- **Nonvolatile Program and Data Memories**
  - **1K Bytes of In-System Programmable Program Memory Flash**
    Endurance: 1,000 Write/Erase Cycles
  - **64 bytes of In-System Programmable EEPROM**
    Endurance: 100,000 Write/Erase Cycles
  - **Programming Lock for Flash Program and EEPROM Data Security**
- **Peripheral Features**
  - **Two 8-bit Timers/Separate Prescalers**
    One High-speed (100 kHz) PWM Output
  - **4-channel 10-bit ADC**
    One Differential Voltage Input with Optional Gain of 20X
  - **On-chip Analog Comparator**
  - **Programmable Watchdog Timer with On-chip Oscillator**
- **Special Microcontroller Features**
  - **In-System Programmable via SPI Port**
  - **External and Internal Interrupt Sources**
  - **Low-power Idle, Noise Reduction and Power Down Modes**
  - **Enhanced Power-on Reset Circuit**
  - **Programmable Brown-out Detection Circuit**
  - **Internal 1.6 MHz Tuneable Oscillator**
  - **Internal 25.6 MHz Clock Generator for Timer/Counter 1**
- **I/O and Packages**
  - **8-pin PDIP/SOIC: 6 Programmable I/O Lines**
- **Operating Voltages**
  - **2.7V - 5.5V (ATtiny15L)**
  - **4.0V - 5.5V (ATtiny15)**
- **Commercial and Industrial Temperature Ranges**

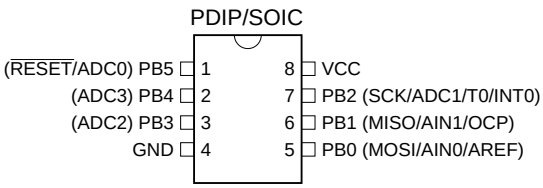
Description

The ATtiny15 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny15 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed

(continued)

Pin Configurations



8-bit AVR® Microcontroller with 1K Bytes Flash

ATtiny15

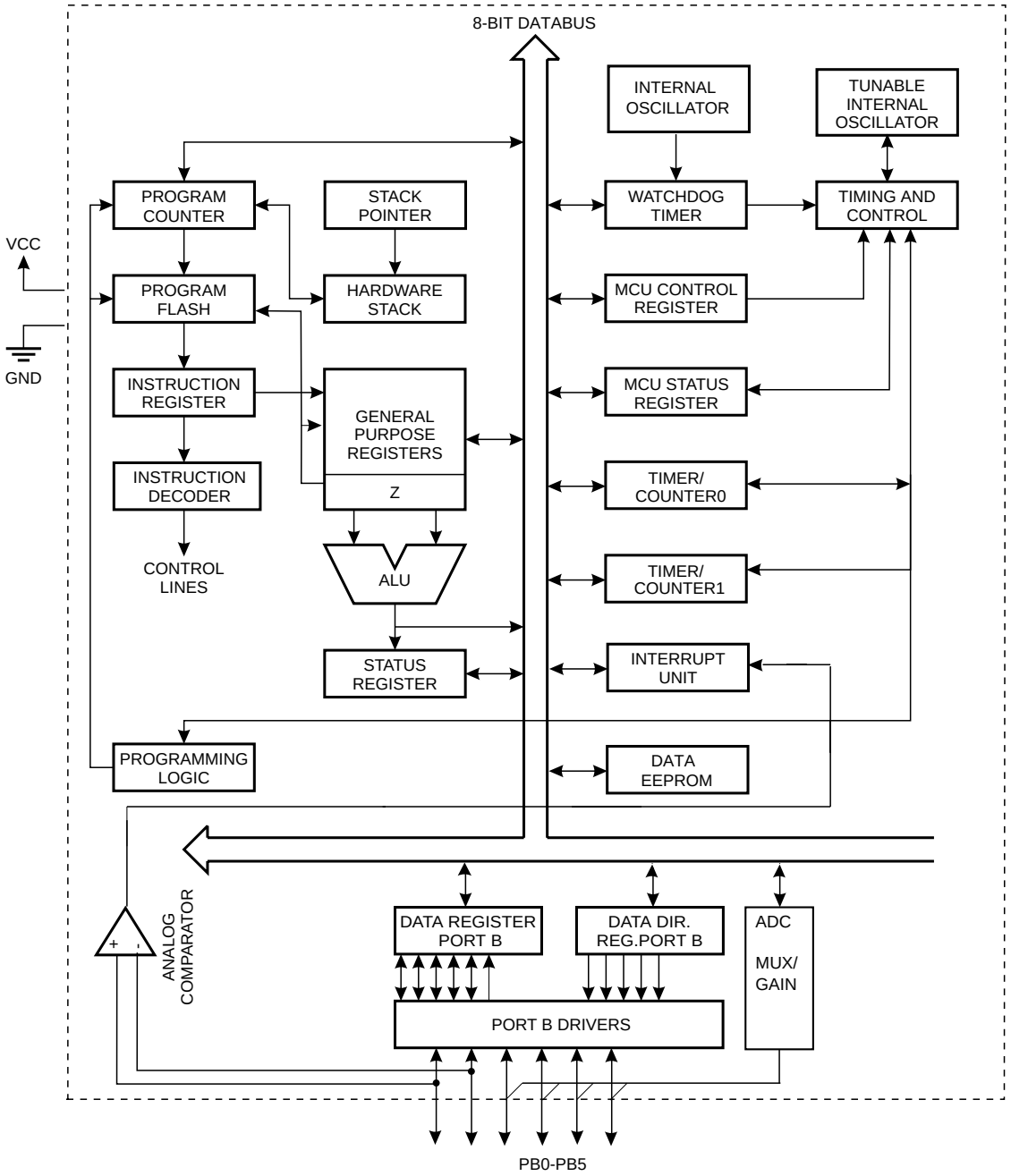
Advance Information

Rev. 1187A–08/99

in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers. The ATtiny15 has a high precision ADC with up to 4 single ended channels and 1 differential channel with up to 20X gain. In addition, the high speed PWM output makes the ATtiny15 ideal for battery charger applications and power regulation circuits.

Block Diagram

Figure 1. The ATtiny15 Block Diagram



The ATtiny15 provides 1K bytes of Flash, 64 bytes EEPROM, 6 general purpose I/O lines, 32 general purpose working registers, two 8-bit timer/counters, one with PWM output, internal oscillators, internal and external interrupts, programmable Watchdog Timer, 4-channel, 10-bit Analog to Digital Converter with one differential voltage input gain stage, and three software selectable power saving modes. The Idle Mode stops the CPU while allowing the timer/counters and interrupt system to continue functioning. The Power Down mode saves the register contents but freezes the oscillators, disabling all other chip functions until the next interrupt or hardware reset. The wakeup or interrupt on pin change features enable the ATtiny15 to be highly responsive to external events, still featuring the lowest power consumption while in the power down mode. The ATtiny15 also has a dedicated ADC Noise Reduction Mode for reducing the noise in ADC conversion. In this Sleep Mode, only the ADC is functioning.

The device is manufactured using Atmel's high density nonvolatile memory technology. By combining an enhanced RISC 8-bit CPU with Flash on a monolithic chip, the Atmel ATtiny15 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny15 AVR is supported with a full suite of program and system development tools including: macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB5..PB0)

Port B is a 6-bit I/O port. PB4..0 are I/O pins that can provide internal pull-ups (selected for each bit). PB5 is input only. The use of pin PB5 is defined by a fuse. The special functions associated with this pin is external Reset or ADC Input Channel0.

Port B also accommodates analog I/O pins.

Analog Pins

Up to four analog inputs can be selected as inputs to the Analog to Digital Converter (ADC).

Table 1. Port B Alternate Functions

Port Pin	Alternate Function
PB0	MOSI (SPI Data Input) AIN0 (Analog Comparator Input Channel 0) VREF (ADC Voltage Reference)
PB1	MISO (SPI Data Output) AIN1 (Analog Comparator Input Channel 1) OCP(T/C1 PWM Output)
PB2	SCK (SPI Clock Input) INT0 (Ext. Interrupt 0 Input) ADC1 (ADC Input Channel 1) T0 (Timer/Counter 0 External Counter Input)
PB3	ADC2 (ADC Input Channel 2)
PB4	ADC3 (ADC Input Channel 3)
PB5	RESET (Ext. Reset Input) ADC0 (ADC Input Channel 0)

Internal Oscillators

The internal oscillator provides nominal 1.6 MHz clock rate for the system clock CK. Due to large initial variation (0.8 MHz to 1.6 MHz) of the internal clock, a tuning capability is built in. Through a 8-bit control register OSCCAL, the system clock rate can be tuned with less than 1% steps of the nominal clock.

An internal PLL provides a 16x clock rate from the system clock (CK) for the use of the Peripheral Timer/Counter1. The maximum frequency of this peripheral clock, PCK, is 25.6 MHz.

Reset and Interrupt Handling

The ATtiny15 provides 9 different interrupt sources. These interrupts and the separate reset vector, each have a separate program vector in the program memory space. All the interrupts are assigned individual enable bits which must be set (one) together with the I-bit in the status register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 2. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 - the External Interrupt Request 0 etc.

Table 2. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	External Pin Reset, Power-on Reset, Brown-out Reset and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	I/O Pins	Pin Change Interrupt
4	$003	TIMER1, COMP	Timer/Counter1 Compare Match
5	$004	TIMER1, OVF	Timer/Counter1 Overflow
6	$005	TIMER0, OVF	Timer/Counter0 Overflow
7	$006	EE_RDY	EEPROM Ready
8	$007	ANA_COMP	Analog Comparator
9	$008	ADC	ADC Conversion Complete

Reset Sources

The ATtiny15 has four sources of reset:

- Power-on Reset—The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POT}).
- External Reset—The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than 500 ns.
- Watchdog Reset—The MCU is reset when the Watchdog timer period expires, and the Watchdog is enabled.
- Brown-out Reset—The MCU is reset when the supply voltage V_{CC} falls below the Brown-out detection level.

Power-on Reset

A Power-on Reset (POR) pulse is generated by an on-chip detection circuit. The detection level is nominally 2.2V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset as well as detect a failure in supply voltage.

A Power-on Reset (POR) circuit ensures that the device is not started until V_{CC} has reached a safe level. Reaching the safe level invokes a delay counter which determines the delay, for which the device is kept in RESET after V_{CC} rise. The time-out period of the delay counter can be defined by the user through CKSEL fuses. The four different selections for the delay period are presented in Table 3. The RESET signal is activated again, without any delay, when the V_{CC} decreases below detection level.

Table 3. Reset Delay Selections

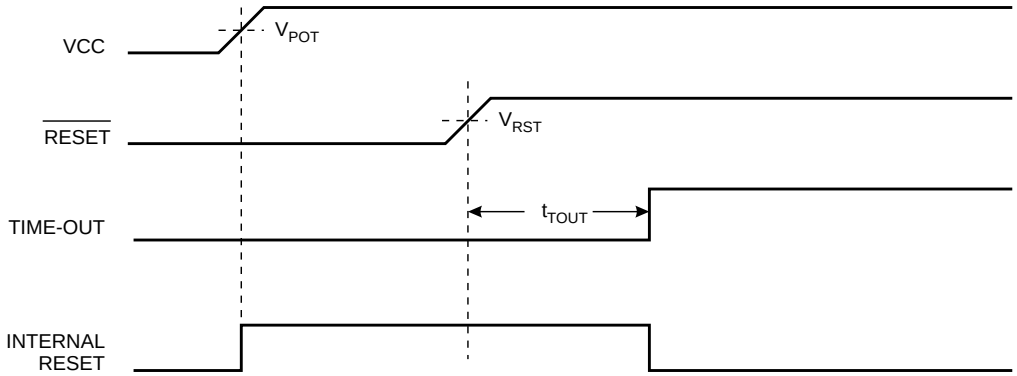
CKSEL [1:0]	Start-up Time, t_{TOUT} at V_{CC} = 2.7V	Start-up Time, t_{TOUT} at V_{CC} = 5.0V	Recommended Usage
00	128 µs + 18CK	32 µs + 18 CK	BOD enabled
01	16 ms + 18 CK	4 ms + 18 CK	BOD disabled, quickly rising power
10	256 ms + 18 CK	64 ms + 18 CK	BOD disabled, slowly rising power
11	256 ms + 1K CK	64 ms + 1K CK	BOD disabled, slowly rising power

Brown-out Detection

ATtiny15 has an on-chip brown-out detection (BOD) circuit for monitoring the V_{CC} level during the operation. The BOD circuit can be enabled/disabled by the fuse BODEN. When BODEN is enabled (BODEN programmed), and V_{CC} decreases below the trigger level, the brown-out reset is immediately activated. When V_{CC} increases above the trigger level, the brown-out reset is deactivated after a delay. The delay is defined by the user in the same way as the delay of POR signal, in Table 3. The trigger level for the BOD can be selected by the fuse BODLEVEL to be 2.7V (BODLEVEL unprogrammed), or 4.0V (BODLEVEL programmed). The trigger level has a hysteresis of 50 mV to ensure spike free brown-out detection.

The BOD circuit will only detect a drop in Vcc if the voltage stays below the trigger level for longer than 3 µs for trigger level 4.0V, 7 µs for trigger level 2.7V (typical values).

Figure 2. MCU Start-Up, $\overline{\text{RESET}}$ Controlled Externally



Pin Change Interrupt

The pin change interrupt is triggered by any change on any input or I/O pin. Change on pins will cause an interrupt if the pin is configured as input or I/O, as described in the section “Pin Descriptions”. Observe that, if enabled, the interrupt will trigger even if the changing pin is configured as an output. This feature provides a way of generating a software interrupt. Also observe that the pin change interrupt will trigger even if the pin activity triggers another interrupt, for example the external interrupt. This implies that one external event might cause several interrupts.

Sleep Modes

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, The CPU is then halted for 4 cycles, it executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the register file and I/O memory are unaltered. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset vector.

Table 4. Sleep Modes

SM1	SM0	Sleep Mode
0	0	Idle Mode
0	1	ADC Noise Reduction Mode
1	0	Power Down Mode
1	1	Reserved

Timer/Counters

The ATtiny15 provides two general purpose 8-bit Timer/Counters. The Timer/Counters have separate prescaling selection from the 10-bit prescaling timer. The Timer/Counter0 uses internal clock (CK) as the clock timebase.

The 8-bit Timer/Counter0

The 8-bit Timer/Counter0 is equal to the Timer/Counter0 of the ATtiny12.

8-bit Timer/Counter1

The 8-bit Timer/Counter1 can select clock source from high speed PCK, or prescaled PCK. The fifteen different prescaled selections are shown in Table 6. The clock can also be stopped as described in the specification for the Timer/Counter Control Register TCCR1.

The different status flags (overflow, compare match) are found in the Timer/Counter Interrupt Flag Register - TIFR. Control signals are found in the Timer/Counter Control Register TCCR1. The interrupt enable/disable settings are found in the Timer/Counter Interrupt Mask Register - TIMSK.

The Timer/Counter supports an Output Compare function using the Output Compare Register OCR10 as the data source to be compared to the Timer/Counter1 contents. The Output Compare function includes optional clearing of the counter on compare match, and action on the Output Compare Pin - PB1(OCP) - on compare match.

Timer/Counter1 can also be used as an 8-bit Pulse Width Modulator. In this mode, Timer/Counter1 and the two output compare registers serve as a stand-alone PWM.

The Timer/Counter1 Control Register - TCCR1

Bit	7	6	5	4	3	2	1	0	
$30 ($50)	**CTC1**	**PWM1**	**COM11**	**COM10**	**CS13**	**CS12**	**CS11**	**CS10**	**TCCR1**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - CTC1: Clear Timer/Counter on Compare Match**

When the CTC1 control bit is set (one), Timer/Counter1 is reset to $00 in the CPU clock cycle after a compare match. If the control bit is cleared, Timer/Counter1 continues counting and is unaffected by a compare match.

- **Bit 6 - PWM1: Pulse Width Modulator Enable**

When set (one) this bit enables PWM mode for Timer/Counter1. This mode is described on page 8.

- **Bits 5,4 - COM11, COM10: Compare Output Mode, bits 1 and 0**

The COM11 and COM10 control bits determins any output pin action following a compare match in Timer/Counter1. Output pin actions affect pin PB1(OC1). Since this is an alternative function to an I/O port, the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 5.

Table 5. Compare Mode Select

COM11	COM10	Description
0	0	Timer/Counter disconnected from output pin OC1
0	1	Toggle the OC1 output line.
1	0	Clear the OC1 output line (to zero).
1	1	Set the OC1 output line (to one).

Note: In PWM mode, these bits have a different function. Refer to Table 7 for a detailed description.When changing the COM11/COM10 bits, the Output Compare 1 Interrupt must be disabled by clearing its Interrupt Enable bit in the TIMSK Register. Otherwise an interrupt can occur when the bits are changed.

- **Bits 3,2,1,0 - CS13, CS12, CS11, CS10: Clock Select bits 3,2,1 and 0**

The Clock Select bits 3, 2,1 and 0 define the prescaling source of Timer/Counter1.

Table 6. Timer/Counter1 Prescale Select

CS13	CS12	CS11	CS10	Description
0	0	0	0	Timer/Counter1 is stopped.
0	0	0	1	CK*16 (=PCK)
0	0	1	0	CK*8
0	0	1	1	CK*4
0	1	0	0	CK*2
0	1	0	1	CK
0	1	1	0	CK/2
0	1	1	1	CK/4
1	0	0	0	CK/8
1	0	0	1	CK/16
1	0	1	0	CK/32
1	0	1	1	CK/64
1	1	0	0	CK/128
1	1	0	1	CK/256
1	1	1	0	CK/512
1	1	1	1	CK/1024

The Stop condition provides a Timer Enable/Disable function.

The Timer/Counter1 - TCNT1

Bit	7	6	5	4	3	2	1	0	
$2F ($4F)	**MSB**							**LSB**	**TCNT1**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

This 8-bit register contains the value of Timer/Counter1.

Timer/Counter1 is realized as an up counter with read and write access. If the Timer/Counter1 is written to and a clock source is selected, it continues counting in the timer clock cycle following the write operation.

Timer/Counter1 Output Compare Register 0 - OCR10

Bit	7	6	5	4	3	2	1	0	
$2E ($4E)	MSB							LSB	OCR10
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The Output Compare Register 10 is an 8-bit read/write register.

The Timer/Counter Output Compare Register 10 contains data to be continuously compared with Timer/Counter1. Actions on compare matches are specified in TCCR1. A compare match does only occur if Timer/Counter1 counts to the OCR10 value. A software write that sets TCNT1 and OCR10 to the same value does not generate a compare match.

A compare match will set the compare interrupt flag in the CPU clock cycle following the compare event.

Timer/Counter1 Output Compare Register 1 - OCR11

Bit	7	6	5	4	3	2	1	0	
$2D ($4D)	MSB							LSB	OCR11
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	1	1	1	1	1	1	1	1	

Timer/Counter1 Output Compare Register 1 is used to limit the Timer/Counter1 full scale value in PWM mode.

Timer/Counter 1 in PWM mode

When PWM mode is selected, Timer/Counter1 and the Output Compare Registers - OCR10 and OCR11 form an 8-bit, free-running and glitch-free PWM with output on the PB1 (OC1) pin. Timer/Counter1 acts as an up counter, counting up from $00 to the value in OCR11, and starting from $00 up again. When the counter value matches the contents of the Output Compare Register 10, the PB1 (OC1) pin is set or cleared according to the settings of the COM11/COM10 bits in the Timer/Counter1 Control Registers TCCR1. Refer to Table 7 for details.

Table 7. Compare Mode Select in PWM Mode

COM11	COM10	Effect on Compare Pin
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match (non-inverted PWM). Set when TCNT1 = $00.
1	1	Set on compare match (inverted PWM). Cleared when TCNT1 = $00.

Note that in PWM mode, the Output Compare register is transferred to a temporary location when written. The value is latched when the Timer/Counter reaches OCR11. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR10 or OCR11 write.

During the time between the write and the latch operation, a read from OCR10 or OCR11 will read the contents of the temporary location. This means that the most recently written value always will read out of OCR10 and OCR11.

When OCR10 contains $00 or the value of OCR11, the output PB1 (OC1) is held low or high according to the settings of COM11/COM10. This is shown in Table 8.

Table 8. PWM Outputs OCR10 = $00 or OCR11

COM11	COM10	OCR1	Output PWMn
1	0	$00	L
1	0	OCR11	H
1	1	$00	H
1	1	OCR11	L

In PWM mode, the Timer Overflow Flag - TOV1, is set when the counter reaches the value of OCR11. Timer Overflow Interrupt 1 operates exactly as in normal Timer/Counter mode, i.e. it is executed when TOV1 is set provided that Timer Overflow Interrupt and global interrupts are enabled. This does also apply to the Timer Output Compare flag and interrupt.

The frequency of the PWM is decided by the OCR11 register and the prescaler settings. The maximum frequency with 8-bits resolution is PCK/256 = 100 kHz.

Analog Comparator

The analog comparator of the ATtiny15 is the same as the analog comparator of the ATtiny12.

Analog to Digital Converter, Analog Multiplexer and Gain Stages

The ADC can measure both differential and single-ended input voltages. The differential input channel has an optional gain step of 20X. This channel is ideal for measuring a small voltage drop across a shunt resistor in current measurements.

Four single-ended input voltage channels are also available, depending on I/O configuration.

The input selection is made by mux control bits in the ADC control register, as well as the selection of input gain. The ADC full scale voltage is V_{CC} for single ended inputs, and 2.56V for differential inputs.

Feature list:

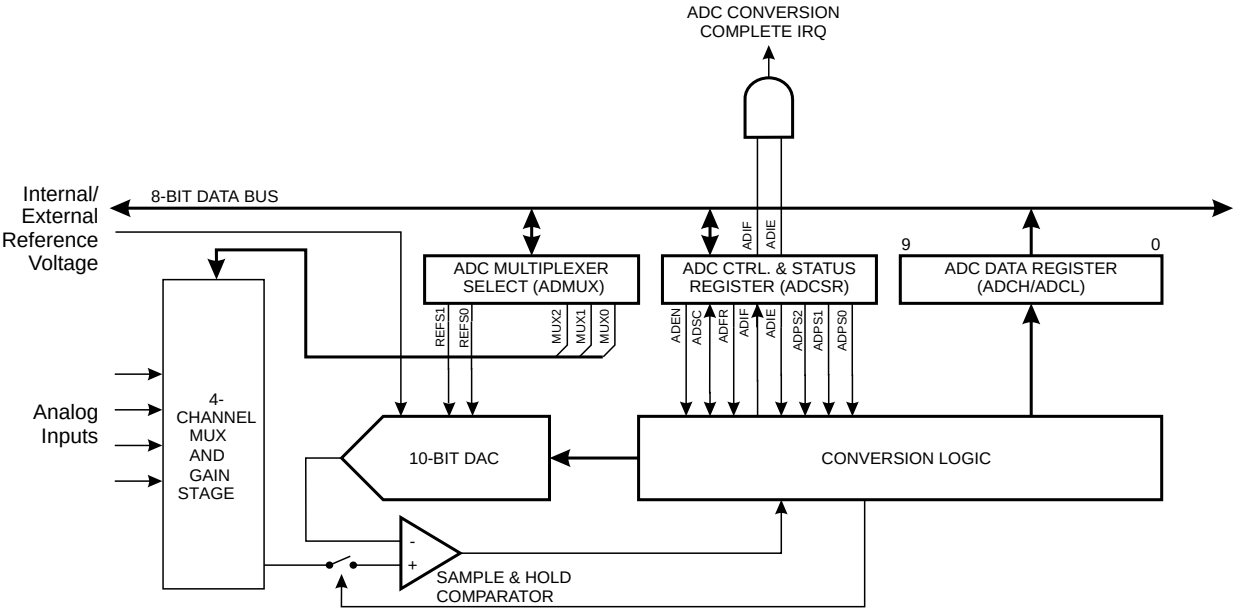
- 10-bit Resolution
- 2 LSB Absolute Accuracy
- 65 - 260 µs Conversion Time
- 4 Multiplexed Input Channels
- 2.56V Internal Voltage Reference
- 0 - 2.56V Differential Input Voltage Range
- 0 - V_{CC} Single Ended Input Voltage Range
- Free Run or Single Conversion Mode
- Interrupt on ADC Conversion Complete
- Sleep Mode Noise Canceler

The ATtiny15 features a 10-bit successive approximation ADC. The ADC is connected to a 4-channel Analog Multiplexer which allows one differential voltage input and four single-ended voltage inputs constructed from the pins of Port B. The differential input (PB3, PB4) is equipped with a programmable gain stage, providing amplification step of 26 dB (20X) on the differential input voltage before the A/D conversion. The single-ended voltage inputs at PB2..PB5 refer to 0V.

The ADC contains a Sample and Hold Amplifier which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 3.

An internal reference voltage of 2.56V is provided on-chip and this reference can optionally be externally bypassed at the AREF pin by a capacitor, for better noise performance. There is also an option to use external voltage reference and turn off the internal V_{REF}. These options are selected using the REFSn bits of the ADMUX control register.

Figure 3. ADC Block Diagram



Operation

The ADC can operate in two modes - Single Conversion and Free Running Mode. In Single Conversion Mode, each conversion will have to be initiated by the user. In Free Running Mode, the ADC is constantly sampling and updating the ADC Data Register. The ADFR bit in ADCSR selects between the two available modes.

The ADC is enabled by writing a logical one to the ADC Enable bit, ADEN in ADCSR. The first conversion that is started after enabling the ADC, will be preceded by a dummy conversion to initialize the ADC. To the user, the only difference will be that this conversion takes 25 ADC clock pulses instead of the normal 14.

A conversion is started by writing a logical one to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be set to zero by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

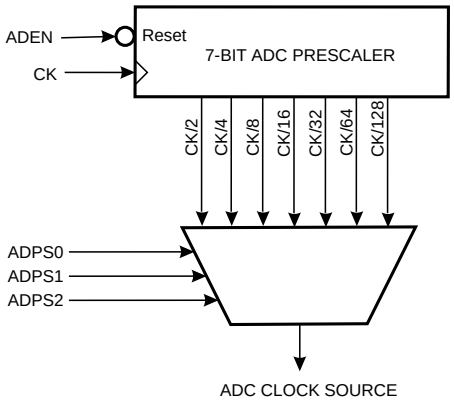
As the ADC generates a 10-bit result, two data registers, ADCH and ADCL, must be read to get the result when the conversion is complete. Special data protection logic is used to ensure that the contents of the data registers belong to the same conversion when they are read. This mechanism works as follows:

When reading data, ADCL must be read first. Once ADCL is read, ADC access to data registers is blocked. This means that if ADCL has been read, and a conversion completes before ADCH is read, none of the registers are updated and the result from the conversion is lost. When ADCH is read, ADC access to the ADCH and ADCL registers is re-enabled.

The ADC has its own interrupt which can be triggered when a conversion completes. When ADC access to the data registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result gets lost.

Prescaling

Figure 4. ADC Prescaler



The ADC contains a prescaler, which divides the system clock to an acceptable ADC clock frequency. The ADC accepts input clock frequencies in the range 50 - 200 kHz. Applying a higher input frequency will result in a poorer accuracy, typically 8 bits at 1 MHz.

The ADPS0 - ADPS2 bits in ADCSR are used to generate a proper ADC clock input frequency from any XTAL frequency above 100 kHz. The prescaler starts counting from the moment the ADC is switched on by setting the ADEN bit in ADCSR. The prescaler keeps running for as long as the ADEN bit is set, and is continuously reset when ADEN is low.

When initiating a conversion by setting the ADSC bit in ADCSR, the conversion starts at the following rising edge of the ADC clock cycle. The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of the conversion. The result is ready and written to the ADC Result Register after 13 cycles. In single conversion mode, the ADC needs one more clock cycle before a new conversion can be started, see Figure 6. If ADSC is set high in this period, the ADC will start the new conversion immediately. In Free Run Mode, a new conversion will be started immediately after the result is written to the ADC Result Register. Using Free Run Mode and an ADC clock frequency of 200 kHz gives the lowest conversion time, 65 µs, equivalent to 15.4 kSPS. For a summary of conversion times, see Table 9.

Figure 5. ADC Timing Diagram, First Conversion (Single Conversion Mode)

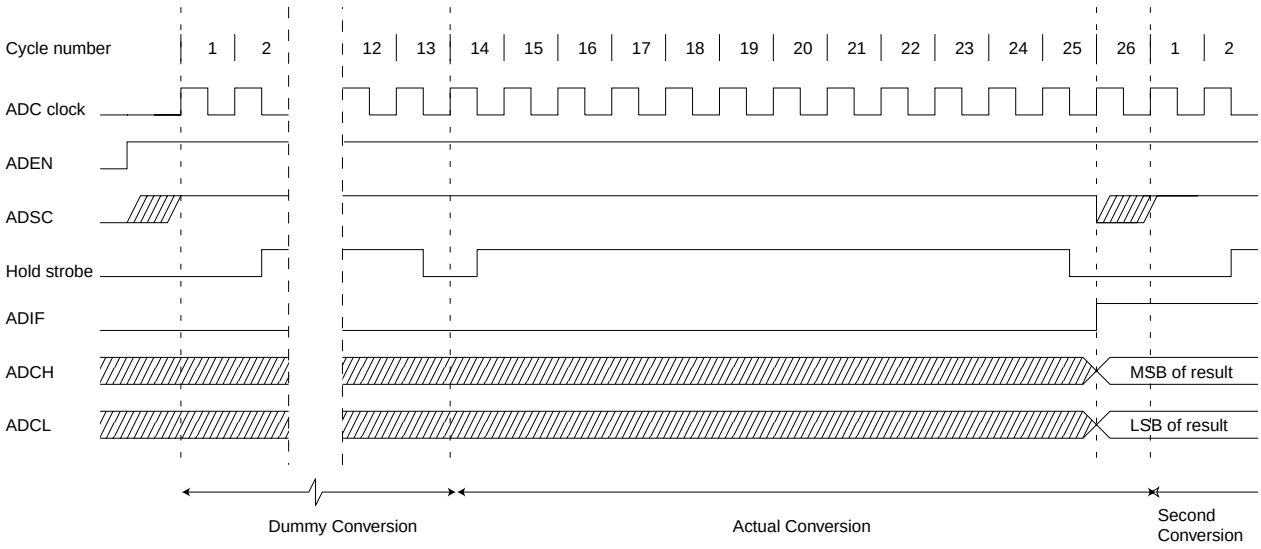


Table 9. ADC Conversion Time

Condition	Sample Cycle Number	Result Ready (Cycle Number)	Total Conversion Time (Cycles)	Total Conversion Time (µs)
1st Conversion, Free Run	14	25	25	125 - 500
1st Conversion, Single	14	25	26	130 - 520
Free Run Conversion	2	13	13	65 - 260
Single Conversion	2	13	14	70 - 280

Figure 6. ADC Timing Diagram, Single Conversion

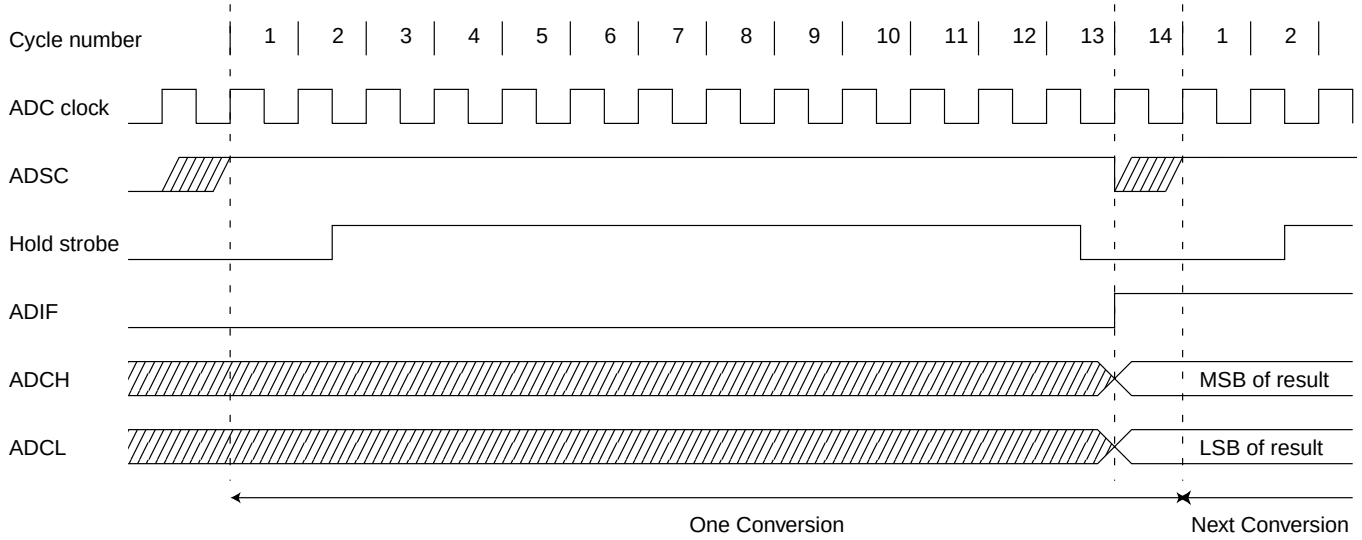
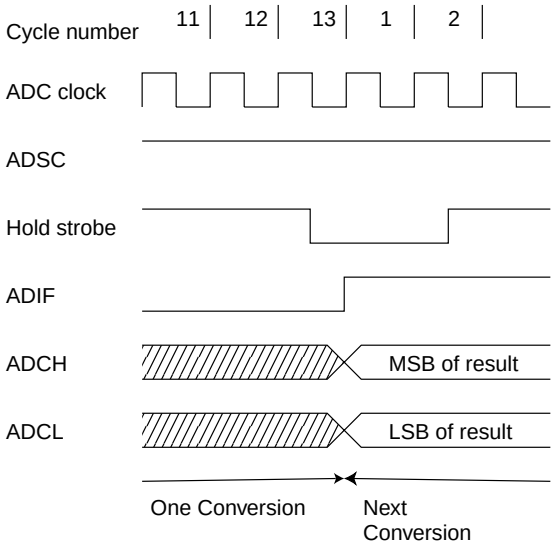


Figure 7. ADC Timing Diagram, Free Run Conversion



ADC Noise Canceler Function

The ADC features a noise canceler that enables conversion during idle mode to reduce noise induced from the CPU core. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion Mode must be selected and the ADC conversion complete interrupt must be enabled.

   ADEN = 1

   ADSC = 0

   ADFR = 0

   ADIE = 1
2. Enable ADC Noise reduction sleep mode by setting SM1:SM0 to 1:0
3. Enter idle mode. The ADC will start a conversion once the CPU has been halted.
4. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the MCU and execute the ADC conversion complete interrupt routine.

The ADC Multiplexer Selection Register - ADMUX

Bit	7	6	5	4	3	2	1	0	
$07 ($27)	**REFS1**	**REFS0**	**-**	**-**	**-**	**MUX2**	**MUX1**	**MUX0**	**ADMUX**
Read/Write	R/W	R/W	R	R	R	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bits 7..6 - REFS1..REFS0: Reference Selection Bits**

These bits select the voltage reference used with the ADC.

Table 10. Reference selection bits

REFS1:REFS0	Reference selected from:
00	V_{CC} used as analog reference
01	External Vref at pin PB0, Internal V_{REF} turned off
10	Internal V_{REF} without external bypass capacitor (disconnected from PB0)
11	Internal V_{REF} with external bypass capacitor at PB0 pin

- **Bits 5..3 - Res: Reserved Bits**

These bits are reserved bits in the ATtiny15 and always read as zero.

- **Bits 2..0 - MUX2..MUX0: Analog Channel and Gain Selection Bits 2-0**

The value of these three bits selects which analog input is connected to the ADC. In case of differential input 1 (PB3 - PB4), gain selection is also made with these bits. Refer to Table 11 for details.

Table 11. Input Channel and Gain Selections

MUX[2:0]	Channel and Gain
000	PB1
001	PB2
010	PB3
011	PB4
100	PB3 - PB3, with Gain of 1X
101	PB3 - PB3, with Gain of 20X
110	PB3 - PB4, with Gain of 1X
111	PB3 - PB4, with Gain of 20X

The ADC Control and Status Register - ADCSR

Bit	7	6	5	4	3	2	1	0	
$06 ($26)	**ADEN**	**ADSC**	**ADFR**	**ADIF**	**ADIE**	**ADPS2**	**ADPS1**	**ADPS0**	**ADCSR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - ADEN: ADC Enable**

Writing a logical “1” to this bit enables the ADC. By clearing this bit to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress, will terminate this conversion.

- **Bit 6 - ADSC: ADC Start Conversion**

In Single Conversion Mode, a logical “1” must be written to this bit to start each conversion. In Free Run Mode, a logical “1” must be written to this bit to start the first conversion. The first time ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, a dummy conversion will precede the initiated conversion. This dummy conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. When a dummy conversion precedes a real conversion, ADSC will stay high until the real conversion completes.

Writing a 0 to this bit has no effect.

- **Bit 5 - ADFR: ADC Free Run Select**

When this bit is set (“1”) the ADC operates in Free Running mode. In this mode, the ADC samples and updates the data registers continuously. Clearing this bit (zero) will terminate Free Running mode.

- **Bit 4 -ADIF: ADC Interrupt Flag**

This bit is set (“1”) when an ADC conversion completes and the data registers are updated. The ADC Conversion Complete Interrupt is executed if the ADIE bit and the I-bit in SREG are set (“1”). ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a read-modify-write on ADCSR, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- **Bit 3 - ADIE: ADC Interrupt Enable**

When this bit is set (“1”) and the I-bit in SREG is set (“1”), the ADC Conversion Complete Interrupt is activated.

- **Bits 2..0 - ADPS2..ADPS0: ADC Prescaler Select Bits**

These bits determine the division factor between the CK frequency and the input clock to the ADC.

Table 12. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Data Register - ADCL AND ADCH

Bit	15	14	13	12	11	10	9	8	
$05 ($25)	-	-	-	-	-	-	ADC9	ADC8	ADCH
$04 ($24)	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

When an ADC conversion is complete, the result is found in these two registers. In free-run mode, it is essential that both registers are read, and that ADCL is read before ADCH.

Scanning Multiple Channels

Since change of analog channel always is delayed until a conversion is finished, the free running mode can be used to scan multiple channels without interrupting the converter. Typically, the ADC Conversion Complete interrupt will be used to perform the channel shift. However, the user should take the following fact into consideration:

The interrupt triggers once the result is ready to be read. In free running mode, the next conversion will start immediately when the interrupt triggers. If ADMUX is changed after the interrupt triggers, the next conversion has already started, and the old setting is used.

ADC Noise Canceling Techniques

Digital circuitry inside and outside the ATtiny15 generates EMI which might affect the accuracy of analog measurements. If conversion accuracy is critical, the noise level can be reduced by applying the following techniques:

1. The analog part of the ATtiny15 and all analog components in the application should have a separate analog ground plane on the PCB. This ground plane is connected to the digital ground plane via a single point on the PCB.
2. Keep analog signal paths as short as possible. Make sure analog tracks run over the analog ground plane, and keep them well away from high-speed switching digital tracks.
3. Use the ADC noise canceler function to reduce induced noise from the CPU.
4. If some Port B pins are used as digital outputs, it is essential that these do not switch while a conversion is in progress.

ATtiny15 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F	SREG	I	T	H	S	V	N	Z	C	
$3E	Reserved									
$3C	Reserved									
$3B	GIMSK	-	INT0	PCIE	-	-	-	-	-	
$3A	GIFR	-	INTF0	PCIF	-	-	-	-	-	
$39	TIMSK	-	OCIE1	-	-	-	TOIE1	TOIE0	-	
$38	TIFR	-	OCF1	-	-	-	TOV1	TOV0	-	
$37	Reserved									
$36	Reserved									
$35	MCUCR	-	PUD	SE	SM1	SM0	-	ISC01	ISC00	
$34	MCUSR	-	-	-	-	WDRF	BORF	EXTRF	PORF	
$33	TCCR0	-	-	-	-	-	CS02	CS01	CS00	
$32	TCNT0	Timer/Counter0 (8 Bit)								
$31	OSCCAL	OSCillator CALibration bits								
$30	TCCR1	CTC1	PWM1	COM11	COM10	CS13	CS12	CS11	CS10	
$2F	TCNT1	Timer/Counter1 (8 Bit)								
$2E	OCR10	Output Compare Register 10 (8-bit)								
$2D	OCR11	Output Compare Register 11 (8-bit)								
$2C	SFIOR						FOC10	PSR1	PSR0	
$2B	Reserved									
$2A	Reserved									
$29	Reserved									
$28	Reserved									
$27	Reserved									
$26	Reserved									
$25	Reserved									
$24	Reserved									
$23	Reserved									
$22	Reserved									
$21	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	
$20	Reserved									
$1F	Reserved									
$1E	EEAR	-	-	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	
$1D	EEDR	EEPROM Data Register (8-bit)								
$1C	EECR	-	-	-	-	EEIE	EEMWE	EEWE	EERE	
$1B	Reserved									
$1A	Reserved									
$19	Reserved									
$18	PORTB	-	-	-	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	
$17	DDRB	-	-	-	DDB4	DDB3	DDB2	DDB1	DDB0	
$16	PINB	-	-	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	
$15	Reserved									
$14	Reserved									
$13	Reserved									
$12	Reserved									
$11	Reserved									
$10	Reserved									
$0F	Reserved									
$0E	Reserved									
$0D	Reserved									
$0C	Reserved									
$0B	Reserved									
$0A	Reserved									
$09	Reserved									
$08	ACSR	ACD	GREF	ACO	ACI	ACIE	-	ACIS1	ACIS0	
$07	ADMUXG	REFS1	REFS0	-	-	-	MUX2	MUX1	MUX0	
$06	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	
$05	ADCH	-	-	-	-	-	-	ADC9	ADC8	
$04	ADCL	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	
$00	Reserved									

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