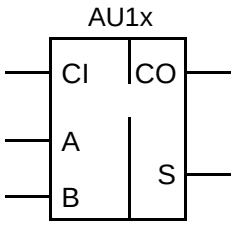
Description

AU1x is a family of combinational one-bit full adders.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

HDL Syntax

Verilog ..... AU1x *inst_name* (CO, S, A, B, CI);

VHDL..... *inst_name*: AU1x port map (CO, S, A, B, CI);

Pin Loading

Pin Name	Equivalent Loads	
	AU11	AU12
A	4.2	8.6
B	4.2	8.5
CI	3.2	6.5

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AU11	7.0	TBD	12.5
AU12	15.0	TBD	26.5

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
AU11	From: A To: S	t_{PLH} t_{PHL}	0.46 0.71	0.58 0.83	0.70 0.98	0.85 1.13	0.95 1.25
	From: B To: S	t_{PLH} t_{PHL}	0.45 0.73	0.57 0.84	0.70 0.99	0.85 1.15	0.96 1.29
	From: CI To: S	t_{PLH} t_{PHL}	0.46 0.72	0.58 0.83	0.71 0.97	0.86 1.14	0.96 1.27
	From: A To: CO	t_{PLH} t_{PHL}	0.44 0.58	0.55 0.75	0.68 0.92	0.84 1.10	0.95 1.22
	From: B To: CO	t_{PLH} t_{PHL}	0.44 0.58	0.54 0.74	0.67 0.90	0.82 1.08	0.93 1.20
	From: CI To: CO	t_{PLH} t_{PHL}	0.40 0.44	0.51 0.58	0.63 0.74	0.78 0.92	0.90 1.06
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
AU12	From: A To: S	t_{PLH} t_{PHL}	0.44 0.69	0.58 0.83	0.69 0.96	0.79 1.08	0.90 1.21
	From: B To: S	t_{PLH} t_{PHL}	0.43 0.72	0.55 0.87	0.66 0.99	0.77 1.10	0.89 1.22
	From: CI To: S	t_{PLH} t_{PHL}	0.44 0.71	0.58 0.84	0.69 0.96	0.79 1.07	0.90 1.19
	From: A To: CO	t_{PLH} t_{PHL}	0.41 0.55	0.54 0.76	0.65 0.90	0.76 1.02	0.87 1.15
	From: B To: CO	t_{PLH} t_{PHL}	0.41 0.55	0.54 0.73	0.65 0.88	0.75 1.01	0.85 1.16
	From: CI To: CO	t_{PLH} t_{PHL}	0.36 0.40	0.49 0.57	0.59 0.70	0.70 0.83	0.82 0.96

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Logic Schematic