AU6258-JBS-GR

USB2.0 HUB Controller

Technical Reference Manual

Rev. 1.00

May, 2011

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Revision History

Date	Revision	Description
May 2011	1.00	Official Release.

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1. Introduction

1.1 Description

AU6258 is a fully compliant with the USB 2.0 hub specification and is designed to work with USB host as a high-speed hub. Its built-in TT (Transaction Translator) allows system to benefit combinational performance under the unbalanced traffic condition.

AU6258 supports four USB downstream ports and one upstream port. Each downstream port could be a device of high-speed, full-speed or low-speed traffic, while the upstream port supports both high-speed and full-speed traffic.

In addition to the application as a stand-alone hub, AU6258 is also very suitable for using in notebook and motherboard design to provide additional USB port. All these product advantages should be attributed to its compliance to standards, performance and low power consumption.

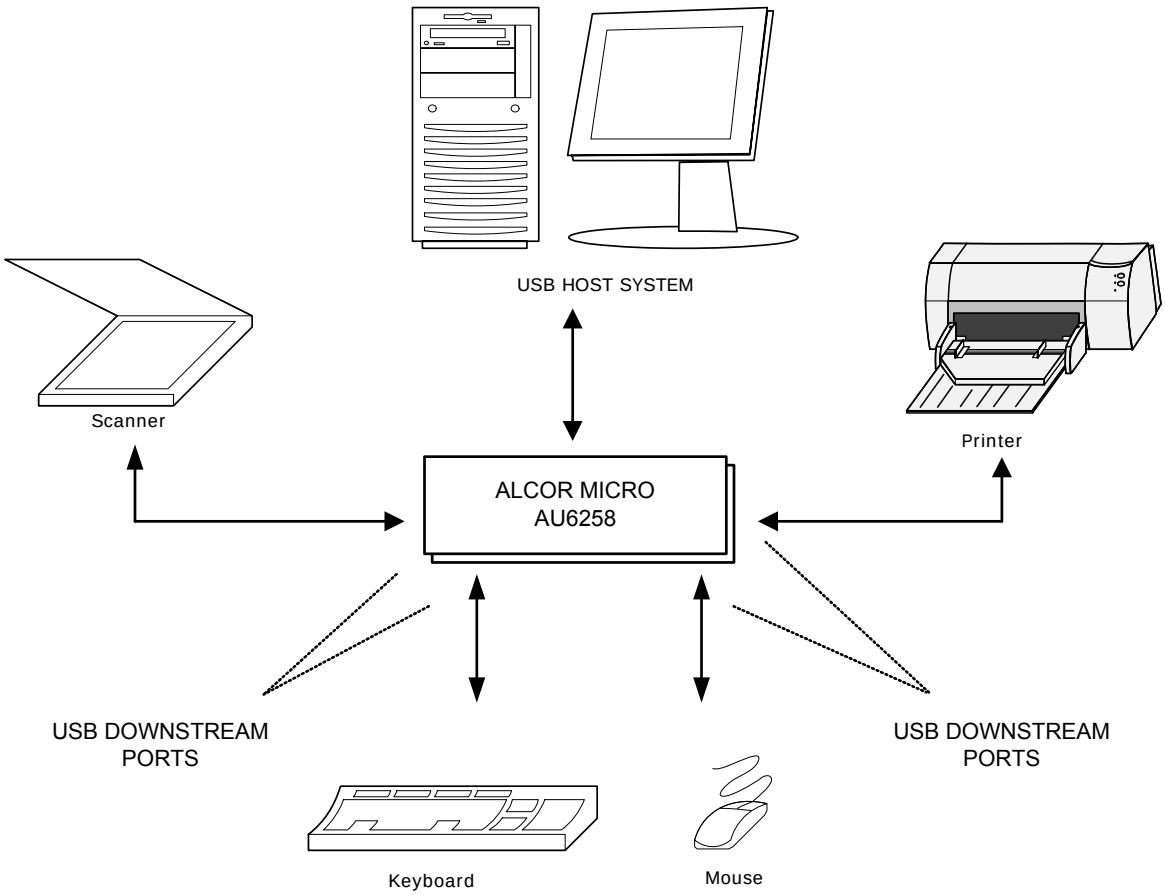
1.2 Features

- Fully compliant with USB Hub Specification version 2.0 and is also backward compatible with USB Hub specification 1.1.
- Single chip USB 2.0 hub controller.
- Supports four bus-powered/self-powered downstream ports.
- Supports automatic switching between bus- and self-powered modes.
- Support USB Charging Downstream Port in USB Battery Charging specification V1.2
- Cost effective design using one transaction translator for all downstream ports.
- Extra low power consumption.
- On chip internal pull-up and meets USB bus power regain emend pull down resistors for all data line.
- Built-in USB 2.0 transceiver.
- Supports gang modes of power management.
- Built-in power switch control for over current sensing control.
- Built-in 1.8V regulator for core logic.
- Embedded in PLL (Phase Lock Loop) circuit for 12MHz operation precision
- Available in 28-pin SSOP package.

2. Application Block Diagram

AU6258 is a single chip 4-port USB hub controller. Its upstream port is connected to a USB Host system. The downstream ports can be used for a mouse, joystick, scanner, printer or other devices.

Figure 2.1 Block Diagram



3. Pin Assignment

AU6258 is available in 28-pin SSOP package. Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

Figure 3.1 AU6258-JBS Pin Assignment Diagram

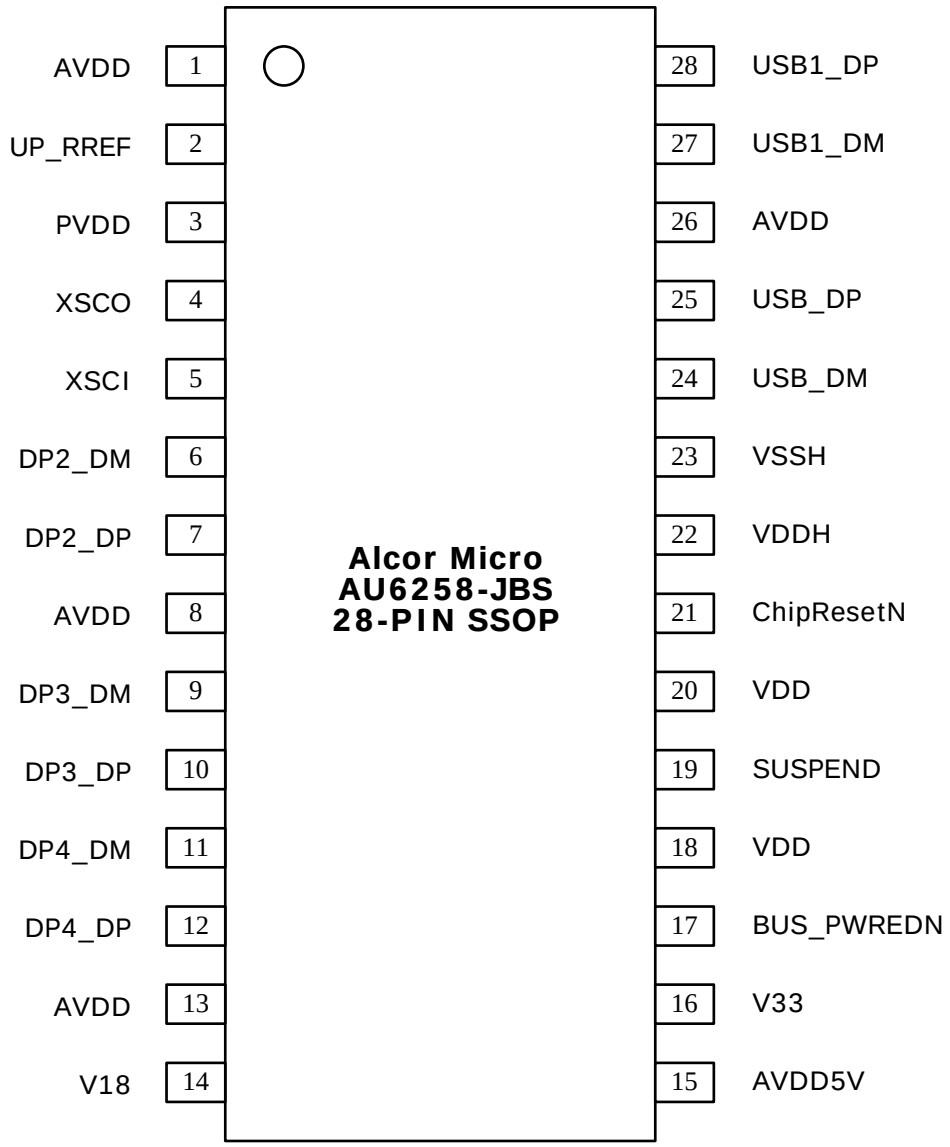


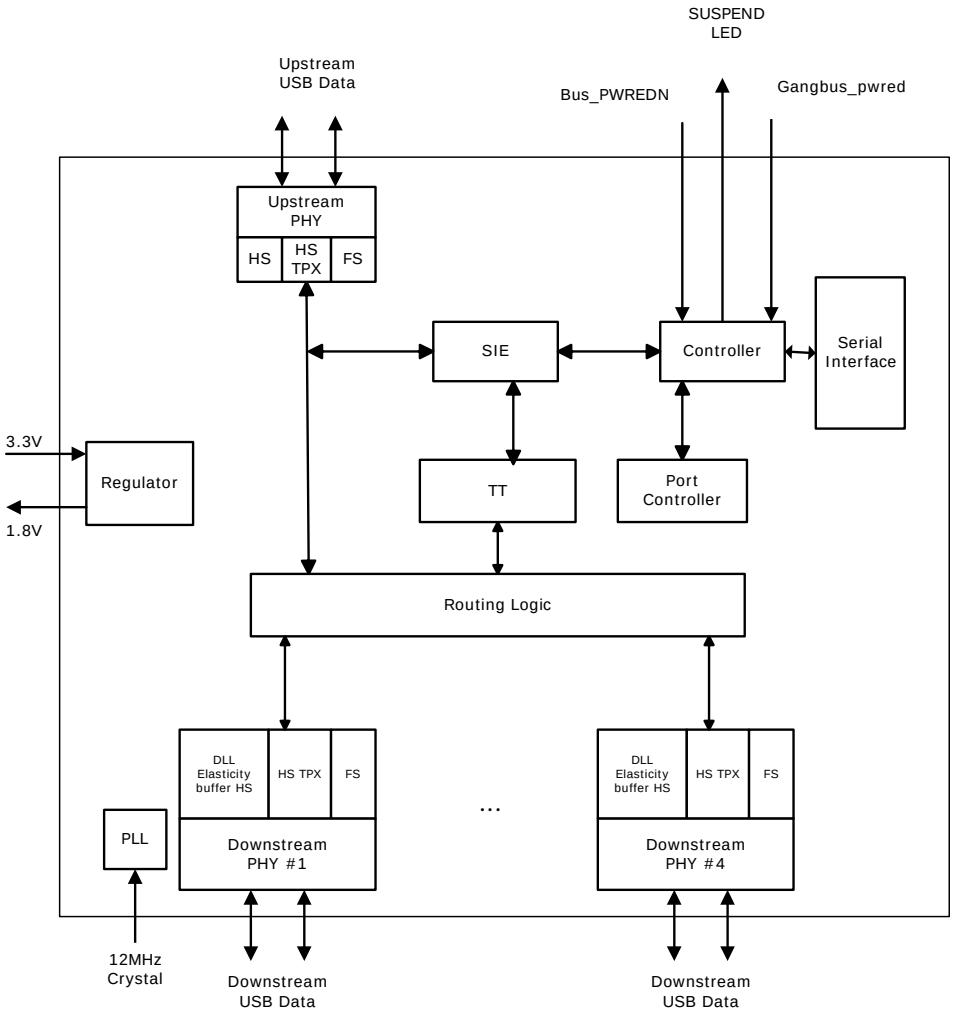
Table 3.1 AU6258-JBS Pin Descriptions

Pin #	Pin Name	I/O	Description
1	AVDD	Power	UTMI Power input 3.3V
2	UP_RREF	I	680Ω 1% current reference resistor
3	PVDD	Power	PLL VDD input 3.3V
4	XSCO	O	12MHz Crystal oscillator output
5	XSCI	I	12MHz Crystal oscillator input
6	DP2_DM	I/O	Port2 USB differential data bus D-
7	DP2_DP	I/O	Port2 USB differential data bus D+
8	AVDD	Power	UTMI Power input 3.3V
9	DP3_DM	I/O	Port3 USB differential data bus D-
10	DP3_DP	I/O	Port3 USB differential data bus D+
11	DP4_DM	I/O	Port4 USB differential data bus D-
12	DP4_DP	I/O	Port4 USB differential data bus D+
13	AVDD	Power	UTMI Power input 3.3V
14	V18	Power	Voltage regulator output 1.8V
15	AVDD5V	Power	Voltage regulator input 5V
16	V33	Power	Voltage regulator output 3.3V
17	BUS_PWREDN	I	'1' = Self Powered '0' = Bus Powered
18	VDD	Power	Core Power input 1.8V
19	SUSPEND	O	Suspend LED Indicator '0' = Not Suspended '1' = Suspended
20	VDD	Power	Core Power input 1.8V
21	ChipResetN	I	'0' = Reset '1' = Normal
22	VDDH	Power	IO power input 3.3V
23	AVSS	Power	UTMI GND
24	USB_DM	I/O	Upstream Port USB differential data bus D-
25	USB_DP	I/O	Upstream Port USB differential data bus D+
26	AVDD	Power	UTMI Power input 3.3V
27	USB1_DM	I/O	Port1 USB differential data bus D-
28	USB1_DP	I/O	Port1 USB differential data bus D+

4. System Architecture and Reference Design

4.1 AU6258-JBS Block Diagram

Figure 4.1 AU6258-JBS Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDH}	Power Supply	-0.3 to V_{DDH} +0.3	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		85	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

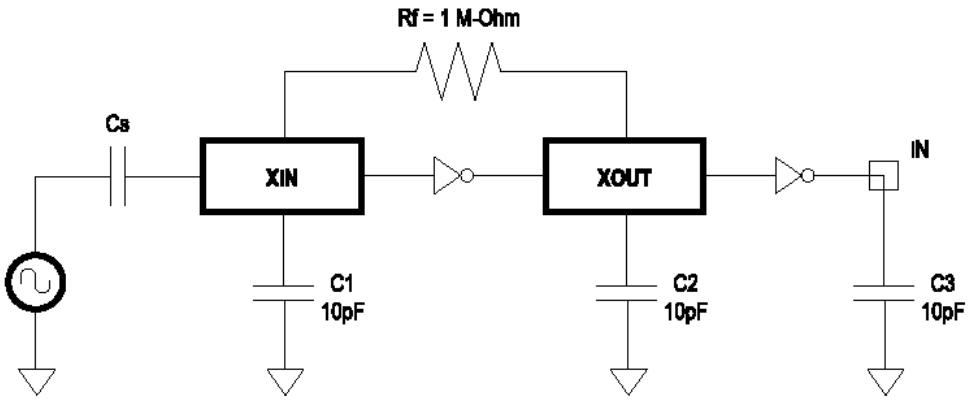
Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDH}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{DDH} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.6 Bus Timing / Electrical Characteristics

Table 5.5 DC Electrical Characteristics

Input Levels for Low-/Full –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{IH}	High (Driven)	2.0		V
V_{IHZ}	High (floating)	2.7	3.6	V
V_{IL}	Low		0.8	V
V_{DI}	Differential Input Sensitivity	0.2		V
V_{CM}	Differential Common Mode Range	0.8	2.5	V

Input Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HHSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	150	mV
V_{HSDSC}	High speed disconnect detection threshold (differential signal amplitude)	525	625	mV

Output Levels for Low-/Full-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{OL}	Low	0.0	0.3	V
V_{OH}	High (driven)	2.8	3.6	V
V_{OSE1}	SE1	0.8		V
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Output Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSOI}	High-speed idle level	-10	10	mV
V_{HSOH}	High-speed data signaling high	360	440	mV
V_{HSOL}	High-speed data signaling low	-10	10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	700	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-500	mV

Terminations:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
R_{PU}	Bus Pull-up Resistor on Upstream Facing Port	1.425	1.575	kΩ
R_{PD}	Bus Pull-down Resistor on Upstream Facing Port	14.25	15.75	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for low-/full-speed)	300		kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	3.0	3.6	V

Terminations in High-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSTERM}	Termination voltage in high-speed	-10	10	mV

Table 5.6 High-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSR}	Rise Time (10%-90%)	500		ps
T_{HSF}	Fall Time (10%-90%)	500		ps
Z_{HSDRV}	Driver Output Resistance (which also serves as high-speed termination)	40.5	49.5	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSDRAT}	High-speed Data Rate	479.76	480.24	Mb/s
T_{HSFRAM}	Micorframe Interval	124.9375	125.0625	μs
T_{HSRFI}	Consecutive Microframe Interval Difference		4 high-speed bit times	

Table 5.7 Full-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{FR}	Rise Time	4	20	ns
T_{FF}	Fall Time	4	20	ns
T_{FRFM}	Differential Rise and Fall Time Matching	90	111.11	%
Z_{ZRV}	Driver Output Resistance for driver which is not high-speed capable	28	44	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high-speed capable	11.994	12.006	Mb/s
T_{FDRATE}	Full-speed Data Rate for devices which are not high-speed capable	11.970	12.030	Mb/s
T_{FRAME}	Frame interval	0.9995	1.0005	Ms
T_{RFI}	Consecutive Frame Interval Jitter		42	ns

Full-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
	Source Jitter Total(including frequency tolerance):			
T_{DJ1}	To Next Transition	-3.5	-3.5	ns
T_{DJ2}	For Paired Transitions	-4	-4	ns
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns
	Receiver Jitter:			
T_{JR1}	To Next Transition	-18.5	-18.5	ns
T_{JR2}	For Paired Transitions	-9	-9	ns
T_{FEPPT}	Source SE0 interval of EOP	160	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	82		ns
T_{FST}	Width of SE0 interval during differential transition		14	ns

Table 5.8 Low-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{LR}	Rise Time	75	300	ns
T_{LF}	Fall Time	75	300	ns
T_{LRFM}	Differential Rise and Fall Time Matching	80	125	%
C_{LINUA}	Upstream Facing Port (w/cable, low-speed only)	200	450	pF

Clock Timings:

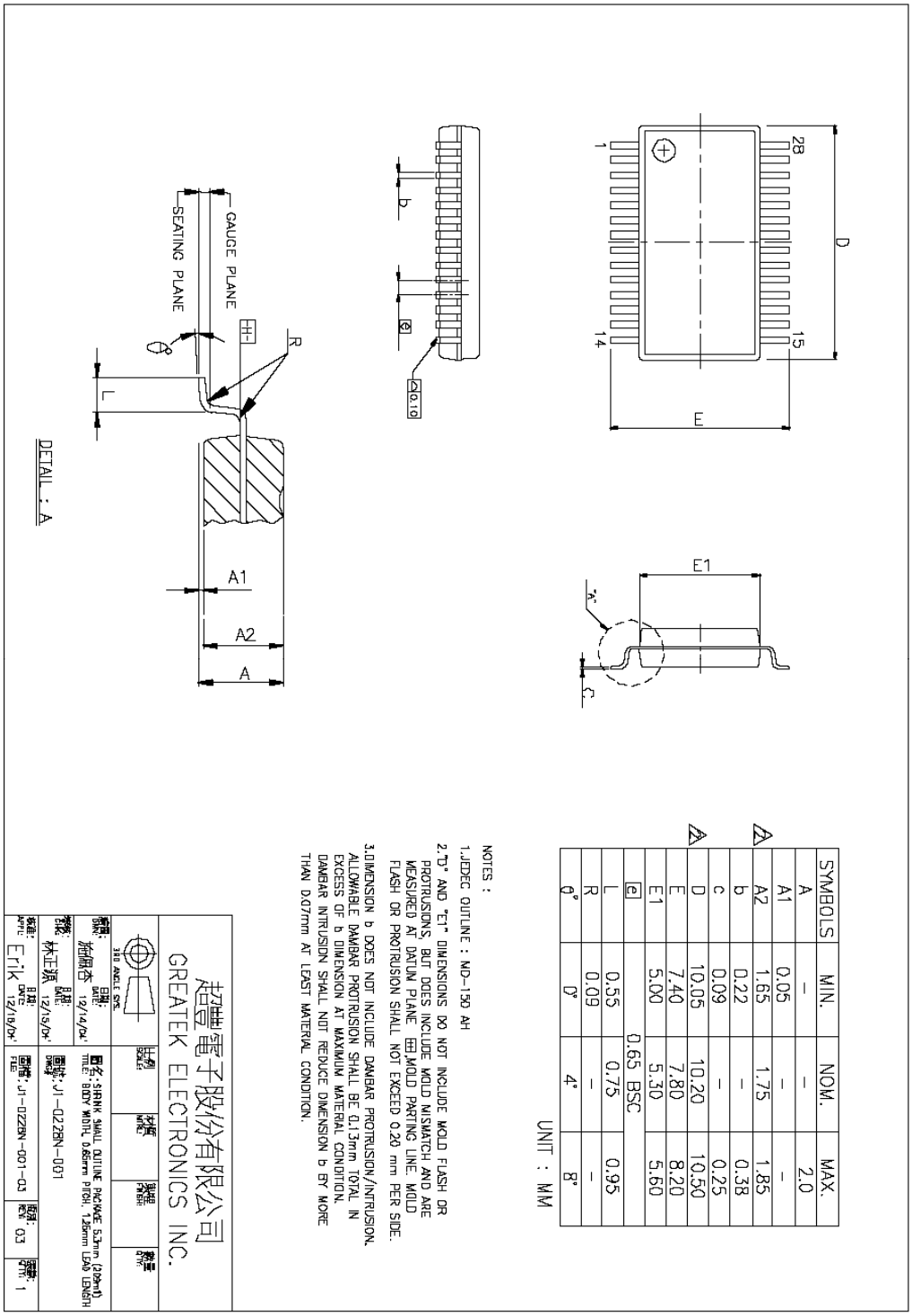
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{LDRATHS}$	Low-speed Data Rate for hubs and devices which are high-speed capable	1.49925	1.50075	Mb/s
T_{LDRATE}	Low-speed Data Rate for devices which are not high-speed capable	1.4775	1.5225	Mb/s

Low-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
	Upstream facing port source Jitter Total(including frequency tolerance):			
T_{UDJ1}	To Next Transition	-95	95	ns
T_{UDJ2}	For Paired Transitions	-150	150	ns
T_{LDEOP}	Upstream facing port source Jitter for Differential Transition to SE0 Transition	-40	100	ns
	Upstream facing port differential Receiver Jitter:			
T_{DJR1}	To Next Transition	-75	75	ns
T_{DJR2}	For Paired Transitions	-45	45	ns
	Upstream facing port differential Receiver Jitter:			
T_{DDJ1}	To Next Transition	-25	25	ns
T_{DDJ2}	For Paired Transitions	-14	14	ns
	Downstream facing port Differential Receiver Jitter:			
T_{UJR1}	To Next Transition	-152	152	ns
T_{UJR2}	For Paired Transitions	-200	200	ns
T_{LEOPT}	Source SE0 interval of EOP	1.25	1.50	μs
T_{LEOPR}	Receiver SE0 interval of EOP	670		ns
T_{LST}	Width of SE0 interval during differential transition		210	ns

6. Mechanical Information

Figure 6.1 Mechanical Information Diagram



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	2.0
A1	0.05	–	–
A2	1.65	1.75	1.85
b	0.22	–	0.38
c	0.09	–	0.25
D	10.05	10.20	10.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e		0.65 BSC	
L	0.55	0.75	0.95
R	0.09	–	–
θ°	0°	4°	8°

7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.