



Data Book

AU6330

USB2.0 SD/MMC

Flash Card Reader Controller

Technical Reference Manual

Product Specification

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Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
Jan. 2005	2.00/	Removed the schematics. Please contact our sales if you need it.



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1.0 Introduction

1.1 Description

The AU6330 is a highly integrated single chip for USB SD/MMC flash card reader controller. It supports USB2.0 high/full speed transmission via USB port interface to Host PC and 4-bit parallel transmission via SD/MMC interface to flash card. The AU6330 supports USB2.0 Storage Class Specification, Bulk-Transport Protocol. It can read digital content stored in SD/MMC flash card designed to cover a wide area of application such as digital camera, PDA, MP3 player and smart phone...etc.

With the AU6330, users can transfer digital data between SD/MMC flash card and PC or these electronic devices.

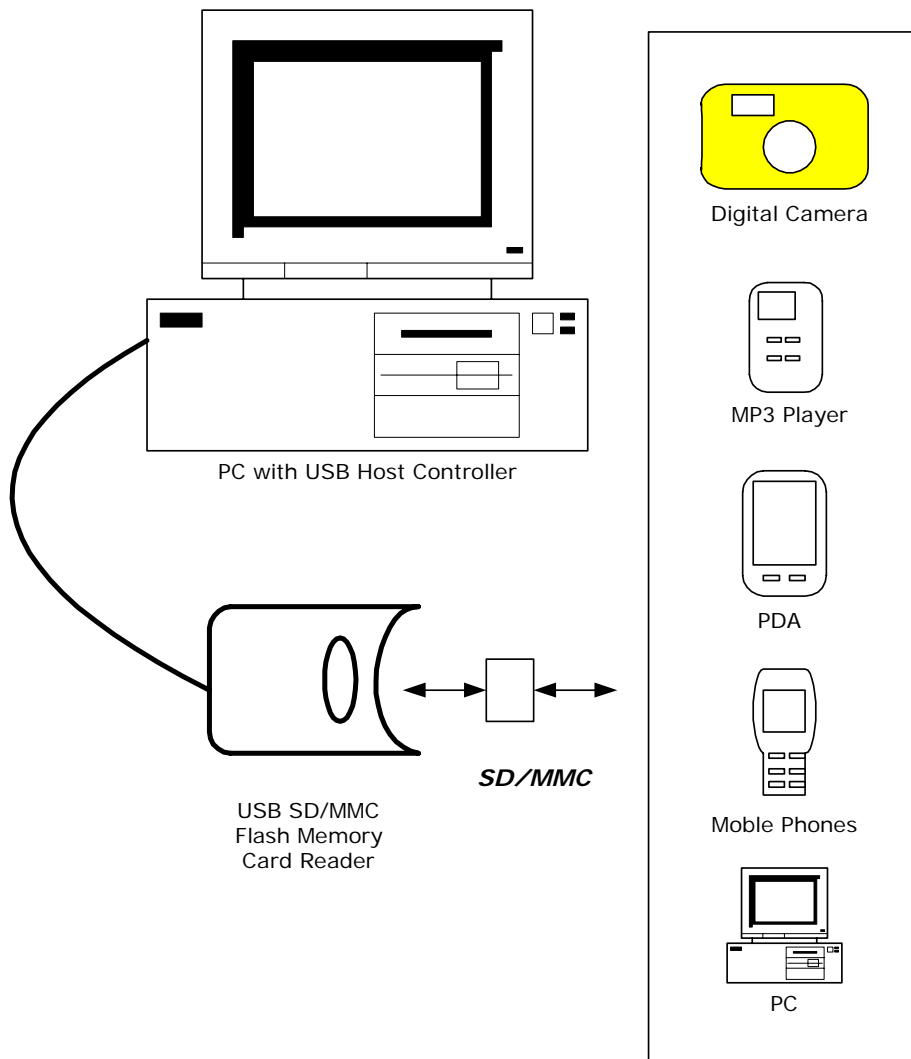
1.2 Features

- Support USB2.0 specification 480Mbps transmission and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Integrated USB2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE)
- Support SD card and MMC specification
- Work with default driver from Windows ME/2000/XP, Mac OS X and Linux kernel 2.4.1 above. Windows 98 & Windows 2000 SP1/2 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- Capable of handling 8 sets of built-in PID, VID and strings to minimize inventory control and improve production lead time
- Support LED for bus activity indication.
- Runs at 30MHz, built-in 480 MHz PLL
- Built-in to 3.3V to 2.5V regulator

2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU6330. By connecting the card reader to a desktop or notebook PC through USB bus, AU6330 is implemented as a bus-powered, full speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram





3.0 Pin Assignment

The AU6330 is packed in 64pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 3.1 Pin Assignment Diagram

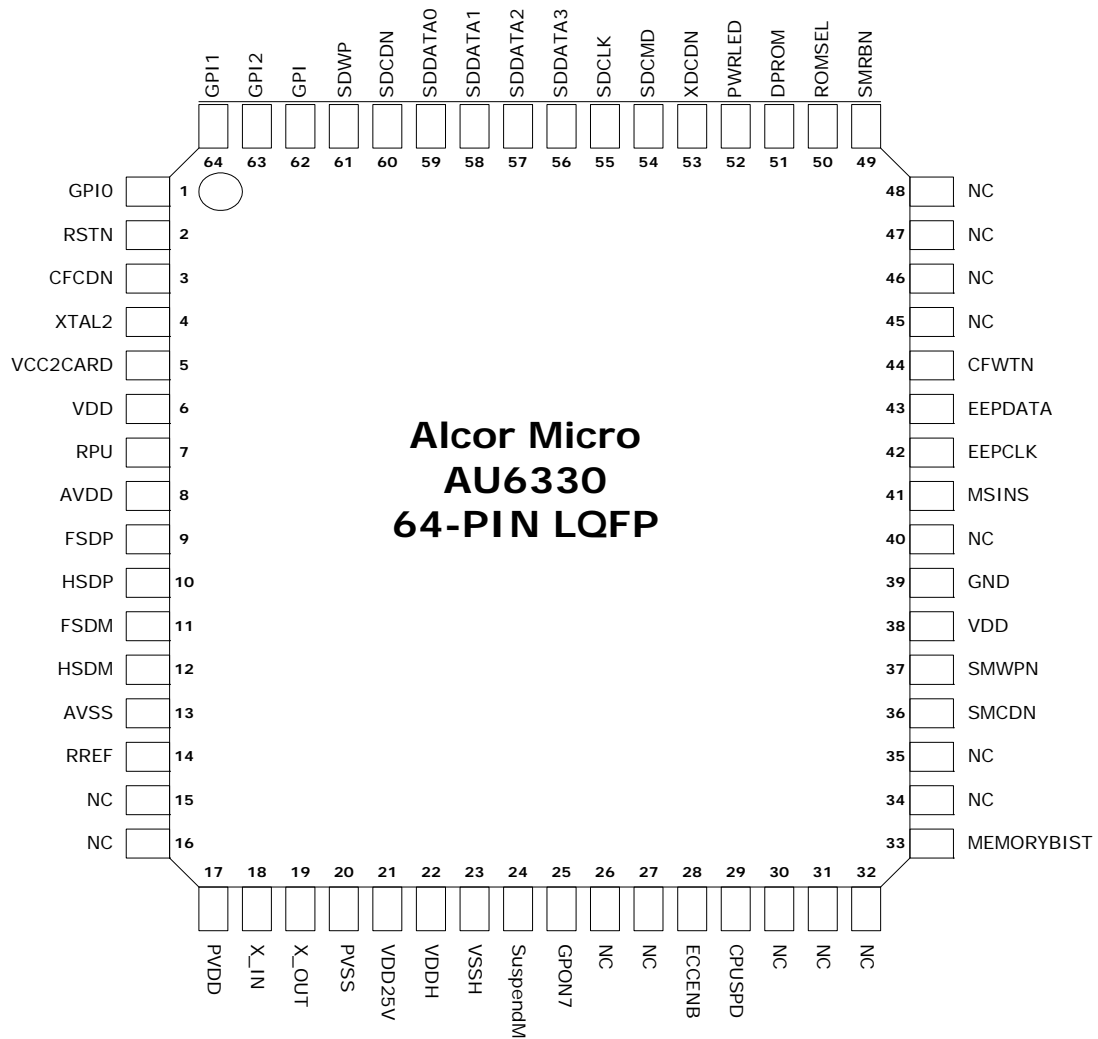




Table 3.1 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GPI0	I	Slot mode selection. (GPI0, GPI1)=(0,0): Reserved (GPI0, GPI1)=(0,1): 4.5 slot mode (GPI0, GPI1)=(1,0): 2 slot mode (GPI0, GPI1)=(1,1): 1 slot mode
2	RSTN	I	Reset. ("0": Reset; "1": Normal) (Need to pull up with RC)
3	CFCDN	I	CF Card Detect. ("0": Detected; "1": unDetected)
5	VDDE	I	3.3V Power Supply
6	VDD	I	Core Power 2.5V
7	RPU	I	Connected with an 1.5k pull up resistor to 3.3 VDD
8	AVDD	I	3.3V Power Supply Input
9	FSDP	I/O	Full speed DP
10	HSDP	I/O	High speed DP
11	FSDM	I/O	High speed DM
12	HSDM	I/O	Full speed DM
13	AVSS	PWR	Analog Ground
14	RREF	I	Connected an 1k resistor to A GND for impedance match
15	NC		
16	NC		
17	PVDD	I	3.3V Power Support Input for Pad
18	X_IN	I	12MHz crystal input
19	X_OUT	O	12MHz crystal output
20	PVSS	PWR	Pad Ground
21	VDD25V	O	2.5V Power Supply Output
22	VDDH	I	3.3V Power Supply for IO
23	VSSH	PWR	IO Ground
24	SuspendM	O	Suspend status. ("0": Suspend; "1": Normal)
25	GPON7	O	LED for card insert/ exsert status
26	NC		
27	NC		
28	ECCENB	I	Selection Ecc. ("0": Disable; "1": Enable; Default:"1")
29	CPUSPD	I	Selection CPU Speed. ("0": 30MHz; "1": 15MHz; Default:"0")
30	NC		
31	NC		
32	NC		
33	MEMORYBIST	I	Reserved. (Need to pull low)
34	NC		
35	NC		
36	SMCDN	I	SMC card detect. ("0": Detected; "1": undetected)

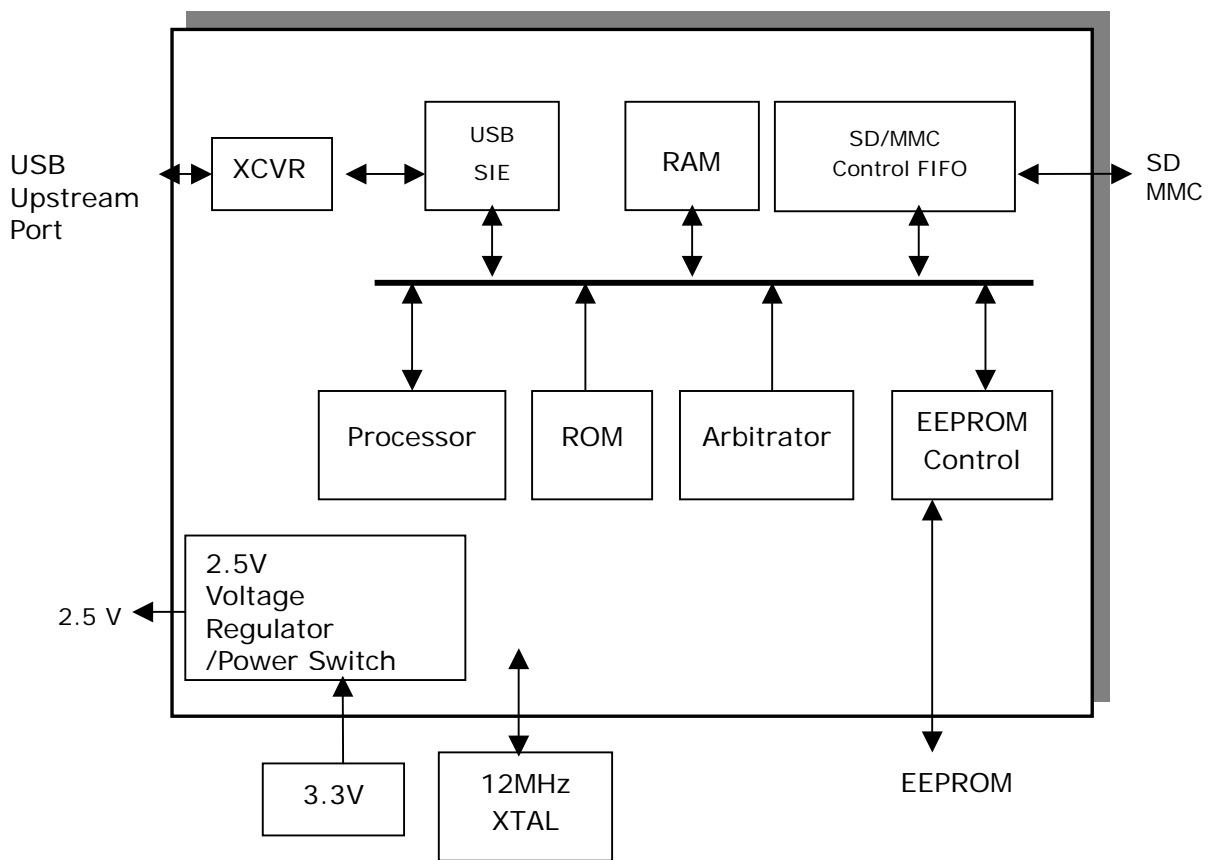


37	SMWPN	I	SMC Write Protect. ("0": Protected; "1": unProtected) (External pull up with 47K to SMPWR)
38	VDD	I	Core Power 2.5V
39	GND	PWR	Core Ground
40	NC		
41	MSINS	I	MS INS
42	EEPCLK	O	EEPROM serial clock.
43	EEPDATA	I/O	EEPROM Data
44	CFWTN	I	CF WAITN. (External pull up with 100K to CFPWR)
45	NC		
46	NC		
47	NC		
48	NC		
49	SMRBN	I	SMC Read/Busy. (External pull up with 470K to 3.3V)
50	ROMSEL	I	External ROM Selection. ("0": Internal ROM; "1": External ROM; Default: "0")
51	DPROM	I	Reserved. (Need to pull low)
52	PWRLED	O	LED for device power, Off when in suspend mode
53	XDCDN	I	XD Card Detect. ("0": Detected; "1": unDetected)
54	SDCMD	I/O	SD CMD
55	SDCLK	O	SD CLK
56	SDDATA3	I/O	SD Data3
57	SDDATA2	I/O	SD Data2
58	SDDATA1	I/O	SD Data1
59	SDDATA0	I/O	SD Data0
60	SDCDN	I	SD Card Detect. ("0": Detected; "1": unDetected)
61	SDWP	I	SD Write Protect. ("1": Protected; "0": unProtected)
62	GPI	I	Reserved. (Need to pull high)
63	GPI2	I	Reserved. (Need to pull high)
64	GPI1	I	Slot mode selection. (GPI0, GPI1)=(0,0): Reserved (GPI0, GPI1)=(0,1): 4.5 slot mode (GPI0, GPI1)=(1,0): 2 slot mode (GPI0, GPI1)=(1,1): 1 slot mode

4.0 System Architecture and Reference Design

4.1 AU6330 Block Diagram

Figure 4.1 AU6330 Block Diagram





5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power Supply	-0.3 to V _{CC} +0.3	V
V _{IN}	Input Voltage	-0.3 to 3.3	V
V _{OUT}	Output Voltage	-0.3 to V _{CC} +0.3	V
T _{STG}	Storage Temperature	-40 to 150	°C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	3.0	3.3	3.6	V
V _{IN}	Input Voltage	0	3.3	5.2	V
T _{OPR}	Operating Temperature	-40		115	°C

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IN}	Input current	no pull-up or pull-down	-10	±1	10	μA
I _{OZ}	Tri-state leakage current		-10	±1	10	μA
C _{IN}	Input capacitance	Pad Limit		2.8		ρF
C _{OUT}	Output capacitance	Pad Limit		2.8		ρF
C _{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF



5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V _{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V _{il}	Input low voltage	LVTTTL			0.8	V
V _{ih}	Input high voltage		2.0			V
V _{ol}	Output low voltage	I _{ol} = 2~16mA			0.4	V
V _{oh}	Output high voltage	I _{oh} = 2~16mA	2.4			V
R _{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R _{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I _{in}	Input leakage current	V _{in} = V _{CC} or 0	-10	±1	10	μA
I _{oz}	Tri-state output leakage current		-10	±1	10	μA



5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply current		3.0	3.3	3.6	V
VCC	Digital supply current		2.25	2.5	2.75	V
I _{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
I _{CC(susp)}	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V _{IL}	Low-level input voltage				0.8	V
V _{IH}	High-level input voltage		2.0			V
Output levels						
V _{OL}	Low-level output voltage				0.2	V
V _{OH}	High-level output voltage		VCC-0.2			V

AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C ~ 115°C



Table 5.7 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage (differential)		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						



V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

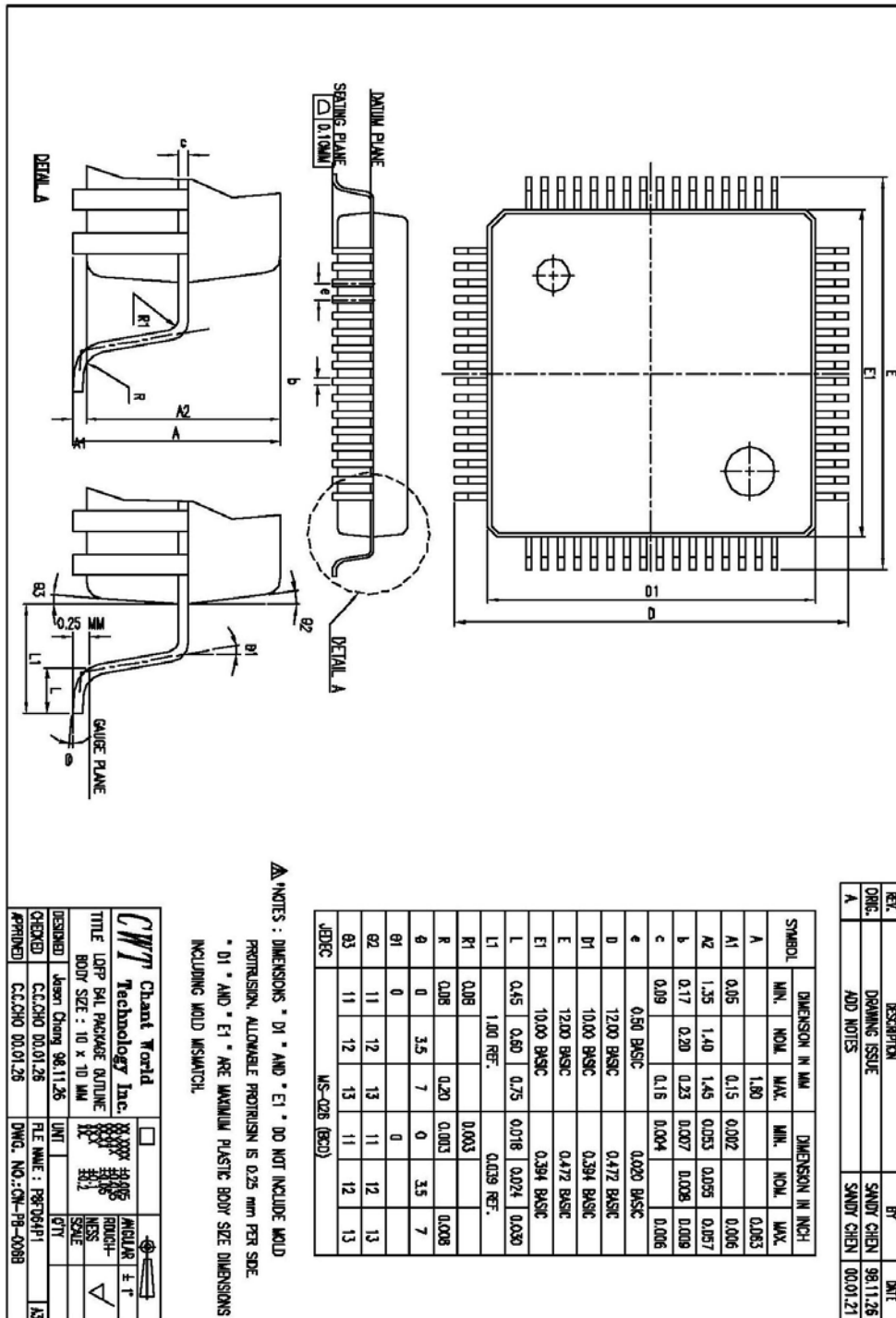
AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C

Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FF}	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram





7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE	Serial Interface Engine
SD	Secure Digital
MMC	Multimedia Card
UTMI	USB Transceiver Macrocell Interface



【MEMO】

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