



Data Book

AU6370

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USB2.0 Multiple Slots Flash Memory Card Reader Controller

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Product specification	This data book contains final product specifications.

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1.0 Introduction

1.1 Description

The AU6370 is an integrated single chip memory card reader controller specially designed for notebook, hand-held and other PC peripheral devices, which require fewer components for small PCB area. It supports a widely used flash memory card such as CF, MD, SMC, xD Picture Card, MS, MS Pro, MS Duo, SD and MMC. It can be used as removable storage disks in enormous data exchange applications between PC and PC or PC and various consumer electronic appliances.

The AU6370 reads digital content saved on memory card that user captured with the portable device such as notebook, digital camera, MP3 player, PDA and mobile phone... etc. In addition, AU6370 allows user to transfer information such as data, graphics, texts or digital images from one electronic device to another quickly and easily. Furthermore, AU6370 integrates power switch function; manufacturers can use fewer components in their product design.

With AU6370, user's experience will be also further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

1.2 Features

- Support USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Support CF/MD, SDHC/SD/MMC, MS/MS PRO/MS ROM/MS Duo AND xD/SMC specification
- Work with default driver from Windows ME, Windows XP, and Mac OS X. Windows 98, Windows 2000 are supported by vendor AP (The AP included both win98 and 2000 driver) from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support slot-to-slot read/write operation.
- Support auto-detecting slot with card inserted on Win 2000 without driver.
- Capable of handing 4 sets of built-in PID, VID and strings to minimize inventory control and improve lead production lead-time.
- Support LED for bus activity indication.
- Each slot can be enables/disabled by 5 independent pins to fit all the different card readers' combination requirement.
- Runs at 30MHz, built-in 480 MHz PLL
- Built-in 3.3V to 1.8V regulator

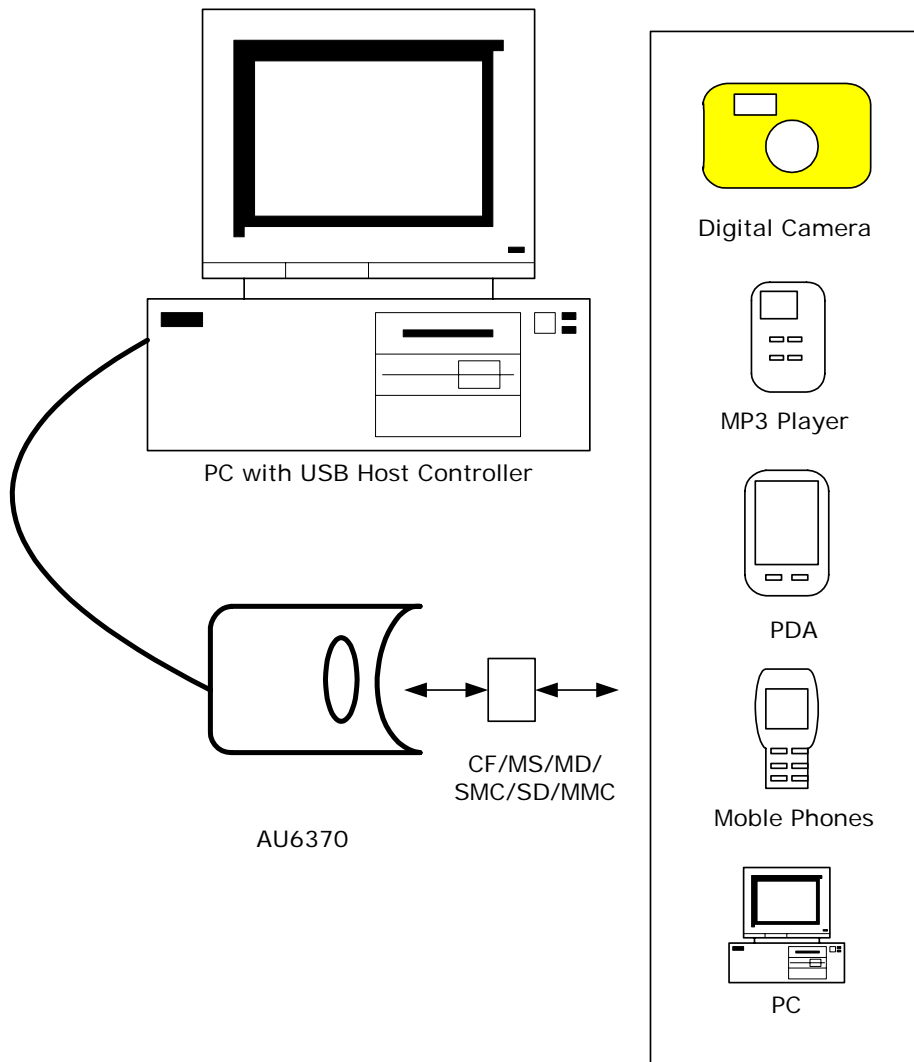


2.0 Application Block Diagram

The following application drawing demonstrates a typical card reader block diagram using AU6370. By connecting one card reader to a desktop or notebook PC through USB bus, the AU6370 becomes a bus-powered, high speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram

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3.0 Pin Assignment

The AU6370 is delivered in 80pin LQFP form factor. Documented below is a figure shows signal names of each pin and a table in the following page describes each pin in more details.

Figure 3.1 Pin Assignment Diagram

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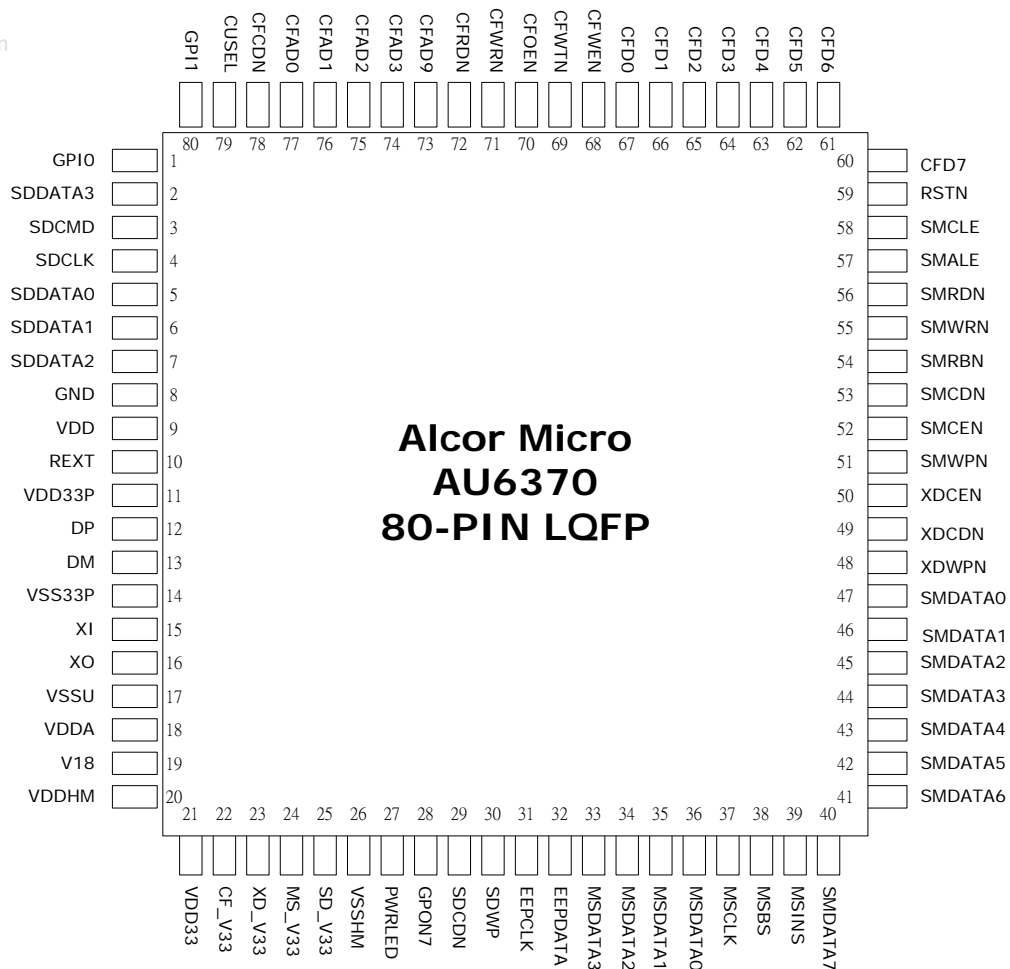




Table 3.1 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GPIO	I	Slot Mode Select (GPI1, GPI0) = (0,0) : Reserved (GPI1, GPI0) = (0,1) : 2 Luns (GPI1, GPI0) = (1,0) : 4.5 Luns (GPI1, GPI0) = (1,1) : 1 Lun
2	SDDATA3	I/O	SD Data3
3	SDCMD	I/O	SD CMD
4	SDCLK	O	SD CLK
5	SDDATA0	I/O	SD Data0
6	SDDATA1	I/O	SD Data1
7	SDDATA2	I/O	SD Data2
8	GND	PWR	core power ground pad
9	VDD	PWR	1.8 V core power pad
10	REXT	PWR	330 R Pull low
11	VDD33P	PWR	3.3 V PHY power pad
12	DP	I/O	USB DP
13	DM	I/O	USB DM
14	VSS33P	PWR	Ground pad. PHY IO ground pad
15	XI	I	12 MHz crystal pads
16	XO	O	12 MHz crystal pads
17	VSSU		Ground pad. PHY ground pad
18	VDDA	PWR	Crystal power pad
19	V18	O	Core Power1.8V
20	VDDHM	I	IO Power 3.3V
21	VDD33	I	Switch Power 3.3V
22	CF_V33	O	CF Card Power
23	XD_V33	O	SMC and XD share XD_V33 Power
24	MS_VCC	O	MS Card Power
25	SD_VCC	O	SD Card Power
26	VSSHM	PWR	IO Ground



Pin #	Pin Name	I/O	Description
27	PWRLED	O	Power LED; (Normal:"0"; Suspend"1")
28	GPON7	O	Card insert LED; (Card inserted:"0";
29	SDCDN	I	SD Card Detect
30	SDWP	I	SD Write Protect
31	EEPCLK	O	EEPROM Clock
32	EEPDATA	I/O	EEPROM Data
33	MSDATA3	I/O	MS Data3
34	MSDATA2	I/O	MS Data2
35	MSDATA1	I/O	MS Data1
36	MSDATA0	I/O	MS Data0
37	MSCLK	O	MS CLK
38	MSBS	O	MS BS
39	MSINS	I	MS INS
40	SMDATA7	I/O	SMDATA7
41	SMDATA6	I/O	SMDATA6
42	SMDATA5	I/O	SMDATA5
43	SMDATA4	I/O	SMDATA4
44	SMDATA3	I/O	SMDATA3
45	SMDATA2	I/O	SMDATA2
46	SMDATA1	I/O	SMDATA1
47	SMDATA0	I/O	SMDATA0
48	XDWPN	O	XD WP
49	XDCDN	I	XD CD
50	XDCEN	O	XD CE
51	SMWPN	I	SMC WP
52	SMCEN	O	SMC CE
53	SMCDN	I	SMC CD
54	SMRBN	I	SMC read/busy. External pull up with 470K to 3.3V.
55	SMWRN	O	SM WRN



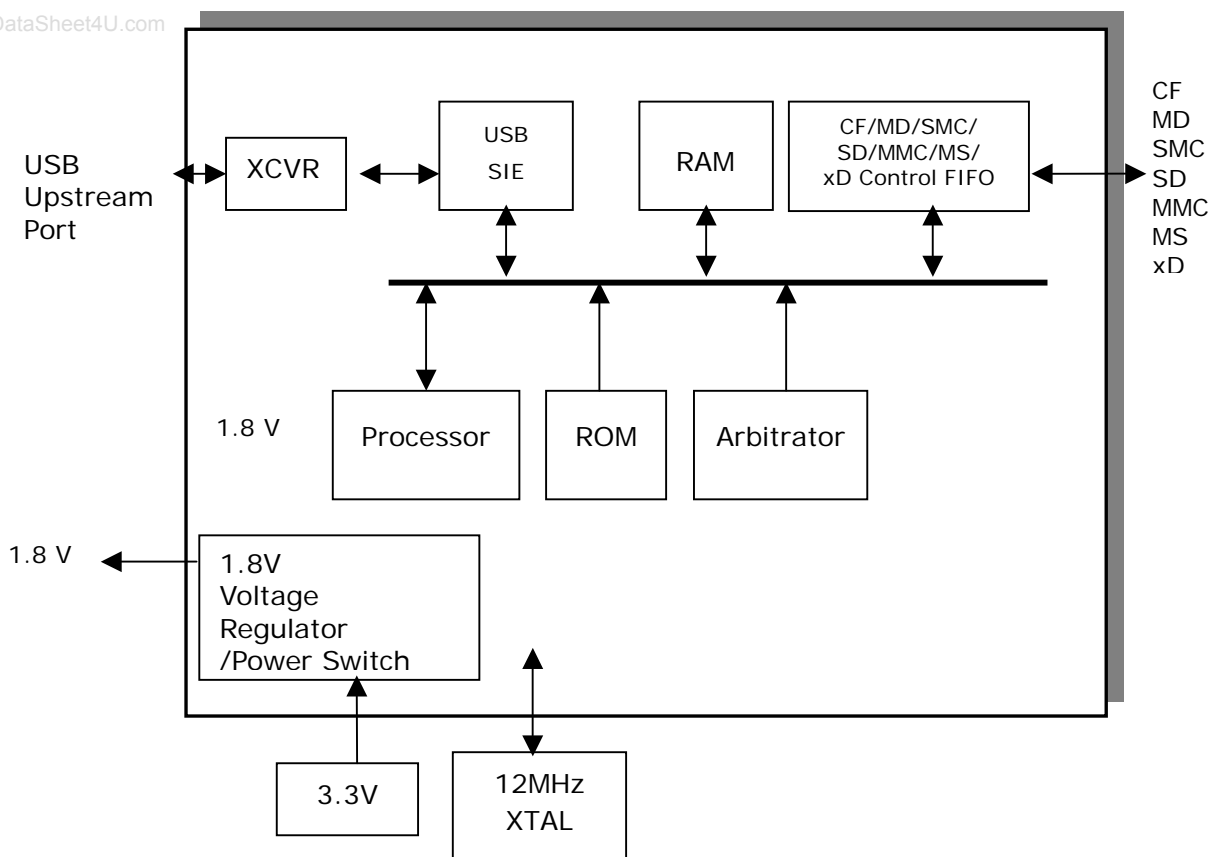
Pin #	Pin Name	I/O	Description
56	SMRDN	O	SMRDN
57	SMALE	O	SM CLE
58	SMCLE	O	SM CLE
59	RSTN	I	Chip Reset (Reset: "0"; Normal: "1"), pull up with RC
60	CFD7	I/O	CF Data7
61	CFD6	I/O	CF Data6
62	CFD5	I/O	CF Data5
63	CFD4	I/O	CF Data4
64	CFD3	I/O	CF Data3
65	CFD2	I/O	CF Data2
66	CFD1	I/O	CF Data1
67	CFD0	I/O	CF Data0
68	CFWEN	O	CF WEN
69	CFWTN	I	CF WAITN
70	CFOEN	O	CF OE
71	CFWRN	O	CF IOWRN
72	CFRDN	O	CF IORDN
73	CFAD9	O	CF Addr9
74	CFAD3	O	CF Addr3
75	CFAD2	O	CF Addr2
76	CFAD1	O	CF Addr1
77	CFAD0	O	CF Addr0
78	CFCDN	I	CF CD
79	CUSEL	I	Always pull High
80	GPI1	I	Slot Mode Select (GPI1, GPIO) = (0,0) : Reserved (GPI1, GPIO) = (0,1) : 2 Luns (GPI1, GPIO) = (1,0) : 4.5 Luns (GPI1, GPIO) = (1,1) : 1 Lun

4.0 System Architecture and Reference Design

4.1 AU6370 Block Diagram

Figure 4.1 AU6370 Block Diagram

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5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDHM}	Power Supply	-0.3 to $V_{DDH} + 0.3$	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to $V_{DDHM} + 0.3$	V
T_{STG}	Storage Temperature	-40 to 150	$^{\circ}C$

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DDHM}	Power Supply	3.0	3.3	3.6	V
V_{DD} V_{18}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	$^{\circ}C$

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	no pull-up or pull-down	-10	± 1	10	μA
I_{OZ}	Tri-state leakage current		-10	± 1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF



5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V _{DDHM}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V _{il}	Input low voltage	LVTTTL			0.8	V
V _{ih}	Input high voltage		2.0			V
V _{ol}	Output low voltage	I _{ol} = 2~16mA			0.4	V
V _{oh}	Output high voltage	I _{oh} = 2~16mA	2.4			V
R _{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R _{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I _{in}	Input leakage current	V _{in} = V _{DDHM} or 0	-10	±1	10	μA
I _{oz}	Tri-state output leakage current		-10	±1	10	μA

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5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VD33P	Analog supply voltage		3.0	3.3	3.6	V
VDD V18	Digital supply voltage		1.62	1.8	1.98	V
I _{CC}	Operating supply current	High speed operating at 480 MHz			55	mA
I _{CC(susp)}	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

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Table 5.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V _{IL}	Low-level input voltage				0.8	V
V _{IH}	High-level input voltage		2.0			V
Output levels						
V _{OL}	Low-level output voltage				0.2	V
V _{OH}	High-level output voltage		VDDU-0.2			V



Table 5.7 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage (differential)		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						



V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FF}	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V



5.6 Power Switch Feature

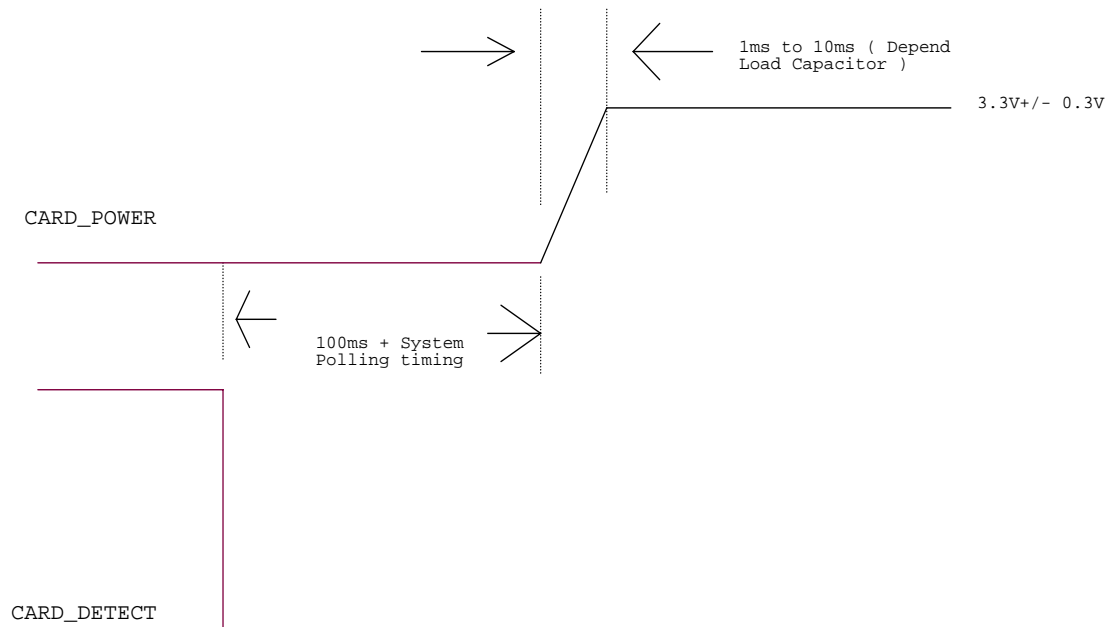
AU6370 integrates a 3.3V to 1.8V voltage regulator and power switch to replace all MOS chips for flash card power supply.

Card Power Output Current Range

- For SD/MS
 - ◆ MAX: 100mA
- For XD/SMC
 - ◆ MAX: 70mA
- For CF
 - ◆ MAX: 250mA
- Card power output voltage range
 - ◆ MS/XD/SD/SMC/CF: 3.3V±0.3V
- AU6370 will turn off all of Card Power in suspend mode

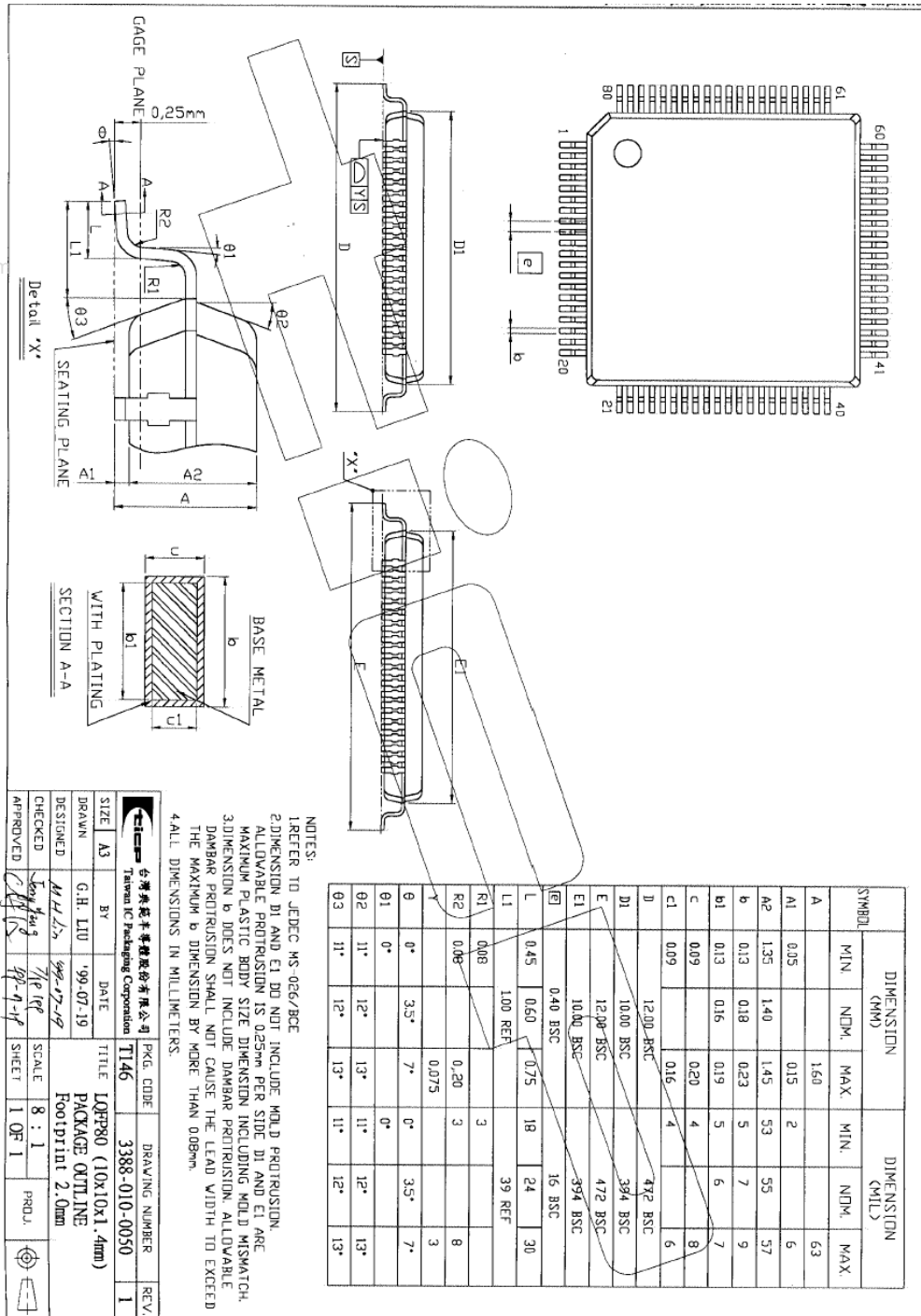
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Figure 5.1 Card Detect Power-on Timing



6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram





7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE	Serial Interface Engine
CF	Compact Flash
MD	Micro Drive
SMC	SmartMedia Card
MS	Memory Stick
SD	Secure Digital
MMC	Multimedia Card
UTMI	USB Transceiver Macrocell Interface



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