Data Book

AU6384

USB 2.0 Flash Disk Controller

Technical Reference Manual

Product Specification

Preliminary Release

Revision 1.02

Public

Jul 2004

Data Sheet Status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
Mar 2004	1.00/A31	Initial release
May 2004	1.01/A31	To modify Pin Descriptions in #15 and #24
Jul 2004	1.02/A31	To modify 1.2 Feature, 3.1 pin description and 4.2 sample schematics.

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1.0. Introduction

1.1. Description

Au6384 is a highly integrated single chip for USB2.0 flash disk controller. It can be used as a removable storage disk in enormous data exchange application between USB enabled PC and NAND type flash memory. Not only it can be used as a removable storage disk in Windows PC, Apple Macintosh, Notebook and Linux/Unix workstation, it also can be configured as bootable disk for system reparation.

AU6384 is an outstanding USB storage device controller; it provides a new innovative feature – Autorun. It will automatically execute the customized images file to illustrate company logo or branding image. Besides, It will be able to allow OEM or manufacturer to change its private label icon and modify arbitrarily label name in order to demonstrate its unique design and make end-user easily to distinguish a removable storage disk from other disks in the computer.

Alcor Micro provides a smart application – iRun handy tool for AU6384 to manage USB storage device. The iRun provides the features as show device status instantly, disk partition management, password protection, software write protection. These unique features give hardware device maker and software vendor tremendous opportunity to develop user-friendly appliance and application.

1.2. Feature

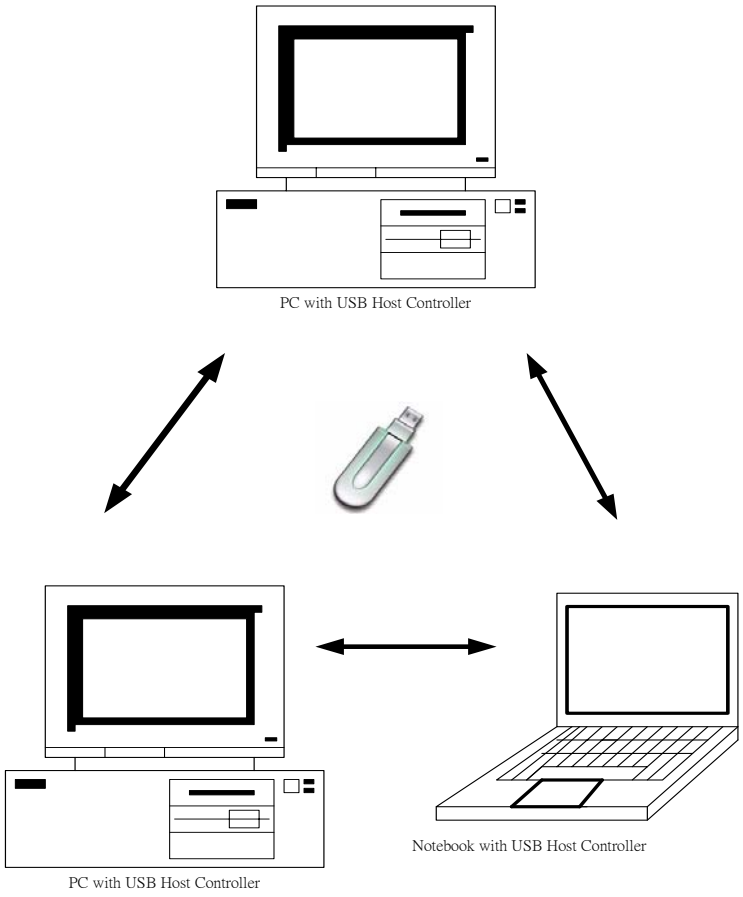
- Support USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac 9.2, Mac OS X and vendor driver from Alcor for Windows 98SE
- Support AutoRun feature.
- AutoRun feature can be supported on Windows ME, Windows 2000, Windows XP and Windows 98 system.
- Multiple FIFO implementation for concurrent bus operation
- 48-pin package supports up to 2 pieces of NAND Flash memory chip; total capacity reaches to 1G byte.
- Vendor ID, product ID and strings can be customized by utility software from Alcor
- Support software write protection function
- Password protection for data security
- LED for bus activity monitoring
- Runs at 30MHz, built-in 480 MHz PLL
- Built-in to 3.3V to 2.5V regulator
- Built-in power on reset circuit

2.0. Application Block Diagram

Following is the application diagram of a typical flash disk product with AU6384. By connecting the flash disk to a desktop or notebook PC through USB bus, AU6384 is implemented as a bus-powered, full speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram

Figure 2.1 Block Diagram



3.0. Pin Assignment

The AU6384 is packed in 48pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail

Figure 3.1 Pin Assignment Diagram

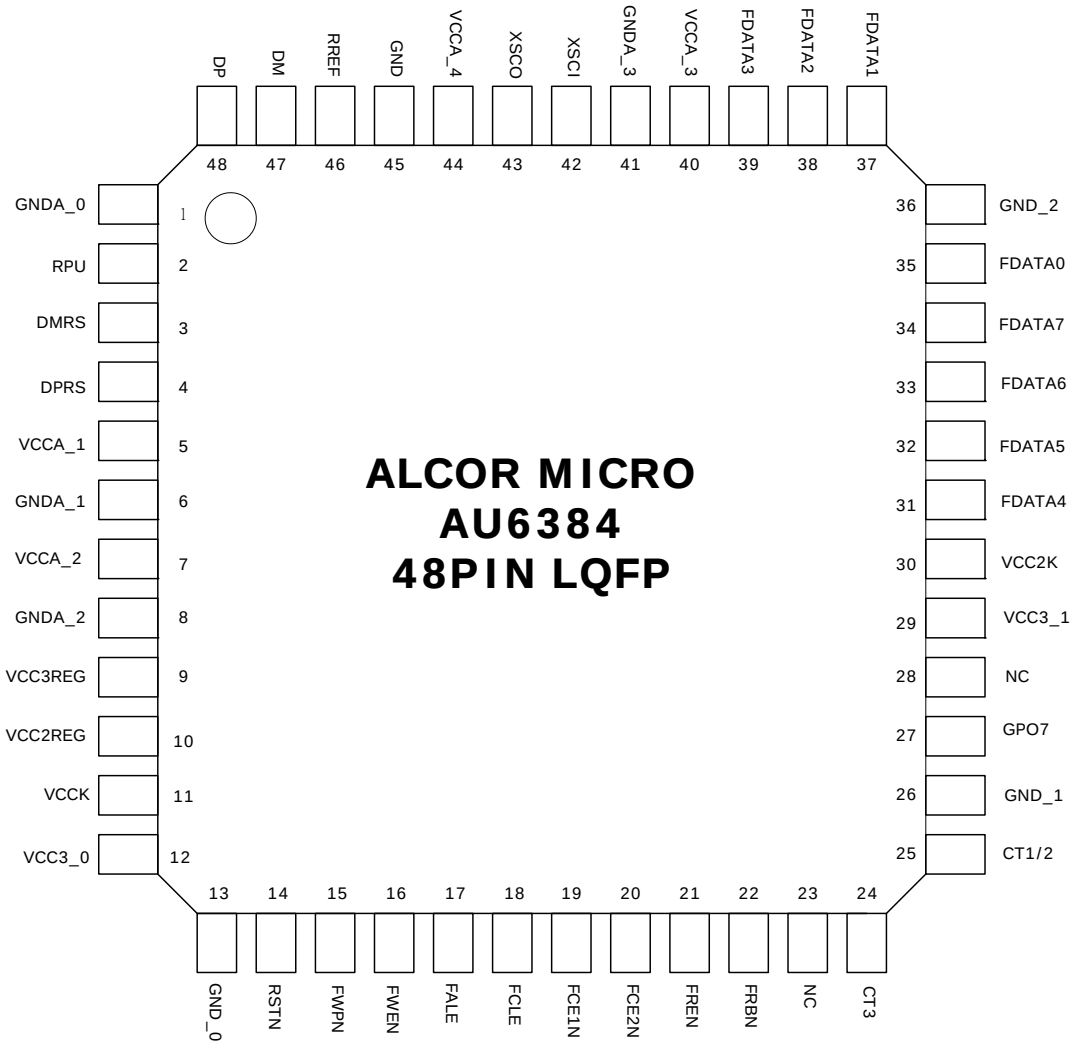


Table 3.1 Pin Descriptions

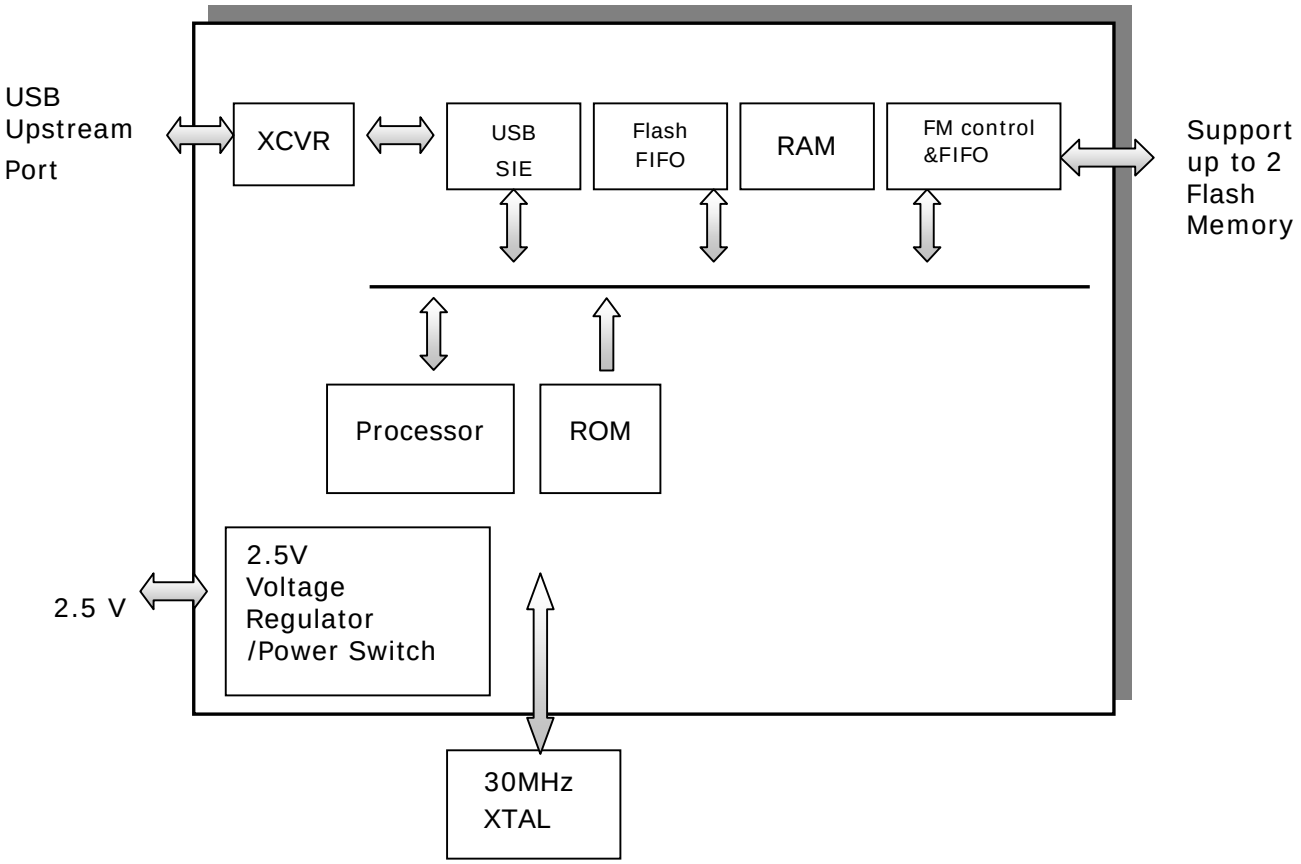
Pin #	Pin Name	I/O	Description
1	GNDA_0	PWR	Ground for USB IO
2	RPU	I	Connects external reference register 1.5K to AVCC .
3	DMRS	I/O	FS Data negative pin terminal.
4	DPRS	I/O	FS Data positive pin terminal.
5	VCCA_1	PWR	Analog Power Supply 3.3V
6	GNDA_1	PWR	Analog Ground
7	VCCA_2	PWR	Analog Power Supply 3.3V
8	GNDA_2	PWR	Analog Ground
9	VCC3REG	PWR	Regulator Power Supply 3.3V Input
10	VCC2REG	O	Regulator Power Supply 2.5V Output
11	VCCK	PWR	Code Power 2.5v
12	VCC3_0	PWR	Power Supply 3.3V
13	GND_0	PWR	Device Ground
14	RSTN	I	Reset Active Low
15	FWPN	I	Flash Memory Write Protect ("1": enable, 0":disable)
16	FWEN	O	Flash Memory Write Enable
17	FALE	O	Flash Memory Address Latch Enable
18	FCLE	O	Flash Memory Command Latch Enable
19	FCE1N	O	FLASH MEMORY CHIP ENABLE #1
20	FCE2N	O	FLASH MEMORY CHIP ENABLE #2
21	FREN	O	FLASH MEMORY Read Enable
22	FRBN	I	FLASH MEMORY Ready and Busy
23	NC		
24	CT3	I	Ecc enable (Pull high)
25	CT1/2	I	Pull low
26	GND_1	PWR	Device Ground
27	GPO7	O	General Purpose Out. Scanout_1 when Scan_test asserted.
28	NC		
29	VCC3_1	PWR	Power Supply 3.3V
30	VCC2K	PWR	Core Power Supply 2.5v Input

31	FDATA4	I/O	FLASH MEMORY Data In/out Pin # 4
32	FDATA5	I/O	FLASH MEMORY Data In/out Pin # 5
33	FDATA6	I/O	FLASH MEMORY Data In/out Pin # 6
34	FDATA7	I/O	FLASH MEMORY Data In/out Pin # 7
35	FDATA0	I/O	FLASH MEMORY Data In/out Pin # 0
36	GND_2	PWR	Device Ground
37	FDATA1	I/O	FLASH MEMORY Data In/out Pin # 1
38	FDATA2	I/O	FLASH MEMORY Data In/out Pin # 2
39	FDATA3	I/O	FLASH MEMORY Data In/out Pin # 3
40	VCCA_3	PWR	Analog supply voltage 3.3v
41	GNDA_3	PWR	Analog Ground
42	XSCI	I	Crytical oscillator input (12/30Mhz)
43	XSCO	O	Crytical oscillator output (12/30Mhz)
44	VCCA_4	PWR	Analog Power supply 3.3V
45	GNDA_4	PWR	Analog Ground
46	RREF	I	Connects external reference register 12.1K to analog GND
47	DM	I/O	HS data negative pin terminal
48	DP	I/O	HS data positive pin terminal

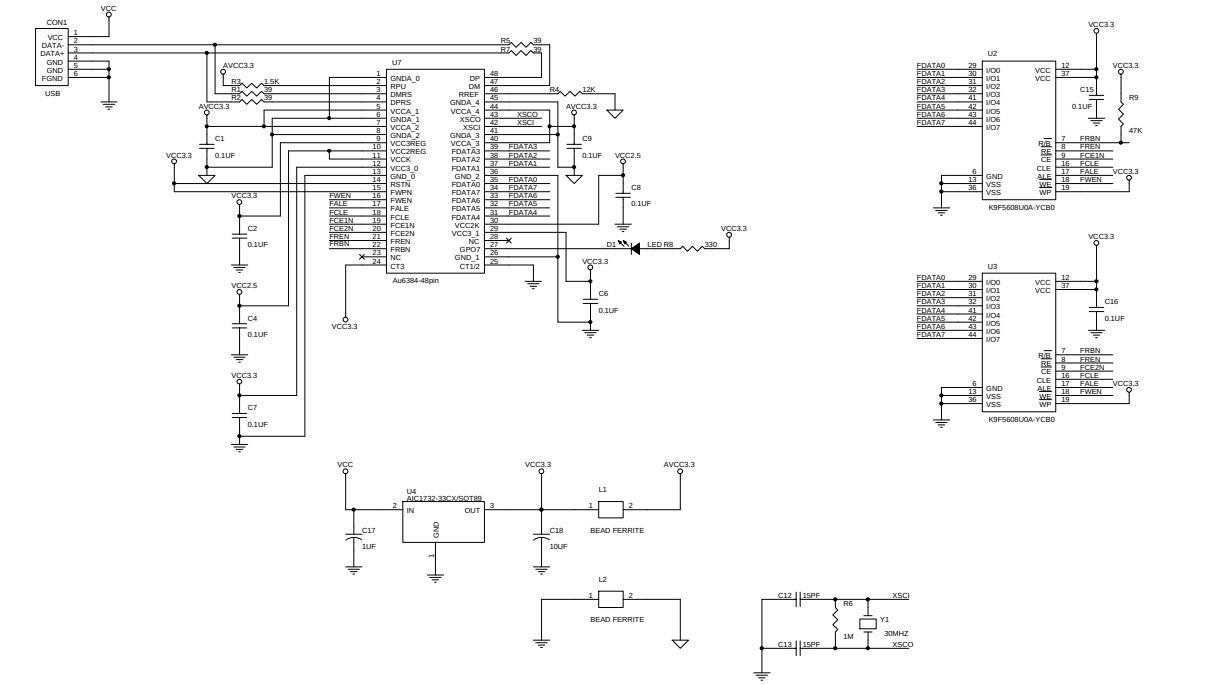
4.0. System Architecture and Reference Design

4.1. Block Diagram

Figure 4.1 AU6384 Block Diagram



4.2. Sample Schematics



Disclaimer: This schematic is for reference only.
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Size	Document Number	Rev
B	Au6384 demostration schematic	1.20
Date:	Thursday, July 01, 2004	Sheet 1 of 1

5.0. Electronic Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to V_{CC}+0.3	V
V_{IN}	Input Voltage	-0.3 to 3.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage	0	3.3	5.2	V
T_{OPR}	Operating	-40		115	^{O}C

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\|I_{ol}\|$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\|I_{oh}\|$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I_{in}	Input leakage current	V_{in}= V_{CC} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply current		3.0	3.3	3.6	V
VCC	Digital supply current		2.25	2.5	2.75	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
$I_{CC(susp)}$	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic：Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VCC-0.2			V

AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV

V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃

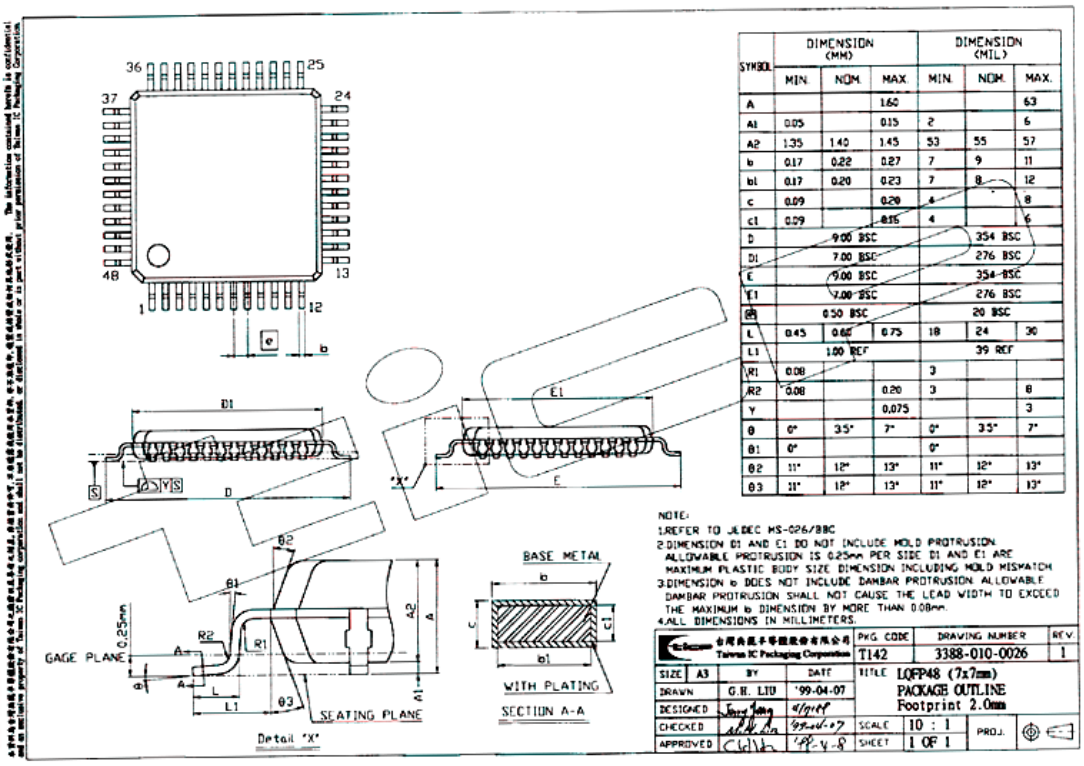
Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns

t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF；10 to 90% of ｜V_{OH}-V_{OL}｜；	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF；90 to 10% of ｜V_{OH}-V_{OL}｜；	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0. Mechanical Information

Figure 6.1 Mechanical Information Diagram



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.50 BSC			20 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

7.0. Abbreviation

This chapter lists and defines terms and abbreviations used throughout this specification

iRUN (The abbreviations is just Application program name)

【MEMO】

About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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