Data Book

AU6389

USB2.0 Flash Disk Controller

Technical Reference Manual

Product Specification

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Data Book status

Objective specification	This data book contains target specifications for product development.
Preliminary specification	This data book contains preliminary data; supplementary data may be published later.
Product specification	This data book contains final product specifications.

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1.0 Introduction

1.1 Description

AU6389 is a single chip USB 2.0 flash disk controller that supports dual channel mode for high performance operation. The AU6389 can be used as a removable storage disk in enormous data exchange applications between USB enabled PC and NAND type flash memory, it can also be configured as bootable disk for system recovery.

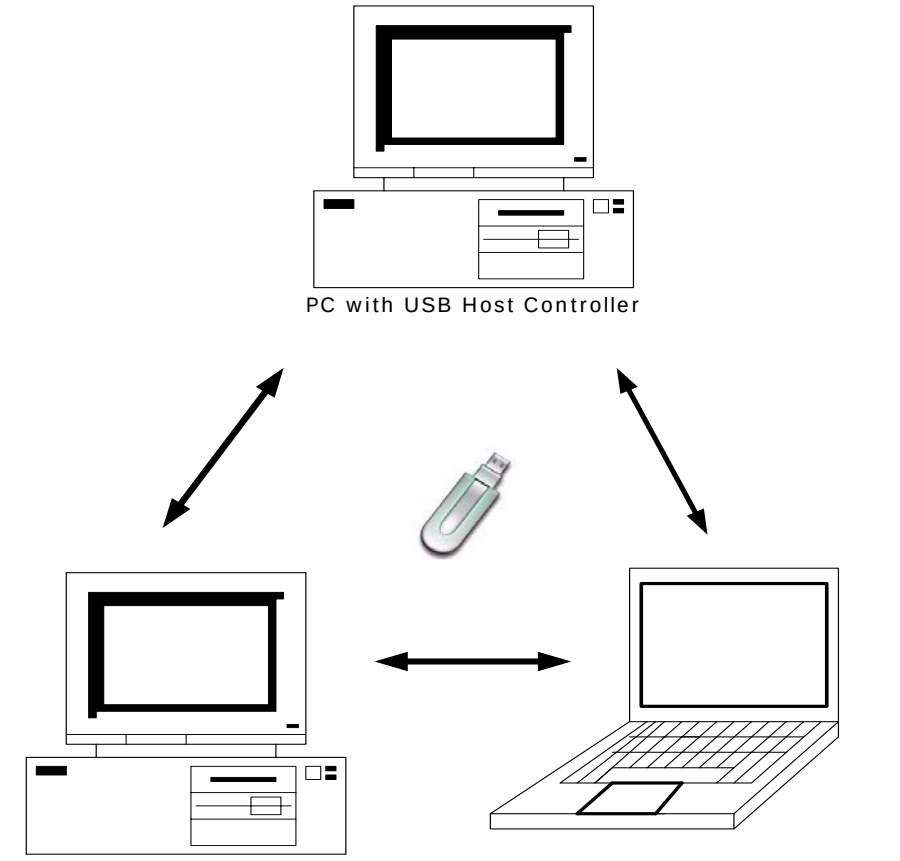
1.2 Features

- Supports dual channel mode for high-speed transfer
- Integrates hardware DMA engine to tune up the operation performance
- Integrates multi-bit ECC correction
- Supports USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Works with default driver from Windows ME, Windows 2000, Windows XP, Mac 9.2, Mac OS X and vendor driver from Alcor for Windows 98SE
- Multiple FIFO implementation for concurrent bus operation
- LED for monitoring bus activities
- Integrates flash memory power control switch
- Supports bad block management
- Supports dynamic serial number modification via mass production utility
- Supports software write-protection
- Supports UFD management application for end users
  - Supports password protection for access security
  - Supports partition and lock-disk function
  - Supports software write protection function
- Available in 48-pin LQFP package

2.0 Application Block Diagram

Following application diagram demonstrates a typical flash disk using the AU6389 chip. By connecting the flash disk to a desktop or notebook PC through USB bus, the AU6389 becomes a bus-powered, high speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram



3.0 Pin Assignment

The AU6389 is packed in 48pin-LQFP . Below figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 3.1 Pin Assignment Diagram

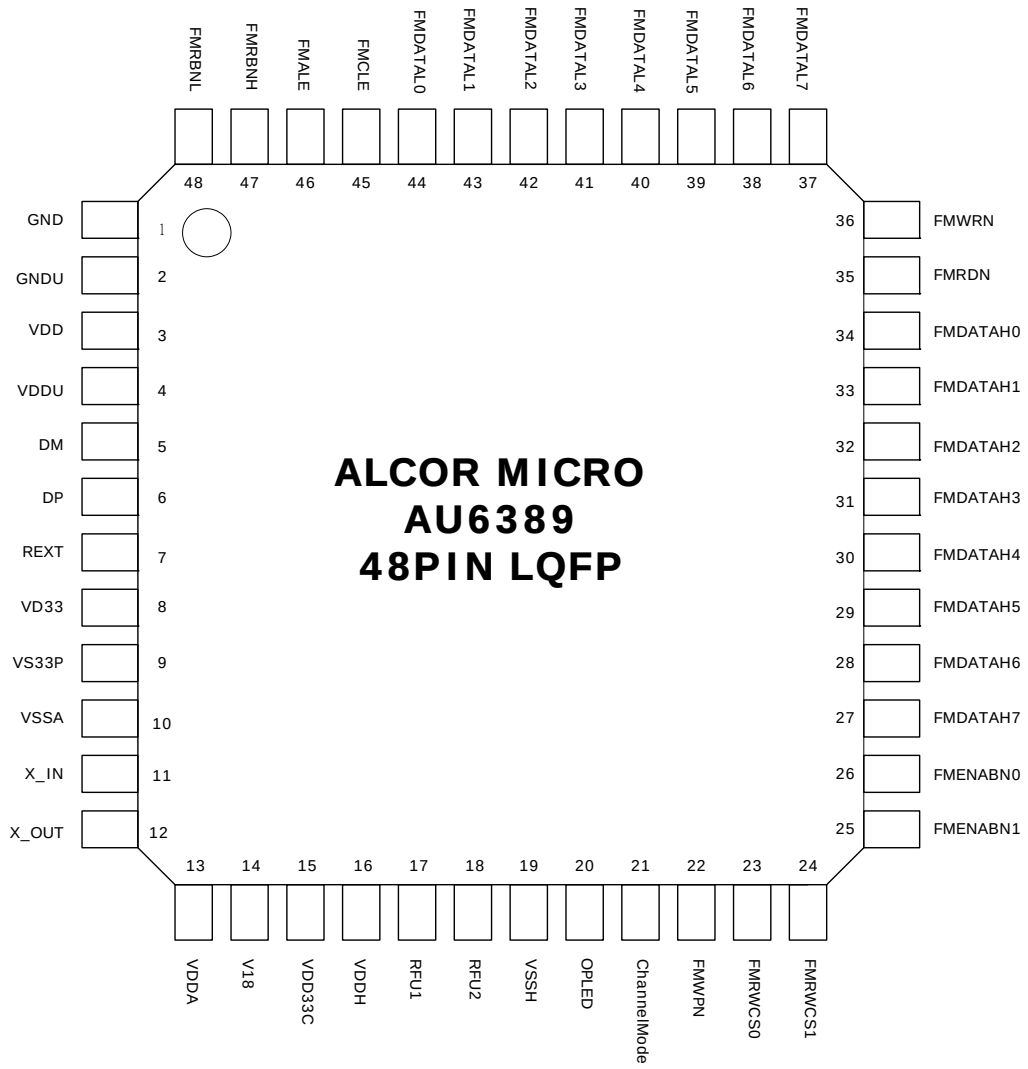


Table 3.1 Pin Descriptions

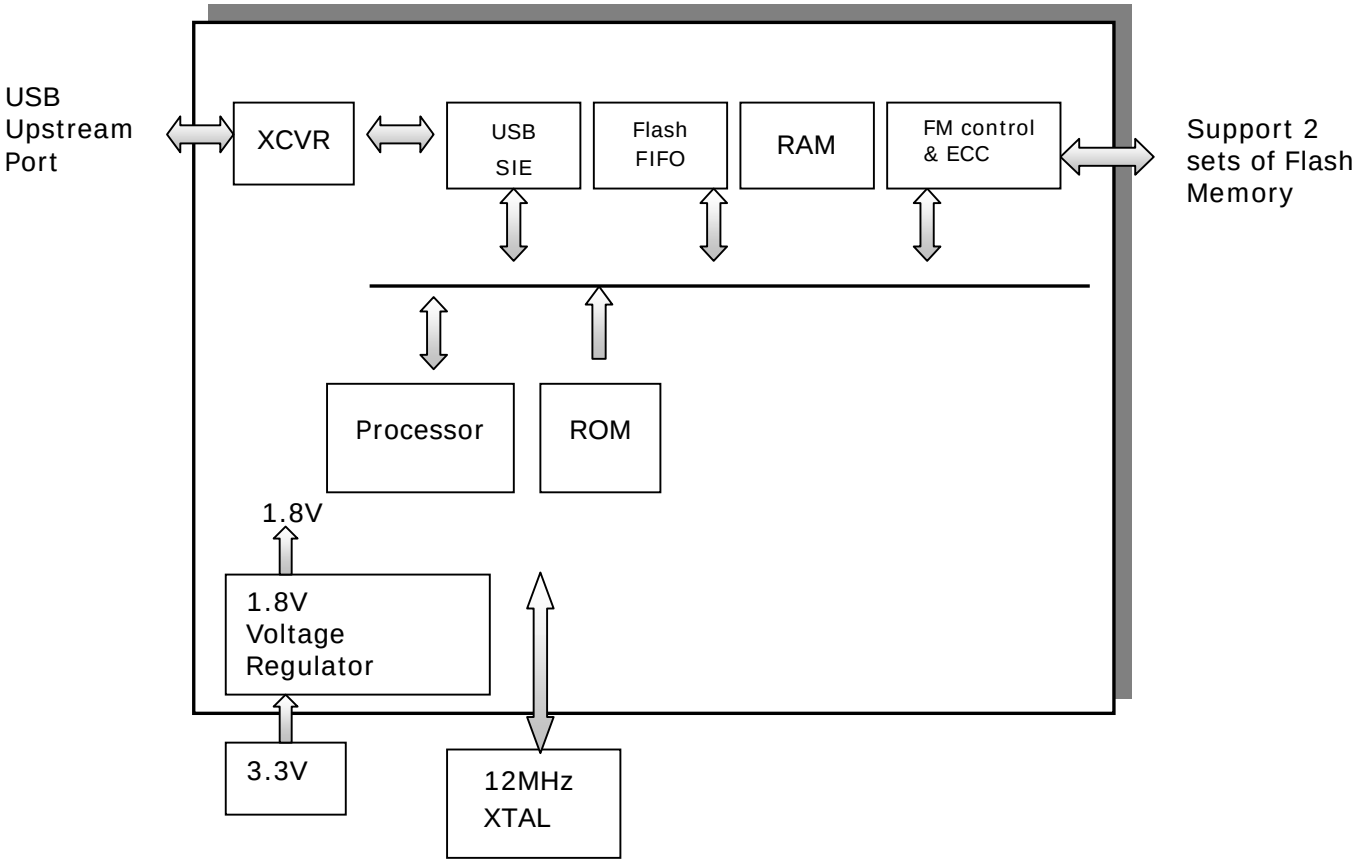
Pin #	Pin Name	I/O	Description
1	GND	GND	Ground
2	GNDU	GND	Ground
3	VDD	I	1.8V Power Source for Core
4	VDDU	I	1.8V Power Source for UTMI
5	DM	I/O	USB DM
6	DP	I/O	USB DP
7	REXT	I	External 6K Resister to Ground
8	VD33	I	3.3V Power Source for UTMI
9	VS33P	GND	Ground
10	VSSA	GND	Ground
11	X_IN	I	12 MHz crystal input.
12	X_OUT	O	12 MHz crystal output.
13	VDDA	I	1.8V Power Source for PLL
14	V18	O	1.8V Power Out for Core
15	VDD33C	O	3.3V Power Out for Flash Memory
16	VDDH	I	3.3V Power Source for IO pad
17	RFU1		Reserved
18	RFU2		Reserved
19	VSSH	GND	Ground
20	OPLED	O	LED for operation indicator
21	ChannelMode	I	Channel Selection (1: Dual Channel; 0: Single Channel[Default])
22	FMWPN	I	Flash Memory Write Protect; High Active
23	FMRWCS0	I	Flash Memory R/W Cycle Selection(11=66ns or ;10=50ns[Default]; Others=33ns)
24	FMRWCS1	I	
25	FMENABN1	O	Flash Memory #1 Enable; Low Active
26	FMENABN0	O	Flash Memory #0 Enable; Low Active
27	FMDATAH7	I/O	Flash Memory DataH[7]
28	FMDATAH6	I/O	Flash Memory DataH[6]
29	FMDATAH5	I/O	Flash Memory DataH[5]
30	FMDATAH4	I/O	Flash Memory DataH[4]
31	FMDATAH3	I/O	Flash Memory DataH[3]
32	FMDATAH2	I/O	Flash Memory DataH[2]
33	FMDATAH1	I/O	Flash Memory DataH[1]
34	FMDATAH0	I/O	Flash Memory DataH[0]
35	FMRDN	O	Flash Memory Read Enable; Low Active
36	FMWRN	O	Flash Memory Write Enable; Low Active
37	FMDATAL7	I/O	Flash Memory DataL[7]
38	FMDATAL6	I/O	Flash Memory DataL[6]

Pin #	Pin Name	I/O	Description
39	FMDATAL5	I/O	Flash Memory DataL[5]
40	FMDATAL4	I/O	Flash Memory DataL[4]
41	FMDATAL3	I/O	Flash Memory DataL[3]
42	FMDATAL2	I/O	Flash Memory DataL[2]
43	FMDATAL1	I/O	Flash Memory DataL[1]
44	FMDATAL0	I/O	Flash Memory DataL[0]
45	FMCLE	O	Flash Memory Command Latch Enable ;High Active
46	FMALE	O	Flash Memory Address Latch Enable; High Active;
47	FMRBNH	I	Flash Memory(H) Ready and Busy Signal (1=Ready ; 0=Busy)
48	FMRBNL	I	Flash Memory(L) Ready and Busy Signal (1=Ready ; 0=Busy)

4.0 System Architecture and Reference Design

4.1 AU6389 Block Diagram

Figure 4.1 AU6389 Block Diagram



5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to V_{CC}+0.3	V
V_{IN}	Input Voltage	-0.3 to 3.6	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	2.25	2.5	2.75	V
V_{IN}	Input Voltage	0	3.3	5.2	V
T_{OPR}	Operating Temperature	0		70	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\|I_{ol}\|$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\|I_{oh}\|$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I_{in}	Input leakage current	V_{in}= V_{CC} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply Voltage		3.0	3.3	3.6	V
VCC	Digital supply Voltage		2.25	2.5	2.75	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
$I_{CC\ (susp)}$	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic：Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VCC-0.2			V

AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV

V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃

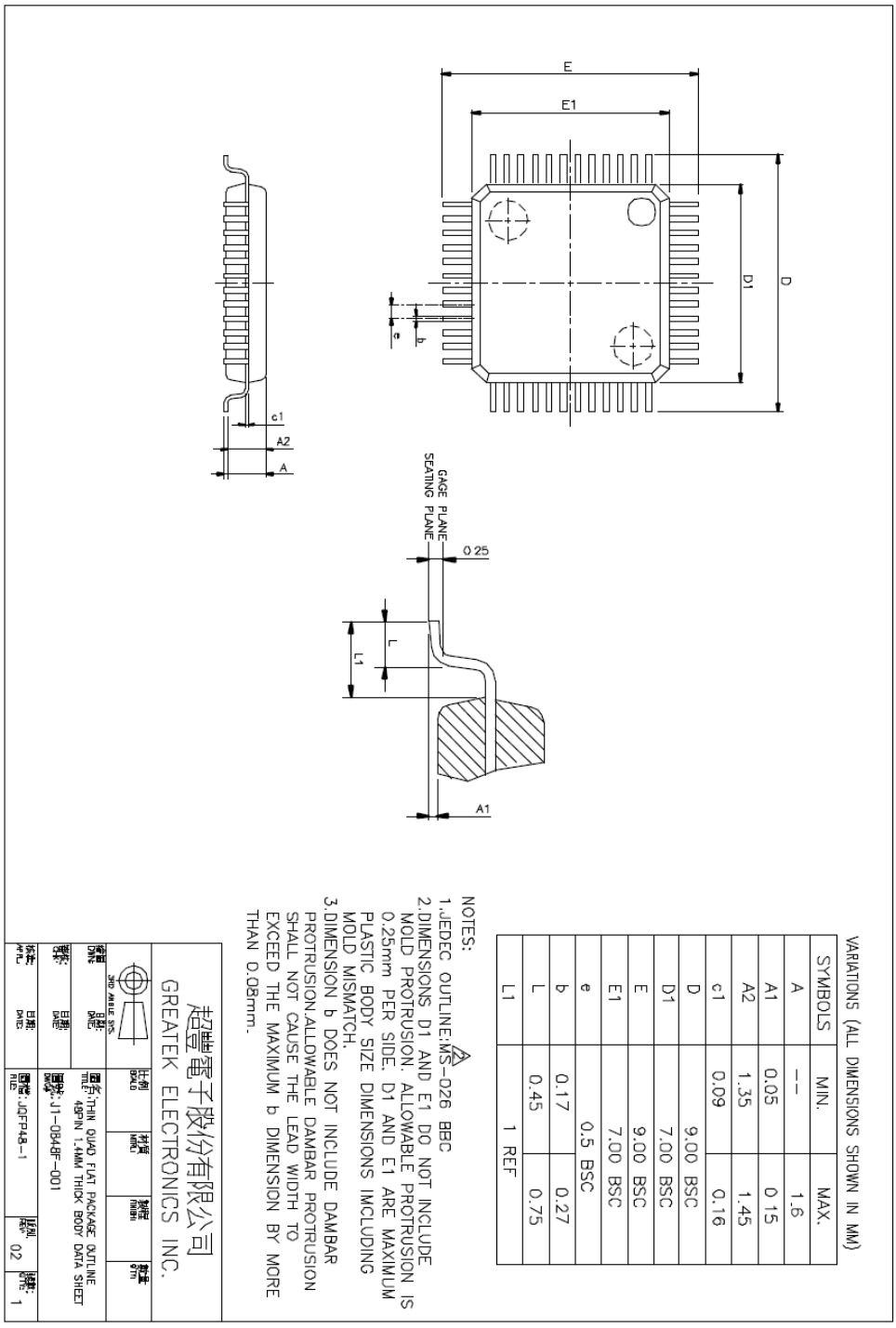
Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%

V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	---	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1.JEDEC OUTLINE:MS-026 BBC
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

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GREATEK ELECTRONICS INC.

TITLE: THIN QUAD FLAT PACKAGE OUTLINE 48PIN 1.4MM THICK BODY DATA SHEET
JT-QB48F-001
JQFP48-1
REV. 02
SHEET 1

7.0 Abbreviations

In this chapter some of the terms and abbreviations used throughout this technical reference manual are listed as follows.

DC Electrical	Direct Current Electrical
PLL	Phase Lock Loop, is a closed-loop frequency control system.
ECC	Error Checking and Correcting
XTAL	Crystal

【MEMO】

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Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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