AU7843 Datasheet

USB Host MP3/WMA Decoder SOC

Rev 1.0

July 7 , 2008

DISCLAIMER

All information and data contained in this document are without any commitment, are not to be considered as an offer for conclusion of a contract, nor shall they be construed as to create any liability. Any new issue of this document invalidates previous issues. Product availability and delivery are exclusively subject to our respective order confirmation form; the same applies to orders based on development samples delivered. By this publication, Shanghai Mountain View Silicon Technology Co. Ltd.("MVSILICON") does not assume responsibility for patent infringements or other rights of third parties that may result from its use.

Shanghai Mountain View Silicon Technology Co. Ltd. assumes no responsibility for any errors contained herein.

Revision History

Data	Revision	Description
2008-7-7	1.0	initial

Contents

Figures

Tables

1. Overview

A highly integrated SOC for MP3/WMA player, AU7843 integrates MCU, MP3/WMA decoder, USB Host controller, SD/MMC card controller, a 16-bit audio decoder and an IR decoder in a single chip. Compared with traditional flash-MP3 player, AU7843 offers a lower cost, lower power consumption, flexible and more powerful host MP3/WMA player solution.

1.1 Features

- Low power 0.18um CMOS technology
- Power supply 1.8V/3.3V, power consumption 125mW, support sleep mode
- Enhanced 8051, up to 10 times faster than standard 8051
- USB2.0 full-speed host controller
- SD/MMC card controller
- Support MPEG 1/2/2.5 layer2/3 decoding, data rate 32kbps ~ 320kbps, including VBR
- Support WMA format, data rate 32kbps ~ 384kbps
- Support 9 sampling frequency: 8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 16-bit sigma-delta audio DAC
- Embedded headphone amplifier
- Support IR Remote control
- GPIO for various purposes
- 2 channel AUX in
- Embedded 64KB OTP memory for program code storage

1.2 Chip Architecture

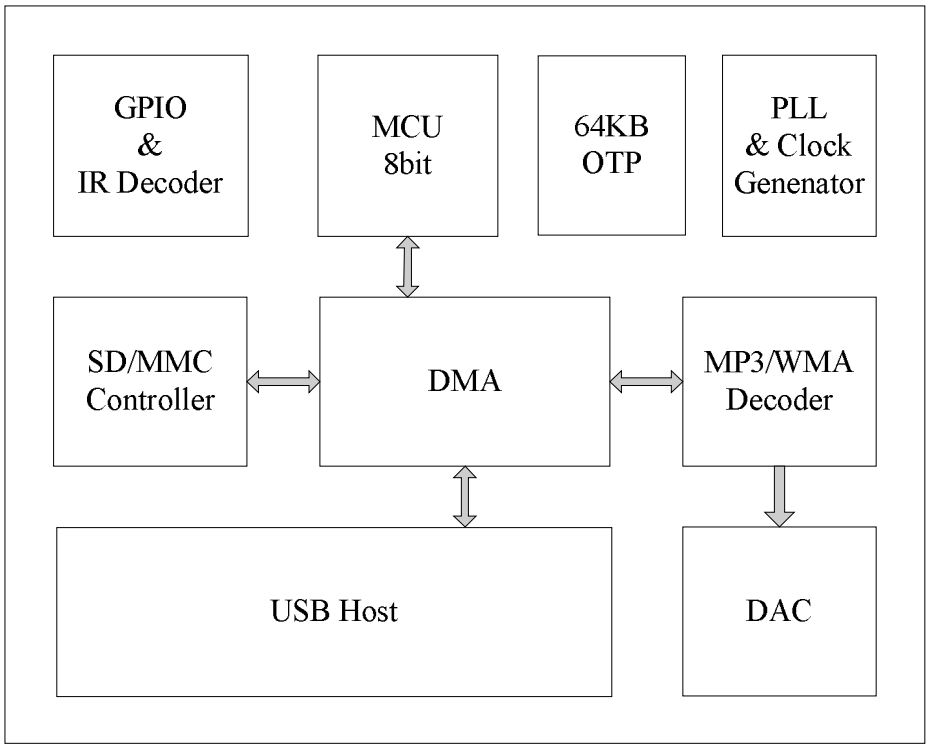

Figure 1 AU7843 Functional Block Diagram

2. System Application

- **MP3/WMA audio system**

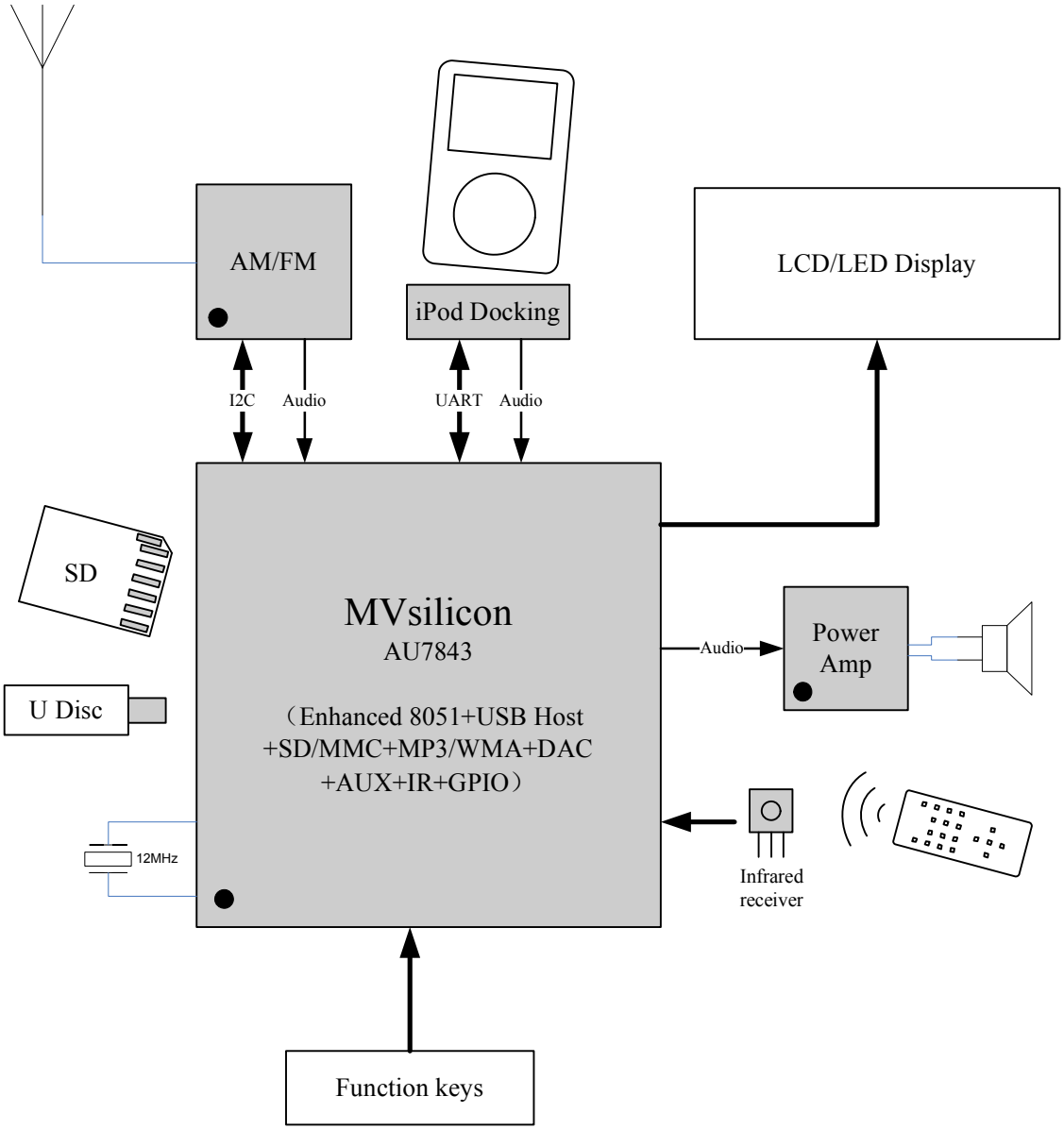

Figure 2 MP3/WMA Audio System

3. Pin Description

AU7843 is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
AI	Analog Input
AO	Analog Output
PWR	Power
GND	Ground

3.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
			USB interface pins
USB_DP	13	I/O	USB Function D+ bus
USB_DM	12	I/O	USB Function D- bus
			CARD interface pins
SD_CLK	33	O	SD Card clock
SD_CMD	35	I/O	SD Card command line
SD_DAT0	36	I/O	SD Card data line
			DAC AUDIO interface pins
DAC_HPOUTL	1	AO	Head phone left channel output
DAC_HPOUTR	3	AO	Head phone right channel output
DAC_VREF	5	AI	Internal voltage reference
AUXIN1_L	61	AI	External AUX in, channel 1 left input
AUXIN1_R	62	AI	External AUX in, channel 1 right input
AUXIN2_L	63	AI	External AUX in, channel 2 left input
AUXIN2_R	64	AI	External AUX in, channel 2 right input
			GPIO/MCU IO pins
GPIO_A[3:0]	20:17	I/O	GPIO PORT, bank A
GPIO_A[7:4]	29:26	I/O	GPIO PORT, bank A
GPIO_B[2:0]	32:30	I/O	GPIO PORT, bank B
GPIO_B[7:3]	53:49	I/O	GPIO PORT, bank B
GPIO_C[1:0]	38:37	I/O	GPIO PORT, bank C
GPIO_C[6:2]	45:41	I/O	GPIO PORT, bank C
GPIO_D[0]	48	I/O	GPIO PORT, bank D
GPIO_D[2:1]	57:56	I/O	GPIO PORT, bank D
GPIO_E[3:2]	22:21	I/O	GPIO PORT, bank E

			CLK & Reset pins
XIN	15	I	12MHz Crystal oscillator input for PLL
XOUT	16	O	12MHz Crystal oscillator output for PLL
RESET_N	25	I	System reset, active low
			mod pin
MOD[1:0]	58:59	I	Chip run mode configure pin
TEST	60	I	Chip test pin
			Power/Ground pins
DAC_AVDD	4	PWR	Analog power for DAC(3.3V)
DAC_AVSS	2	GND	Analog ground for DAC
PLL_VSS	6	GND	Analog ground for PLL
PLL_VDD	7	PWR	Analog power for PLL(1.8V)
VPP	47	PWR	OTP program power
IO_VDD	8 14 34 46	PWR	Digital power for I/O(3.3V)
VSS	11 24 39 54	GND	Digital IO/core ground
VDD	23 40 55	PWR	Digital power for core (1.8V)
Reserved	9 10	NC	

4. Package

4.1 Package Diagram

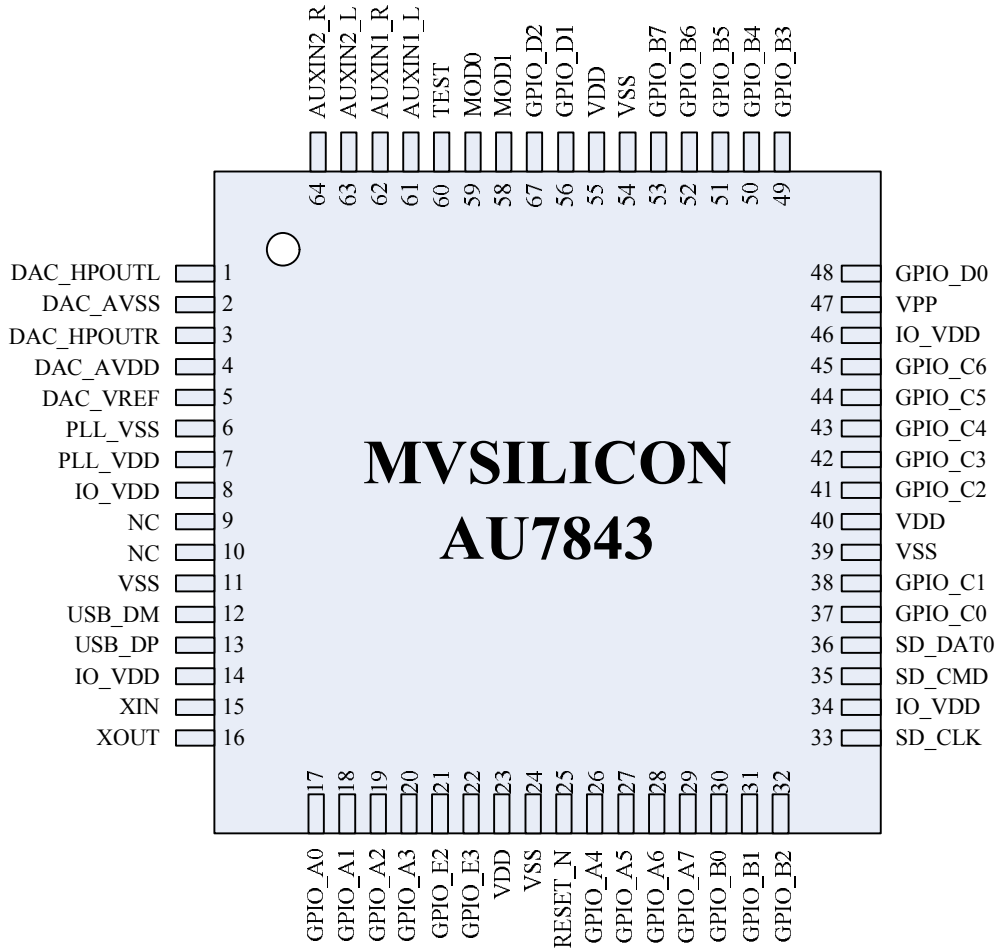

Figure 3 Package Diagram (LQFP64-10x10mm / TOP View)

4.2 Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00BSC	
θ	0	—	8°

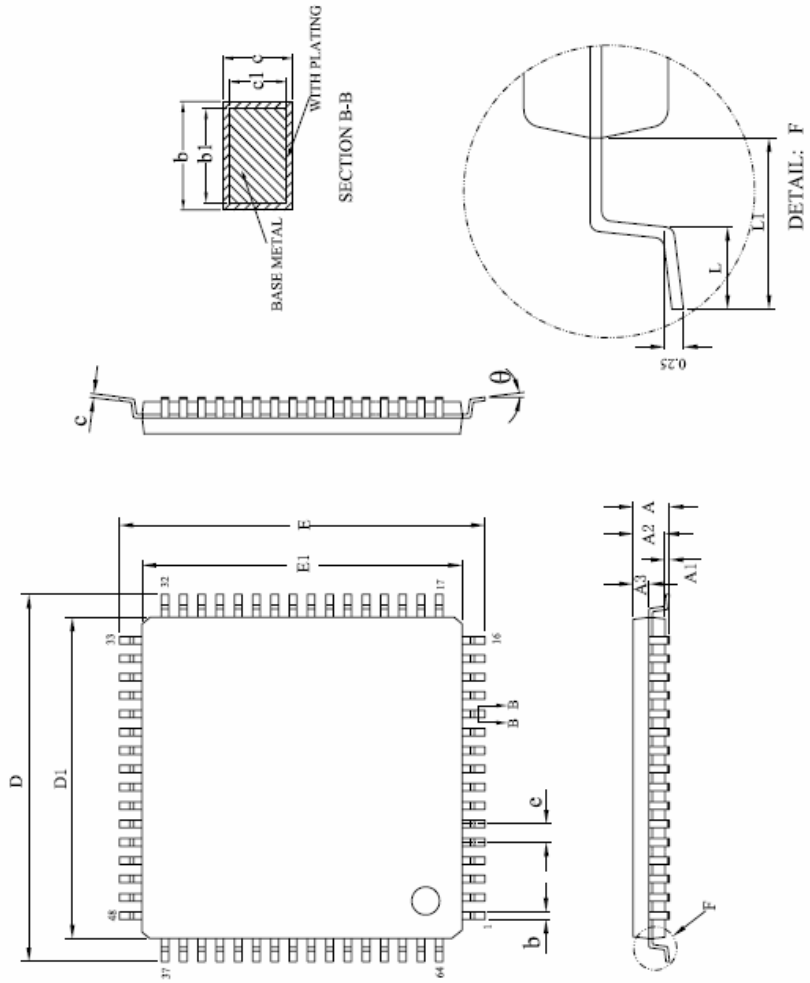

Figure 4 LQFP64-10x10mm Package Dimension Parameter

5. Electrical Specification

5.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCC_IO_AB	-0.5 to 4.6	V
Power Supply Voltage (Core)	VCC_CORE_AB	0 to 2	V
Power Supply Voltage (PLL)	VCC_PLL_AB	-0.2 to 2.2	V
Power Supply Voltage (DAC)	VCC_DAC_AB	-0.3 to 3.6	V
Storage Temperature	TEMP_STG	-65 to 150	C

5.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (IO)	VCC_IO_OP	2.97	3.3	3.63	V
Power Supply Voltage (Core)	VCC_CORE_OP	1.62	1.8	1.98	V
Power Supply Voltage (PLL)	VCC_PLL_OP	1.62	1.8	1.98	V
Power Supply Voltage (DAC)	VCC_DAC_OP	3.0	3.3	3.6	V
Power Supply Voltage (ADC)	VCC_ADC_OP	3.15	3.3	3.45	V
Input Voltage (digital)	VIN	-0.3		5.5	V
Operating_Free Air Temperature	TEMP_OPR	-20		70	C

5.3 Electrical Characteristics

Table 4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		2.0		5.5	V
VIL	Input Low Voltage		-0.3		0.8	V
VOH	Output high voltage	@IOH=2mA	2.4			V
VOL	Output low voltage	@IOL=2mA			0.4	V
IOL	Low level output current for 8mA pins	@VOL = 0.4V	9.7	15.6	18.8	mA
IOH	Low level output current for 8mA pins	@VOH = 2.4V	11.6	23.5	36.0	mA
IL	Input leakage current		-10		10	uA
IOZ	Tri-state output leakage current		-10		10	uA
P_PLAY	Power consumption when playing	Playing mode		125		mW
P_SLEEP	Power consumption when sleeping	Sleeping mode		1		mW

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Contact Information

Shanghai Mountain View Silicon Technology Co Ltd

Shanghai Headquarter:
Suite 403, Jinying Tower A, 1518 Minsheng Road, Pudong New Area,
Shanghai, P.R. China
Zip code: 200135
Tel: 86-21-68549851
Fax: 86-21-68549859

Shenzhen Sales & Technical Support Office:
Suite 8C Olympic Plaza, Shangbao Road, Futian District,
Shenzhen, Guangdong, P.R. China
Zip code: 518034
Tel: 86-755-83522955
Fax: 86-755-83522957

Email: support@mvsilicon.com
Website: http://www.mvsilicon.com