



AU7845 USB HOST MP3/WMA DECODER SOC

# AU7845 Datasheet

**USB Host MP3/WMA Decoder SOC**

**Rev 1.01**

**Aug 28 , 2008**

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## Revision History

<b>Data</b>	<b>Revision</b>	<b>Description</b>
<b>2008-7-7</b>	<b>1.0</b>	<b>initial</b>
<b>2008-8-28</b>	<b>1.01</b>	<b>1. Pin order modified 2. Change some electrical specification</b>

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## 1. Overview

A highly integrated SOC for MP3/WMA player, AU7845 integrates MCU, MP3/WMA decoder, USB Host controller, SD/MMC card controller, a 16-bit audio decoder, RTC, ADC and an IR decoder in a single chip. Compared with traditional flash-MP3 player, AU7845 offers a lower cost, lower power consumption, flexible and more powerful host MP3/WMA player solution.

### 1.1 Features

- Low power 0.18um CMOS technology
- Power supply 1.8V/3.3V, power consumption 125mW, support sleep mode
- Enhanced 8051, up to 10 times faster than standard 8051
- USB2.0 full-speed host controller
- SD/MMC card controller
- Support MPEG 1/2/2.5 layer2/3 decoding, data rate 32kbps ~ 320kbps, including VBR
- Support WMA format, data rate 32kbps ~ 384kbps
- Support 9 sampling frequency:  
8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 16-bit sigma-delta audio DAC
- Embedded headphone amplifier
- Support IR Remote control
- GPIO for various purposes
- RTC embedded
- 4 channel 10-bit SAR ADC for peripheral controls
- 2 channel AUX in
- Embedded 64KB OTP memory for program code storage
- Support external NOR flash for program code storage
- Support in-system debug through external emulator
- In-system firmware upgrade through U-disk or SD/MMC

## 1.2 Chip Architecture

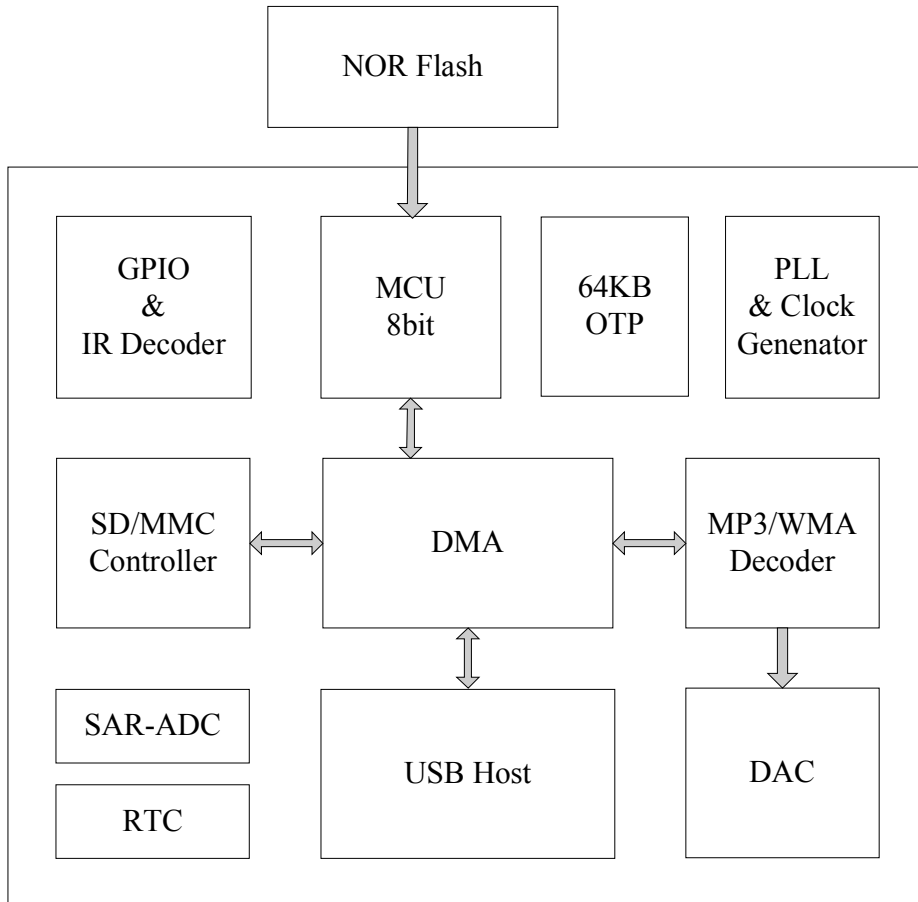


Figure 1 AU7845 Functional Block Diagram



## 2. System Application

- **MP3/WMA audio system**

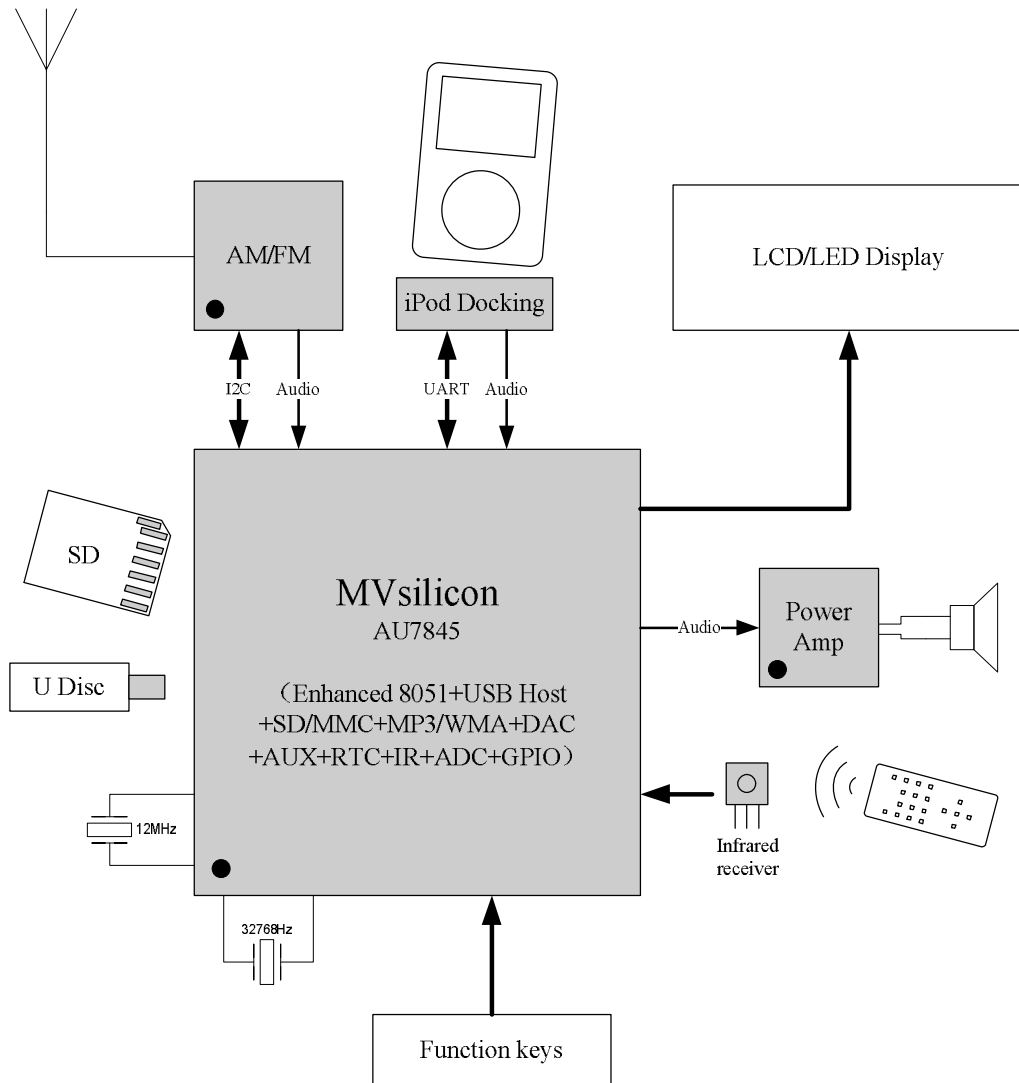


Figure 2 MP3/WMA Audio System

### 3. Pin Description

AU7845 is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
AI	Analog Input
AO	Analog Output
PWR	Power
GND	Ground

#### 3.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
<b>NOR flash memory interface pins</b>			
<b>FSH_DB [7:0]</b>	32:39	I/O	Flash memory data bus
<b>FSH_AB [0:1]</b>	40:41	I/O	Flash memory address bus
<b>FSH_AB [2:3]</b>	57:58	I/O	Flash memory address bus
<b>FSH_AB [4:7]</b>	61:64	I/O	Flash memory address bus
<b>FSH_AB [8:9]</b>	88:89	I/O	Flash memory address bus
<b>FSH_AB [10]</b>	60	I/O	Flash memory address bus
<b>FSH_AB [11]</b>	90	I/O	Flash memory address bus
<b>FSH_AB [12]</b>	65	I/O	Flash memory address bus
<b>FSH_AB [13:14]</b>	87:86	I/O	Flash memory address bus
<b>FSH_AB [15]</b>	66	I/O	Flash memory address bus
<b>FSH_WR</b>	91	I/O	Flash memory write signal
<b>FSH_RD</b>	92	I/O	Flash memory read signal
<b>USB interface pins</b>			
<b>USB_DP</b>	22	I/O	USB Function D+ bus
<b>USB_DM</b>	21	I/O	USB Function D- bus
<b>CARD interface pins</b>			
<b>SD_CLK</b>	51	O	SD Card clock
<b>SD_CMD</b>	53	I/O	SD Card command line
<b>SD_DAT0</b>	54	I/O	SD Card data line
<b>DAC AUDIO interface pins</b>			
<b>DAC_HPOUTR</b>	1	AO	Head phone right channel output
<b>DAC_HPOUTL</b>	3	AO	Head phone left channel output
<b>DAC_VREF</b>	5	AI	Internal voltage reference
<b>AUXINI_R</b>	97	AI	External AUX in, channel 1 right input

<b>AUXIN1_L</b>	98	AI	External AUX in, channel 1 left input
<b>AUXIN2_R</b>	99	AI	External AUX in, channel 2 right input
<b>AUXIN2_L</b>	100	AI	External AUX in, channel 2 left input
<b>SAR ADC interface pins</b>			
<b>ADC_VREF</b>	8	AI	ADC voltage reference
<b>ADC_REXT100K</b>	9	AI	ADC connected with a 100kohm external resistor
<b>ADC_CH1</b>	10	AI	Analog voltage input, channel 1
<b>ADC_CH2</b>	11	AI	Analog voltage input, channel 2
<b>ADC_CH3</b>	12	AI	Analog voltage input, channel 3
<b>ADC_CH4</b>	13	AI	Analog voltage input, channel 4
<b>GPIO/MCU IO pins</b>			
<b>GPIO_A[3:0]</b>	29:26	I/O	GPIO PORT, bank A
<b>GPIO_A[7:4]</b>	47:44	I/O	GPIO PORT, bank A
<b>GPIO_B[2:0]</b>	50:48	I/O	GPIO PORT, bank B
<b>GPIO_B[7:3]</b>	80:76	I/O	GPIO PORT, bank B
<b>GPIO_C[1:0]</b>	56:55	I/O	GPIO PORT, bank C
<b>GPIO_C[7:2]</b>	73:68	I/O	GPIO PORT, bank C
<b>GPIO_D[0]</b>	75	I/O	GPIO PORT, bank D
<b>GPIO_D[3:1]</b>	85:83	I/O	GPIO PORT, bank D
<b>CLK &amp; Reset pins</b>			
<b>XIN</b>	24	I	12MHz Crystal oscillator input for PLL
<b>XOUT</b>	25	O	12MHz Crystal oscillator output for PLL
<b>RTC_XIN</b>	18	I	32.768KHz Crystal oscillator input for RTC
<b>RTC_XOUT</b>	19	O	32.768KHz Crystal oscillator output for RTC
<b>RESET_N</b>	42	I	System reset, active low
<b>mod pin</b>			
<b>MOD[1:0]</b>	93:94	I	Chip run mode configure pin
<b>TEST</b>	95	I	Chip test pin
<b>Power/Ground pins</b>			
<b>DAC_AVDD</b>	4	PWR	Analog power for DAC(3.3V)
<b>DAC_AVSS</b>	2	GND	Analog ground for DAC
<b>PLL_VSS</b>	14	GND	Analog ground for PLL
<b>PLL_VDD</b>	15	PWR	Analog power for PLL(1.8V)
<b>ADC_AVDD</b>	7	PWR	Analog power for ADC(3.3V)
<b>ADC_AVSS</b>	6	GND	Analog ground for ADC
<b>VPP</b>	74	PWR	OTP program power
<b>IO_VDD</b>	17 23 52 96	PWR	Digital power for I/O(3.3V)
<b>VSS</b>	20 31 59 81	GND	Digital IO/core ground
<b>VDD</b>	16 30 43 67 82	PWR	Digital power for core (1.8V)

## 4. Package

### 4.1 Package Diagram

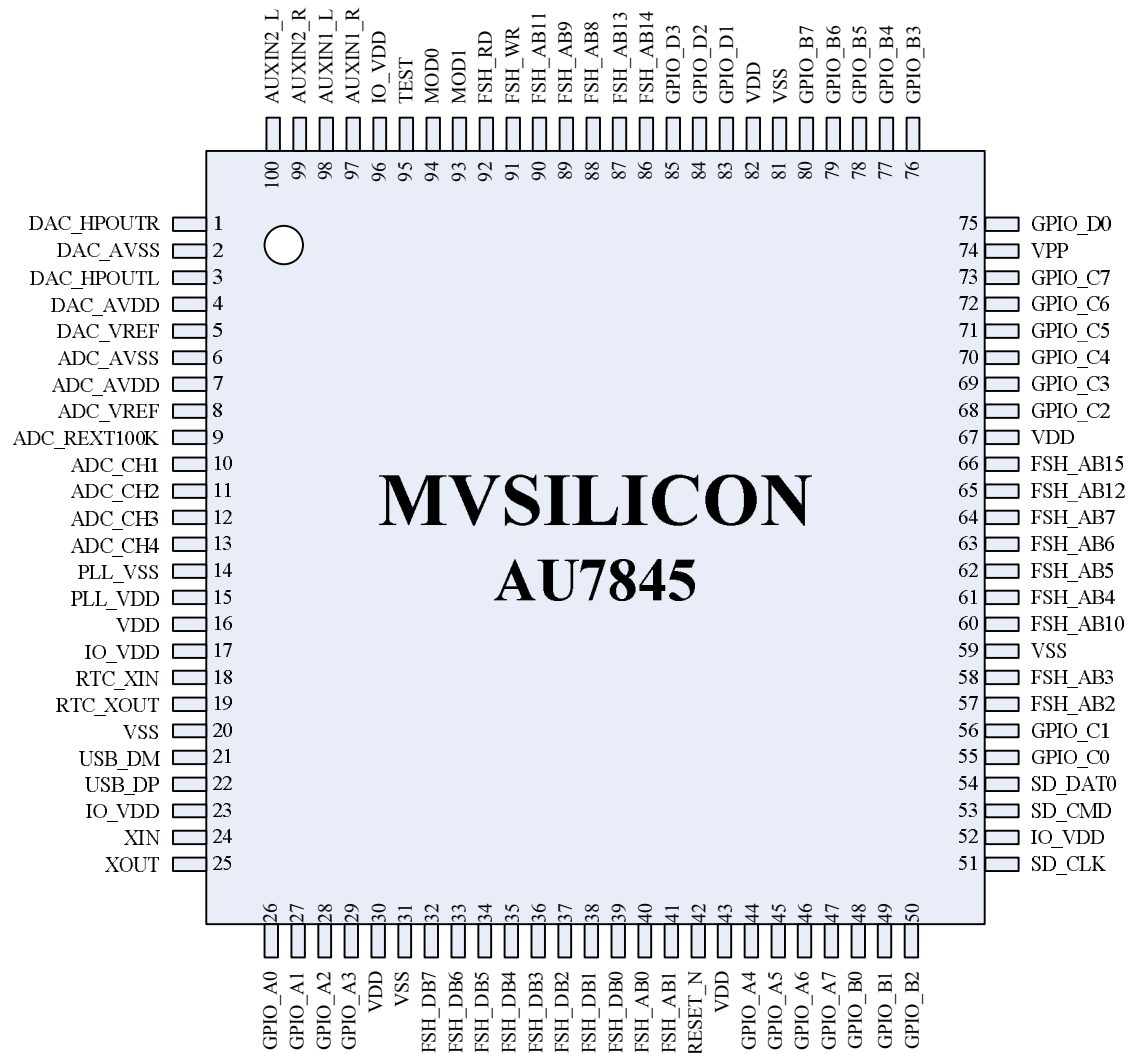


Figure 3 Package Diagram (LQFP100-14x14mm / TOP View)



### 4.2 Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e	0.50BSC		
L	0.40	0.60	0.80
L1	1.00BSC		
θ	0	—	8°

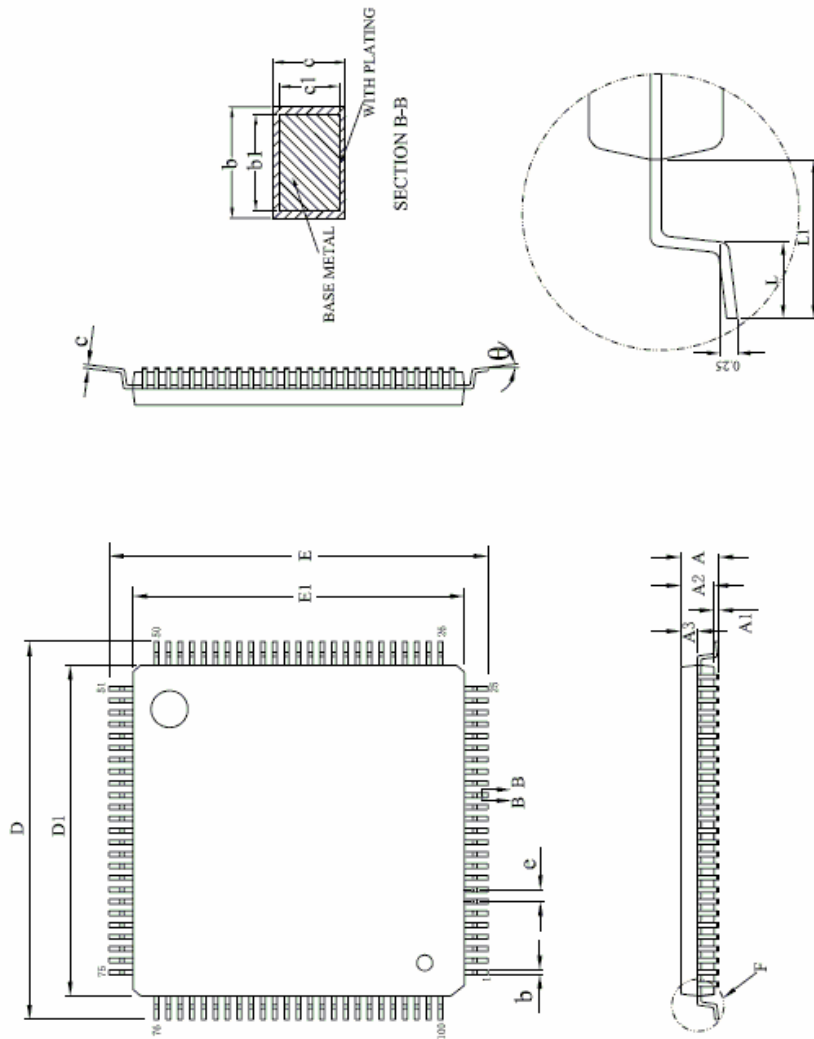


Figure 4 LQFP100-14x14mm Package Dimension Parameter

## 5. Electrical Specification

### 5.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCC_IO_AB	-0.5 to 4.6	V
Power Supply Voltage (Core)	VCC_CORE_AB	0 to 2	V
Power Supply Voltage (PLL)	VCC_PLL_AB	-0.2 to 2.2	V
Power Supply Voltage (DAC)	VCC_DAC_AB	-0.3 to 3.6	V
Storage Temperature	TEMP_STG	-65 to 150	C

### 5.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (IO)	VCC_IO_OP	2.97	3.3	3.63	V
Power Supply Voltage (Core)	VCC_CORE_OP	1.62	1.8	1.98	V
Power Supply Voltage (PLL)	VCC_PLL_OP	1.62	1.8	1.98	V
Power Supply Voltage (DAC)	VCC_DAC_OP	3.0	3.3	3.6	V
Power Supply Voltage (ADC)	VCC_ADC_OP	3.15	3.3	3.45	V
Input Voltage (digital)	VIN	-0.3		5.5	V
Operating Free Air Temperature	TEMP_OPR	-20		70	C

### 5.3 Electrical Characteristics

Table 4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>IH</sub>	Input High Voltage		2.0		5.5	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V
V <sub>OH</sub>	Output high voltage	@I <sub>OH</sub> =2mA	2.4			V
V <sub>OL</sub>	Output low voltage	@I <sub>OL</sub> =2mA			0.4	V
I <sub>OL</sub>	Low level output current for 8mA pins	@V <sub>OL</sub> = 0.4V	9.7	15.6	18.8	mA
I <sub>OH</sub>	Low level output current for 8mA pins	@V <sub>OH</sub> = 2.4V	11.6	23.5	36.0	mA
I <sub>L</sub>	Input leakage current		-10		10	uA
I <sub>OZ</sub>	Tri-state output leakage current		-10		10	uA
P <sub>PLAY</sub>	Power consumption when playing	Playing mode		125		mW
P <sub>SLEEP</sub>	Power consumption when sleeping	Sleeping mode		1.5		mW

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.



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