Data Book

AU9362
USB Multiple Slots Flash Memory Card Reader
Technical Reference Manual

Product Specification

Official Release

Revision 1.03

Public

Jun 2004

Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision	Description
Aug 2003	1.00/A21	Add 5th slot support for xD.
Oct 2003	1.01/A23,D23	Add additional configuration to support 2-slots version.
May 2004	1.02/A23,D23	Update 5.2 “Sample Schematics”
Jun 2004	1.03/A23,D23	Update 5.2 “Sample Schematics”

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1.0 Introduction

1.1 Description

The AU9362 is a single chip USB flash memory reader controller which supports the widely used flash memory cards such as Compact Flash (CF) card, Micro Drive (MD), Smart Media Card (SMC), XD Picture Card, Memory Stick (MS), Memory Stick Duo, Memory Stick PRO, Secure Digital (SD) and Multimedia Card (MMC). It can be used as removable storage disks in enormous data exchange applications between PC and PC or PC and various consumer electronic appliances.

The AU9362 reads digital contents saved on memory card that user captured with consumer electronic devices such as digital cameras, MP3 players, PDAs and mobile phones… etc.

In addition, AU9362 allows user to transfer information such as data, graphics, texts or digital images from one electronic device to another quickly and easily. With AU9362, users' experience will be further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows 2000/XP and Mac OS X.

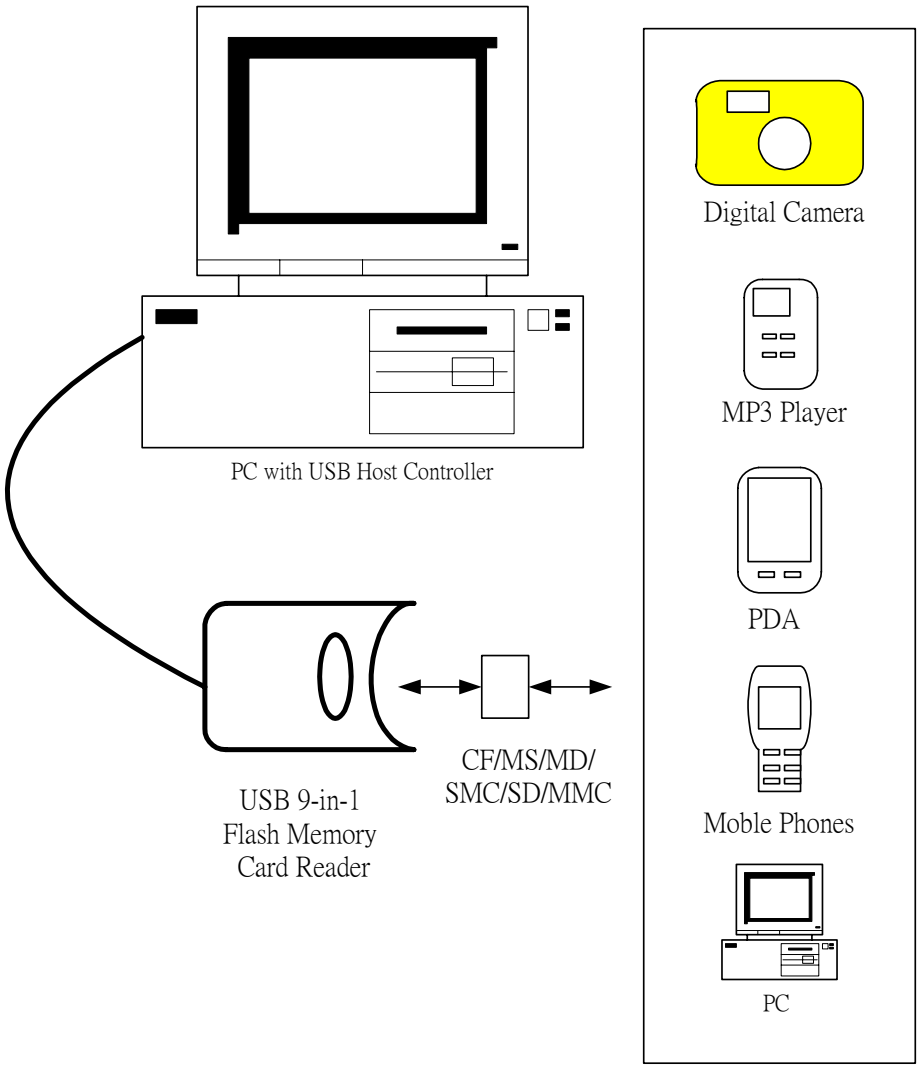
1.2 Features

- Support USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Support Compact Flash (CF) v1.4 Specification
- Support Secure Digital (SD) v1.0 Specification.
- Support Memory Stick (MS) v1.3 Specification.
- Support Memory Stick PRO v1.0 Specification.
- Support Memory Stick ROM Format v1.0 Specification.
- Support Smart Media Card (SMC) Standard 2000 Specification.
- Support xD-Picture Card Format V1.0 Specification
- Support IBM Microdrive device.
- Work with default driver from Windows ME, Windows XP, Mac OS 9, and Mac OS X. Windows 98, Windows 2000 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer to 4GB to optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- Support multiple slot concurrent operation.
- Integrated power switch and power management circuit for each slot to meet USB 500uA power consumption during suspend with card in the slot.
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- 64-pin LQFP package

2.0 Application Block Diagram

Following is the application diagram of a typical flash memory card reader using AU9362. By connecting the reader to a PC through USB bus, the AU9362 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.

Figure 2.1 Block Diagram



3.0 Operating Mode Selection

The Au9362 offers two operating modes. Mode 0 is used for SD/SMC/MS combo socket. While mode 1 is designed for single function socket. Mode 1 support xD card in a shared SMC socket.

Table 3.1 Mode Table

Mode 0 (2SLOTSEL : 0)		Mode 1 (2SLOTSEL : 1)	
Slot 1	CF	Slot 1	SD
		Slot 2	CF
Slot 2	SD/SMC/MS	Slot 3	SMC/XD
		Slot 4	MS

4.0 Pin Assignment

The AU9362 is packed in 64-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 4.1 Pin Assignment Diagram

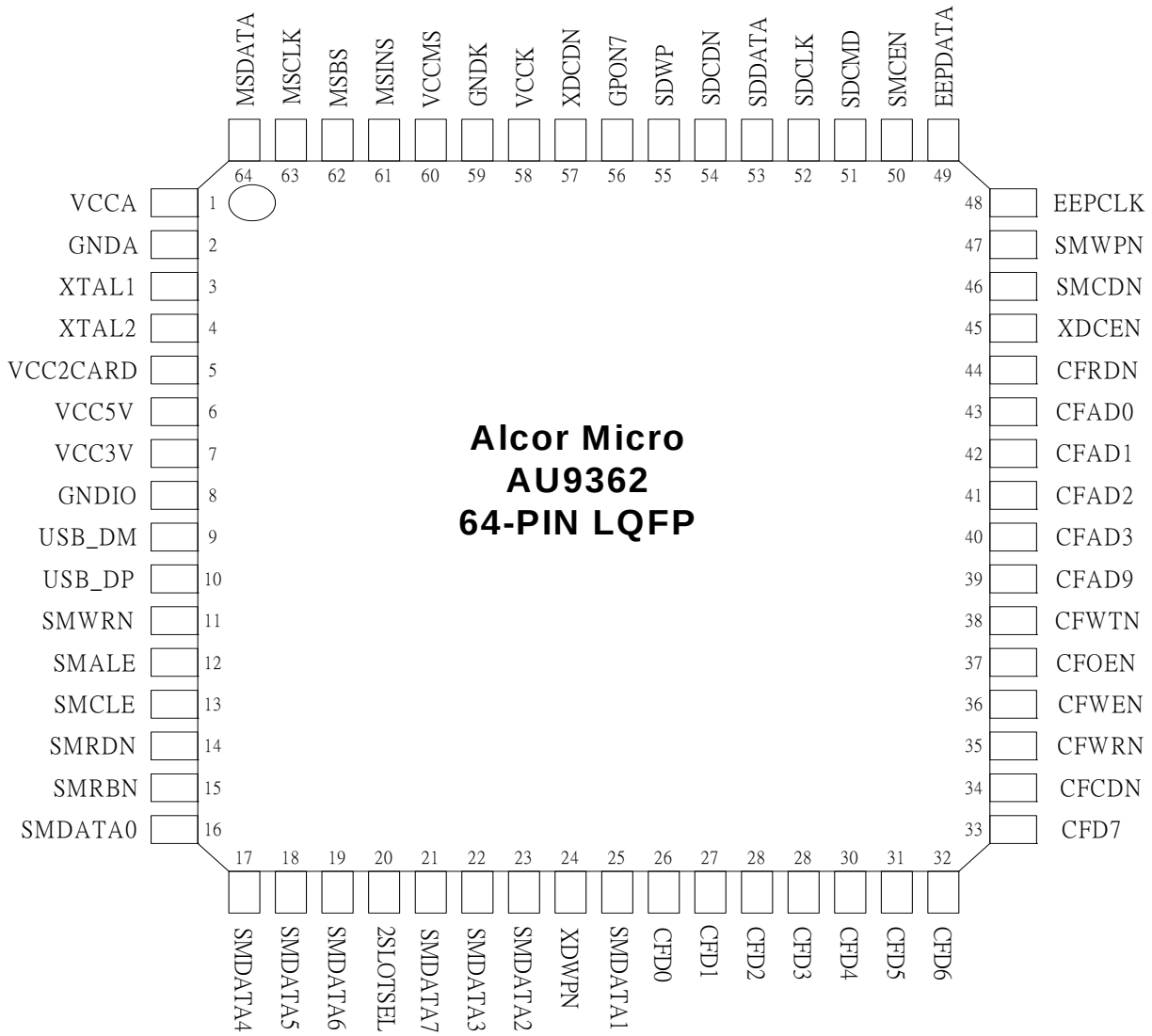


Table 4-1. Pin Descriptions

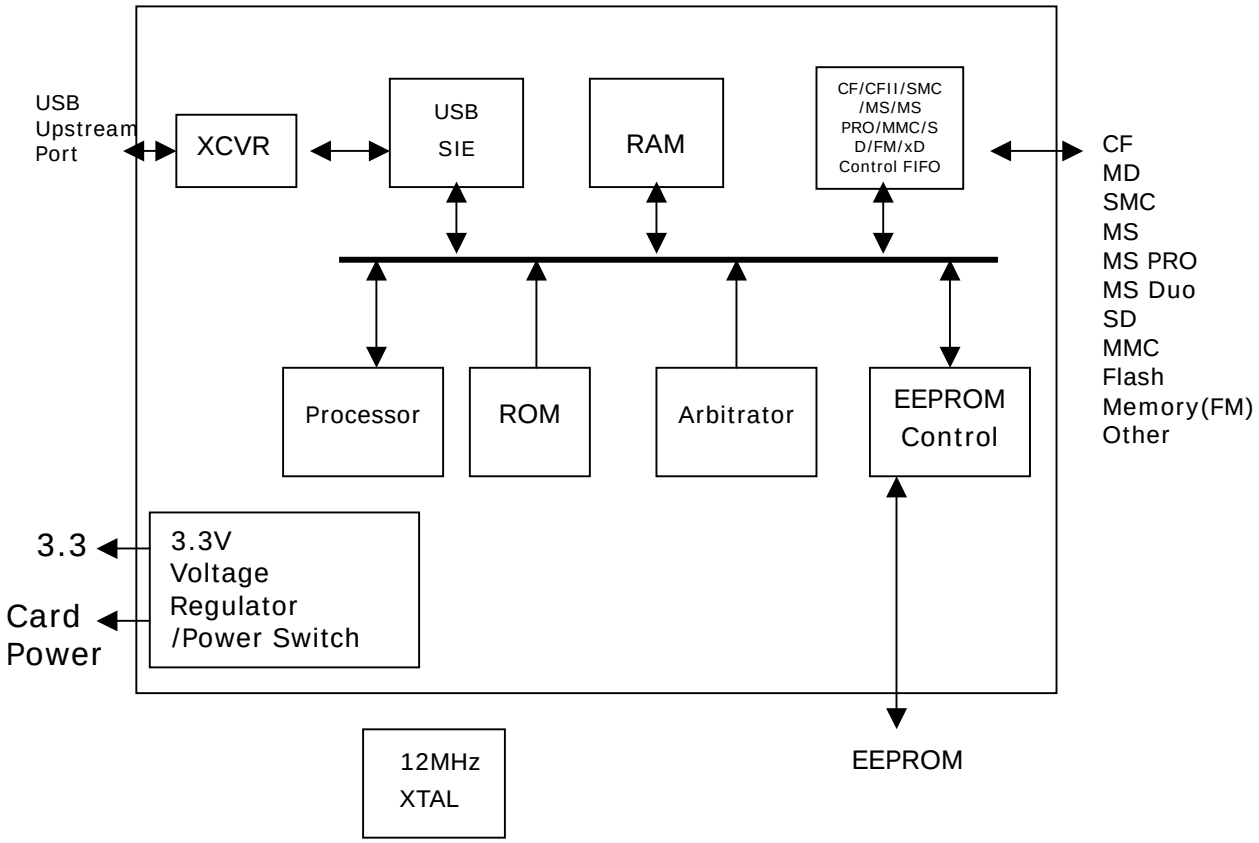
Pin	Pin Name	I/O Type	Description
1	VCCA	PWR	Analog 3.3V input.
2	GNDA	PWR	Ground. Analog ground.
3	XTAL1	I	Crystal Oscillator Input (12MHz).
4	XTAL2	O	Crystal Oscillator Output (12MHz).
5	VCC2CARD	O	Connect to Card Power.
6	VCC5V	PWR	5V power supply from USB connector.
7	VCC3V	PWR	Internally regulated 3.3V power supply output.
8	GNDIO	PWR	Ground :I/O
9	USB_DM	I/O	USB DM.
10	USB_DP	I/O	USB DP.
11	SMWRN	O	SMC Write Enable.(0: write enable, 1: write disable.)
12	SMALE	O	SMC Address Latch Enable. (0: ALE closed, 1: ALE open.)
13	SMCLE	O	SMC Command Latch Enable. (0: CLE closed, 1: CLE open.)
14	SMRDN	O	SMC Read Enable. (0: read enable, 1: read disable.)
15	SMRBN	I	SMC Ready/Busy. (0: busy, 1: ready.)
16	SMDATA0	I/O	SMC Data0.
17	SMDATA4	I/O	SMC Data4.
18	SMDATA5	I/O	SMC Data5.
19	SMDATA6	I/O	SMC Data6.
20	2SLOTSEL	I	Mode Selection. (0: 2 slots mode, 1: 4 slots mode.)
21	SMDATA7	I/O	SMC Data7.
22	SMDATA3	I/O	SMC Data3.
23	SMDATA2	I/O	SMC Data2.
24	XDWPN	I	XD Write protect (0: protect, 1: not protect.)
25	SMDATA1	I/O	SMC Data1.
26	CFD0	I/O	CF Card Data0.
27	CFD1	I/O	CF Card Data1.
28	CFD2	I/O	CF Card Data2.
29	CFD3	I/O	CF Card Data3
30	CFD4	I/O	CF Card Data4.
31	CFD5	I/O	CF Card Data5.
32	CFD6	I/O	CF Card Data6.
33	CFD7	I/O	CF Card Data7.
34	CFCDN	I	CF Card Detect. Internal pull-up pad.
35	CFWRN	O	CF Card IOWRN.
36	CFWEN	O	CF Card WE.
37	CFOEN	O	CF Card OE.
38	CFWTN	I	CF Card WAIT.
39	CFAD9	O	CF Card Addr9.
40	CFAD3	O	CF Card Addr3.
41	CFAD2	O	CF Card Addr2.
42	CFAD1	O	CF Card Addr1.
43	CFAD0	O	CF Card Addr0.
44	CFRDN	O	CF Card IORD.
45	XDCEN	O	XD Card Enable. (0: enable, 1: disable.)
46	SMCDN	I	SMC Card Detect. Internal pull-up pad.
47	SMWPN	I	SMC Write Protect. (0: protected, 1: not protected.)
48	EEPCLK	O	EEPROM Serial Clock.
49	EEPDATA	I/O	EEPROM Serial Data.
50	SMCEN	O	SMC Enable. (0: disable, 1: enable.)

51	SDCMD	I/O	SD CMD.
52	SDCLK	O	SD CLK.
53	SDDATA	I/O	SD Data.
54	SDCDN	I	SD Card Detect. Internal pull-up pad.
55	SDWP	I	SD Write Protect.
56	GPON7	I/O	General Purpose Out, used as activity LED.
57	XDCDN	I	XD Card Detect. Internal pull-up pad.
58	VCCK	PWR	Core 3.3V Input.
59	GNDK	PWR	Ground.
60	VCCMS	PWR	MS 3.3V Input.
61	MSINS	I	MS Card INS. Internal pull-up pad.
62	MSBS	O	MS Card BS.
63	MSCLK	O	MS Card SCLK.
64	MSDATA	I/O	MS Card DATA.

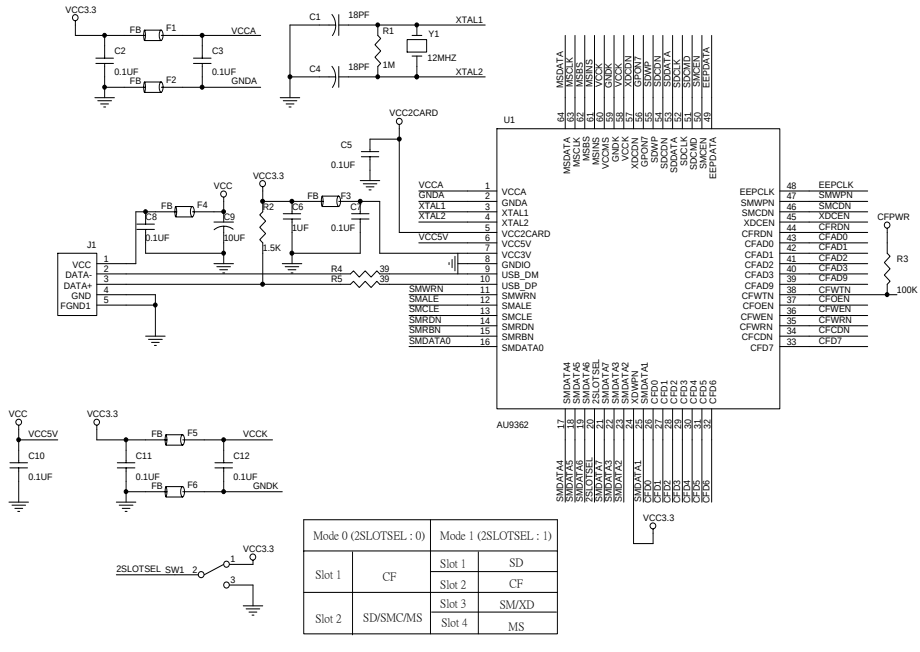
5.0 System Architecture and Reference Design

5.1 AU9362 Block Diagram

Figure 5.1 AU9362 Block Diagram



5.2 Sample Schematics



Mode 0 (2SLOTSEL : 0)		Mode 1 (2SLOTSEL : 1)	
Slot 1	CF	Slot 1	SD
		Slot 2	CF
Slot 2	SD/SMC/MS	Slot 3	SM/XD
		Slot 4	MS

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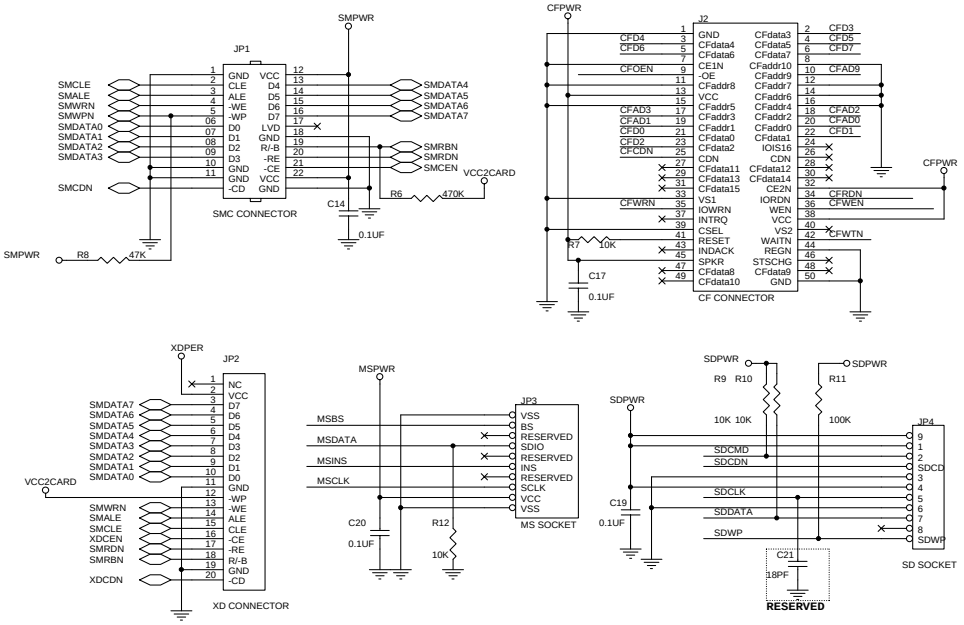
Size	Document Number	Rev
A4	Au9362 card reader demostration schematics	2.51
Date: Thursday, June 24, 2004	Sheet 1 of 3	



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A4	Au9362 card reader demostration schematics	2.51
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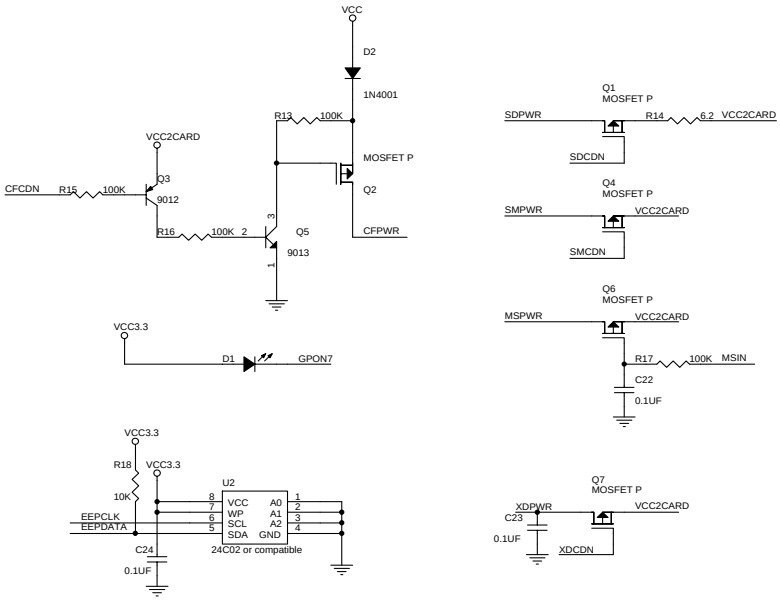

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A4	Au9362 card reader demostration schematics	2.51
Date: Thursday, June 24, 2004	Sheet 3 of 3	

6.0 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	°C

6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	-5		85	°C

6.3 General DC Characteristics

Table 6.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	μA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	μA
I_{OZ}	Tri-state leakage current		-10		10	μA
C_{IN}	Input capacitance			4		ρF
C_{OUT}	Output capacitance			4		ρF
C_{BID}	Bi-directional buffer capacitance			4		ρF

6.4 DC Electrical Characteristics for 5 volts operation

Table 6.4 DC Electrical Characteristics for 5 volts operation

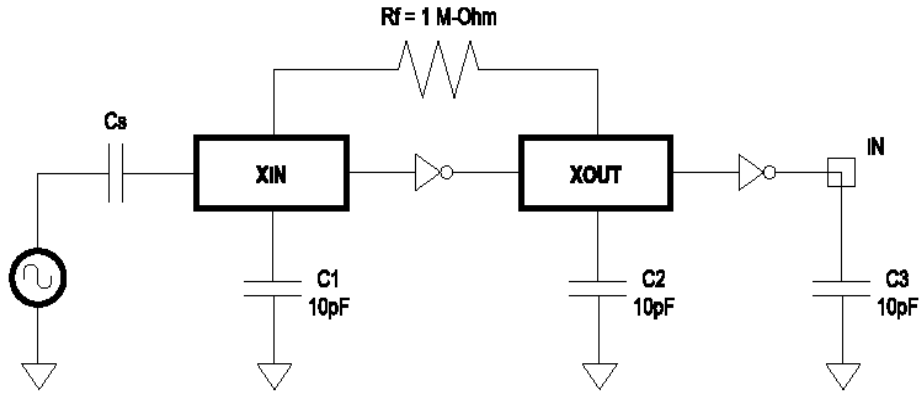
(Under Recommended Operating Conditions and V_{CC}=4.5v ~ 5.5v , Tj= -40°C to + 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IL}	Input Low Voltage	CMOS			0.3*V_{CC}	V
V_{IL}	Schmitt input Low Voltage	TTL		1.10		V
V_{IL}	Schmitt input Low V oltage	CMOS		1.84		V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IH}	Input Hight Voltage	CMOS	0.7*V_{CC}			V
V_{IH}	Schmitt input High Voltage	TTL		1.87		V
V_{IH}	Schmitt input High Voltage	CMOS		3.22		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	3.5			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		50		KΩ

6.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.

Figure 6.1 Crystal Oscillator Circuit Setup for Characterization



6.6 USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

Table 6.5 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Table 6.6 Absolute Maximum Rating System

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	Vi<0		-50	mA
V_I	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
I_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_O	DC output voltage	Note 3	-0.5	Vcc +0.5	V
I_O	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
I_O	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{CC}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STO}	Storage temperature range		-60	+150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

Table 6.7 DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40°C to +85°C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.6V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.6V (Note 3)	0.8	1.1		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	Vcc=3.6V VI=Vcc or GND Io=0		330	600	µA
Isup	Supply current in suspend	Vcc=3.6V VI=Vcc or GND Io=0			70	µA
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Input leakage current	Vcc=3.6V VI=5.5V or GND, not for I/O Pins		+/-0.1	+/-0.5	µA
IOFF	3-state output OFF-state current	Vi=Vih or ViL; Vo=Vcc or GND			+/-10	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

Table 6.8 ACElectricalCharacteristics

GND=0V, t_R = t_F =3.0 ns; C_L =50 pF; RL=500 Ohms

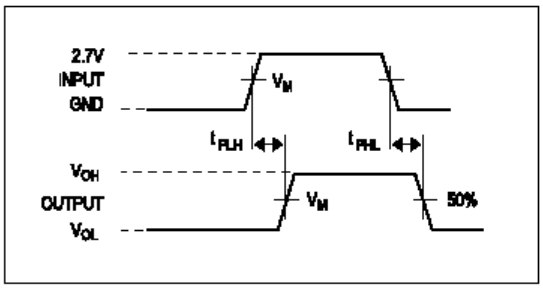
SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{AMB})					UNIT
			0˚C to +25˚C			0˚C to +70˚C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point[1]	3	1.3		2.0	1.3	2.0	V

NOTES:

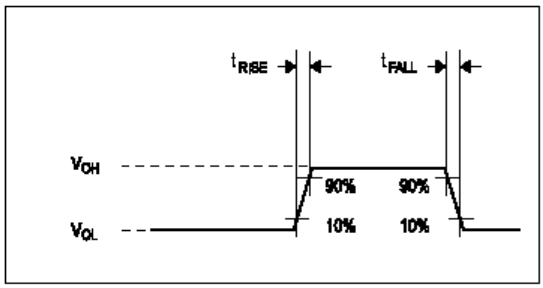
1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.

Figure 6.2 Electrical Characteristics Diagram

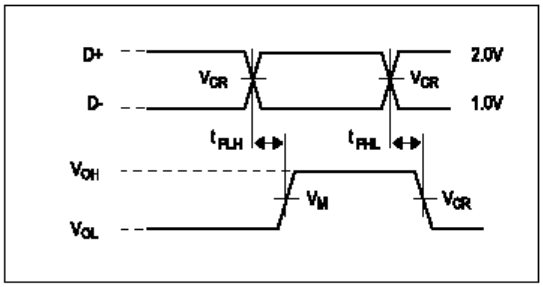
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



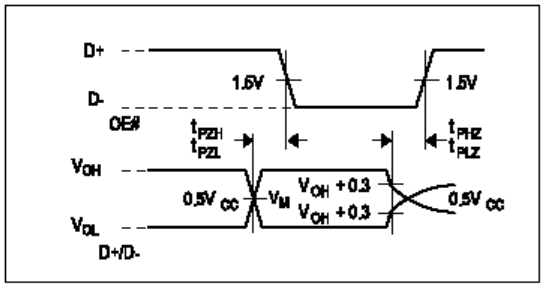
AC WAVEFORM 2.
RISE AND FALL TIMES



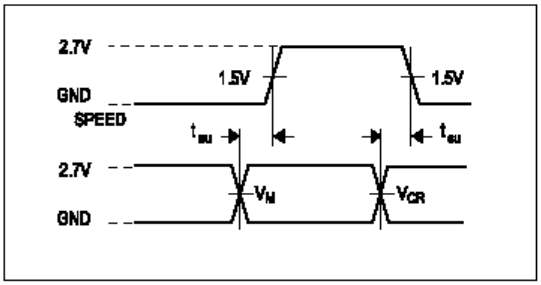
AC WAVEFORM 3.
D+/D- TO RCV



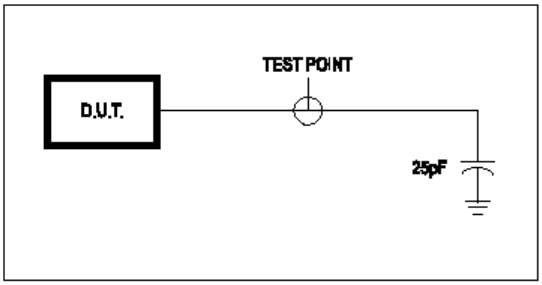
AC WAVEFORM 4.
OE# TO D/+/D-



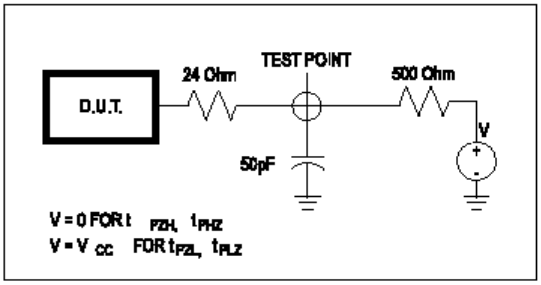
AC WAVEFORM 5.
SETUP FOR SPEED



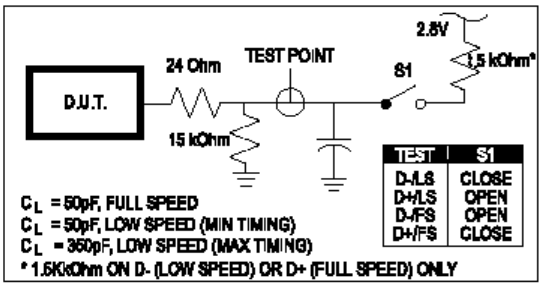
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



6.7 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test circuit & condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

Table 6.9 ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	6000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

6.8 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

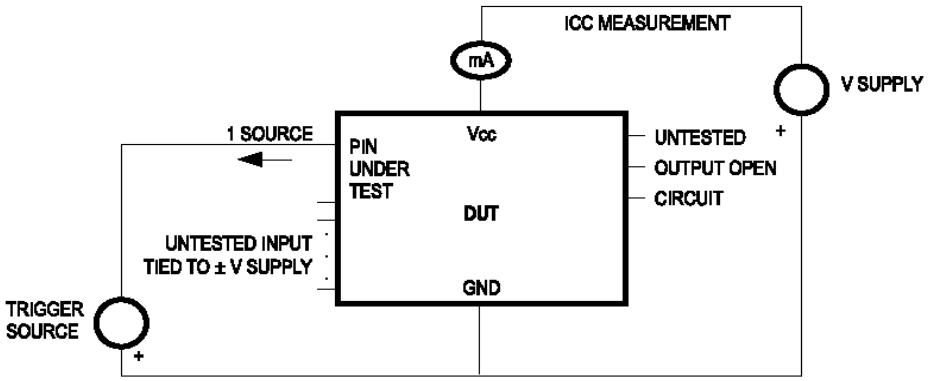
Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

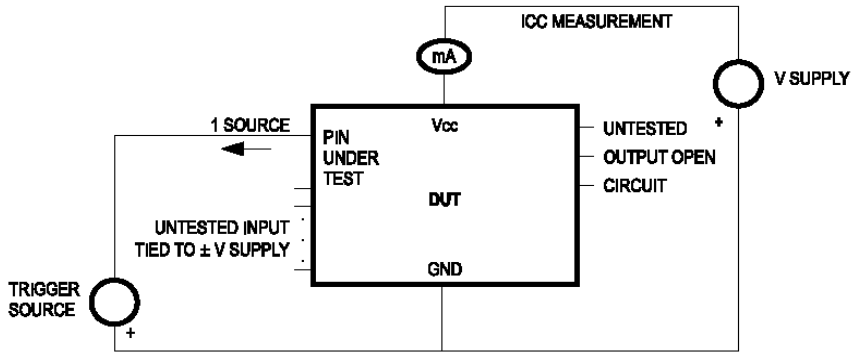
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:
1. DUT: Device Under Test.
2. PUT: Pin Under Test.

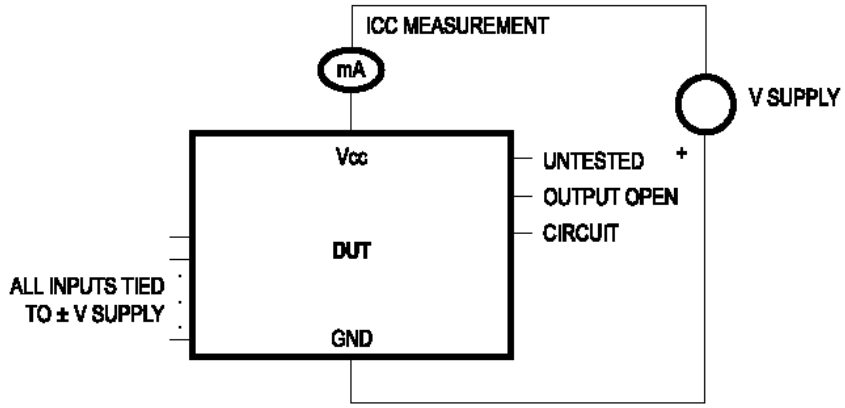
Figure 6.3 Latch-Up Test Results Diagram



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



Supply Overvoltage Test

Table 6.10 Latch-Up Data Table

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

7.0 Mechanical Information

Figure 7.1 Mechanical Information Diagram

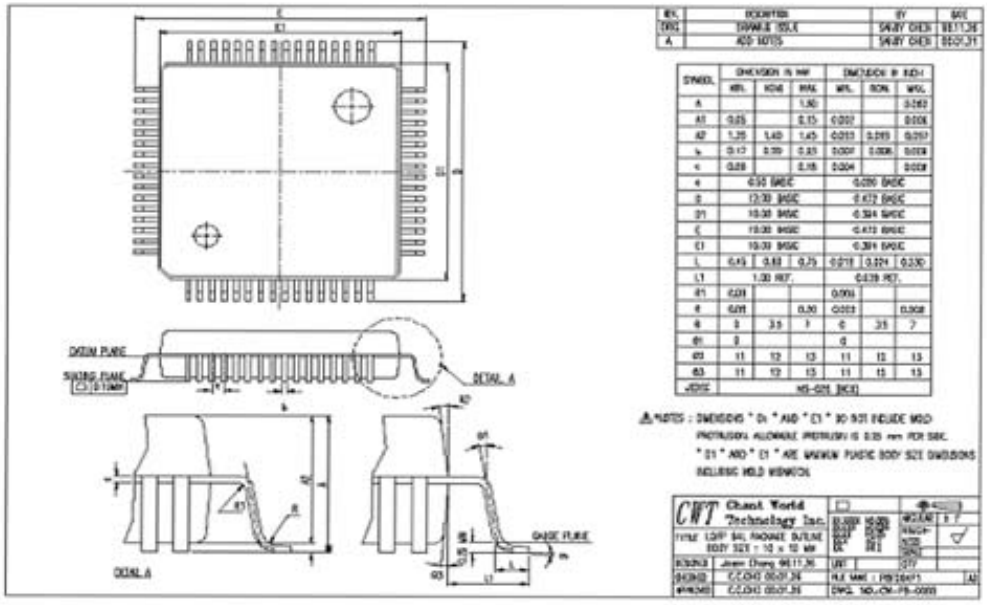


Table 7.1 Mechanical Information Table

body size		lead count	A1	A2	L1	b	c	e
D1	E1							
14	14	100	0.1	1.4	1	0.2	0.127	0.5

A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch

8.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE	Serial Interface Engine
CF	Compact Flash
MD	Micro Drive
SMC	SmartMedia Card
MS	Memory Stick
SD	Secure Digital
MMC	Multimedia Card

【MEMO】

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