AU9510
USB Smart Card Reader Chip
Technical Reference Manual

Revision 1.0

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1.0 Introduction

1.1. Description

The AU9510 is a self-contained single chip USB Smart Card controller chip. It can be used in a stand-alone USB Smart Card reader or in an embedded USB device in the downstream port of an USB hub. Its high integration enables the lowest BOM cost of an USB Smart Card reader. The dedicated hardware smart card block and full speed bulk transfer mechanism ensures the highest performance.

1.2. Features

- Fully compliant with the Universal Serial Bus Specification, version 1.1.
- Based on ISO7816 implementation
- PC Smart Card industry standard – PC/SC 1.0 compliant
- Supports Microsoft Smart Card for Windows
- Meet Microsoft WHQL USB Smart Card Reader requirements
- Include WDM driver to work on Windows 98 and Windows 2000
- Support T0, T1 protocol and I2C memory card
- Dedicated hardware block implementation for IC and memory card protocols for highest performance
- Implemented as an USB full speed device with bulk transfer endpoint
- Built-in 3.3v regulator for single 5v operation
- Built-in PLL for USB and Smart Card clocks requirement
- Support EEPROM for USB descriptors customization, including VID/PID
- Available in 28-SSOP

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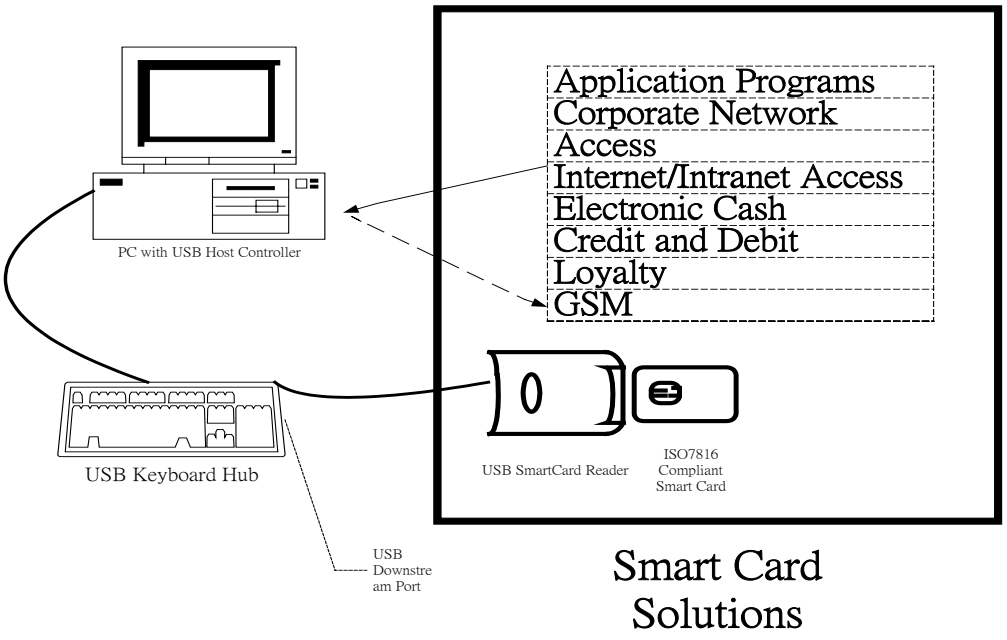
2.0 Application Block Diagram

The AU9510 is a single chip USB smart card controller chip. It can be used in a standalone USB Smart Card reader or in an embedded USB device in the downstream port of a USB hub.



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3.0 Pin Assignment

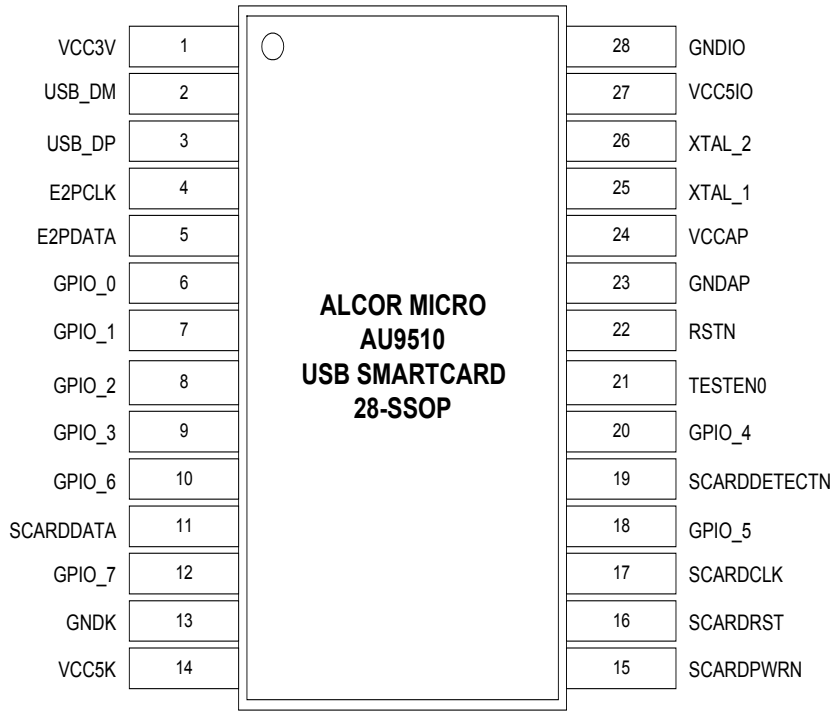

Table 3-1. Pin Descriptions for the 28-pin SSOP

Pin #	Pin Name	I/O	Description
1	VCC3V	O	Regulated 3V for DP pullup resistor
2	USB_DM	I/O	USB Downstream port D-
3	USB_DP	I/O	USB Downstream port D+
4	E2PCLK	I/O	I2C Eeprom Clock signal
5	E2PDATA	I/O	I2C Eeprom Data signal
6	GPIO_0	I/O	General purpose IO
7	GPIO_1	I/O	General purpose IO
8	GPIO_2	I/O	General purpose IO
9	GPIO_3	I/O	General purpose IO
10	GPIO_6	I/O	General purpose IO
11	SCARDDATA	I/O	Smart_Card Serial Data
12	GPIO_7	I/O	General purpose IO
13	GNDK	GND Kernel	Ground
14	VCC5K	5V VCC Kernel	+5V power supply

Table 3-1 (continued). Pin Description for the 28-pin SSOP

Pin #	Pin Name	I/O	Description
15	SCARDPWRN	O	Smart_Card power enable (active low for power switch)
16	SCARDRST	O/Tri	Smart_Card Reset
17	SCARDCLK	I/O	Smart_Card Clock
18	GPIO_5	I/O	General purpose IO
19	SCARDDETECTN	I	Smart_Card Inserted (active low)
20	GPIO_4	I/O	General purpose IO
21	TESTEN0	I	Testenable
22	RSTN	I	Hardware reset (active low)
23	GNDAP	Analog Ground Output	Analog ground
24	VCCAP	Analog Input	Analog VCC
25	XTAL_1	I	12 MHz crystal input
26	XTAL_2	O	12 MHz crystal output
27	VCC5IO	5V VCC I/O	+5V power supply
28	GNDIO	5V GND I/O	Ground

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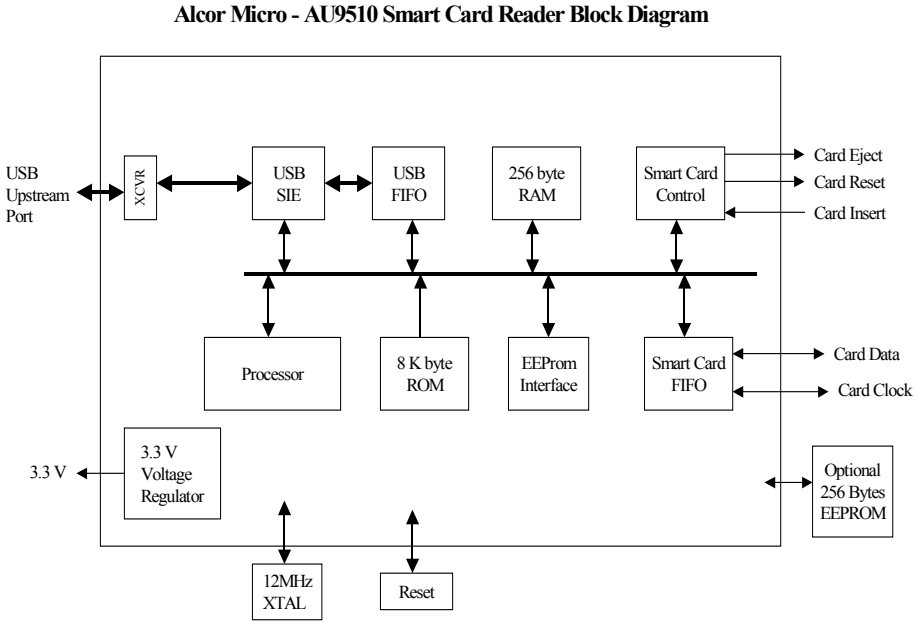
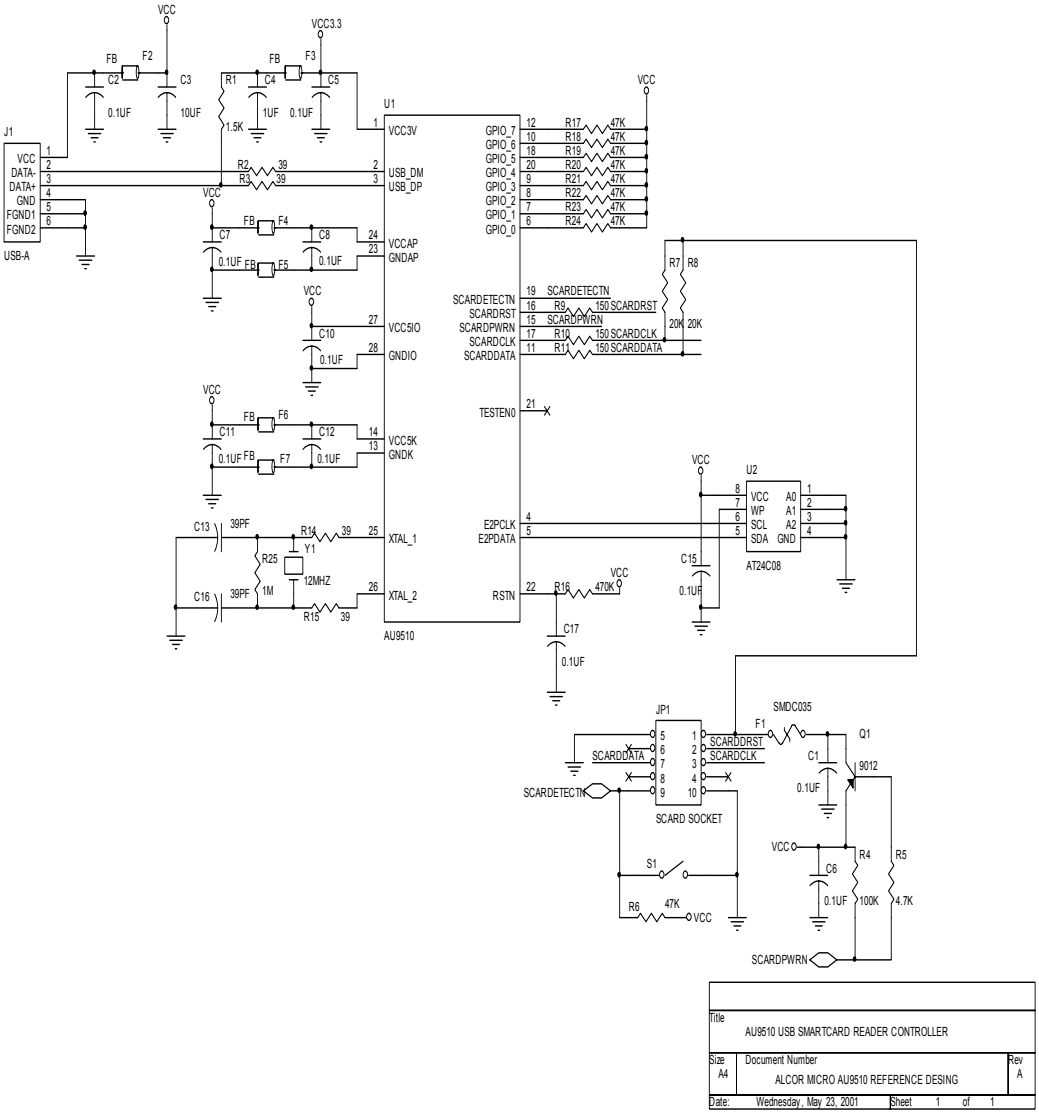
4.0 System Architecture and Reference Design

4.1. AU9510 Block Diagram



4.2. Sample Schematics



Title	AU9510 USB SMARTCARD READER CONTROLLER	
Size A4	Document Number ALCOR MICRO AU9510 REFERENCE DESING	Rev A
Date: Wednesday, May 23, 2001	Sheet 1 of 1	

Disclaimer: This schematic is for reference only. Alcor Micro Corp. bears no responsibility for any error that appear in this document. Specifications are subject to change without notice.

5.0 Programming Interface

AU9510 is a dedicated single chip USB SmartCard reader controller. In addition to silicon itself, Alcor Micro provides WDM drivers on Windows 2000 and Windows 98 platforms to ensure Microsoft PC/SC compliance. However, for non-Windows application platforms, software driver developers may wish to access the reader directly. This document describes Alcor's vendor unique USB commands. Table 1-1 shows all commands. (For details of the USB request specification, please refer to USB spec. Chapter 9)

USB request (bRequest)	Description
20h	Warm Reset
21h	Cold Reset
22h	Power Down
10h	Write SmartCard
11h	Read SmartCard
30h	Host Abort
31h	Set Protocol

AU9510 Vendor Unique USB Requests

Warm Reset

bmRequestType	bRequest	Wvalue	wIndex	wLength	Data
11000000B	00100000B	Zero	Zero	Two	ATR Length & TA2 Present

Device will perform a "warm reset" and return two bytes data. The first byte indicates the ATR byte length and the second byte returns 00000001B if TA2 present (specific mode of card operation). Following this command, host can use Endpoint 2 (Bulk Transfer) to get ATR information. The number of bytes to transfer is indicated by "ATR Length".

Cold Reset

bmRequestType	bRequest	WValue	wIndex	wLength	Data
11000000B	00100001B	Zero	Zero	Two	ATR Length & TA2 Present

Device will perform a "cold reset" and return two bytes data. The first byte indicates the ATR byte length and the second byte returns 00000001B if TA2 present (specific mode of card operation). Following this command, host can use Endpoint 2 (Bulk Transfer) to get ATR information. The number of bytes to transfer is indicated by "ATR Length".

Power Down

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01000000B	00100010B	Zero	Zero	Zero	None

This command will reset the device and deactivate the SmartCard

Write SmartCard

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01000000B	00010000B	Number of bytes to transfer	Zero	Zero	None

Following this command, host can use Endpoint 2 (Bulk Transfer) to transfer data to SmartCard. The number of bytes to transfer is indicated by "Number of bytes to transfer".

Read SmartCard

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01000000B	00010001B	Number of bytes to transfer	Zero	Zero	None

Following this command, host can use Endpoint 2 (Bulk Transfer) to transfer data from SmartCard. The number of bytes to transfer is indicated by "Number of bytes to Process".

Host Abort

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01000000B	00110000B	Zero	Zero	Zero	None

Host timeout, current command will be aborted.

Set Protocol

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01000000B	00110001B	Zero	Zero	Two	Protocol Type, FI & DI

Host will send two bytes data. The first byte codes the protocol type (T). The second byte codes Clock rate conversion factor (FI) over the most significant half byte, and Bit rate adjustment factor (DI) over the least significant half byte.

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6.0 Electrical Characteristics

6.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	C

6.2. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	-5		85	^{O}C

6.3. General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			4		ρF
C_{OUT}	Output capacitance			4		ρF
C_{BID}	Bi-directional buffer capacitance			4		ρF

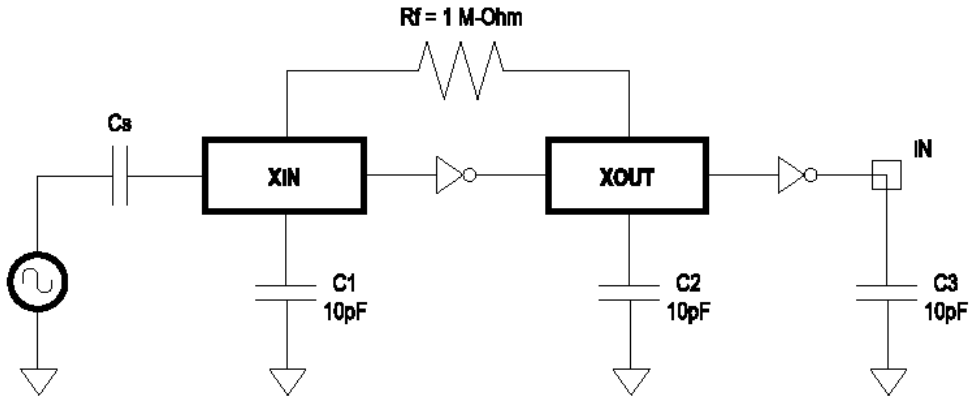
6.4. DC Electrical Characteristics for 5 volts operation

(Under Recommended Operating Conditions and V_{CC}=4.5v ~ 5.5v , Tj= -40°C to + 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IL}	Input Low Voltage	CMOS			0.3*V_{CC}	V
V_{IL}	Schmitt input Low Voltage	TTL		1.10		V
V_{IL}	Schmitt input Low V oltage	CMOS		1.84		V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IH}	Input Hight Voltage	CMOS	0.7*V_{CC}			V
V_{IH}	Schmitt input High Voltage	TTL		1.87		V
V_{IH}	Schmitt input High Voltage	CMOS		3.22		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	3.5			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		50		KΩ

6.5. Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



6.6. USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	Vi<0		-50	mA
V_I	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
I_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_O	DC output voltage	Note 3	-0.5	Vcc +0.5	V
I_O	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
I_O	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{CC}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STO}	Storage temperature range		-60	+150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			-40°C to +85°C			
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.6V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.6V (Note 3)	0.8	1.1		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	Vcc=3.6V VI=Vcc or GND Io=0		330	600	µA
Isup	Supply current in suspend	Vcc=3.6V VI=Vcc or GND Io=0			70	µA
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Input leakage current	Vcc=3.6V VI=5.5V or GND, not for I/O Pins		+/- 0.1	+/-0.5	µA
IOFF	3-state output OFF-state current	Vi=Vih or ViL; Vo=Vcc or GND			+/-10	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

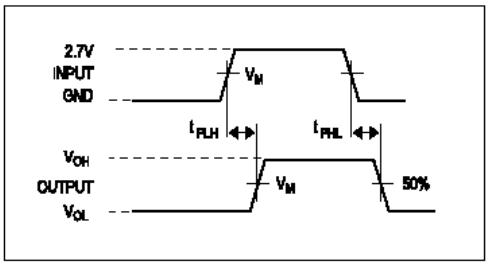
GND=0V, $t_R = t_F$ =3.0 ns; C_L =50 pF; RL=500 Ohms

SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{AMB})					UNIT
			0°C to +25°C			0°C to +70°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point[1]	3	1.3		2.0	1.3	2.0	V

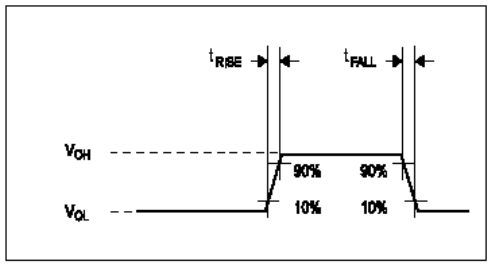
NOTES:

1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.

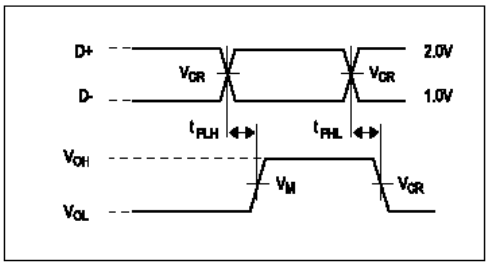
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



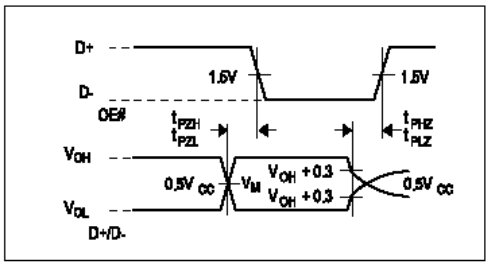
AC WAVEFORM 2.
RISE AND FALL TIMES



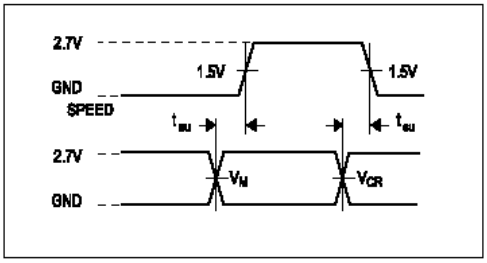
AC WAVEFORM 3.
D+/D- TO RCV



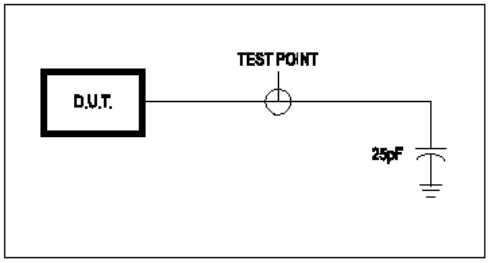
AC WAVEFORM 4.
OE# TO D/+/D-



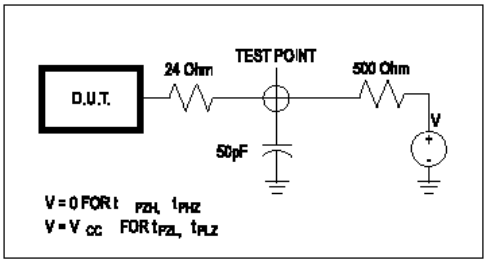
AC WAVEFORM 5.
SETUP FOR SPEED



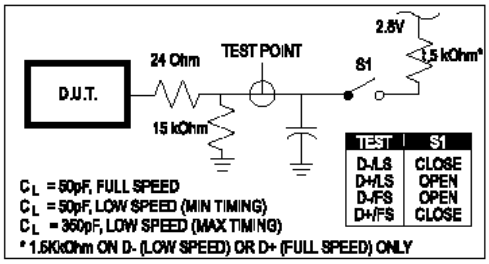
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



6.7. ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test Circuit & Condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	6000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

6.8. Latch-Up Test Results

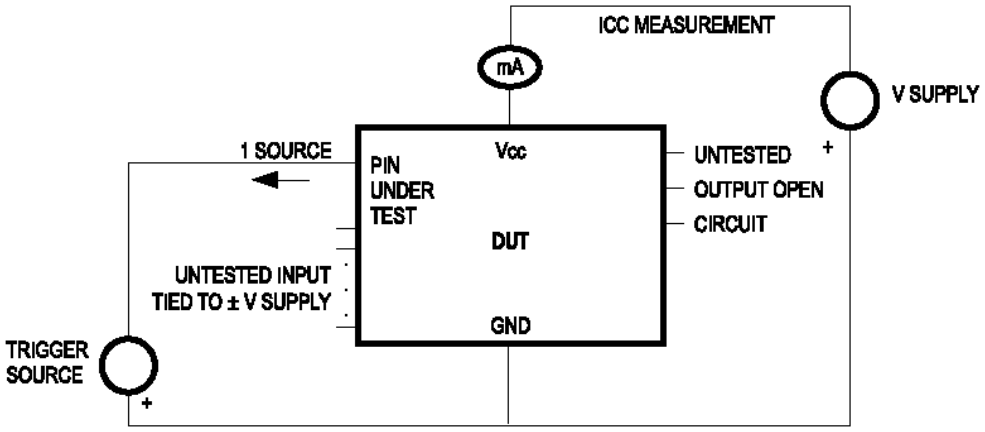
Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

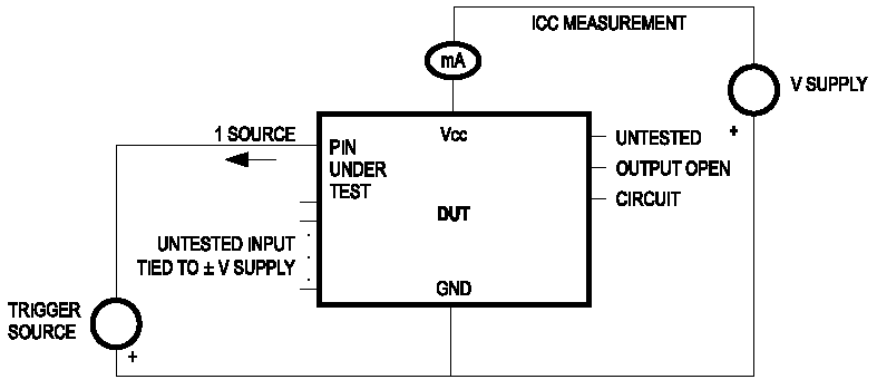
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

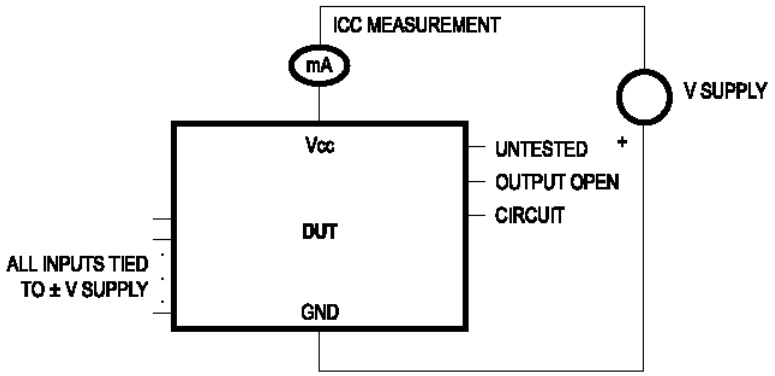
Notes:
1. DUT: The device under test.
2. PUT: The pin under test.



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



Supply Overvoltage Test

Latch-Up Data

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

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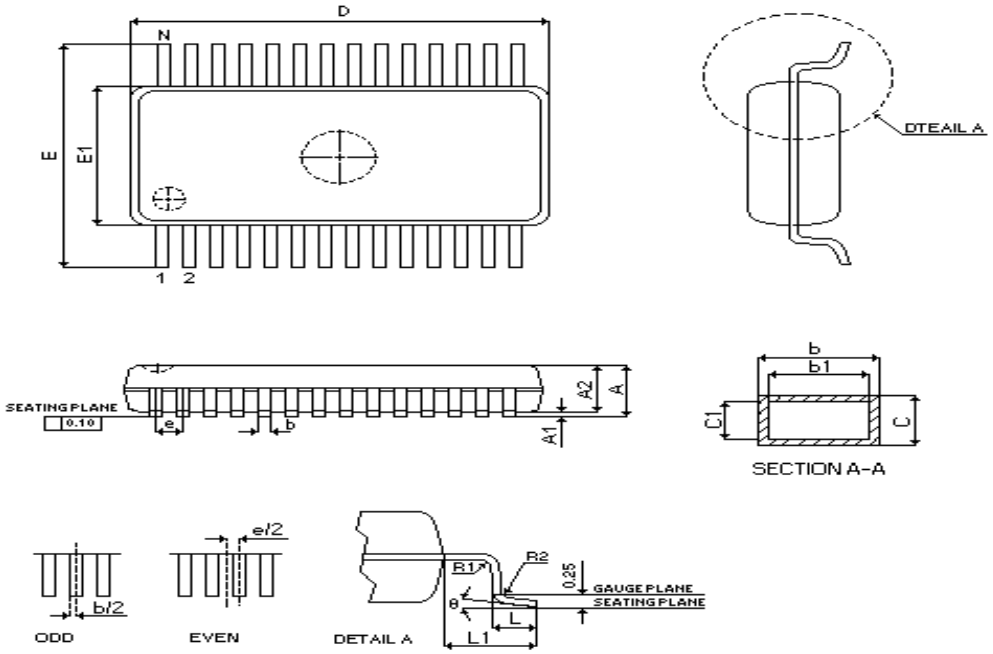
7.0 Mechanical Information

Following diagrams show the dimensions of the AU9510 28-pin SSOP. Measurements are in inches. Dimensions do not include mold flash and dambar protrusion; allowable mold flash is 0.010 inch.



REV.	DESCRIPTION	BY	DATE
ORIG.	1. REGENERATED FROM PO-P402 VERSION"A" 2. ADD GAUGE PLANE	JIMMY	97.04.21
①	ADD CROSS SECTIONA-A" DRAWING	STEVEN	97.07.31
②	MODIFY 0.020 TO 0.002	IRIS	97.08.21
③	ADD E-PIN CHANGE PIN "I" DOT DIMENSION	IRIS	98.06.10

SYMBOL	COMMON DIMENSION MILLIMETERS			COMMON DIMENSION INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			2.00			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
b1	0.22	0.30	0.33	0.009	0.012	0.013
c	0.09		0.25	0.004		0.010
c1	0.09	0.15	0.21	0.004	0.006	0.008
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BSC			0.0256 BSC		
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	0.25 REF.			0.050 REF.		
R1	0.09			0.004		
θ	0^0	4^0	8^0	0^0	4^0	8^0

N	14	16	18	20	24	28
0 ± 0.30	6.20	6.20	7.20	7.20	8.20	10.20
JEDEC NO.	MO-150 AB	MO-150 AC	MO-150 AD	MO-150 AE	MO-150 AG	MO-150 AH

UNLESS OTHERWISE SPECIFIED	DECMAL X ± XX ±10 XXX ±.05	ANGULAR ±3⁰	ORENT SEMCONOUCTOR ELECTRONICS	UNIT	MM	SCALE : 10:1
				SHEET:1 OF1		
DRAWN	IRIS 98.06.10		TITLE SSOP 14/16/20/21/28L (209 MIL) PACKAGE OUTLINE	FILE: PD-P503C		A3
CHECKED				DWG. NO. : PD-P503C		
APPROVED						