

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

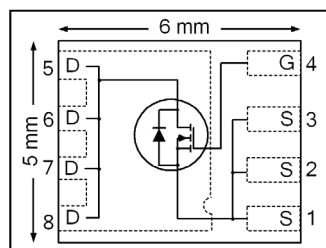
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this product an extremely efficient and reliable device for use in Automotive and wide variety of other applications.

Applications

- Motor Control
- Reverse Battery Protection
- Heavy Loads

HEXFET® POWER MOSFET

V_{DS}	40V
$R_{DS(on)}$ typ.	3.6mΩ
max	4.6mΩ
I_D (Silicon Limited)	84A



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFN8401	PQFN 5mm x 6mm	Tape and Reel	4000	AUIRFN8401TR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_{C(Bottom)} = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	84	A
I_D @ $T_{C(Bottom)} = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	59	
I_{DM}	Pulsed Drain Current ①	336	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation	4.2	W
P_D @ $T_{C(Bottom)} = 25^\circ\text{C}$	Power Dissipation	63	
	Linear Derating Factor	0.028	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	69	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy ②	93	
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	2.4	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	34	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	36	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	—	23	

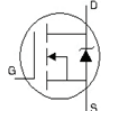
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

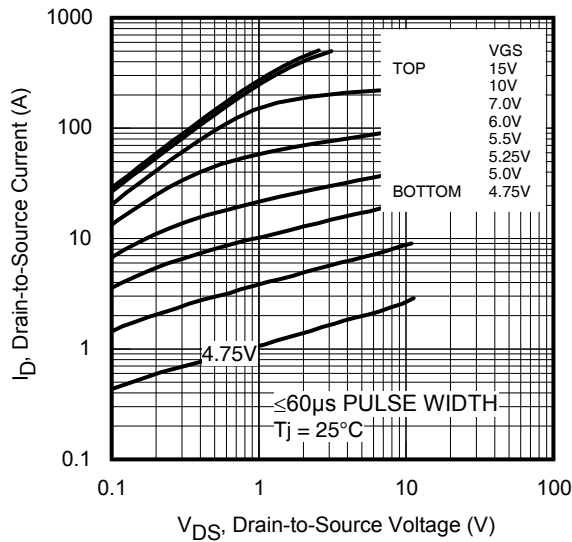
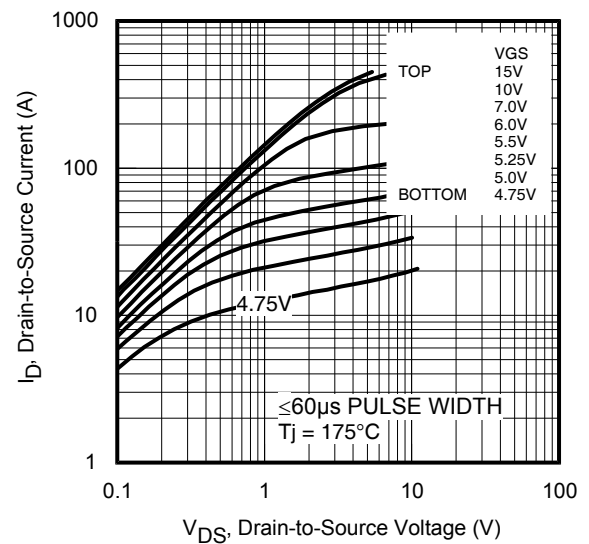
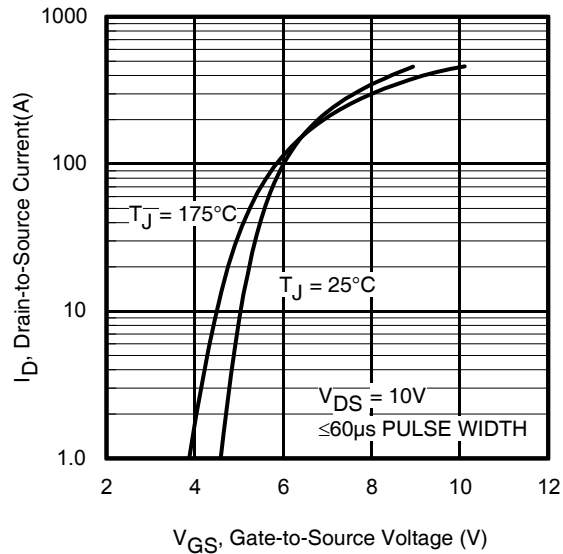
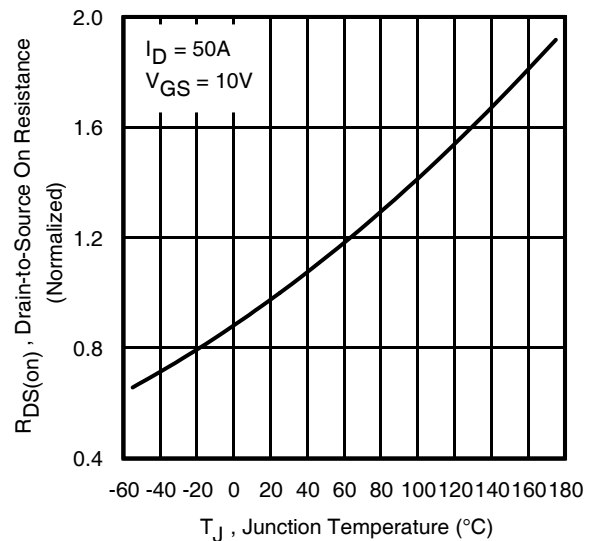
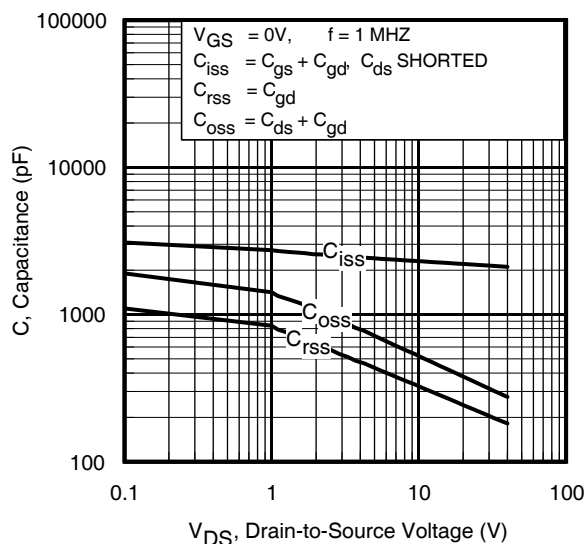
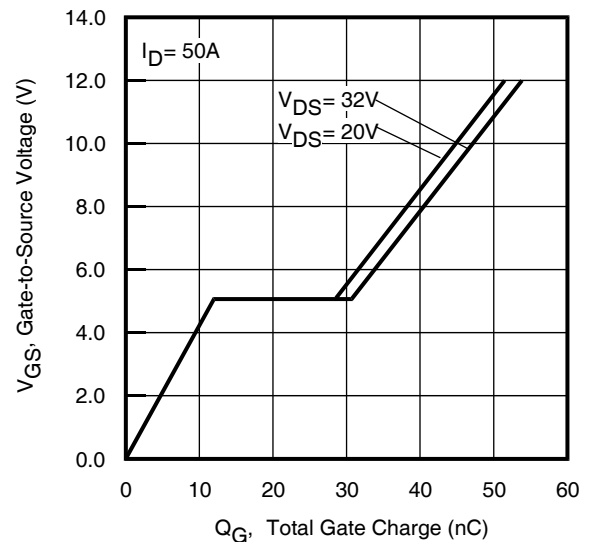
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	35	—	mV/°C	Reference to 25°C , $I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.6	4.6	mΩ	$V_{GS} = 10V, I_D = 50A$
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	2.2	—	Ω	

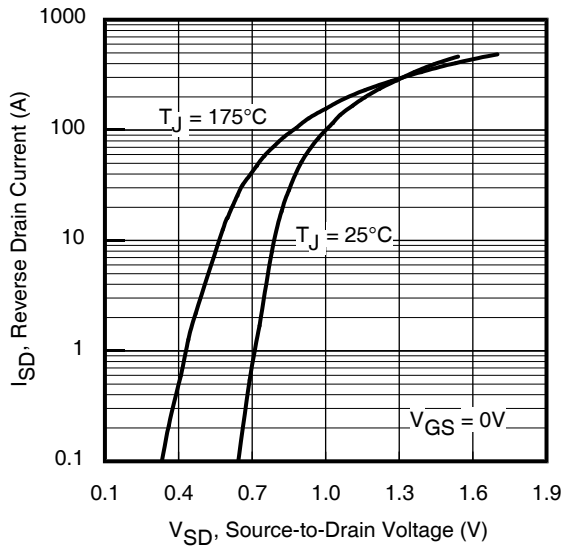
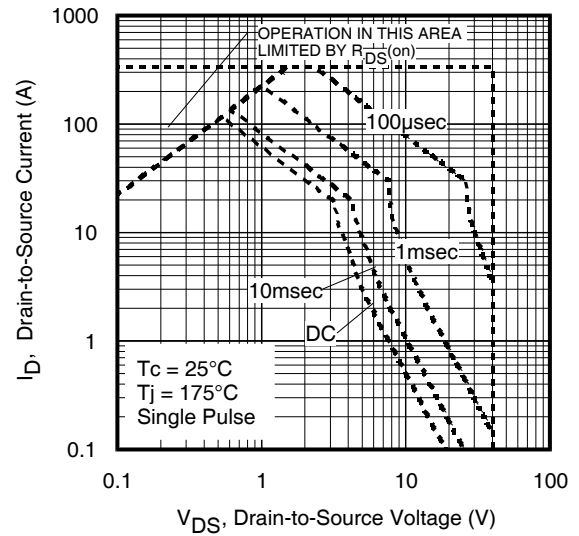
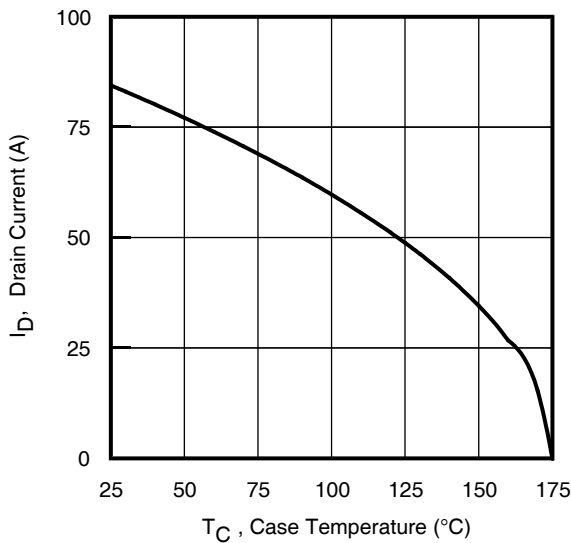
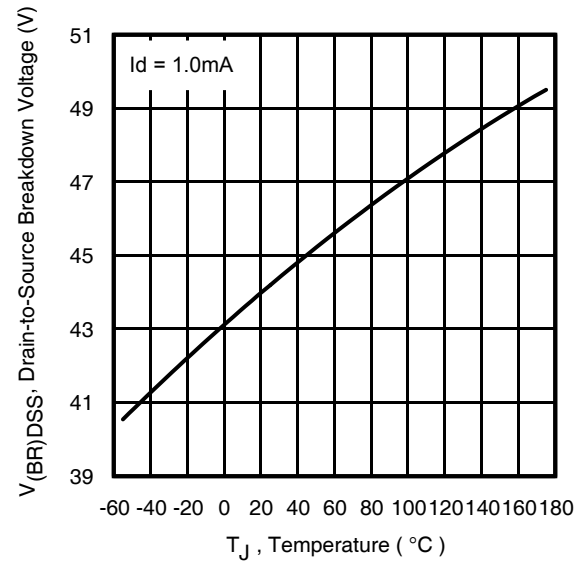
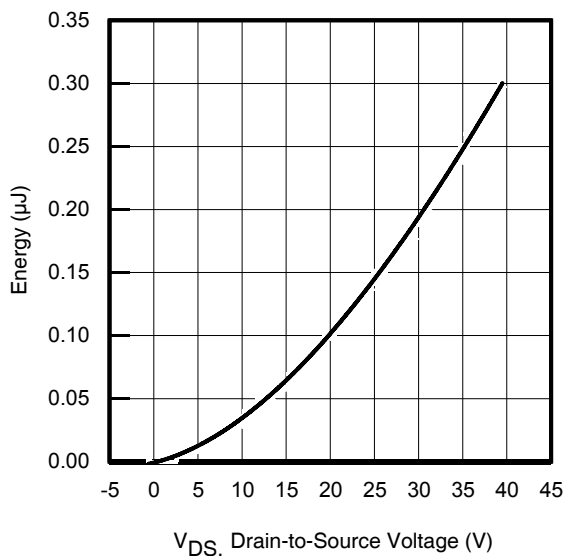
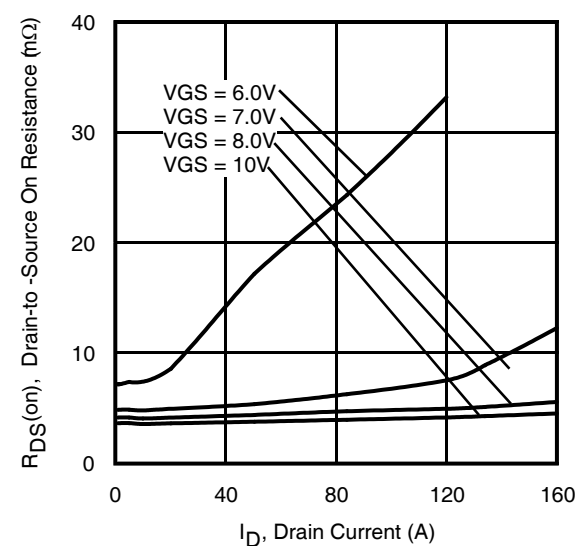
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

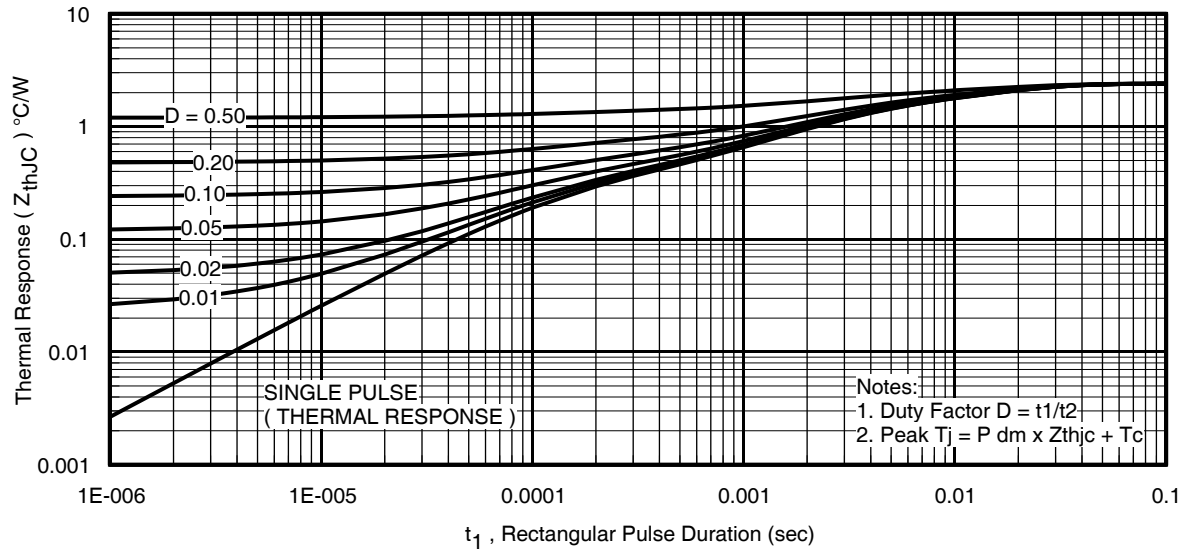
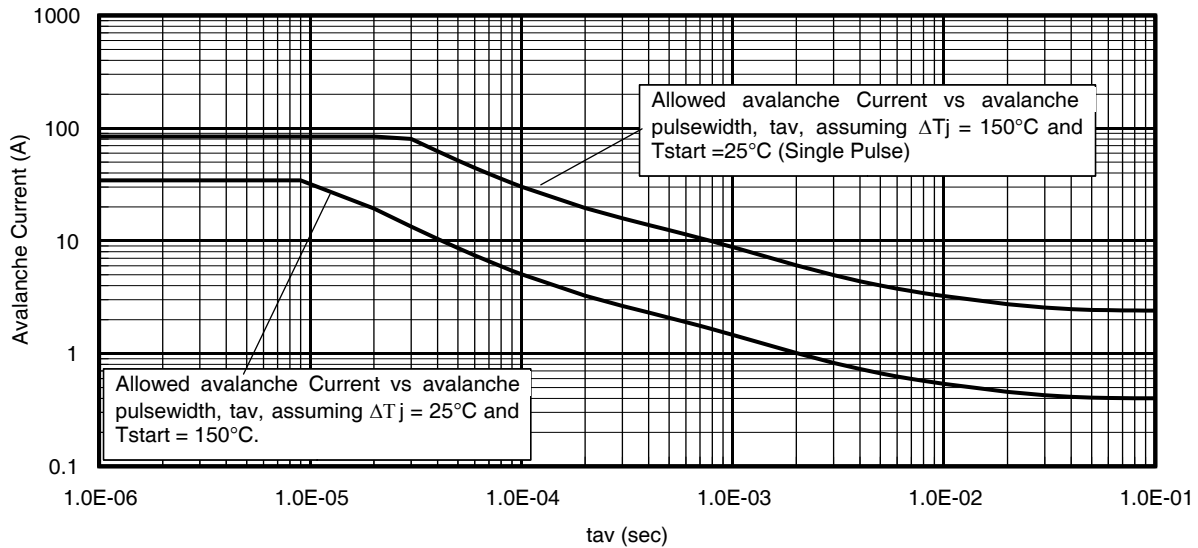
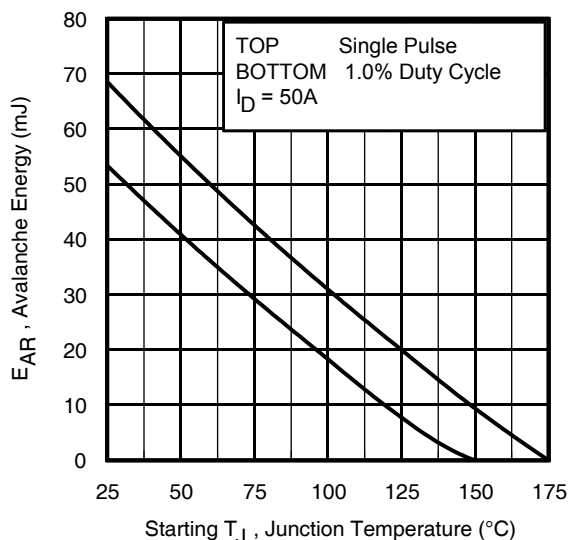
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	144	—	—	S	$V_{DS} = 10V, I_D = 50A$
Q_g	Total Gate Charge	—	44	66	nC	$I_D = 50A$
Q_{gs}	Gate-to-Source Charge	—	13	—		$V_{DS} = 20V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	15	—		$V_{GS} = 10V$
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	29	—		
$t_{d(on)}$	Turn-On Delay Time	—	6.1	—	ns	$V_{DD} = 20V$
t_r	Rise Time	—	13	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	22	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	12	—		$V_{GS} = 10V$ ③
C_{iss}	Input Capacitance	—	2170	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	340	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	220	—		$f = 1.0\text{MHz}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	422	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$ ⑦
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	502	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$ ⑧

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	84	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	336		
V_{SD}	Diode Forward Voltage	—	0.9	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
dv/dt	Peak Diode Recovery	—	7.8	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 50A, V_{DS} = 40V$
t_{rr}	Reverse Recovery Time	—	20	—	ns	$T_J = 25^\circ\text{C}$
		—	22	—		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	12	—	nC	$T_J = 25^\circ\text{C}$
		—	15	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.1	—	A	$T_J = 25^\circ\text{C}$


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 Typical Source-to-Drain Diode

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical Coss Stored Energy

Fig 12. Typical On-Resistance vs. Drain Current

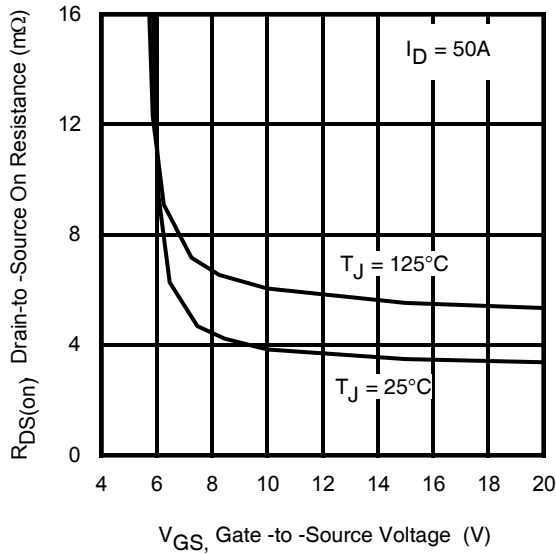
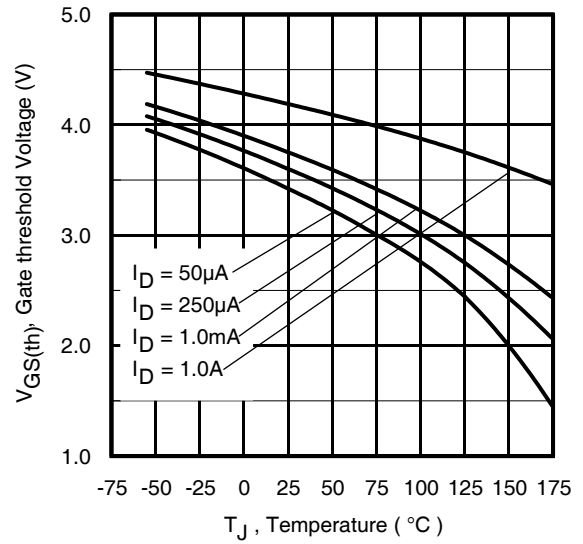
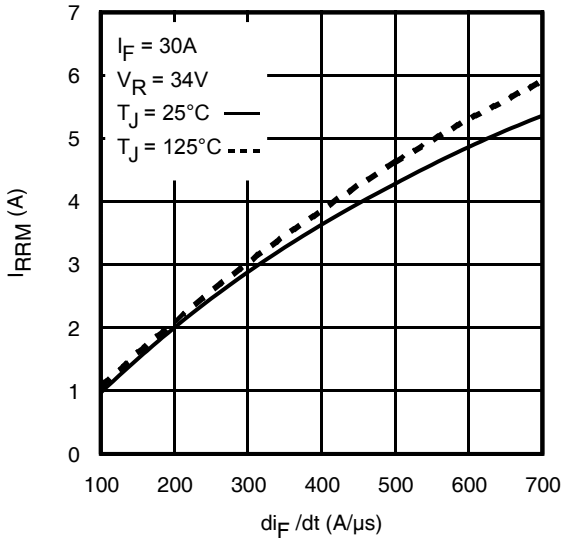
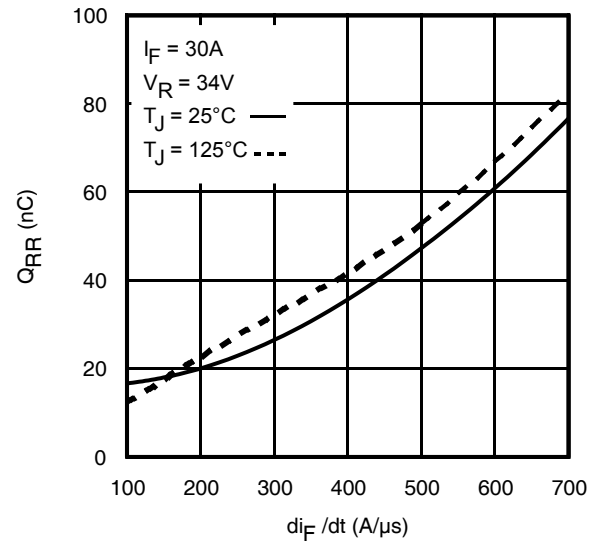
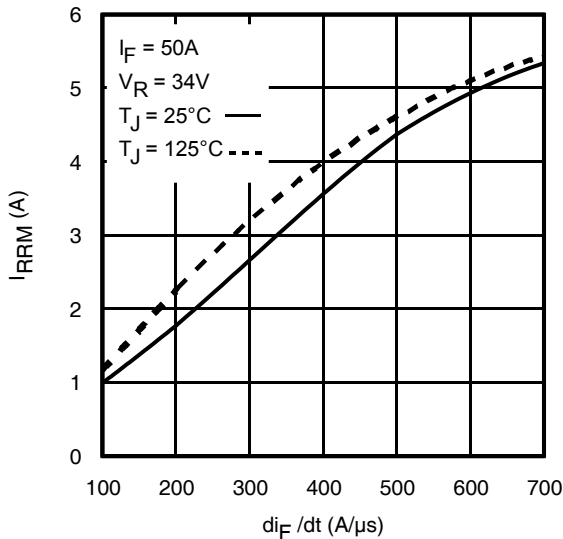
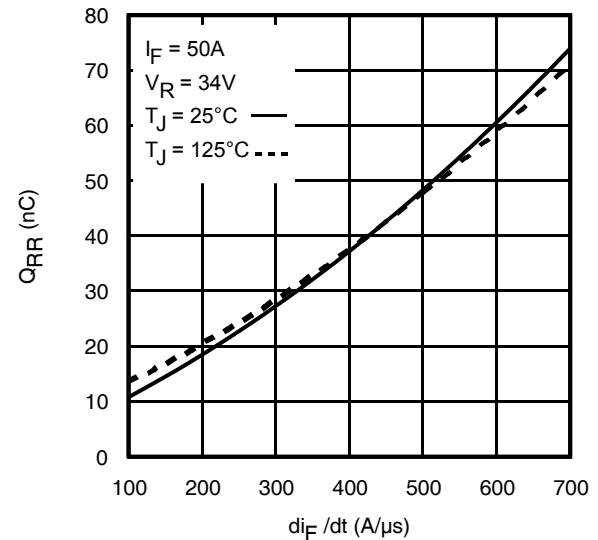

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulse Width

Fig 15. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 16. Typical On-Resistance vs. Gate Voltage

Fig 17. Threshold Voltage vs. Temperature

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Stored Charge vs. di_F/dt

Fig. 20 - Typical Recovery Current vs. di_F/dt

Fig. 21 - Typical Stored Charge vs. di_F/dt

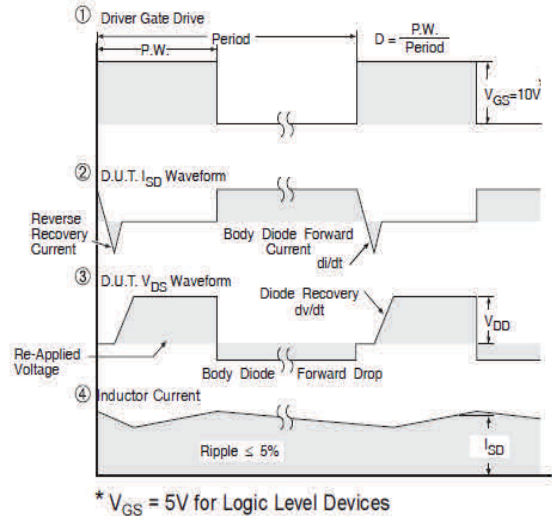
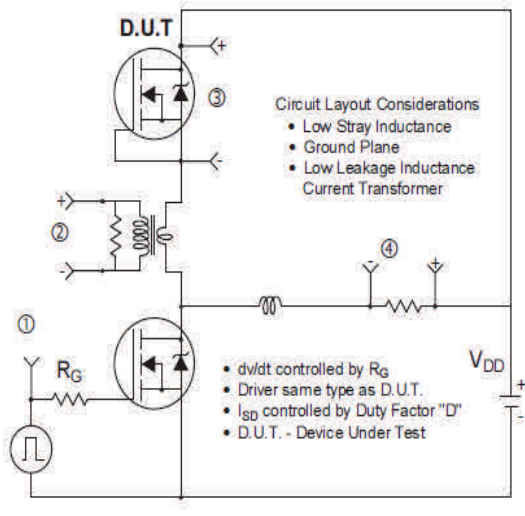


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

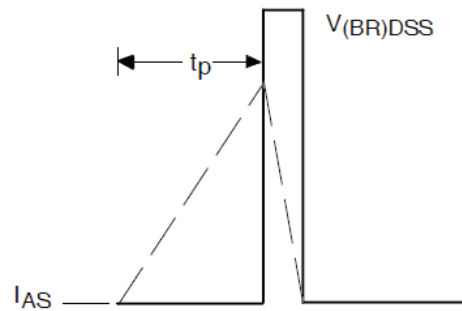
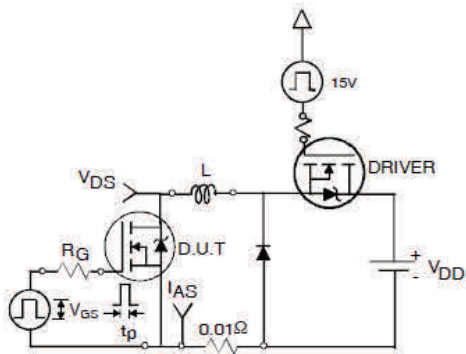


Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

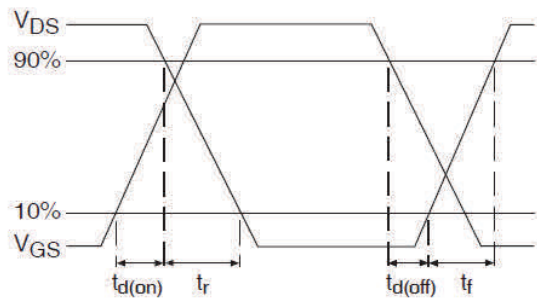
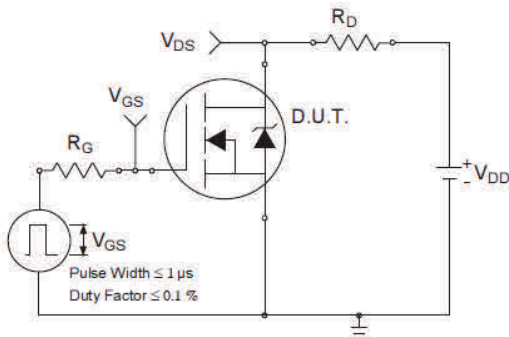


Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

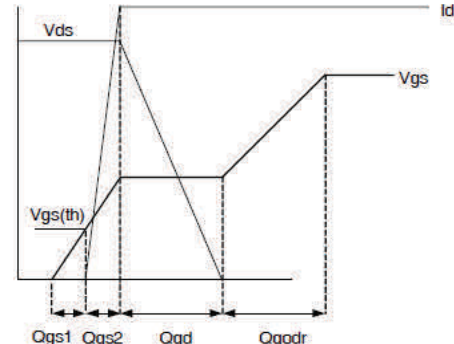
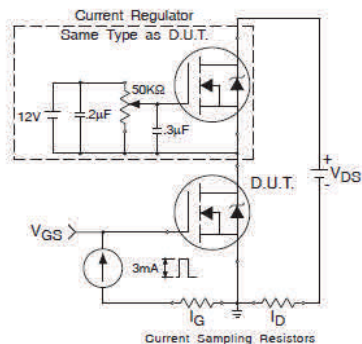
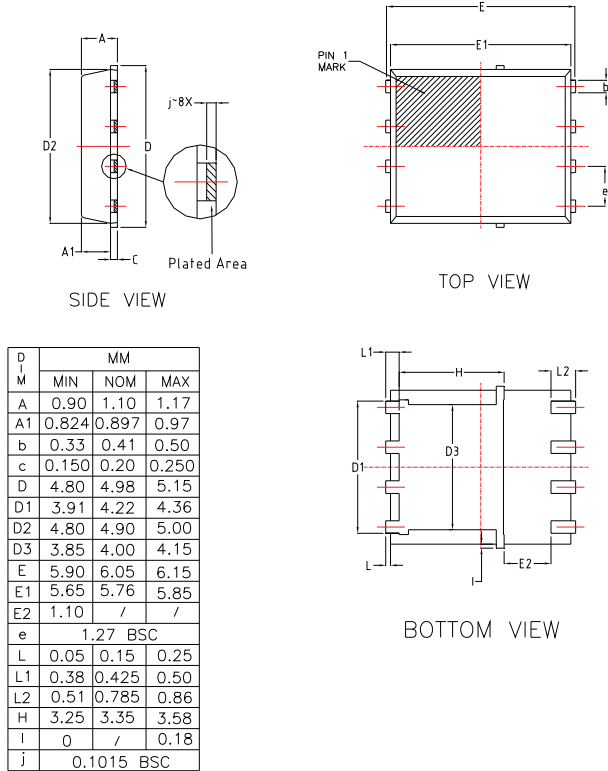


Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

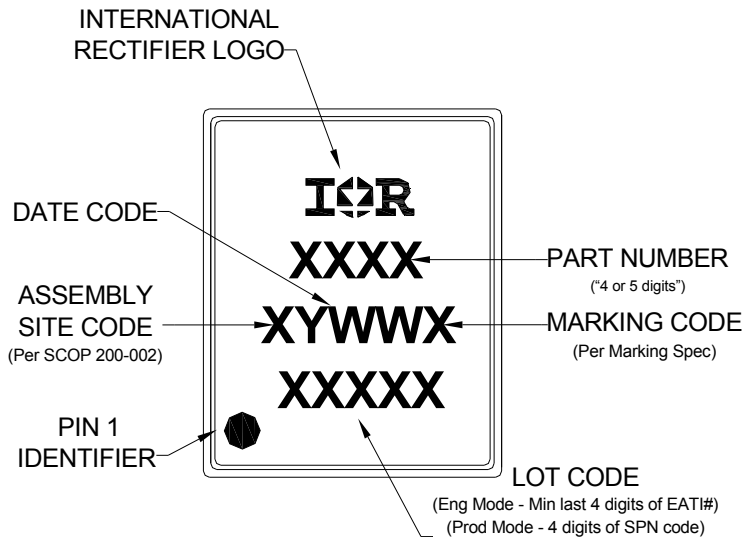
PQFN 5x6 Outline "E" Package Details



For footprint and stencil design recommendations, please refer to application note AN-1136 at <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

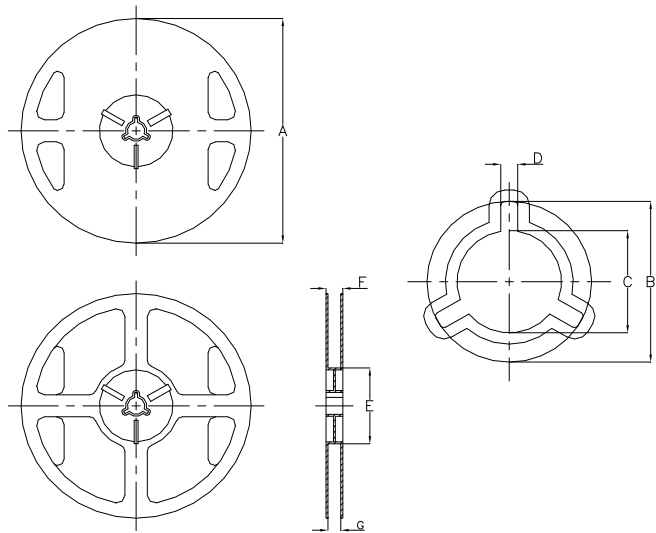
For visual inspection recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "E" Part Marking

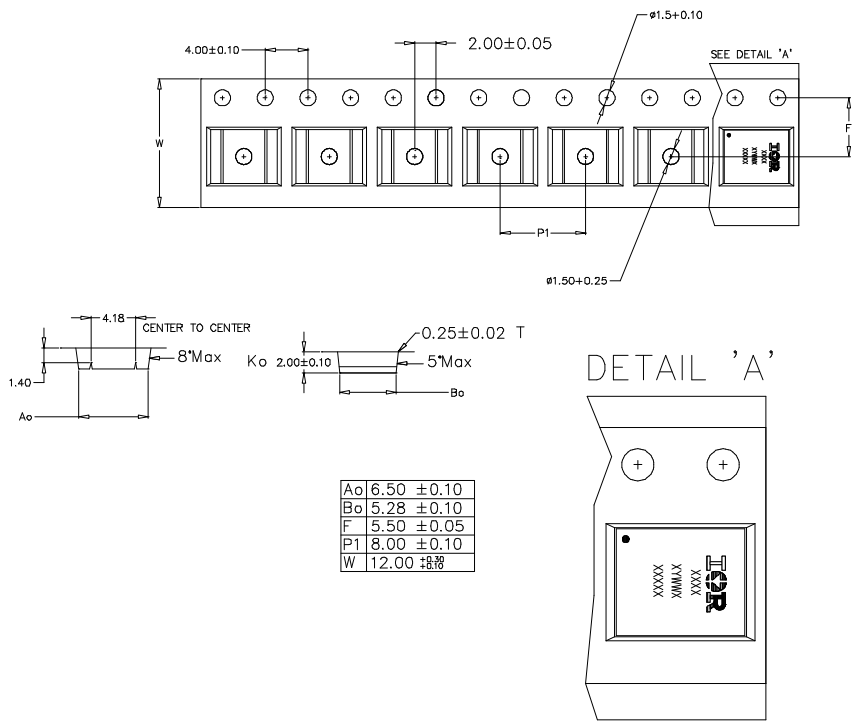


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 5x6 Outline "E" Tape and Reel



REEL DIMENSIONS				
STANDARD OPTION (QTY 4000) TR				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	329.5	330.5	12.972	13.011
B	20.9	21.5	0.823	0.846
C	12.8	13.5	0.504	0.532
D	1.7	2.3	0.067	0.091
E	97	99	3.819	3.898
F	Ref	17.4		
G	13	14.5	0.512	0.571



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		PQFN 5mm x 6mm	MSL1
ESD	Human Body Model	Class H1B (+/- 1000V) ^{††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) ^{††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Highest passing voltage.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^{\circ}\text{C}$, $L = 0.055\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 80% VDSS.
- ⑦ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while VDS is rising from 0 to 80% VDSS.

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<http://www.irf.com/technical-info/>

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