

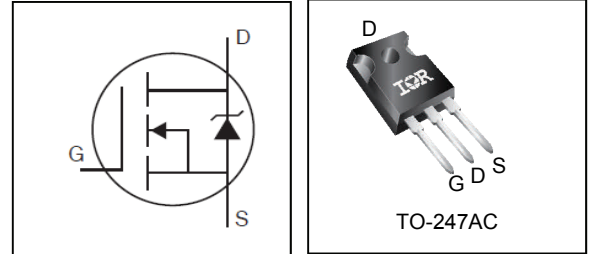
**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

V <sub>DSS</sub>	100V
R <sub>DS(on)</sub> <b>typ.</b>	4.8mΩ
	<b>max.</b>
I <sub>D</sub> (Silicon Limited)	128AⓈ
I <sub>D</sub> (Package Limited)	120A

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFP4310Z	TO-247AC	Tube	25	AUIRFP4310Z

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	128Ⓢ	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	90	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	120	
I <sub>DM</sub>	Pulsed Drain Current ②	480	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	278	W
	Linear Derating Factor	1.9	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ③	355	mJ
I <sub>AR</sub>	Avalanche Current ②	See Fig.14,15, 22a, 22b	A
E <sub>AR</sub>	Repetitive Avalanche Energy		mJ
dv/dt	Peak Diode Recovery ④	17	V/ns
T <sub>J</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T <sub>STG</sub>			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ⑤	—	0.54	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface	0.24	—	
R <sub>θJA</sub>	Junction-to-Ambient	—	40	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

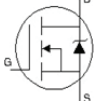
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	4.8	6.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 77A ⑤
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
g <sub>fs</sub>	Forward Trans conductance	169	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 77A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G</sub>	Gate Resistance	—	0.7	—	Ω	

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

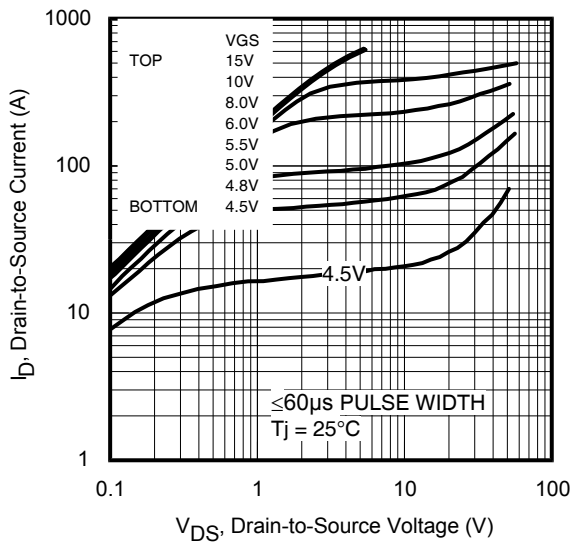
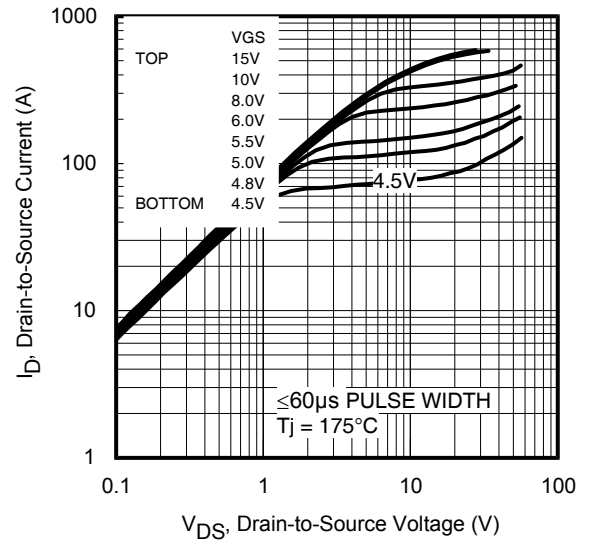
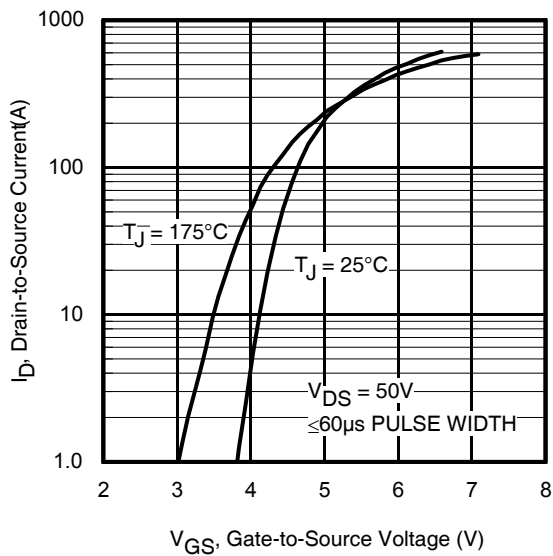
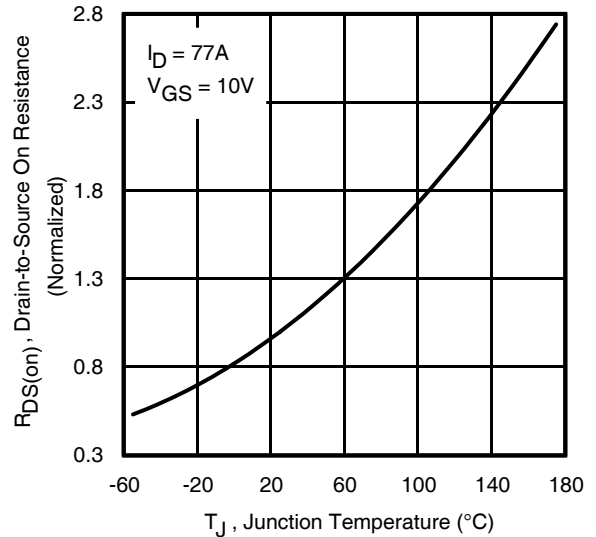
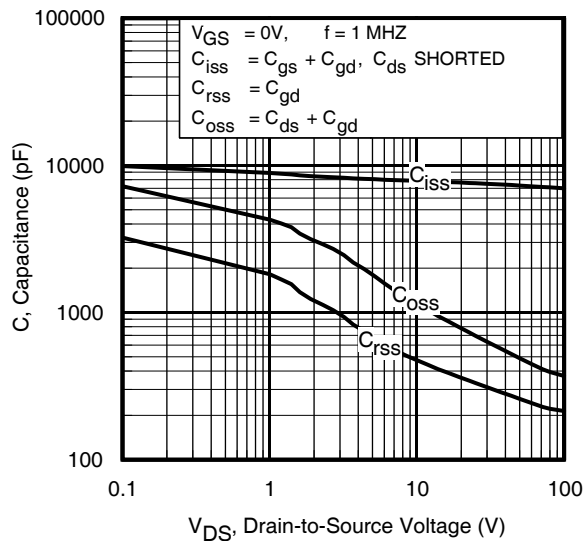
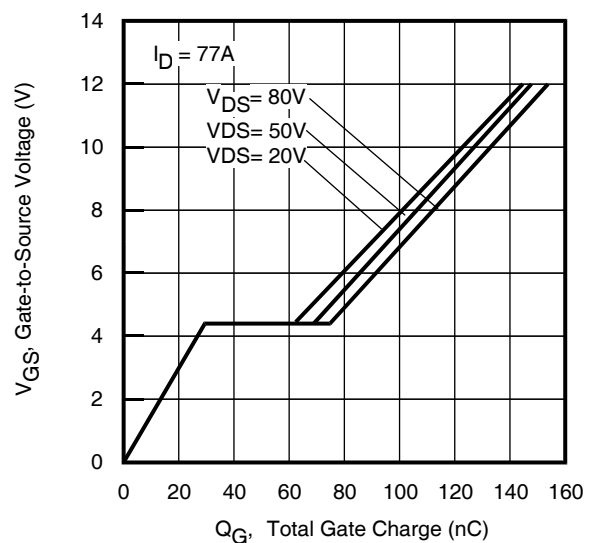
Q <sub>g</sub>	Total Gate Charge	—	125	188	nC	I <sub>D</sub> = 77A V <sub>DS</sub> = 50V V <sub>GS</sub> = 10V ⑥
Q <sub>gs</sub>	Gate-to-Source Charge	—	32	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	37	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	88	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	22	—	ns	V <sub>DD</sub> = 65V I <sub>D</sub> = 77A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V ⑥
t <sub>r</sub>	Rise Time	—	81	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	58	—		
t <sub>f</sub>	Fall Time	—	83	—		
C <sub>iss</sub>	Input Capacitance	—	7120	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	490	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	250	—		
C <sub>oss eff. (ER)</sub>	Effective Output Capacitance (Energy Related)	—	540	—		
C <sub>oss eff. (TR)</sub>	Effective Output Capacitance (Time Related)	—	705	—		

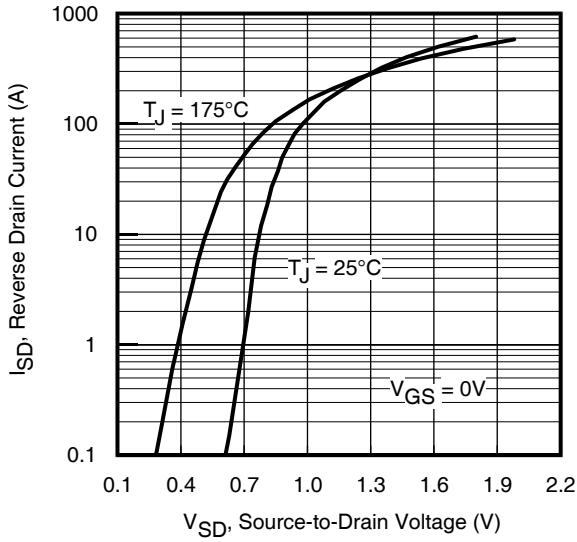
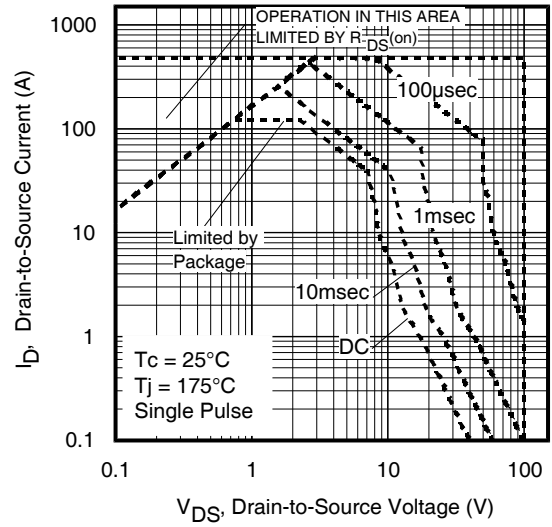
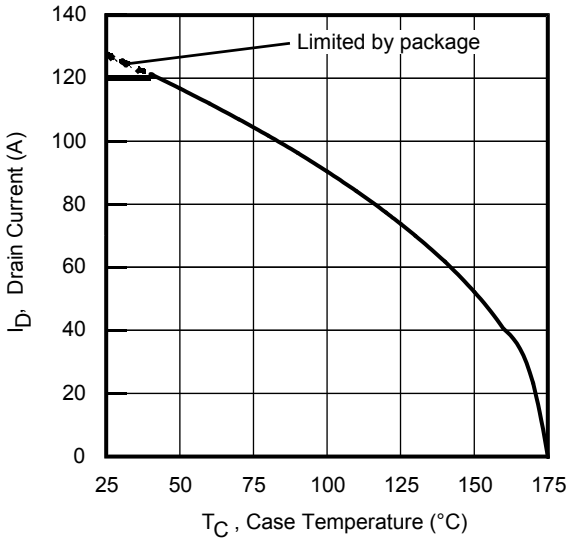
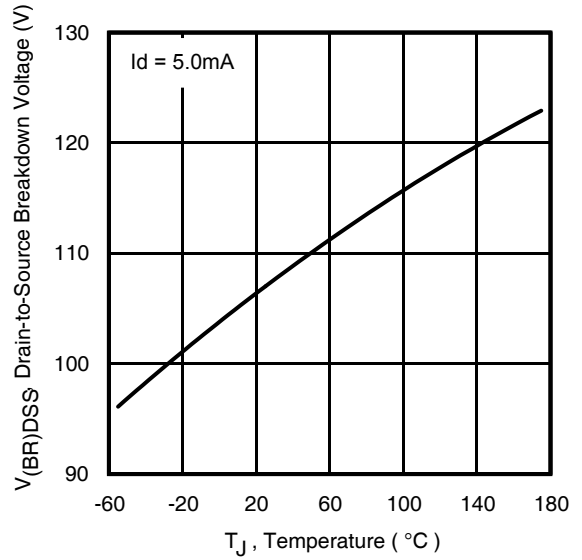
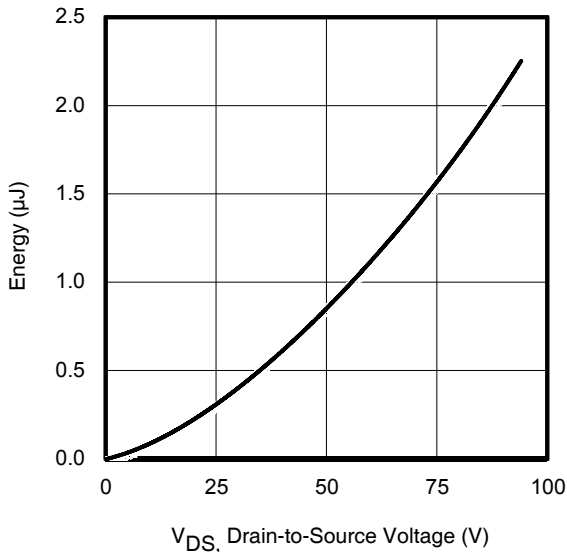
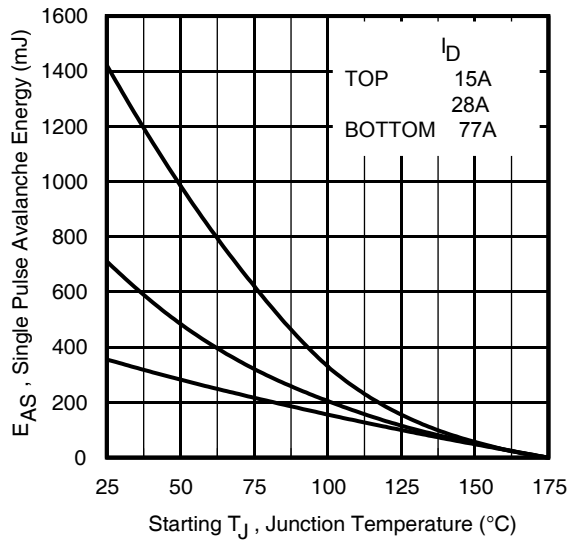
**Diode Characteristics**

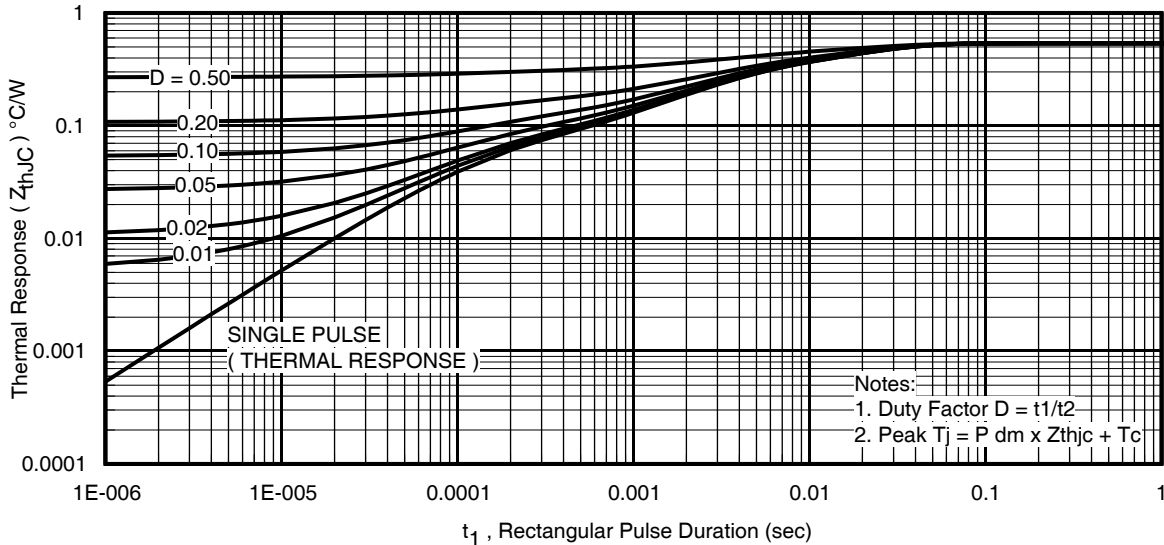
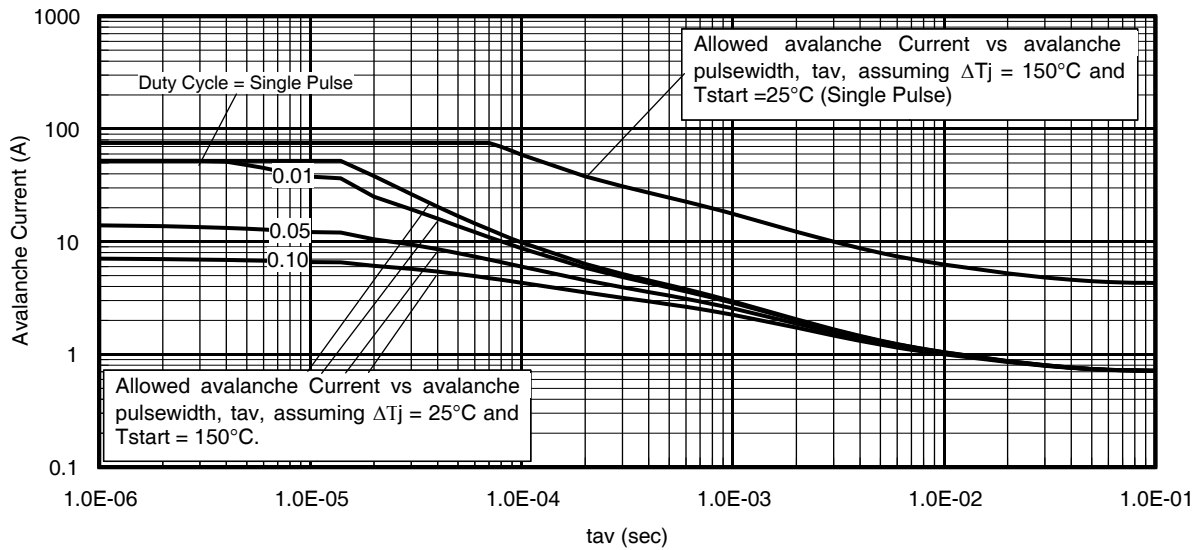
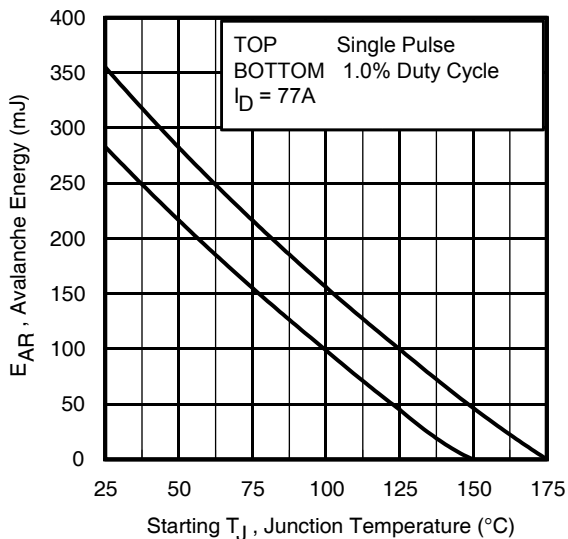
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	128①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ②	—	—	480		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 77A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	49	—	ns	T <sub>J</sub> = 25°C V <sub>DD</sub> = 85V T <sub>J</sub> = 125°C I <sub>F</sub> = 77A,
		—	57	—		
Q <sub>rr</sub>	Reverse Recovery Charge	—	102	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs ⑤ T <sub>J</sub> = 125°C
		—	133	—		
I <sub>RSM</sub>	Reverse Recovery Current	—	3.7	—	A	T <sub>J</sub> = 25°C

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.120mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 77A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ④ I<sub>SD</sub> ≤ 77A, di/dt ≤ 1505A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑧ R<sub>G</sub> is measured at T<sub>J</sub> approximately 90°C.


**Fig. 1 Typical Output Characteristics**

**Fig. 2 Typical Output Characteristics**

**Fig. 3 Typical Transfer Characteristics**

**Fig. 4 Normalized On-Resistance vs. Temperature**

**Fig. 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

**Fig. 8.** Maximum Safe Operating Area

**Fig. 9.** Maximum Drain Current vs. Case Temperature

**Fig. 10.** Drain-to-Source Breakdown Voltage

**Fig. 11.** Typical Coss Stored Energy

**Fig. 12.** Maximum Avalanche Energy vs. Drain Current


**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Avalanche Current vs. Pulse width**

**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))**

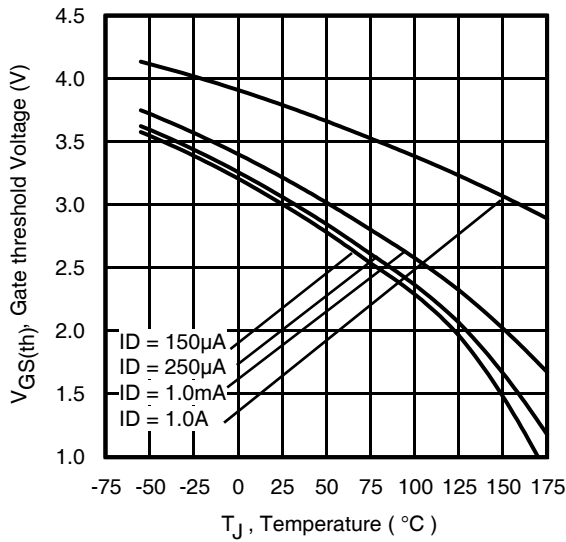
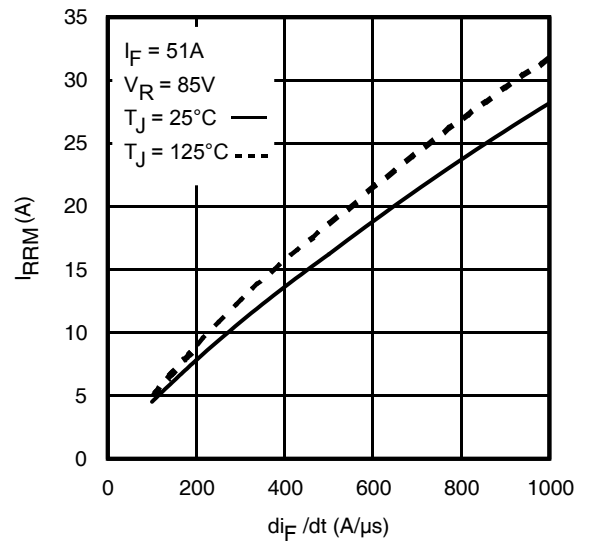
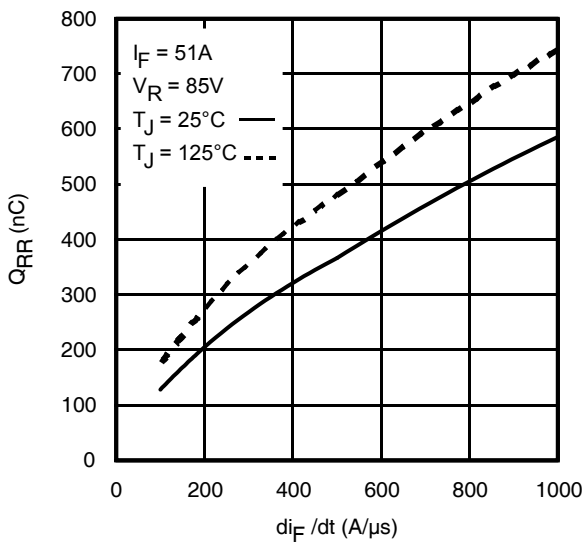
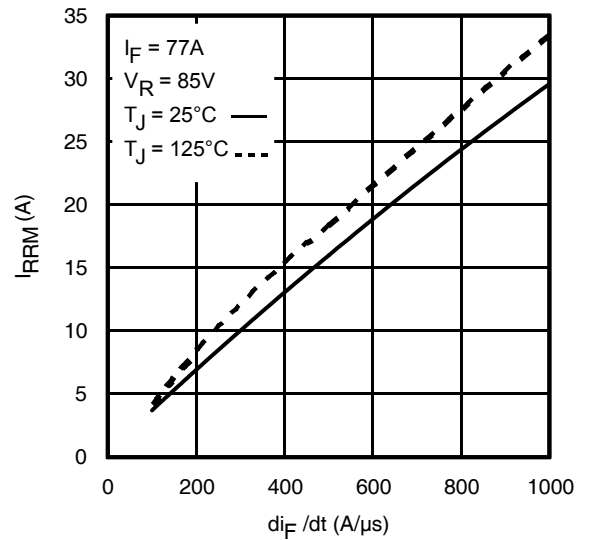
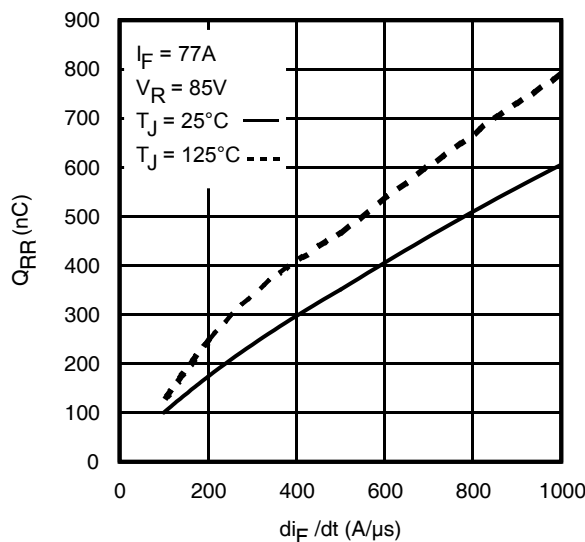
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 13, 14).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

**Fig 15. Maximum Avalanche Energy vs. Temperature**


**Fig. 16.** Threshold Voltage vs. Temperature

**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 18 -** Typical Stored Charge vs.  $di_F/dt$ 

**Fig. 19 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$

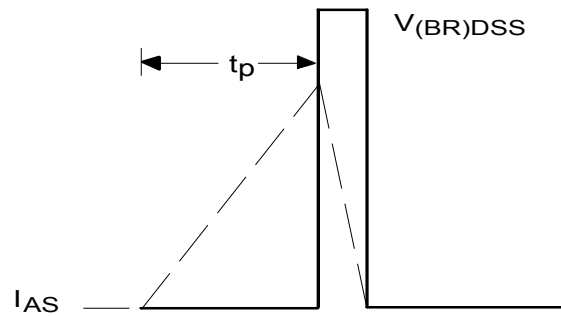


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 21.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



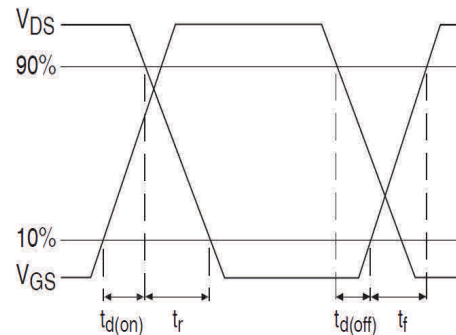
**Fig 22a.** Unclamped Inductive Test Circuit



**Fig 22b.** Unclamped Inductive Waveforms



**Fig 23a.** Switching Time Test Circuit



**Fig 23b.** Switching Time Waveforms

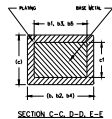
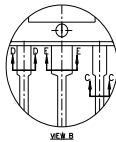
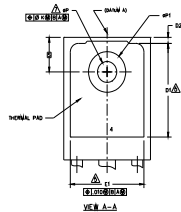
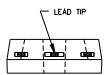
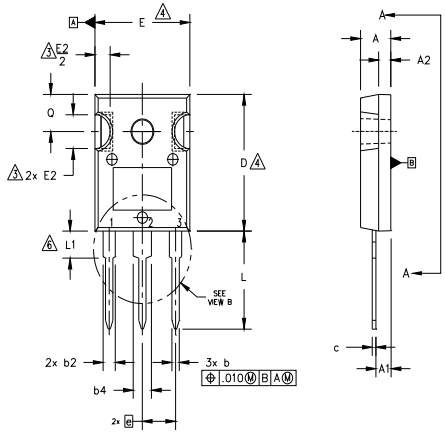


**Fig 24a.** Gate Charge Test Circuit



**Fig 24b.** Gate Charge Waveform

## TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
O	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

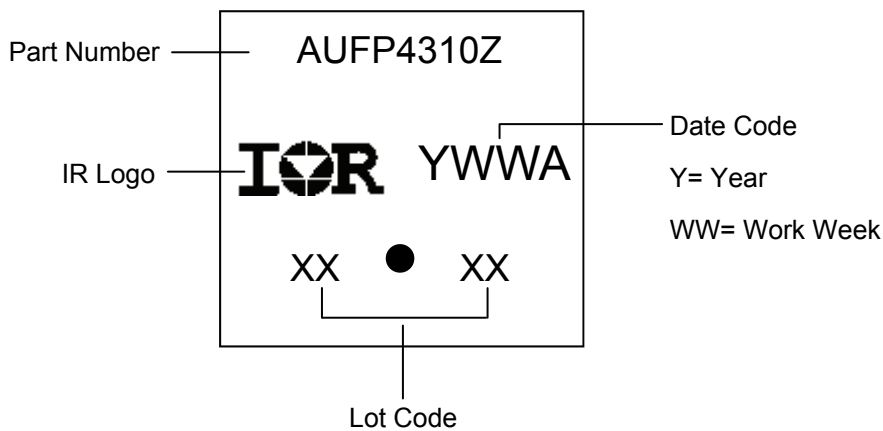
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.



**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		TO-247AC	N/A
<b>ESD</b>	Human Body Model	Class H2 (+/- 4000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

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