

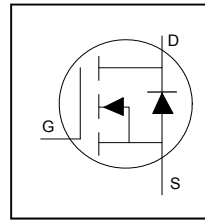
Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

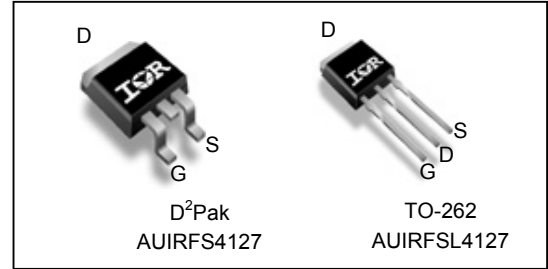
Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET



V_{DSS}	200V
R_{DS(on)} typ.	18.6mΩ
	max
I_D	72A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFSL4127	TO-262	Tube	50	AUIRFSL4127
AUIRFS4127	D ² -Pak	Tube	50	AUIRFS4127
		Tape and Reel Left	800	AUIRFS4127TRL

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	72	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	51	
I _{DM}	Pulsed Drain Current ①	300	
P _D @ T _C = 25°C	Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	57	V/ns
E _{AS}	Single Pulse Avalanche Energy (Thermally limited) ②	250	mJ
I _{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E _{AR}	Repetitive Avalanche Energy ④		mJ
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300(1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑧⑨	—	0.4	°C/W
R _{θJA}	Junction-to-Ambient ⑦	—	40	

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

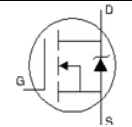
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I _D = 5mA ^①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	18.6	22	mΩ	V _{GS} = 10V, I _D = 44A ^④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Trans conductance	79	—	—	S	V _{DS} = 50V, I _D = 44A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	250		V _{DS} = 200V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _G	Internal Gate Resistance	—	3.0	—	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

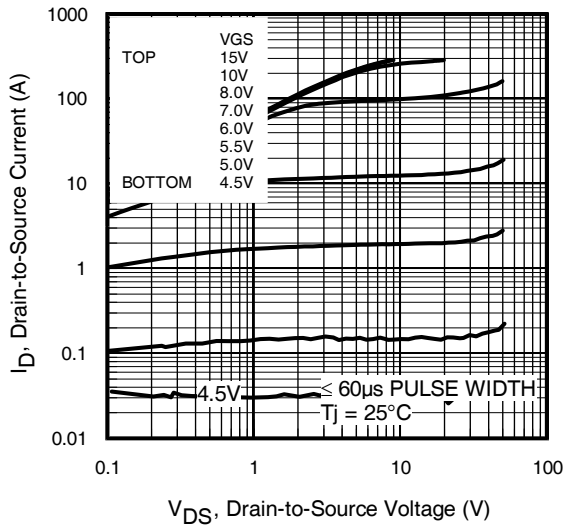
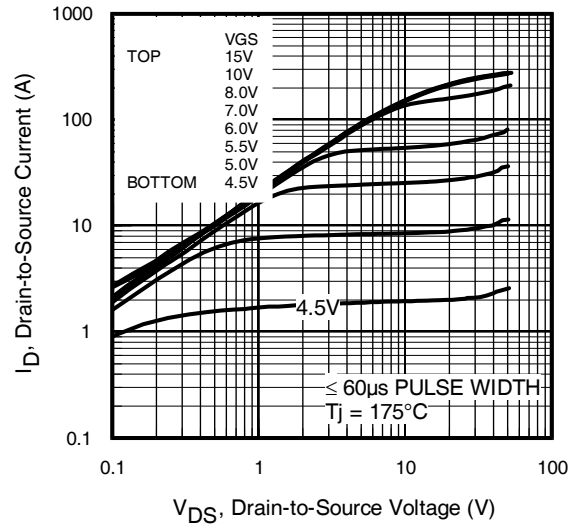
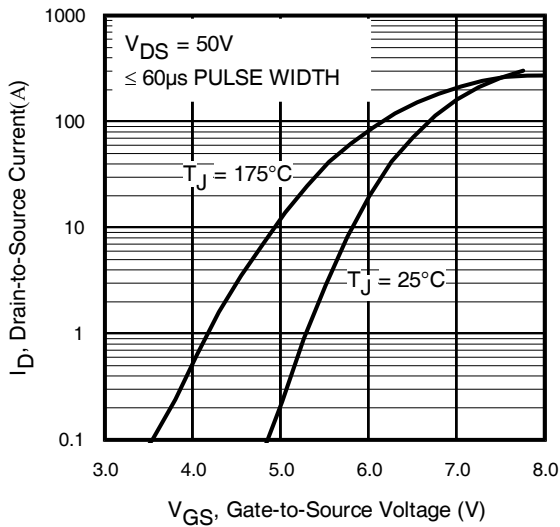
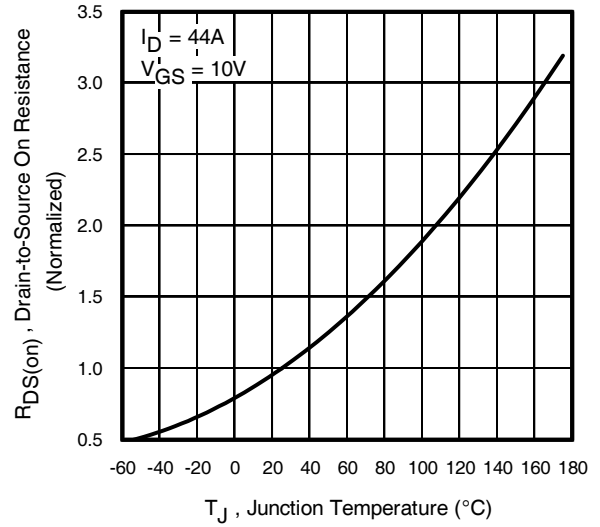
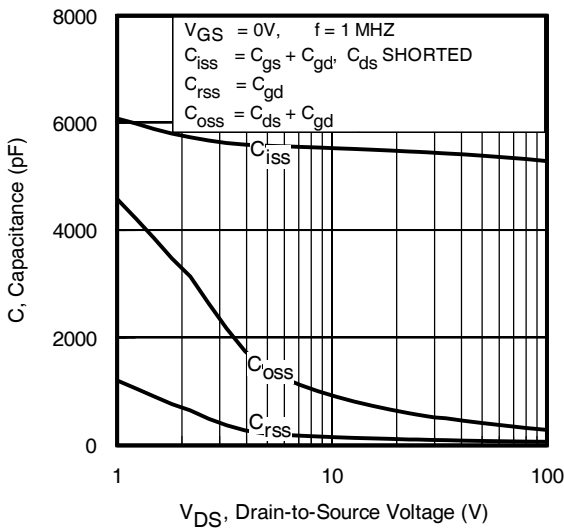
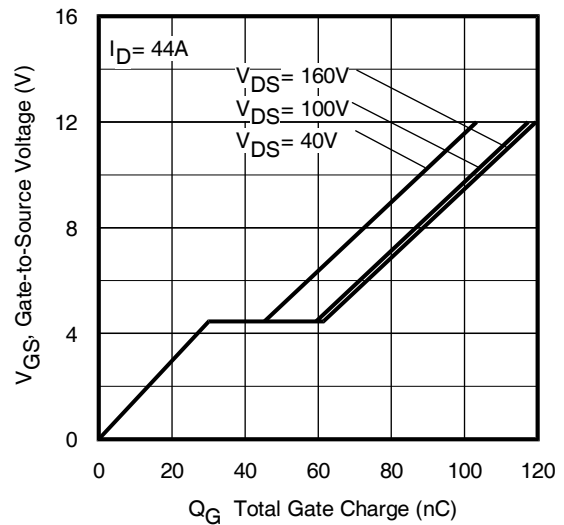
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q _g	Total Gate Charge	—	100	150	nC	I _D = 44A V _{DS} = 100V V _{GS} = 10V ^④
Q _{gs}	Gate-to-Source Charge	—	30	—		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	31	—		
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	69	—		
t _{d(on)}	Turn-On Delay Time	—	17	—	ns	V _{DD} = 130V I _D = 44A R _G = 2.7Ω V _{GS} = 10V ^④
t _r	Rise Time	—	18	—		
t _{d(off)}	Turn-Off Delay Time	—	56	—		
t _f	Fall Time	—	22	—		
C _{iss}	Input Capacitance	—	5380	—	pF	V _{GS} = 0V V _{DS} = 50V f = 1.0 MHz (See Fig. 5) V _{GS} = 0V, V _{DS} = 0V to 160V ^⑥ V _{GS} = 0V, V _{DS} = 0V to 160V ^⑤
C _{oss}	Output Capacitance	—	410	—		
C _{rss}	Reverse Transfer Capacitance	—	86	—		
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	360	—		
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	590	—		

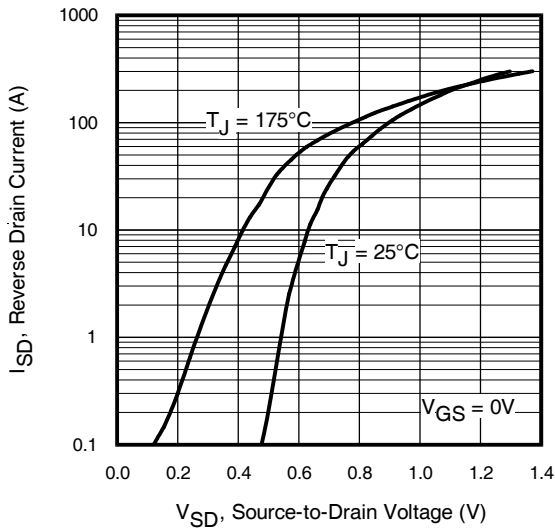
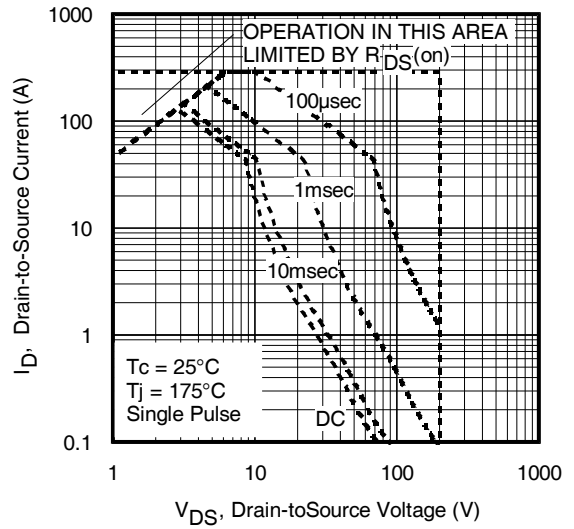
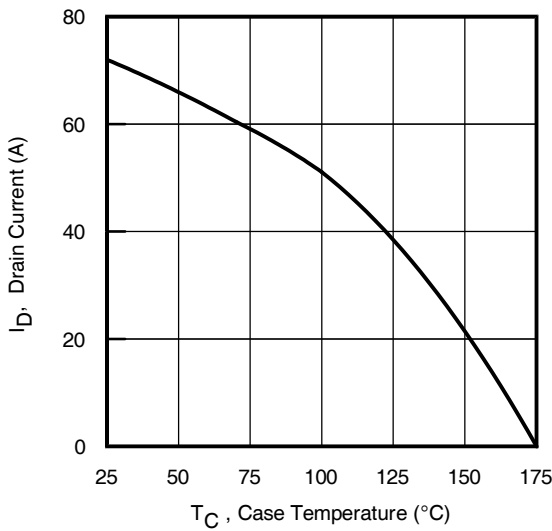
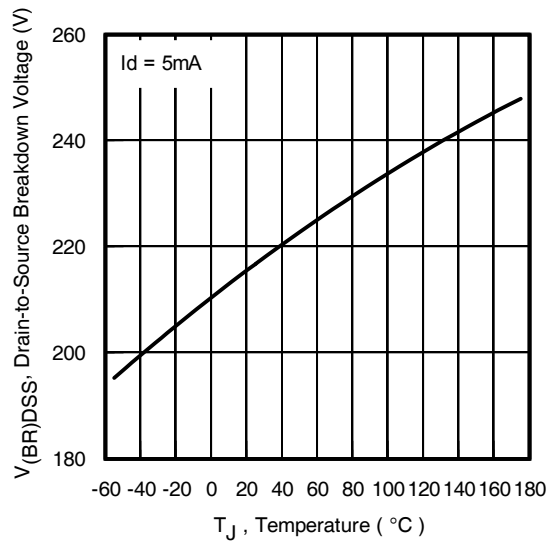
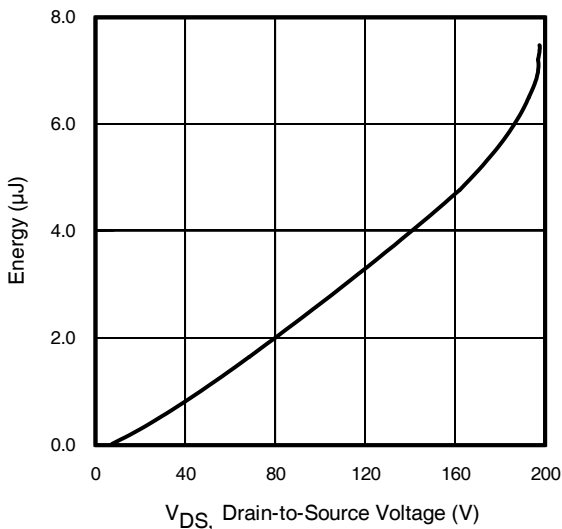
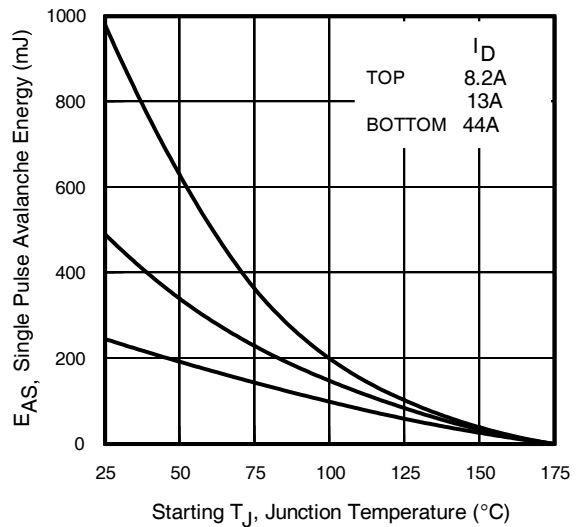
Diode Characteristics

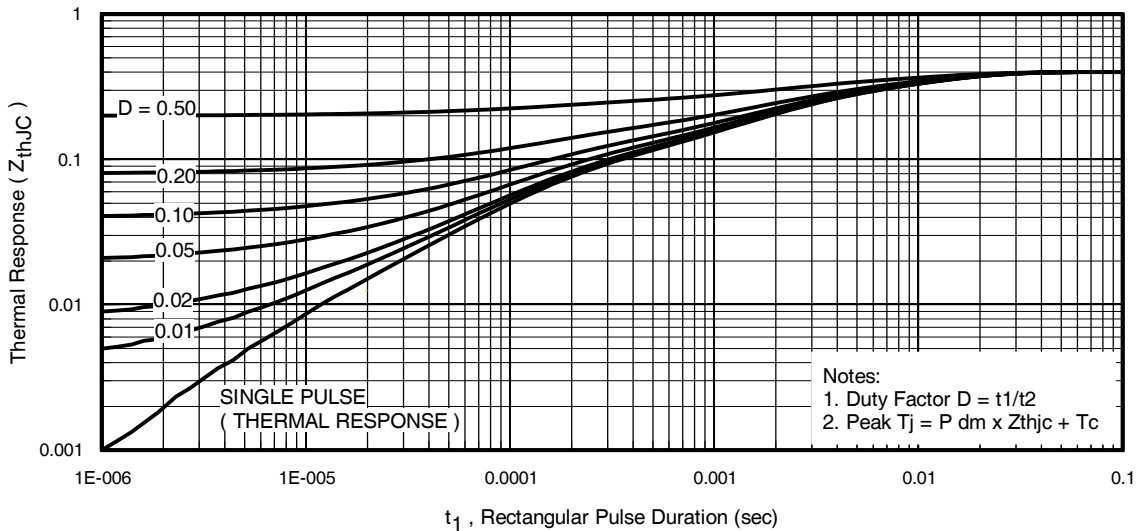
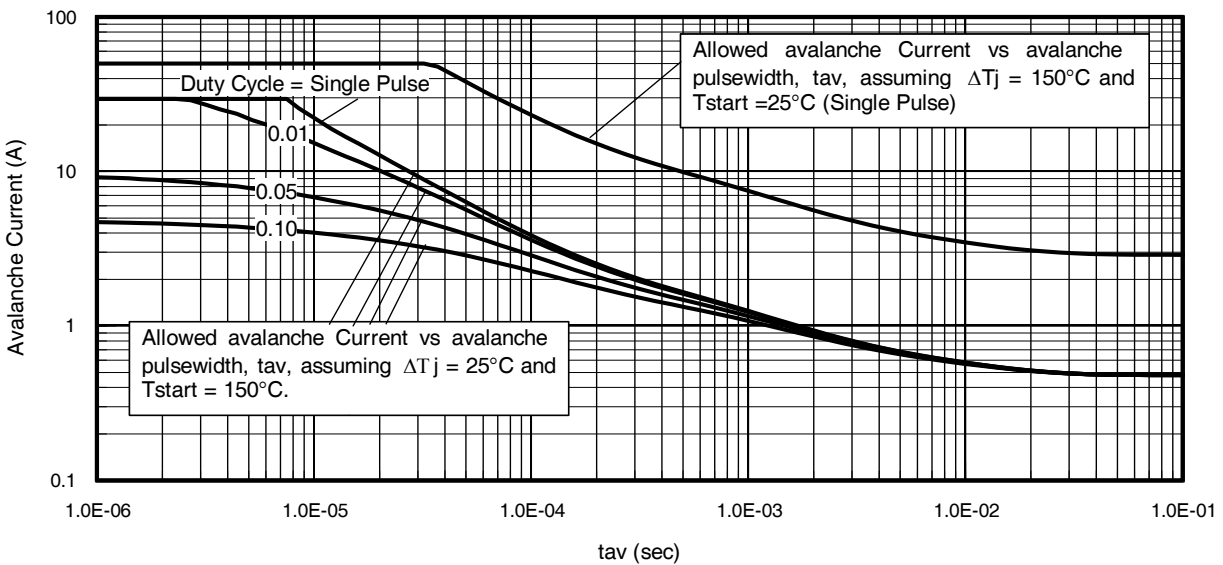
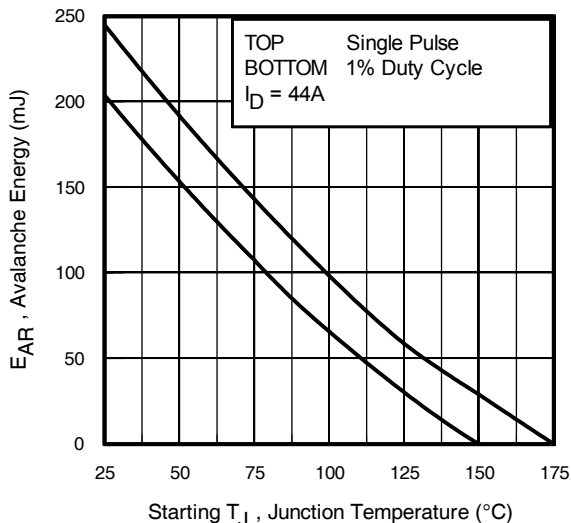
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	72	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	300		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 44A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	136	—	ns	T _J = 25°C
		—	139	—		T _J = 125°C
Q _{rr}	Reverse Recovery Charge	—	458	—	nC	T _J = 25°C
		—	688	—		T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	8.3	—	A	T _J = 25°C

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.26mH, R_G = 25Ω, I_{AS} = 44A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 44A, di/dt ≤ 760A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ R_{θJC} value shown is at time zero.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical C_{oss} Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Avalanche Current vs. Pulse Width

Fig 15. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

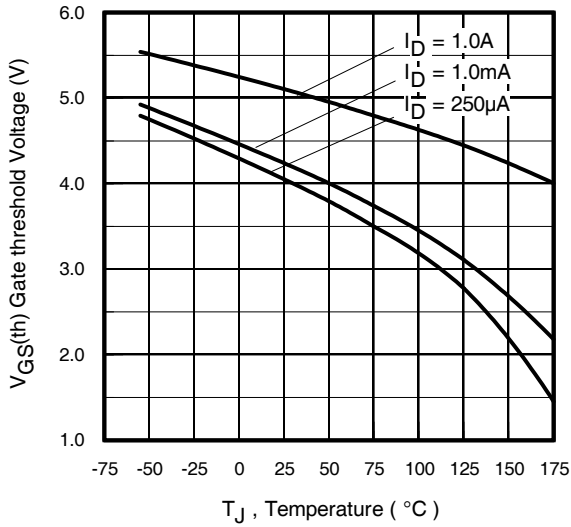
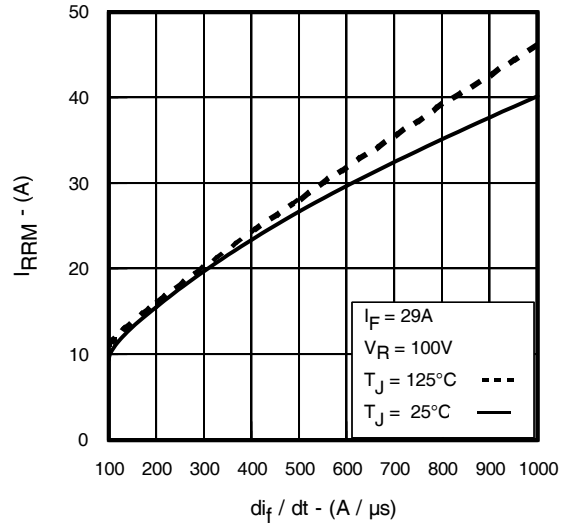
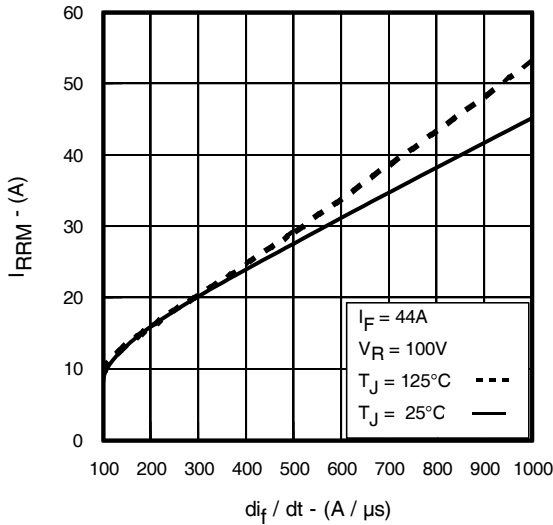
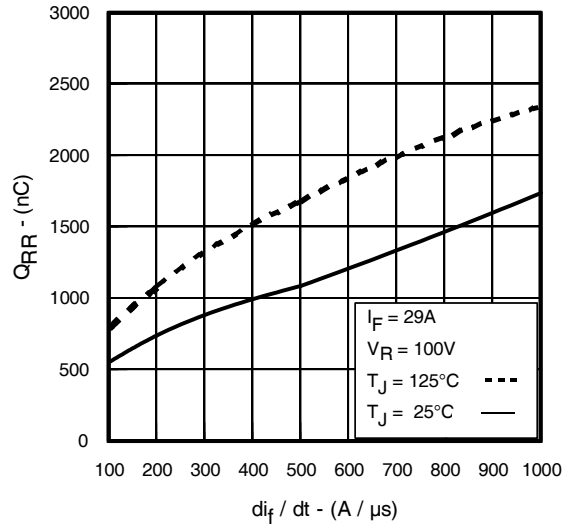
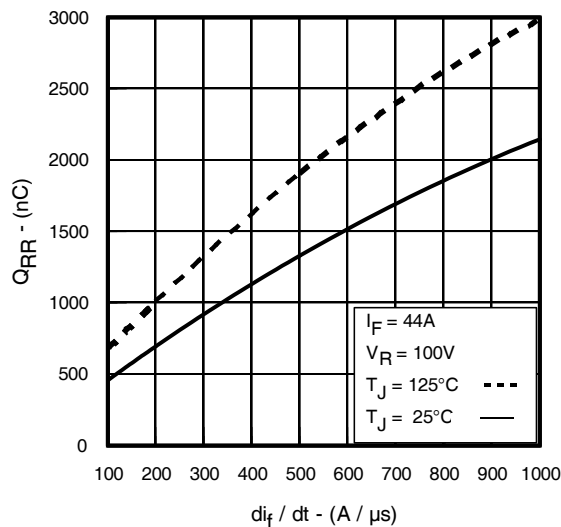
 t_{av} = Average time in avalanche.

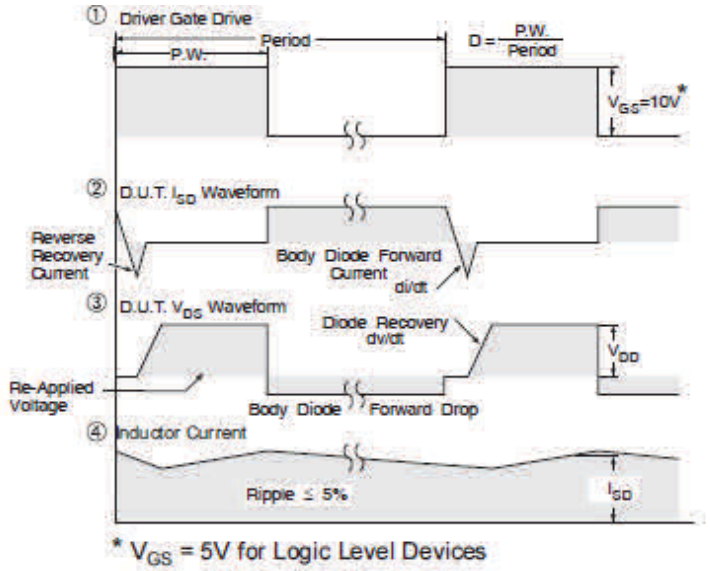
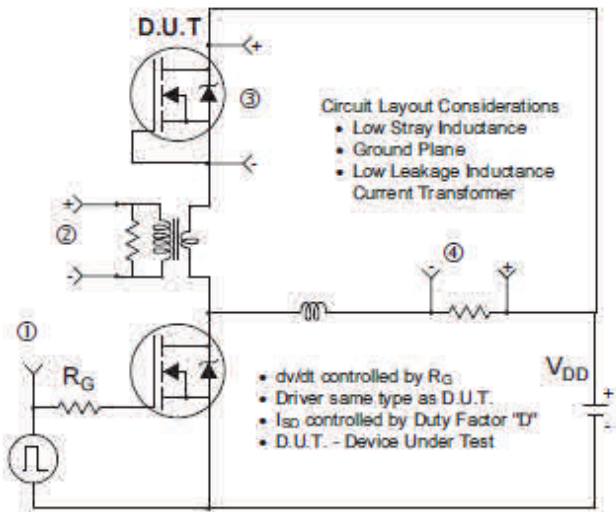
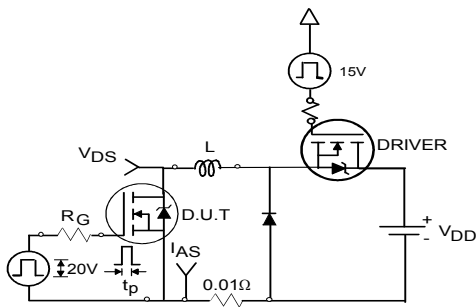
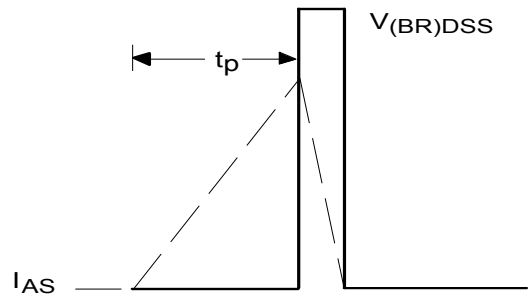
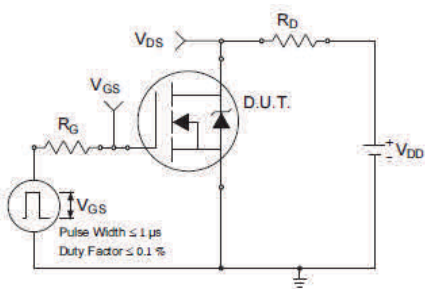
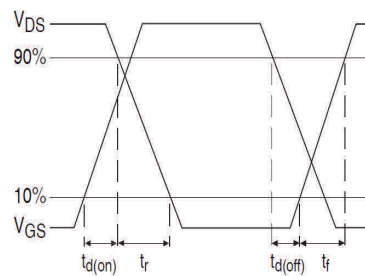
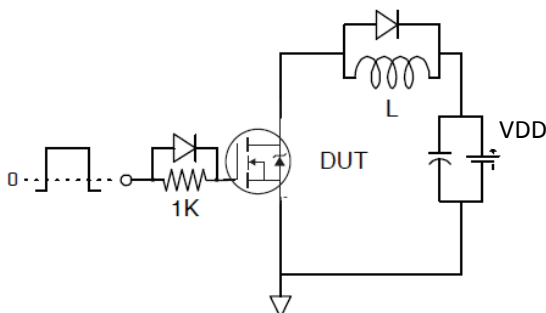
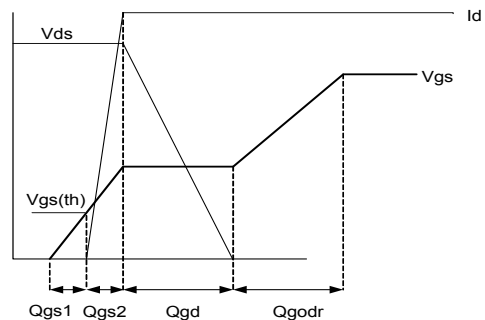
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

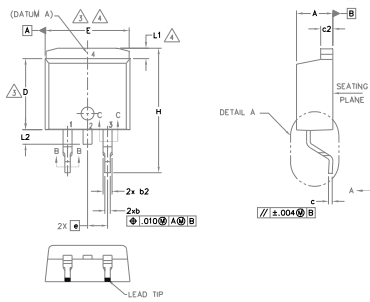
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

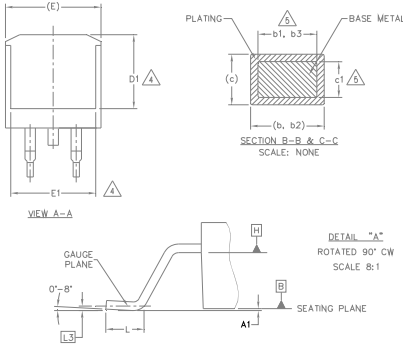
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 16. Threshold Voltage vs. Temperature

Fig 17. Typical Recovery Current vs. dif/dt

Fig 18. Typical Recovery Current vs. dif/dt

Fig 19. Typical Stored Charge vs. dif/dt

Fig 20. Typical Stored Charge vs. dif/dt


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS
DIODES

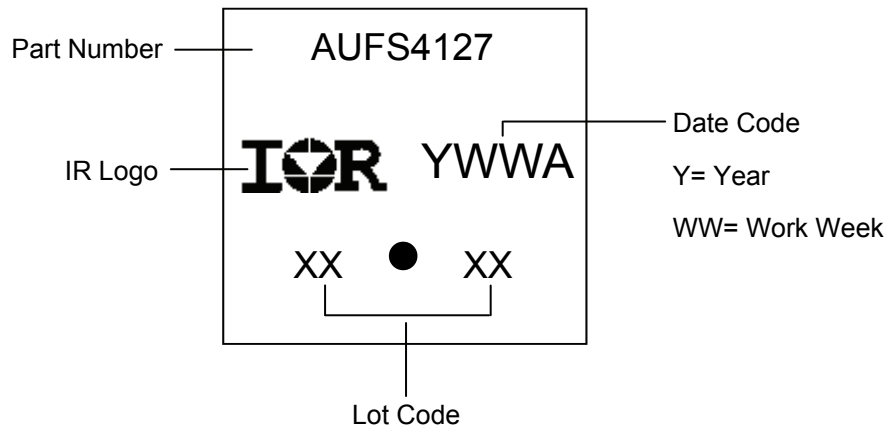
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- 2.- CATHODE
- 3.- ANODE

HEXFET

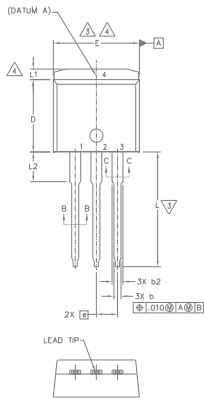
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

D²Pak (TO-263AB) Part Marking Information


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS
IGBTs, CoPACK

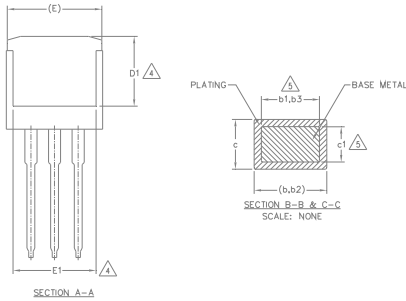
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

HEXFET

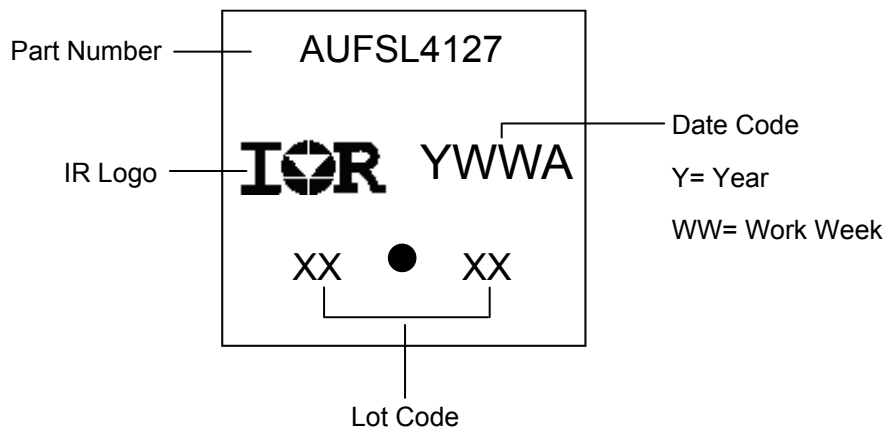
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

DIODES

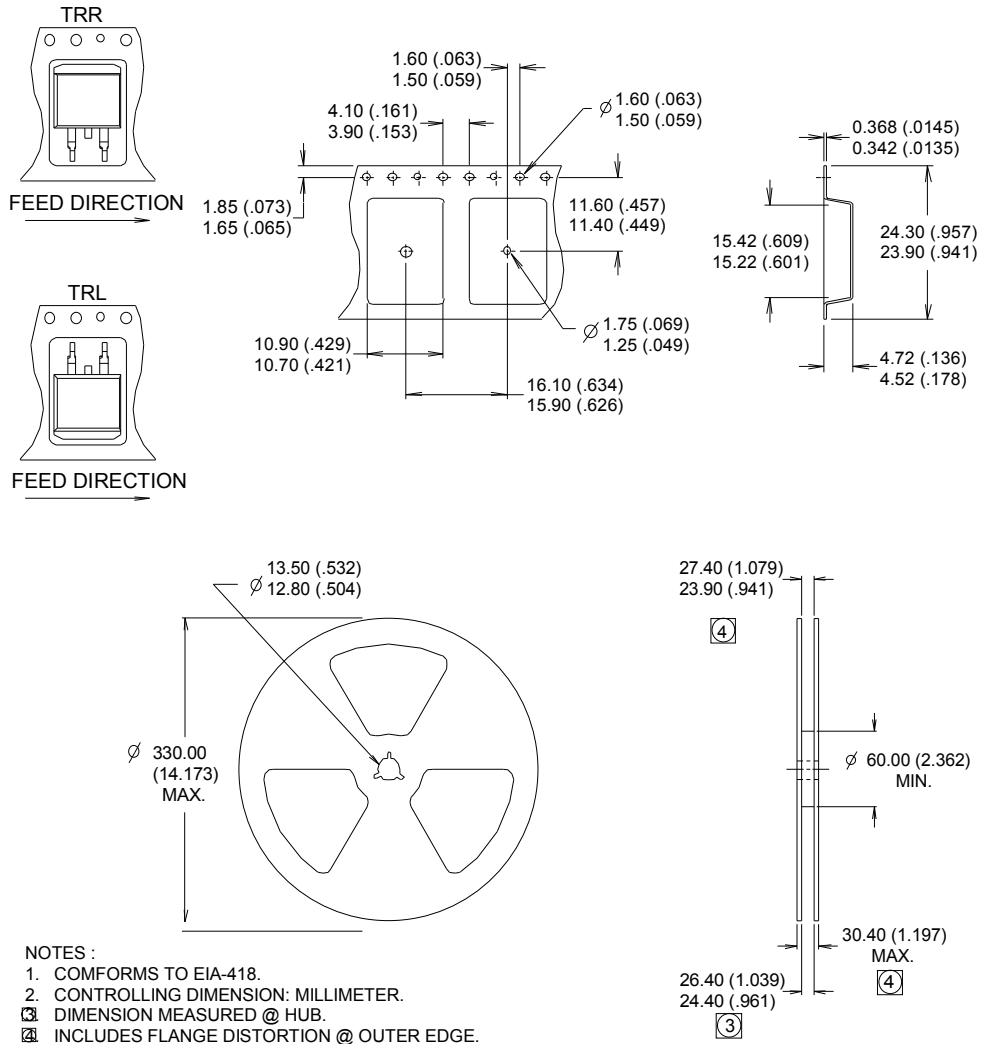
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE
- 4.- DRAIN



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

TO-262 Part Marking Information


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D ² -Pak	MSL1
		TO-262	
ESD	Human Body Model	Class H2 (+/- 4000V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
10/27/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1.

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