AVL2108

DVB-S2/DVB-S Channel Receiver Data Sheet

Description

The AVL2108 is a highly integrated DVB-S2 and DVB-S channel receiver IC. It converts a baseband analog IQ signal from a satellite tuner and performs a set of sophisticated demodulating and decoding operations to output an MPEG video/audio stream. The AVL2108 provides simple and flexible control via a standard two-wire bus. A simplified block diagram of the device is shown in Figure 1-1.

The AVL2108 includes dual, differential, high performance, analog to digital converters (ADC) with a built-in compensation circuit for DC offset and IQ imbalance. An RF AGC output is provided for simple gain control of the satellite tuner via an RC network.

After passing a timing recovery loop and frequency recovery loop, the signal samples are further processed by an equalizer to output decision bits to an FEC decoder. The decoded bits are finally packetized in the MPEG interface block.

The configuration of the AVL2108 is easily performed through a set of registers via a standard two-wire bus. To simplify the interface to the host system, this same two-wire bus is used to communicate with the separate tuner two-wire bus and the DiSEqC™ interface to the LNB.

The AVL2108 can achieve fast acquisition at frequency offsets up to 5 MHz and maintains synchronization under the most severe front-end phase noise.

Applications

- Digital satellite receiver for standard and high definition TV
- High speed satellite data receiver

Features

- High performance QPSK/8PSK satellite TV receiver
- 80 pin LQFP in 12x12 mm package
- Low 420-470 mW power (clear sky)
- Low 630-820 mW power (threshold)
- DVB-S2:
  - Data Rate: 1-45 Msps
  - Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10
  - Roll-off factors for pulse shaping: 0.2, 0.25 and 0.35
- DVB-S:
  - Data Rate: 1-45 Msps
  - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- DIRECTV mode support
- Directly interfaces with tuner for easy implementation
- Integrated dual A/D converters
- Fast automatic blind scan of symbol rates and carrier frequencies
- Carrier frequency acquisition range: ±5MHz
- Signal quality and BER monitors
- Equalizer compensates for channel impairment
- Standard two-wire serial bus with four selectable addresses for easy chip configuration
- DiSEqC™ 2.x compatible with LNB controller
- Standard MPEG-2 transport output parallel and serial interfaces

20201 Century Blvd. Suite 160
Germantown, MD 20874 USA
Tel: 301-515-6716
Fax: 301-916-6199
www.availink.com

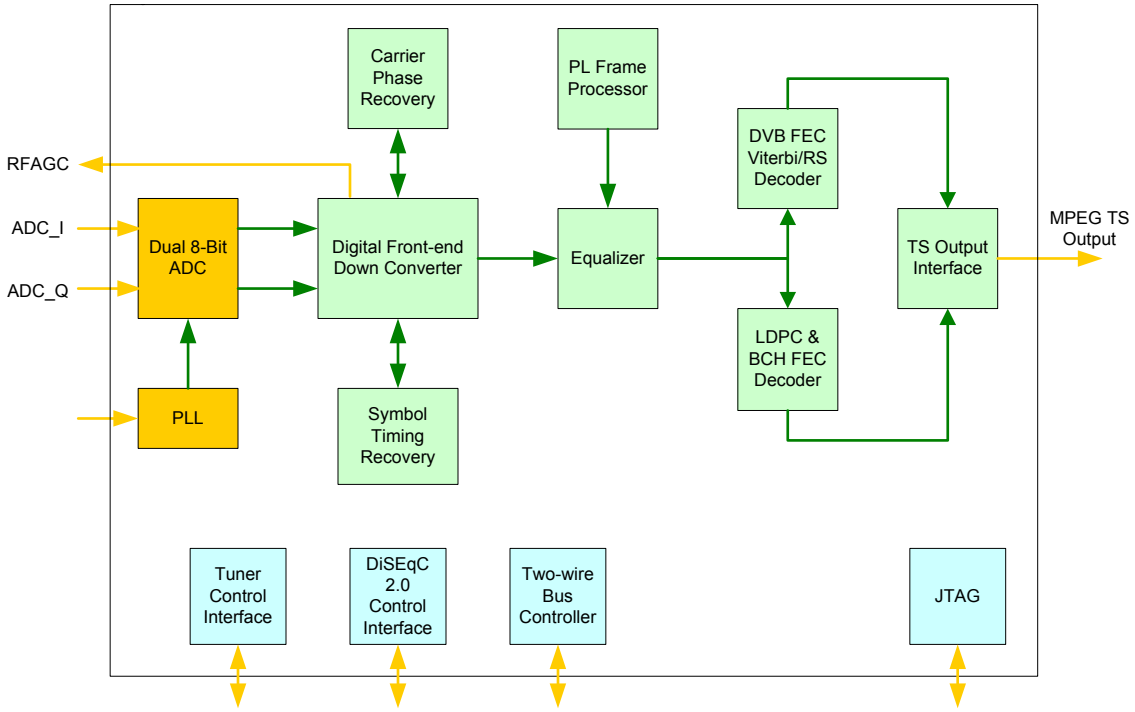
Table of Contents

List of Tables

Table of Figures

1 BLOCK DIAGRAM

Figure 1-1 - AVL2108 Block Diagram



2 PIN DEFINITION

Table 2-1 - Pin Type Definition

TYPE	DEFINITION
I	Input
O	Output, pin is always driven
BI	Bidirectional
OD	Open drain. Either driven low or held in Hi-Z

Table 2-2 - Pin Definition

NAME	PIN	TYPE	DESCRIPTION
Signal Inputs			
ADC_IP ADC_IN	4 5	I	Analog in Phase Component
ADC_QP ADC_QN	8 9	I	Analog in Quadrature Component
Front End Controls			
PLL_REFCLK_XI	12	I	Reference clock input or crystal oscillator input
PLL_REFCLK_XO	13	O	Crystal oscillator output
RFAGC	17	O	RF analog gain control output (external RC Filter required)
SCL2	66	I/OD	2-wire bus clock to tuner front end; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SCL and 3.3V for proper operation
SDA2	67	I/OD	2-wire serial bus data for tuner front end; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SDA and 3.3V for proper operation

NAME	PIN	TYPE	DESCRIPTION
Others			
GPIO_CLK	21	BI	General purpose clock output and general purpose IO
LOCK	22	BI	In normal operation mode an output signal that is high when the receiver is locked and low otherwise. During reset, the pin is used to select reference clock frequency; when using a reference clock of 4 MHz, 4.5 MHz or 10 MHz, the input voltage level during reset MUST be lower than V_{IL} defined in Table 6; when using a reference clock of 16 MHz or 27 MHz, the input voltage level during reset MUST be higher than V_{IH} defined in Table 6.
SLEEP	60	I	Power down request input; When HIGH power down is requested. Held LOW for normal operation. Contact Availink for details on proper operation
SCL1	61	I/OD	Host 2-wire serial bus clock input; nominally a square wave with a maximum frequency of 400 kHz generated by the bus master; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SDA and 3.3V for proper operation
SDA1	62	I/OD	Host 2-wire serial bus data; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SDA and 3.3V for proper operation
CS_1 CS_0	73 74	BI	During reset the CS_1 and CS_0 input signals comprise the two LSB's of the seven bit two-wire bus address. The remaining bits of the address are fixed internally to 00011, therefore the complete two-wire serial bus address is (MSB to LSB): 0,0,0,1,1, CS_1, CS_0. After reset, these two pins serve as general purpose IO. These two pins **must** be pulled high or low and not left unconnected during reset. **See important reset information in** Figure 6-6 **regarding the use of CS_1.**
RST_B	75	I	Active low digital device reset.
NC	80		No Connect

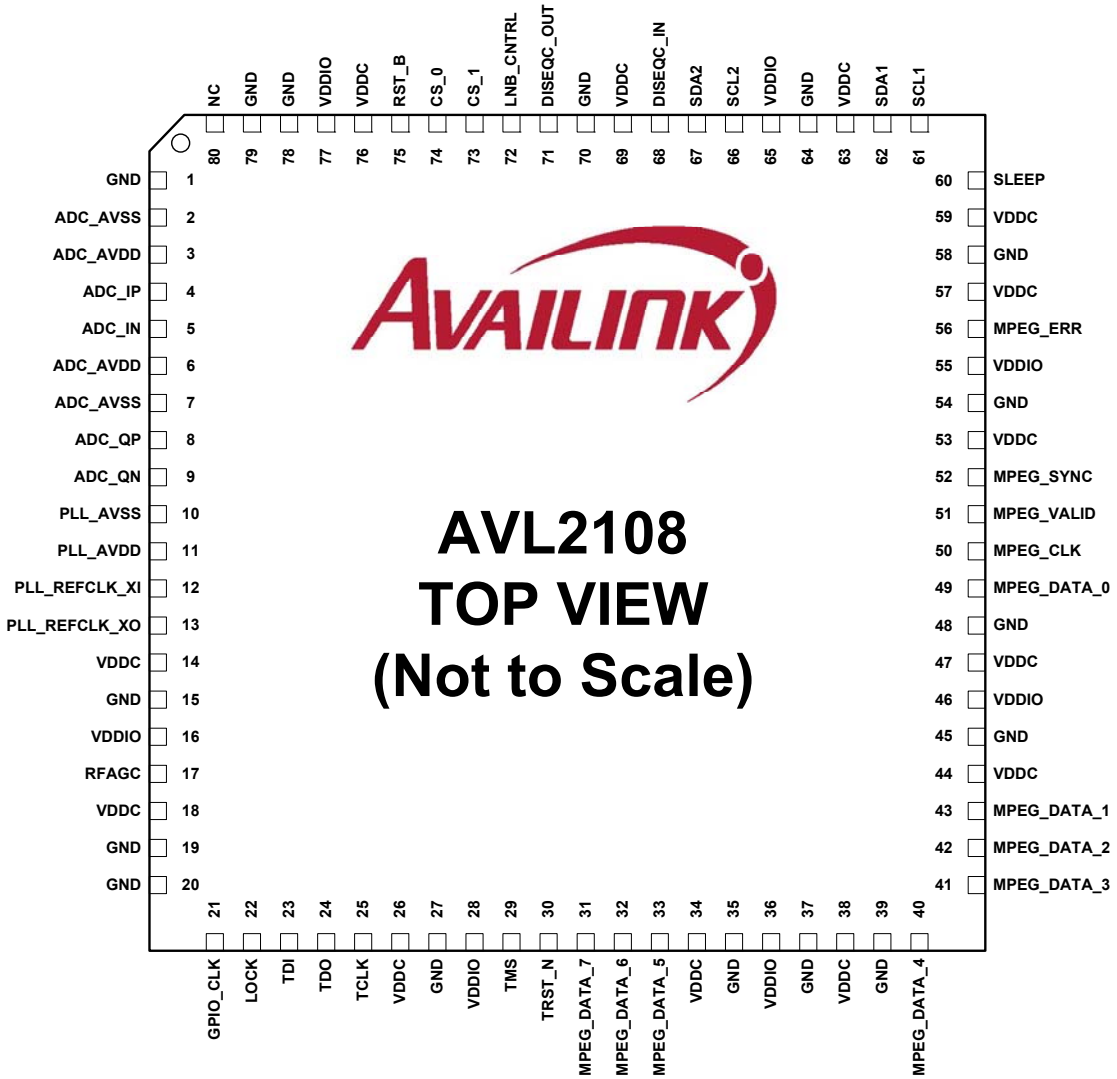
NAME	PIN	TYPE	DESCRIPTION
JTAG and Scan			
TDI	23	I	JTAG serial test data input; data is shifted in on the rising edge of TCLK. This signal can be tied to ground if not used and should not be left unconnected.
TDO	24	O	JTAG serial test data output; data is shifted out on the falling edge of TCLK, This signal can be left unconnected if not used.
TCLK	25	I	JTAG clock input. This signal can be tied to ground if not used and should not be left unconnected.
TMS	29	I	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCLK. Therefore, TMS should be set up before the rising edge of TCLK. This signal can be tied to ground if not used and should not be left unconnected.
TRST_N	30	I	Active-low input to asynchronously reset the boundary-scan circuit. This signal can be tied to ground if not used and should not be left unconnected.

NAME	PIN	TYPE	DESCRIPTION
MPEG Outputs			
MPEG_DATA_7 MPEG_DATA_6 MPEG_DATA_5 MPEG_DATA_4 MPEG_DATA_3 MPEG_DATA_2 MPEG_DATA_1 MPEG_DATA_0	31 32 33 40 41 42 43 49	O	MPEG transport packet data output. In serial mode, MPEG_DATA_7 is serial data output
MPEG_CLK	50	O	MPEG clock output at the data *byte* rate in parallel mode. In serial mode, output at the data *bit* rate
MPEG_VALID	51	O	MPEG data output valid. High during the MPEG_CLK cycles when valid data *bytes* are being output in parallel mode. In serial mode HIGH during the MPEG_CLK cycles when valid data *bits* are being output
MPEG_SYNC	52	O	MPEG sync output signal goes HIGH during the MPEG_CLK each time the first *byte* of a packet is provided in parallel mode. In serial mode, MPEG sync output signal goes HIGH during the MPEG_CLK each time the first *bit* of a packet is provided
MPEG_ERR	56	O	Uncorrectable packet output signal goes HIGH during the MPEG_CLK when the packet provided is uncorrectable
LNB control			
DISEQC_IN	68	I	DiSEqC data encoding input; Polarity can be controlled by internal register
DISEQC_OUT	71	BI	In normal operation mode serves as DiSEqC code output; during reset, an input signal to select debug mode. In order for the chip to work in normal operation mode, the input voltage level during reset MUST be lower than V_{IL} defined in Table 6. If not used, this pin should be tied to GND through 10 kΩ resistor and cannot be left unconnected.
LNB_CNTRL	72	BI	In normal operation mode, a digital output useful for controlling non-DiSEqC LNBs that can be driven out high or low. In a typical application, a low output would be used to set voltage to 18 V, and a high output would be used to set voltage to 13 V; during reset, an input signal that indicates active low PLL bypass debug mode; In order to use the chip in normal operation mode, the input voltage level during reset MUST be higher than V_{IH} defined in Table 6. If not used, it should be tied to VDDIO through 10 kΩ resistor and cannot be left unconnected.

NAME	PIN	TYPE	DESCRIPTION
Power and Ground			
ADC_AVDD	3 6	SUPPLY	Analog supply voltage for the ADC (typically 1.2 V). All pins **must** be connected
PLL_AVDD	11	SUPPLY	Analog supply voltage for the PLL (typically 1.2 V)
ADC_AVSS	2 7	GROUND	Analog grounds for the ADC. All pins **must** be connected
PLL_AVSS	10	GROUND	Analog grounds for the PLL
VDDC	14 18 26 34 38 44 47 53 57 59 63 69 76	SUPPLY	Digital supply voltage (typically 1.2 V). All pins **must** be connected
VDDIO	16 28 36 46 55 65 77	SUPPLY	Digital supply voltage (typically 3.3 V). All pins **must** be connected
GND	1 15 19 20 27 35 37 39 45 48 54 58 64 70 78 79	GROUND	Digital ground. All pins **must** be connected

3 PIN CONFIGURATION

Figure 3-1 - Pin Configuration



4 POWER SEQUENCING AND RESET

4.1 Clock Frequency selection during Reset

During reset, LOCK pin indicates reference clock frequency as shown in the following table.

Table 4-1 - Reference Clock Selection

INPUT REFERENCE FREQUENCY[1]	LOCK PIN
4 MHz	Input voltage level lower than V_{IL} during reset
4.5 MHz	Input voltage level lower than V_{IL} during reset
10 MHz	Input voltage level lower than V_{IL} during reset
16 MHz	Input voltage level higher than V_{IH} during reset
27 MHz	Input voltage level higher than V_{IH} during reset

4.2 Power Sequencing and Reset

ADC_AVDD (1.2V), PLL_AVDD (1.2V), VDDC (1.2V), VDDIO (3.3V) power supplies can be brought up in any order. However, the RST_B pin should be held low until the voltages reach the nominal values. The RST_B shall meet the requirement illustrated in Figure 6-6 - Reset and Mode Signal Timing.

[1] If using reference clock rather than the frequency listed in this table, please contact Availink for further details.

5 THERMAL CHARACTERISTICS

Estimated AVL2108 thermal performance is listed in the following table for several airflow and board construction conditions. These values may be dependent on environmental conditions, adjacent components, board materials, board construction, copper thickness, mounting effectiveness and other factors beyond Availink's control and can not be guaranteed.

Table 5-1 - Thermal Characteristics

SYMBOL	PARAMETER	Airflow			UNIT	PCB CONDITIONS (JEDEC JESD51-9)
		0 m/s	1 m/s	2 m/s		
θ_{ja}	Thermal resistance from junction to ambient	50.4	42.3	39.3	°C/W	2 PCB layers
θ_{jc}	Thermal resistance from junction to case	9.1			°C/W	2 PCB layers
Ψ_{jt}	Junction to top characterization parameter	0.56			°C/W	2 PCB layers

6 ELECTRICAL CHARACTERISTICS

6.1 Test Conditions

Unless otherwise stated, the Min and Max values in Section 6.3 represent operation for 0C ≤ T_a ≤ 70C within the min/max voltage ranges listed. Where included, typical conditions reflect T_a = 25°C± 5°C, ambient humidity = 65% ± 10%, VDDIO = 3.3 V, ADC_AVDDC, PLL_AVDDC, and VDDC = 1.2 V.

6.2 Absolute Maximum Ratings[1]

Table 6-1 - Limiting Values

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDDC	Digital core supply voltage	-0.3	+1.32	V
VDDIO	Digital I/O supply voltage	-0.5	+3.63	V
ADC_AVDDC	ADC Analog core supply voltage	-0.3	+1.32	V
PLL_AVDDC	PLL Analog core supply voltage	-0.3	+1.32	V
V_i	Digital input voltage	-0.5	VDDIO + 0.5	V
VA_i	Analog input voltage	-0.5	AVDDC + 0.5	V
T_a	Ambient temperature	-10	+70	°C
T_j	Junction temperature	-10	+125	°C
T_s	Storage Temperature	-40	+150	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

6.3 Characteristics

Table 6-2 - Characteristics

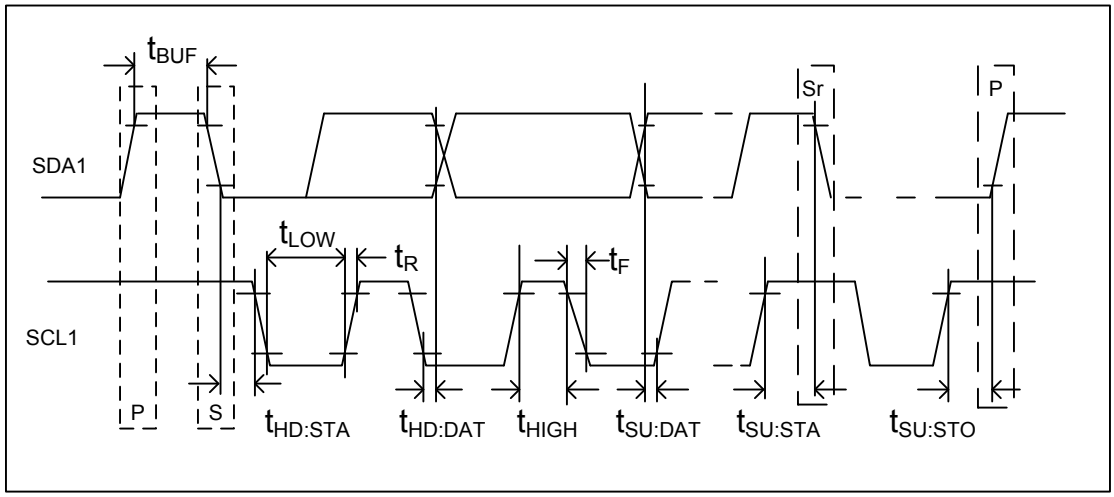
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
VDDC	Digital core supply voltage		1.1	1.2	1.3	V
VDDIO	Digital I/O supply voltage		3.0	3.3	3.6	V
ADC_AVDD	ADC Analog core supply voltage		1.1	1.2	1.3	V
PLL_AVDD	PLL Analog core supply voltage		1.1	1.2	1.3	V
I_{DDC}	Digital core peak current			800[2]	900[2,4]	mA
I_{DDIO}	Digital I/O current			20	50[5]	mA
$I_{ADC} + I_{PLL}$	1.2V Analog core current			85	130	mA
P_{AVG}	Average power in Clear Sky (See Table 13)			430 to 470[3]		mW
P_{AVGT}	Average power at threshold (See Table 13)			620 to 830[3,4]		mW
P_{SLEEP}	Average power in sleep mode			140		mW
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
V_{OL}	Low level output voltage	VDDIO = 3.3 V – 5% I_{SOURCE} = 1.6 mA			0.4	V
V_{OH}	High level output voltage		2.4			V
Reference Clock Frequency						
f_{REF}	Reference clock frequency		4	10	27	MHz
ADC						
V_{FSR}	Analog input differential voltage range	FSCTRL Register = 00	±679	±697	±715	mV
V_{FSR}	Analog input differential voltage range	FSCTRL Register = 11	±340	±348	±361	mV
	Input impedance, differential			5		pF
	Input resistance, differential			5.6		kΩ

[2] Test Condition: 8PSK, symbol rate 30 Msps, code rate 2/3, pilot on, at threshold, V_{DDC} = 1.2.
[3] Test Condition: DVB-S2, 30 Msps. Power consumption varies with code rate and modulation, see Table 13 for details. Typical Average Power includes 20mA (66 mW) of 3.3V power with the remainder being 1.2V analog and digital.
[4] Availink recommends that 1.2V power supply current be based on Average power at threshold plus desired margin. Digital core peak current is supplied by adjacent decoupling capacitors.
[5] Availink recommends digital IO power supply current be based on maximum digital I/O current.

6.4 Timing Characteristics

6.4.1 Host 2-Wire Bus Timing

Figure 6-1 - Host 2-Wire Bus Timing



Where: S = Start
Sr = Restart, i.e., Start without stopping first.
P = Stop

Table 6-3 - Host 2-Wire Bus Timing

Parameter: Host 2-wire bus only	Symbol	Value		Unit
		Min.	Max.	
SCL1 clock frequency	f_{CLK}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1300		ns
Hold time (repeated) START condition	$t_{HD:STA}$	600		ns
LOW period of SCL1 clock	t_{LOW}	1300		ns
HIGH period of SCL1 clock	t_{HIGH}	600		ns
Set-up time for a repeated START condition	$t_{SU:STA}$	600		ns
Data hold time (when input)	$t_{HD:DAT}$	0		ns
Data set-up time	$t_{SU:DAT}$	100		ns
Rise time of both SCL1 and SDA1 signals	t_R	20+0.1Cb[5]	300[6]	ns
Fall time of both SCL1 and SDA1 signals, (100pF to ground)	t_F	20+0.1Cb[5]	300[6]	ns
Set-up time for a STOP condition	$t_{SU:STO}$	600		ns

[5] Cb = the total capacitance on either clock or data line in pF.
[6] The rise time depends on the external bus pull-up resistor and bus capacitance.

6.4.2 MPEG Interface Timing

Figure 6-2 - MPEG Interface Timing In Parallel Mode with Falling Edge Clock

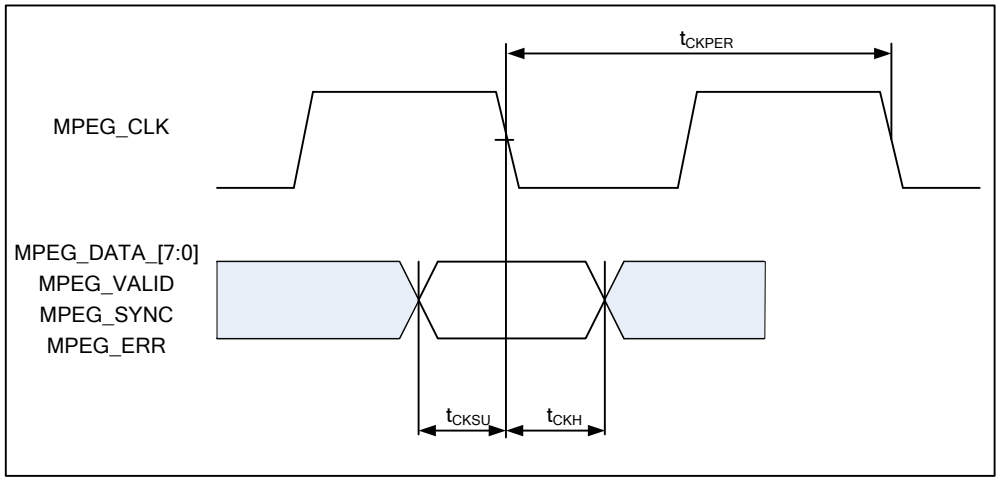


Table 6-4 - MPEG Interface Timing In Parallel Mode with Falling Edge Clock Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK falling edge	t_{CKSU}	10[7] 28[8]		ns
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK falling edge	t_{CKH}	10[7] 28[8]		ns
MPEG_CLK Parallel Mode Edge to Edge Time	t_{CKPER}	60		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. t_{CKPER} represents the minimum MPEG_CLK period in parallel mode in 8PSK modes with pilot on and all QPSK modes.

[7] AVL2108LG
[8] AVL2108LGa

Figure 6-3 - MPEG Interface Timing In Parallel Mode with Rising Edge Clock

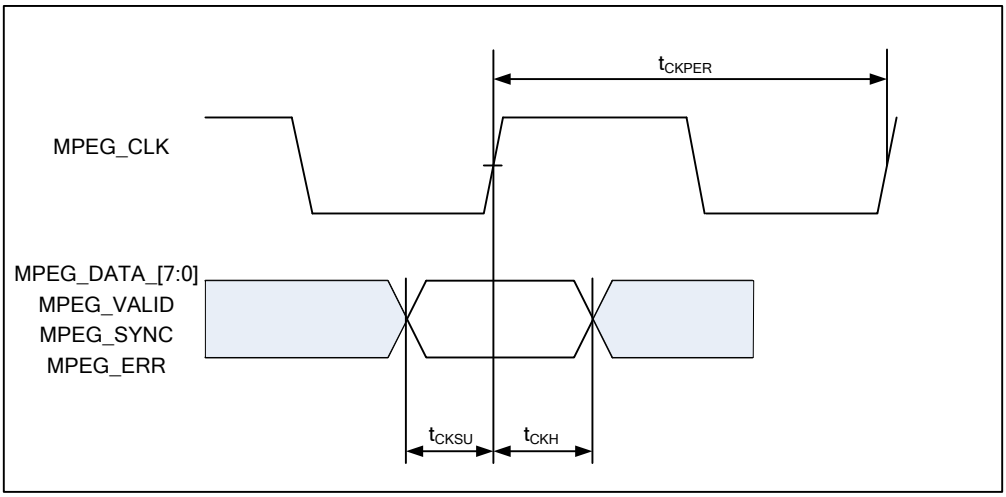


Table 6-5 - MPEG Interface Timing In Parallel Mode with Rising Edge Clock Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK rising edge	t_{CKSU}	10[9] 28[10]		ns
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK rising edge	t_{CKH}	10[9] 28[10]		ns
MPEG_CLK Parallel Mode Edge to Edge Time	t_{CKPER}	60		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. t_{CKPER} represents the minimum MPEG_CLK period in parallel mode in 8PSK modes with pilot on and all QPSK modes.

[9] AVL2108LG
[10] AVL2108LGa

Figure 6-4 - MPEG Interface Timing In Serial Mode with Falling Edge Clock

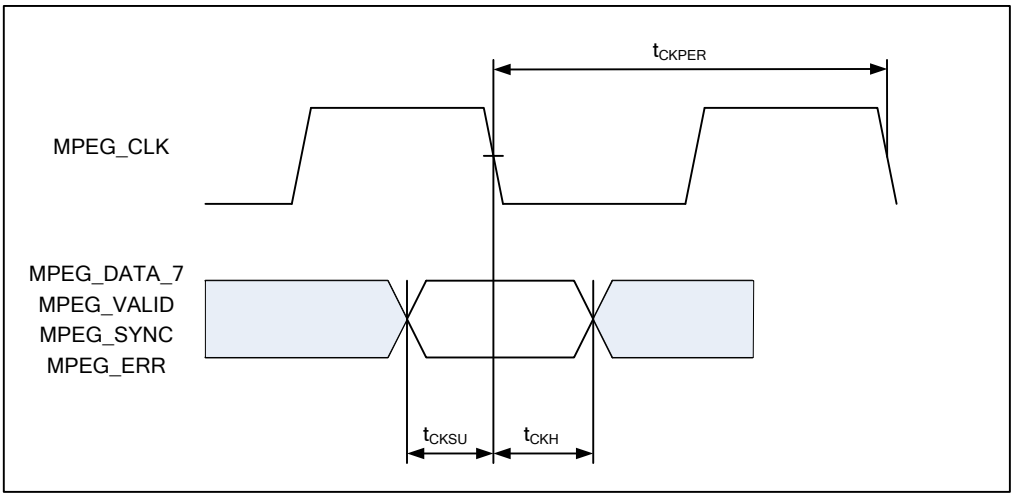


Table 6-6 - MPEG Interface Timing In Serial Mode with Falling Edge Clock Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK falling edge	t_{CKSU}	4.2		ns
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK falling edge	t_{CKH}	2.5		ns
MPEG_CLK Serial Mode Edge to Edge Time	t_{CKPER}	8.9[2]		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. Serial mode limits the transport stream to 112.5 Mbps.

Figure 6-5 - MPEG Interface Timing In Serial Mode with Rising Edge Clock

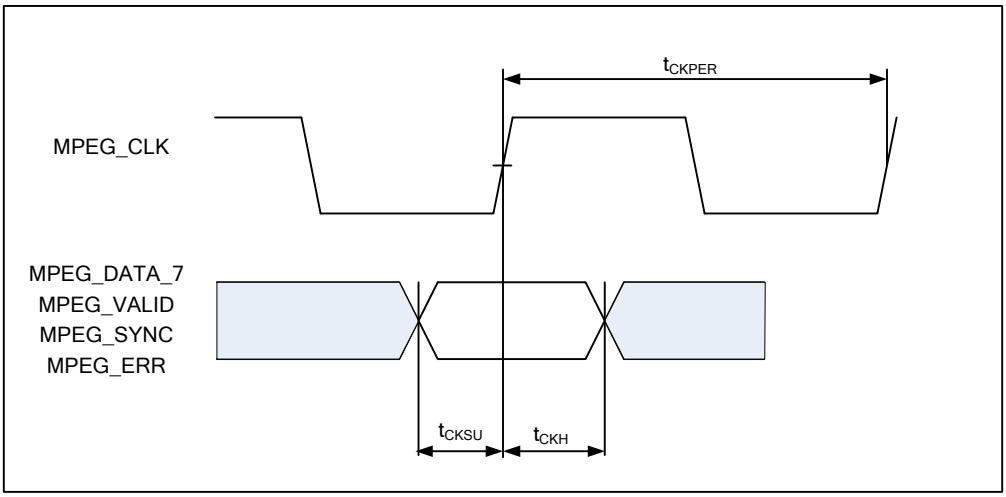


Table 6-7 - MPEG Interface Timing In Serial Mode with Rising Edge Clock Timing

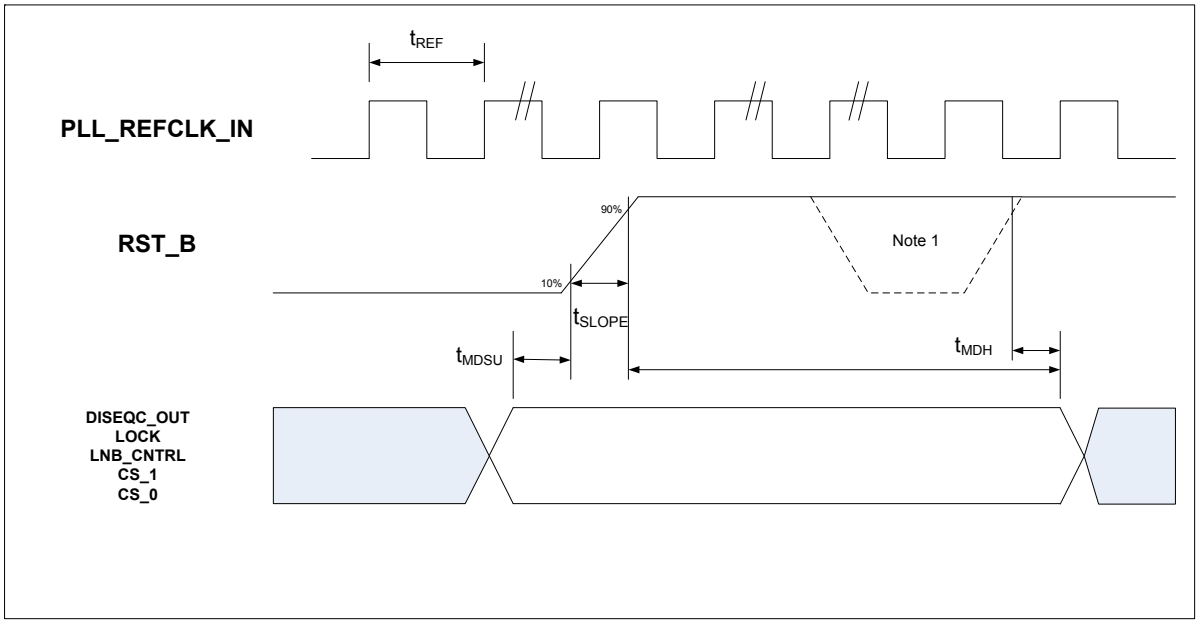
Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK rising edge	t_{CKSU}	4.2		ns
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK rising edge	t_{CKH}	2.5		ns
MPEG_CLK Serial Mode Edge to Edge Time[2]	t_{CKPER}	8.9[2]		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. Serial mode limits the transport stream to 112.5 Mbps.

6.4.3 Reset and Mode Signal Timing

Figure 6-6 - Reset and Mode Signal Timing



NOTE 1: Second RST_B pulse shown by dotted line above is only required when using CS_1 address value of 1 (pull-up). Typical one or two device configurations using a pull-down on CS_1 do not require this.

Table 6-8 - Reset and Mode Signal Timing

Parameter	Symbol	Value					Unit
PLL_REFCLK_IN Clock Frequency		4	4.5	10	16	27	MHz
PLL_REFCLK_IN Clock Period	t_{REF}	250	222	100	63	37	ns
Minimum DISEQC_OUT, LOCK, LNB_CNTRL, CS_1 and CS_0 stable before RST_B rising edge	t_{MDSU}	2500	2220	1000	630	370	ns
Minimum DISEQC_OUT, LOCK, LNB_CNTRL, CS_1 and CS_0 stable after RST_B rising edge	t_{MDH}	750	666	300	189	111	ns
Maximum Reset Slope Time	t_{SLOPE}	1750	1554	700	630	259	ns

7 TYPICAL PERFORMANCE CHARACTERISTICS

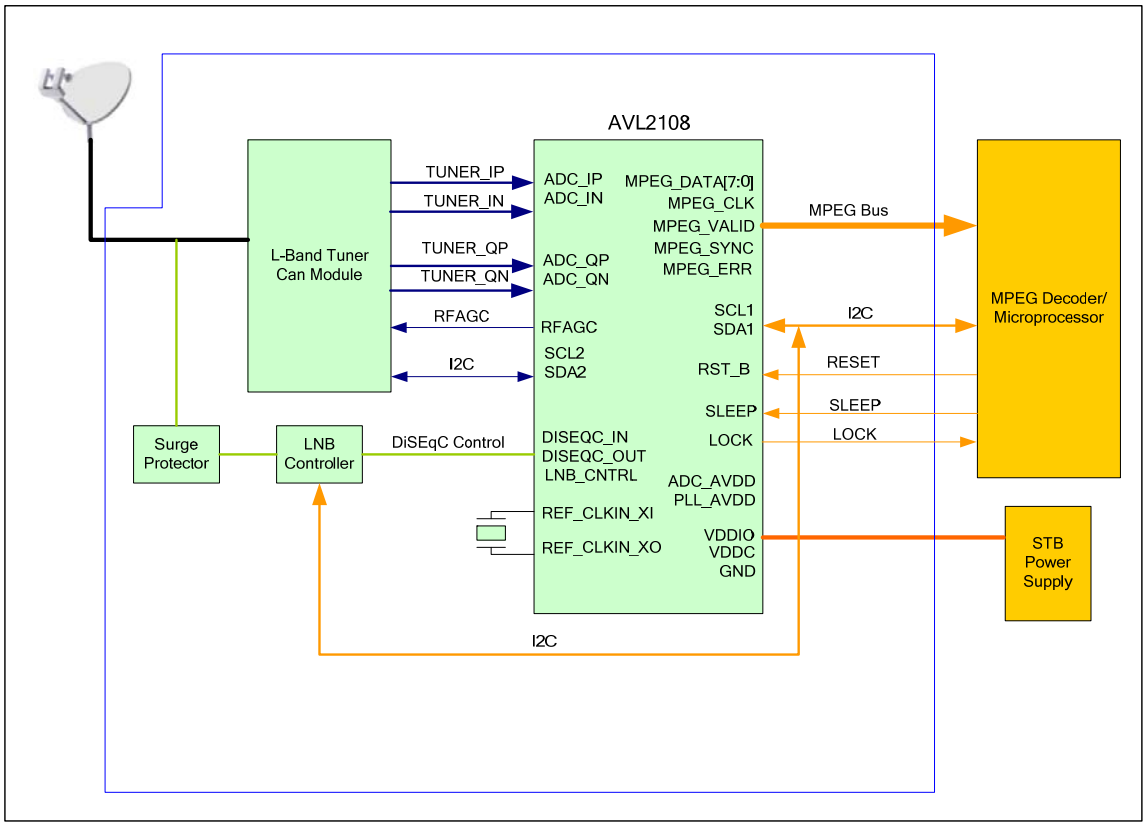
Table 7-1 – AVL2108 Average Power, DVB-S2, 30MSPS

Mode	Clear Sky SNR (mW)	Threshold SNR (mW)
QPSK 1/2	430	780
QPSK 3/5	430	790
QPSK 2/3	430	800
QPSK 3/4	430	800
QPSK 4/5	430	790
QPSK 5/6	430	790
QPSK 8/9	430	630
QPSK 9/10	430	620
8PSK 3/5	470	820
8PSK 2/3	460	830
8PSK 3/4	460	830
8PSK 5/6	470	830
8PSK 8/9	470	700
8PSK 9/10	460	680

Note: Pilot off for QPSK, pilot on 8PSK modes.
Includes all 3.3V and 1.2V supplies.

8 APPLICATION INFORMATION

Figure 8-1 - Typical Application



As shown in Figure 8-1, the AVL2108 device communicates with an L-Band Tuner intended for DVB-S2 set top box (STB) applications. The Tuner outputs a differential I/Q pair of signals which are then sampled within the AVL2108 device. The AVL2108 demodulates the signal and applies an advanced FEC algorithm on the data. The device then forwards an MPEG data stream to the adjacent MPEG decoder chip. The STB host controls the AVL2108 device and Tuner IC via an I2C Bus interface.

The reference design below can be used by the board designer as a general guideline to help construct an application schematic.

Figure 8-2 - Sample Reference Design

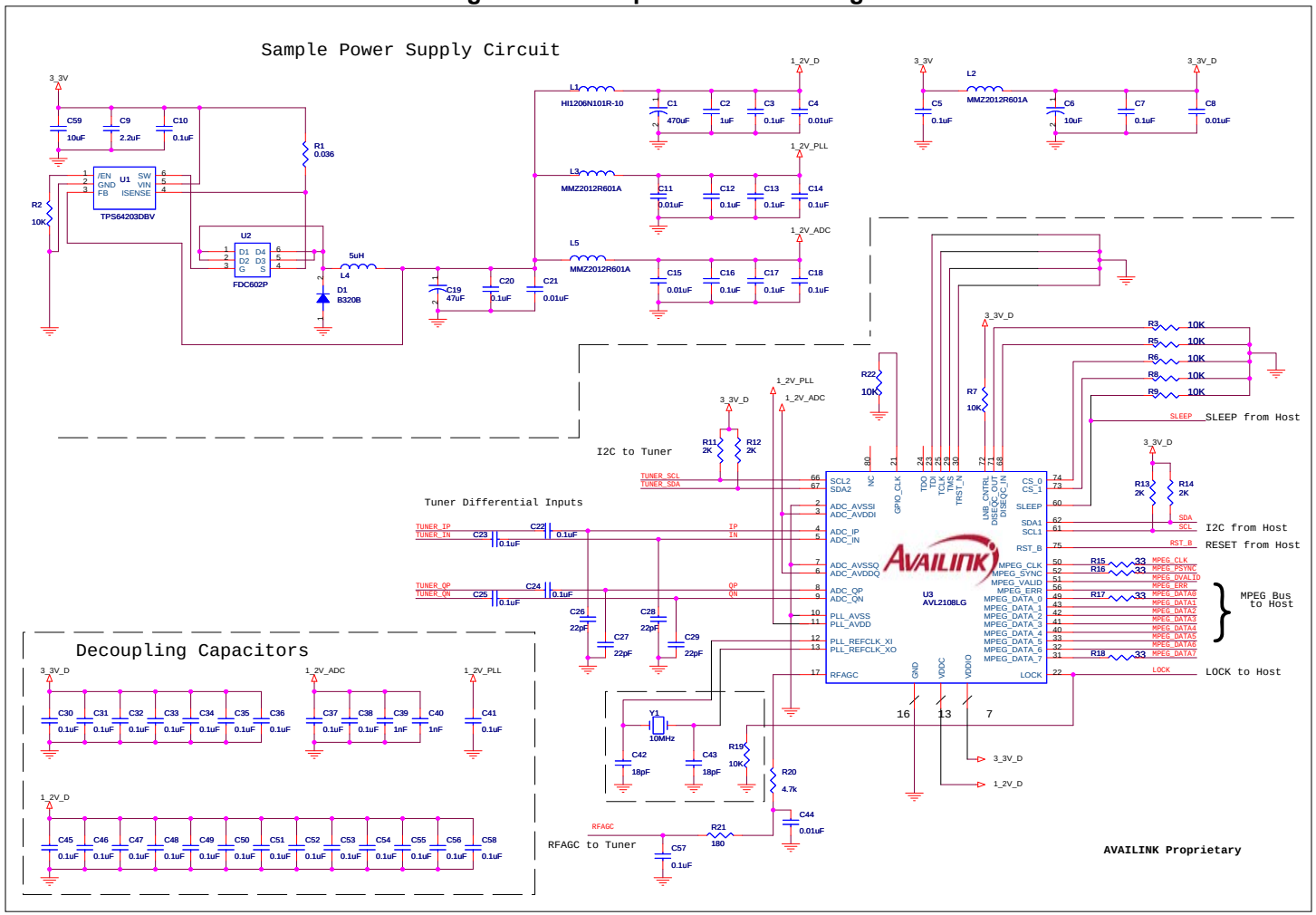


Figure 8-2, illustrates a sample reference design for the AVL2108 device. The schematic is divided into four sections:

- AVL2108 clock circuit options
- Sample power supply circuitry
- AVL2108LG device
- Sample power decoupling capacitors

8.1 AVL2108 Clock Options

The AVL2108 device can accommodate three different clock circuit options. The board designer must be aware that it is important for overall chip performance to select a low jitter clock source. The designer can select from one of the following three clock sources:

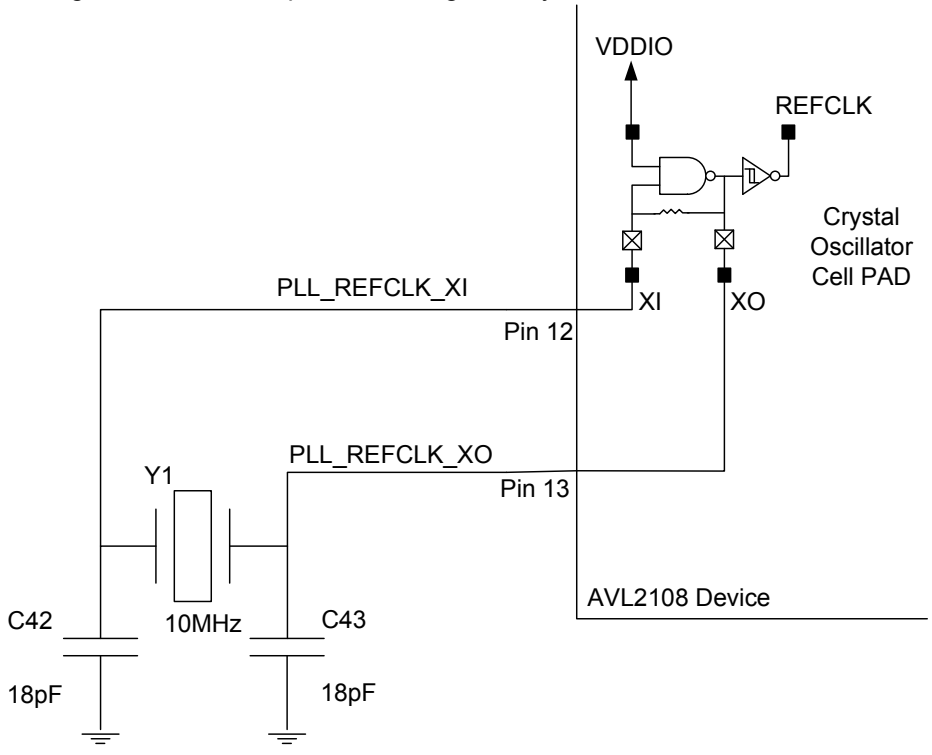
- Clock input using a crystal
- Use an external digital input clock
- Clock input using an external sine wave

The following sub-sections describe in detail each clock circuit option, clock frequency selection and tolerances.

8.1.1 Clock Input Using a Crystal

The AVL2108, PLL_REFCLK_XI input pin can be driven using a crystal oscillator source. The diagram below shows how such a circuit is implemented and connected to the AVL2108 device.

Figure 8-3 - Clock input circuit diagram Crystal Oscillator at 10 MHz



The clock circuit diagram shown in Figure 8-3 is used in the sample reference design. The crystal should meet the following specifications:

- Tolerance overall: ±50 ppm
- Nominal load capacitance: 12 pF
- Maximum equivalent series resistance: 160 ohms

Select from one of the following crystal resonant frequencies:

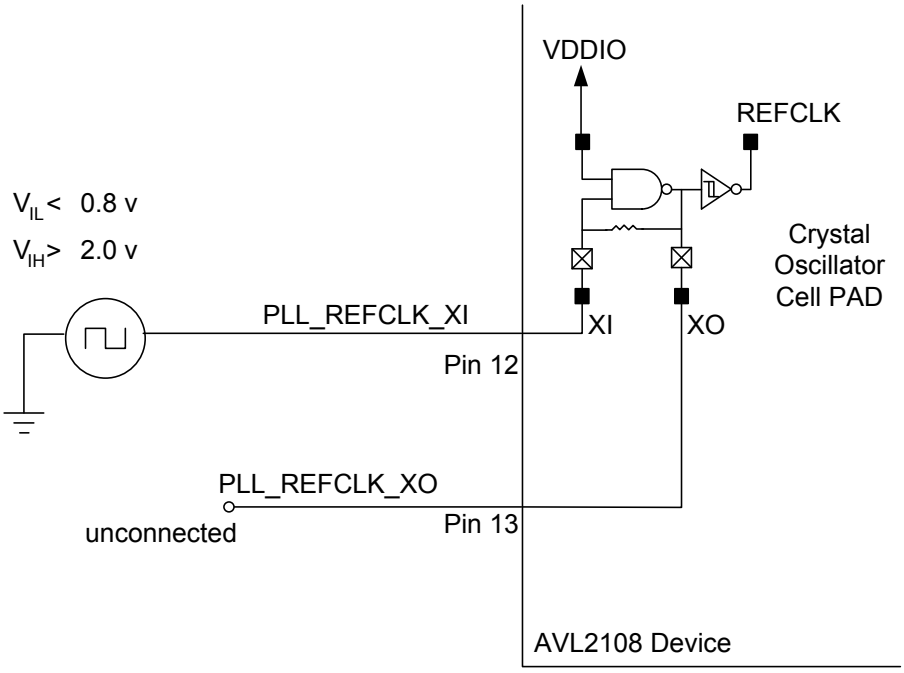
- Parallel resonant fundamental frequency: 4 MHz, 4.5 MHz, 10 MHz, 16 MHz, or 27 MHz.

After selecting a clock frequency the designer must configure the AVL2108 LOCK pin, as specified in Table 4-1. For example, selecting a 10 MHz crystal, the LOCK pin requires a 10k ohm pull down resistor to ground as shown in Figure 8-2.

8.1.2 External Digital Input Clock

PLL_REFCLK_XI input pin can be driven by an external LVTTL level square wave clock. The diagram below shows how a LVTTL level square wave clock source is implemented and connected to the AVL2108 device.

Figure 8-4 - Square Wave Clock Input Source Circuit



The clock source should meet the following specifications:

- For LVTTL level square wave clock, it must meet V_{IL} and V_{IH} defined in Table 6-2.
- Tolerance overall: ±50 ppm

Select from one of the following frequencies:

- Frequency: 4 MHz, 4.5 MHz, 10 MHz, 16 MHz, or 27 MHz.

For this clock circuit option, the PLL_REFCLK_XO pin, (Pin 13), is left unconnected.

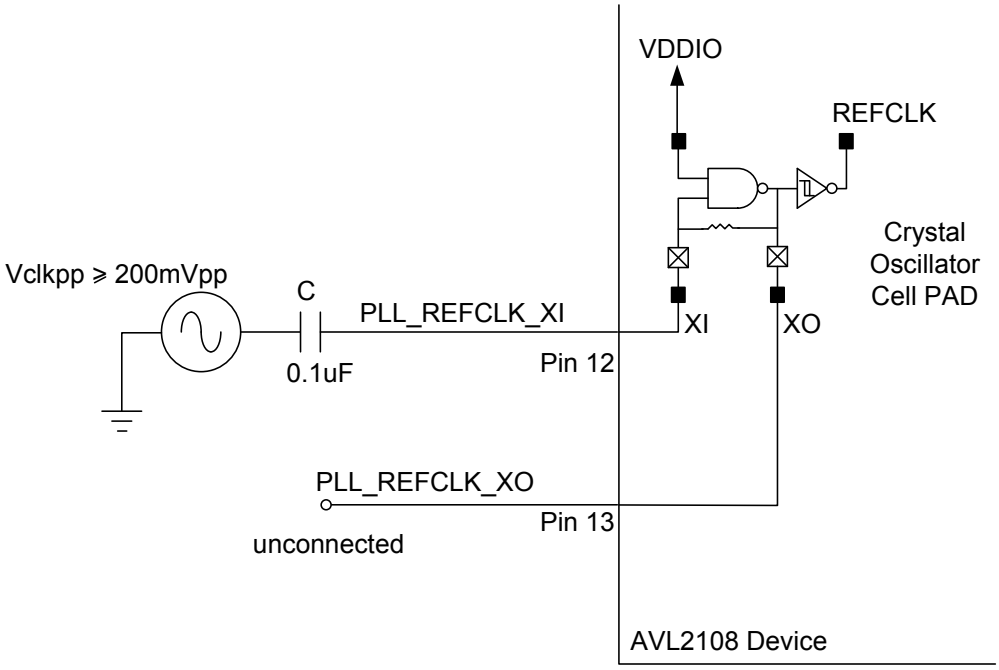
Note: If the clock source is from a Tuner device, then the Tuner device must be properly configured from the power-on-reset event. The AVL2108 device requires a stable clock in order to boot up and in turn communicate to the Tuner device via the I2C interface.

Finally after selecting a clock frequency the designer must configure the AVL2108 LOCK pin, as specified in Table 4-1. For example, selecting a 27 MHz fundamental frequency, the LOCK pin requires a 10k ohm pull up resistor to digital IO supply voltage.

8.1.3 External Clock Using Sine Wave Source

The AVL2108, PLL_REFCLK_XI input pin can be driven from the tuner crystal output. The tuner crystal output is a sine wave source. The diagram below shows how this clock source is connected to the AVL2108 device.

Figure 8-5 - Sine Wave Clock Input Source Circuit



The Sine Wave clock source should meet the following specifications:

- Tolerance overall: ±50 ppm
- Vclkpp ≥ 200mVpp

Select from one of the following frequencies:

- Frequency: 4 MHz, 4.5 MHz, 10 MHz, 16 MHz, or 27 MHz.

For this clock circuit option, the PLL_REFCLK_XO pin, (Pin 13), is left unconnected.

Note: If the clock source is from a Tuner device, then the Tuner device must be properly configured from the power-on-reset event. The AVL2108 device requires a stable clock in order to boot up and in turn communicate to the Tuner device via the I2C interface.

Finally after selecting a clock frequency the designer must configure the AVL2108 LOCK pin, as specified in Table 4-1.

8.2 Sample Power Supply Guidelines

A reference power supply circuit is shown in Figure 8-2. The board designer provides a 3.3 volt DC power supply input to the circuit. The power circuit generates four separate voltage supplies to the AVL2108 device:

- 1.2V_D that powers the core's digital logic. (Digital supply)
- 1.2V_PLL that powers the phase lock loop circuitry. (Analog supply)
- 1.2V_ADC that powers the Analog to Digital converter circuitry. (Analog supply)
- 3.3V_D that powers the digital inputs/outputs. (Digital supply)

Refer to Section 2 for the number of power inputs and grounds to the device.

IMPORTANT: As shown in Figure 8-2, a minimum 470uF capacitor (C1) is required on the AVL2108 1.2V digital supply, close to the AVL2108, to prevent VDDC below minimum during device step current transients.

8.3 AVL2108LG Device

The reference schematic shows the AVL2108LG part with a sample setup configuration. Specifically the part is implemented with a 10 MHz crystal and with the appropriate pull-down resistor configuration on the LOCK pin. For different input clock configurations that are supported by the device, refer to Table 3.

In addition, as shown in the reference design, the pins CS_0 and CS_1 are configured using a pull-down resistor. To understand the functionality and proper use of these two pins, refer to the pin description, Table 2.

The AVL2108LG part communicates and connects to a variety of other devices.

- The Tuner IC's differential inputs connect to ADC_IP/IN and ADC_QP/QN input pins. RFAGC output signal is connected to the Tuner. An I2C bus interfaces between the Tuner and the AVL2108LG part.
- A host processor and video device connect to the AVL2108LG device's I2C bus and MPEG bus respectively.
- The SLEEP, RESET and LOCK pins are connected to a host processor and used as control/status to/from the AVL2108LG part.
- After reset, the CS_1 and CS_0 pins can serve as general purpose IOs. However when RST_B is asserted, CS_1 and CS_0 serve as input signals. These input signals represent the LSbs of the I2C seven bit address bus.

8.3.1 RF AGC Filter Circuitry

The sample reference schematic shows the RF AGC output signal passing through two RC filters before connecting to the Tuner IC. It is advisable that the board designer adhere to the following rules when implementing the RC AGC filter circuitry:

- Place the first RC filter components, R20 and C44, close to the AVL2108LG part.

- Place the second RC filter components, R21 and C57, close to the Tuner IC.
- Use ground shielding on the RFAGC trace to reduce the interference from other signals.
- If possible, avoid the use of vias when routing the RFAGC trace.

8.4 Power Decoupling Capacitors

The sample reference design, Figure 8-2, shows the recommended number and size of the power decoupling capacitors.

In order to achieve superior AVL2108 device performance it is important to select a minimum 470uF capacitor (C1) and a minimum 1uF capacitor (C2). Both capacitors reside on the 1.2V digital supply and help prevent VDDC dropping below minimum levels during device step current transients.

8.5 PCB Routing Guidelines

This section provides the board designer with trace width and length guidelines for the wires that connect to/from the AVL2108LG device.

8.5.1 Tuner Differential Signal Routing

- Pair width, based on the tuner output impedance.
- I/Q pair spacing: >24 mils
- I/Q pair length matching: ± 200 mils.
- Differential pair, (i.e. IP/IN) length matching: ± 50 mils.
- Route differential pair, (i.e. IP/IN), close together to help maximize common-mode rejection.
- Use ground shielding for I and Q traces to prevent signal interference from surrounding traces.
- If possible, avoid use of via to route signal.

For more detailed PCB routing guidelines, refer to the 2108 evaluation board.

8.6 Sample Component List

The following table provides a summary of the key components used to build the sample reference design.

Table 8-1 - Key Schematic Components

Supplier	Part Number	Description
Texas Instrument	TPS64203DBV	A non synchronous step down controller that can be used for systems powered from a 5V or 3.3V bus.
Fairchild Semiconductor	FDC602P	P-Channel 2.5V specified MOSFET, used for power management applications.
Availink	AVL2108LG	DVB-S2/DVB-S Channel Receiver, used for satellite receiver applications.
Siward Crystal Technology Co., Ltd.	XTL021050J-10-12	10 MHz Crystal (clock), used in cable modems, network cards etc.
TDK Corporation	MMZ2012R601A	Inductor; sch. ref. no. L2, L3 and L5.
Steward a unit of Laird Technologies.	HI1206N101R-10	Inductor; sch. ref. no. L1.
Sumida Corporation	CDRH6D28-5R0	5uH Inductor; sch. ref. no. L4.
Diodes Incorporated	B320B	Schottky Rectifier diode
Susumu Co. Ltd	PRL1632-R036-F-T1	0.036 ohm Resistor. A low resistance value chip resistor use for high-precision current detection.

9 MECHANICAL SPECIFICATION

9.1 Mass

Total package weight at 0.5 ± 5% gram.

9.2 Package Outline

Figure 9-1 - 80 Pin LQFP

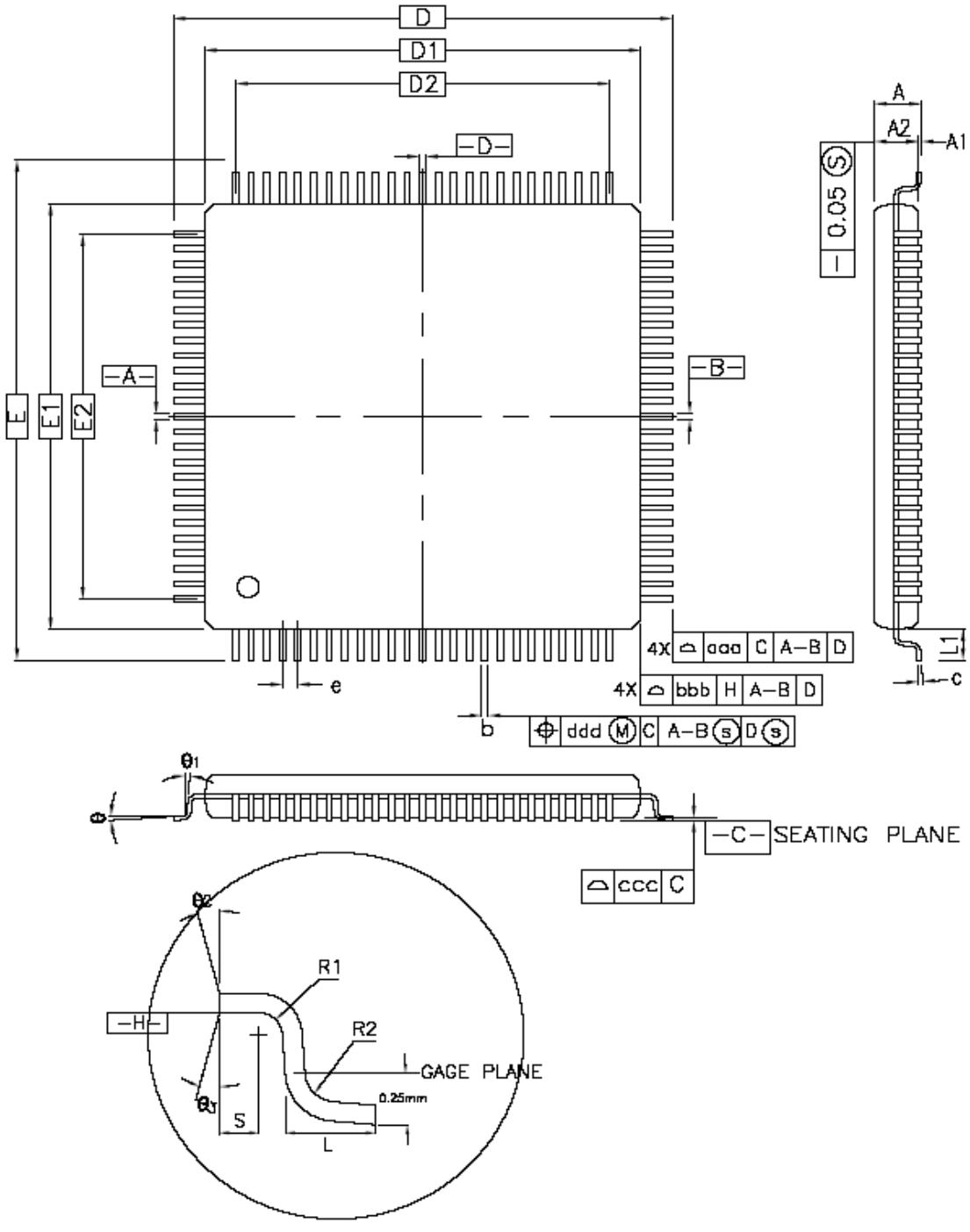


Table 9-1 - 80 Pin LQFP Dimension

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E1	12.00 BSC.			0.472 BSC.		
R2	0.08	-	0.20	0.003	-	0.008
R1	0.08	-	-	0.003	-	-
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	-	-	0.008	-	-
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.5			0.374		
E2	9.5			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Notes:

1. **DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.**
2. **DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm.**
3. **DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 mm AND 0.5 mm PITCH PACKAGES.**

9.3 Moisture Sensitivity

The package is compliant with Moisture Sensitivity Level 3 defined by IPC/JEDEC Standard J-STD-020C, July 2004, which means the maximum allowed floor life before soldering is 168 hours. Once this time is exceeded, a 24-hour bake at 125 °C is recommended to avoid the potential for structural damage during high temperature excursions due to residual moisture present in the package (popcorning).

9.4 Storage Condition

Calculated shelf life in sealed bag: 12 months at < 40 °C and < 90% Relative Humidity (RH)

10 ORDERING INFORMATION

Table 10-1 - Ordering Information

PART NUMBER	DESCRIPTION
AVL2108LG	80 pin LQFP (Pb-free/RoHS Compliant) (trays)
AVL2108LGa	80 pin LQFP (Pb-free/RoHS Compliant) (trays) with enhanced MPEG interface timing