AVL6211

DVB-S2/DVB-S Channel Receiver Data Sheet

Description

The AVL6211 is an enhanced version of the AVL2108 device. The AVL6211 is a highly integrated DVB-S2 and DVB-S channel receiver IC. It converts a baseband analog IQ signal from a satellite tuner and performs a set of sophisticated demodulating and decoding operations to output an MPEG video/audio stream. The AVL6211 provides simple and flexible control via a standard two-wire bus. A simplified block diagram of the device is shown in Figure 1-1.

The AVL6211 includes dual, differential, high performance, analog to digital converters (ADC) with a built-in compensation circuit for DC offset and IQ imbalance. An RF AGC output is provided for simple gain control of the satellite tuner via an RC network.

After passing a timing recovery loop and frequency recovery loop, the signal samples are further processed by an equalizer to output decision bits to an FEC decoder. The decoded bits are finally packetized in the MPEG interface block.

The configuration of the AVL6211 is easily performed through a set of registers via a standard two-wire bus. To simplify the interface to the host system, this same two-wire bus is used to communicate with the separate tuner two-wire bus and the DiSEqC™ interface to the LNB.

The AVL6211 can achieve fast acquisition at frequency offsets up to 5 MHz and maintains synchronization under the most severe front-end phase noise.

**Refer to Table 7-1

Applications

- Digital satellite receiver for standard and high definition TV
- High speed satellite data receiver

Features

- High performance QPSK/8PSK satellite TV receiver
- 64 pin LQFP in 7x7 mm package
- Low 250 - 270 mW power (clear sky)**
- Low 330 - 460 mW power (threshold)**
- DVB-S2:
  - Data Rate: QPSK 1-55 Msps
  - Data Rate: 8PSK 1-45 Msps
  - Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10
  - Roll-off factors for pulse shaping: 0.2, 0.25 and 0.35
- DVB-S:
  - Data Rate: 1-55 Msps
  - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Directly interfaces with tuner for easy implementation
- Integrated dual A/D converters
- Fast automatic blind scan of symbol rates and carrier frequencies
- Carrier frequency acquisition range: ±5MHz for symbol rates above 3 Msps and ±3MHz for the remaining symbol rates
- Signal quality and BER/PER monitors
- Equalizer compensates for channel impairment
- Standard two-wire serial bus with two selectable addresses for easy chip configuration
- Multi-purpose modulator for DiSEqC™ applications
- Standard MPEG-2 transport output parallel and serial interfaces
- Software controlled tri-state MPEG and RFAGC outputs
- Software controlled LNB interface (GPIOs)

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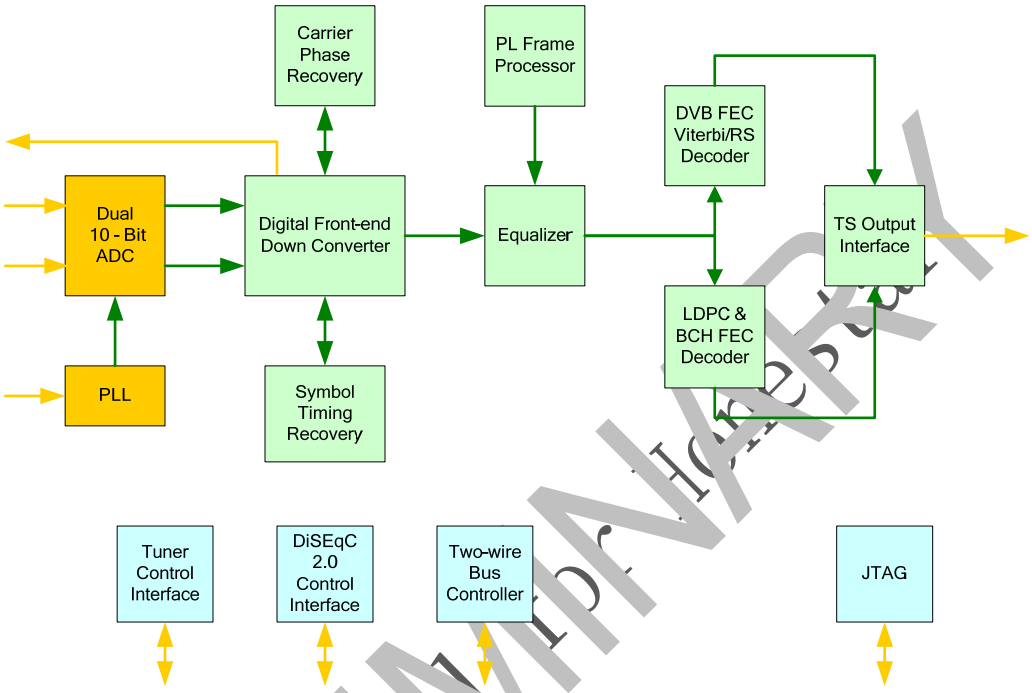
1 BLOCK DIAGRAM

Figure 1-1 - AVL6211 Block Diagram



2 PIN DEFINITION

Table 2-1 - Pin Type Definition

TYPE	DEFINITION
I	Input
O	Output, pin is always driven
BI	Bidirectional
OD	Open drain. Either driven low or held in Hi-Z
TRI	Tri-state. Either driven output or held in Hi-Z state.

Table 2-2 - Pin Definition

NAME	PIN	TYPE	DESCRIPTION
Signal Inputs			
ADC_IP ADC_IN	3 4	I	Analog in Phase Component
ADC_QP ADC_QN	7 8	I	Analog in Quadrature Component
Front End Controls			
PLL_REFCLK_XI	14	I	Reference clock input or crystal oscillator input
PLL_REFCLK_XO	15	O	Crystal oscillator output
RFAGC	16	TRI	Tri-state controlled through programmable user interface. RF analog gain control output (external RC Filter required)
SCL2	53	I/OD	2-wire bus clock to tuner front end; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SCL and 3.3V for proper operation
SDA2	54	I/OD	2-wire serial bus data for tuner front end; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SDA and 3.3V for proper operation

NAME	PIN	TYPE	DESCRIPTION
Others			
GPIO_CLK	18	BI	In normal operation mode, a general purpose clock output and general purpose IO. During reset, the pin is used to select reference clock frequency; when using a reference clock of 4 MHz, 4.5 MHz or 10 MHz, the input voltage level during reset MUST be lower than V_{IL} defined in Table 6-2; when using a reference clock of 16 MHz or 27 MHz, the input voltage level during reset MUST be higher than V_{IH} defined in Table 6-2.
LOCK	19	O	An output signal that is high when the receiver is locked and low otherwise.
SLEEP	49	I	Power down request input; When HIGH power down is requested. Held LOW for normal operation. Contact Availink for details on proper operation
SCL1	50	I/OD	Host 2-wire serial bus clock input; nominally a square wave with a maximum frequency of 400 kHz generated by the bus master; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SDA and 3.3V for proper operation
SDA1	51	I/OD	Host 2-wire serial bus data; the open-drain output requires a pull-up resistor (typically 2.7 kΩ) to be connected between SDA and 3.3V for proper operation
CS_0	61	BI	During reset the CS_0 input signal is the one LSb of the seven bit two-wire bus address. The remaining bits of the address are fixed internally to 000110, therefore the complete two-wire serial bus address is (MSB to LSB): 0,0,0,1,1, 0, CS_0. After reset, the pin serves as a general purpose IO. This pin must be pulled high or low and not left unconnected during reset.
RST_B	62	I	Active low digital device reset which holds device in inactive minimum power mode. Must be asserted for more than 18 reference clock input cycles for device reset to take effect as shown in Figure 6-6.

NAME	PIN	TYPE	DESCRIPTION
JTAG and Scan			
TDI	20	I	JTAG serial test data input; data is shifted in on the rising edge of TCLK. This signal can be tied to ground if not used and should not be left unconnected.
TDO	21	O	JTAG serial test data output; data is shifted out on the falling edge of TCLK, This signal can be left unconnected if not used.
TCLK	22	I	JTAG clock input. This signal can be tied to ground if not used and should not be left unconnected.
TMS	24	I	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCLK. Therefore, TMS should be set up before the rising edge of TCLK. This signal can be tied to ground if not used and should not be left unconnected.
TRST_N	25	I	Active-low input to asynchronously reset the boundary-scan circuit. This signal can be tied to ground if not used and should not be left unconnected.

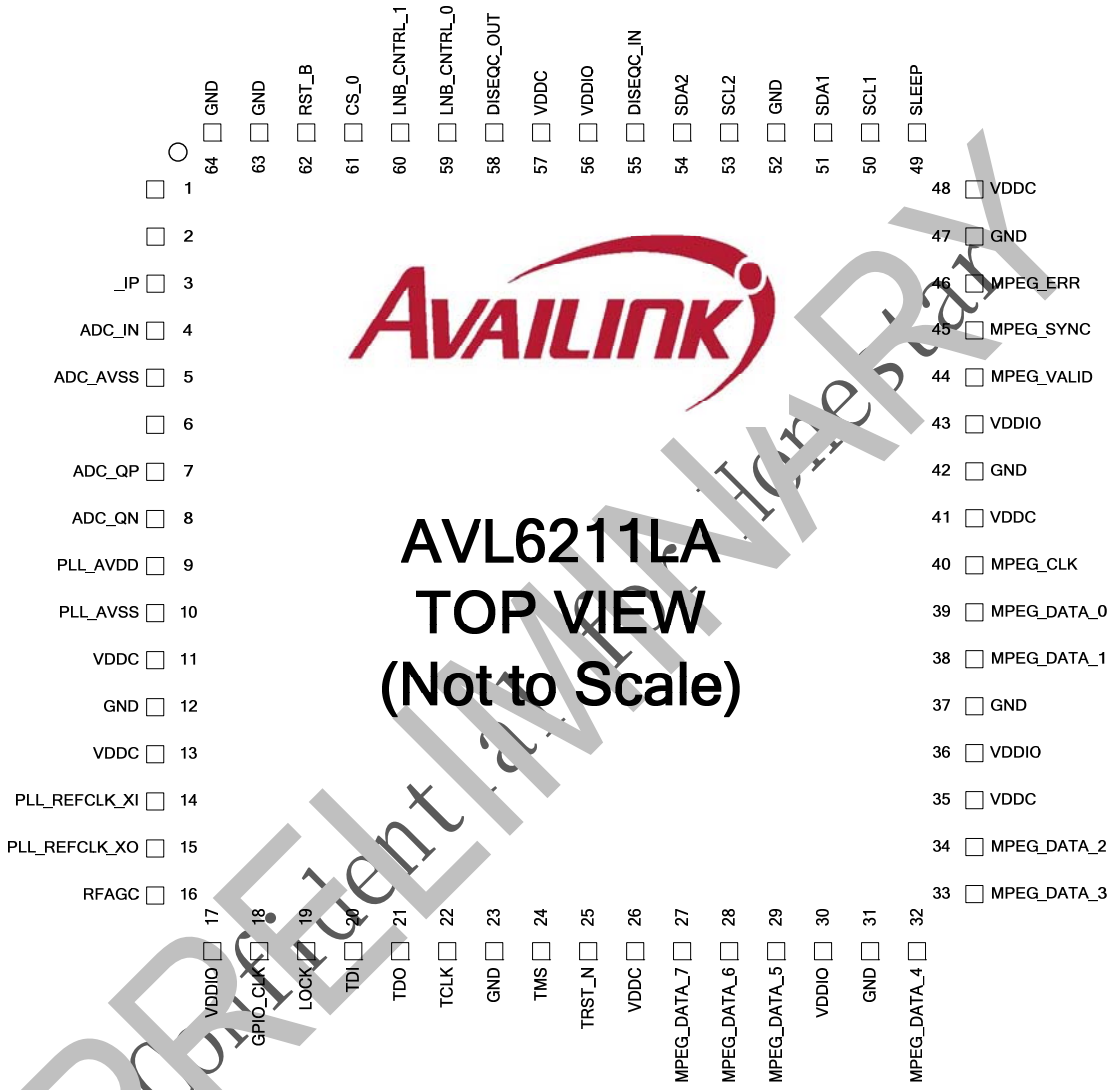
NAME	PIN	TYPE	DESCRIPTION
MPEG Outputs			
MPEG_DATA_7 MPEG_DATA_6 MPEG_DATA_5 MPEG_DATA_4 MPEG_DATA_3 MPEG_DATA_2 MPEG_DATA_1 MPEG_DATA_0	27 28 29 32 33 34 38 39	TRI	Tri-state controlled through programmable user interface. When configured as outputs: In parallel mode, MPEG transport packet data output. In serial mode, MPEG_DATA_7 or MPEG_DATA_0 are the serial data outputs. For more details refer to section 8.5.
MPEG_CLK	40	TRI	Tri-state controlled through programmable user interface. When configured as output: MPEG clock output at the data *byte* rate in parallel mode. In serial mode, output at the data *bit* rate Maximum period jitter is less than 10ns.
MPEG_VALID	44	TRI	Tri-state controlled through programmable user interface. When pin is configured as an output: Software configures the signal level (active high or low) to indicate valid bytes/bits detected. MPEG data output valid. Asserted during the MPEG_CLK cycles when valid data *bytes* are being output in parallel mode. In serial mode asserted during the MPEG_CLK cycles when valid data *bits* are being output
MPEG_SYNC	45	TRI	Tri-state controlled through programmable user interface. When configured as output: MPEG sync output signal goes HIGH during the MPEG_CLK each time the first *byte* of a packet is provided in parallel mode. In serial mode, MPEG sync output signal goes HIGH during the MPEG_CLK each time the first *bit* of a packet is provided
MPEG_ERR	46	TRI	Tri-state controlled through programmable user interface. When pin is configured as an output: Software configures the signal level (active high or low) to indicate a packet error detected.
LNB control			

DISEQC_IN	55	I	DiSEqC data encoding input; Polarity can be controlled by internal register
DISEQC_OUT	58	O	In normal operation mode serves as DiSEqC code output.
LNB_CNTRL_0	59	O	A digital output useful for controlling non-DiSEqC LNBs. The pin can be driven high or low. In a typical application, a low output would be used to set the LNB control voltage to 18 V, and a high output would be used to set the LNB control voltage to 13 V.
LNB_CNTRL_1	60	BI	General purpose IO. In a typical application the pin can be used to enable/disable a third party LNB controller device.

NAME	PIN	TYPE	DESCRIPTION
Power and Ground			
ADC_AVDD	1 6	SUPPLY	Analog supply voltage for the ADC (typically 1.2 V). All pins **must** be connected
PLL_AVDD	9	SUPPLY	Analog supply voltage for the PLL (typically 1.2 V)
ADC_AVSS	2 5	GROUND	Analog grounds for the ADC. All pins **must** be connected
PLL_AVSS	10	GROUND	Analog grounds for the PLL
VDDC	11 13 26 35 41 48 57	SUPPLY	Digital supply voltage (typically 1.2 V). All pins **must** be connected
VDDIO	17 30 36 43 56	SUPPLY	Digital supply voltage (typically 3.3 V). All pins **must** be connected
GND	12 23 31 37 42 47 52 63 64	GROUND	Digital ground. All pins **must** be connected

3 PIN CONFIGURATION

Figure 3-1 - Pin Configuration



4 POWER SEQUENCING AND RESET

4.1 Power Sequencing and Reset

ADC_AVDD (1.2V), PLL_AVDD (1.2V), VDDC (1.2V), VDDIO (3.3V) power supplies can be brought up in any order. However, the RST_B pin should be held low until the voltages reach the nominal values. The RST_B shall meet the requirement illustrated in Figure 6-6 - Reset and Mode Signal Timing.

4.2 Clock Frequency selection during Reset

During reset, GPIO_CLK pin indicates reference clock frequency as shown in the following table.

Table 4-1 - Reference Clock Selection

INPUT REFERENCE FREQUENCY[1]	GPIO_CLK PIN
4 MHz, 4.5 MHz or 10 MHz	Input voltage level lower than V_{IL} during reset
16 MHz or 27 MHz	Input voltage level higher than V_{IH} during reset

[1] If using reference clock other than the frequency listed in this table, please contact Availink for further details.

5 THERMAL CHARACTERISTICS

Estimated AVL6211 thermal performance is listed in the following table for several airflow and board construction conditions. These values may be dependent on environmental conditions, adjacent components, board materials, board construction, copper thickness, mounting effectiveness and other factors beyond Availink's control and cannot be guaranteed.

Table 5-1 - Thermal Characteristics

SYMBOL	PARAMETER	Airflow			UNIT	PCB CONDITIONS (JEDEC JESD51-9)
		0 m/s	1 m/s	2 m/s		
θ_{ja}	Thermal resistance from junction to ambient	74.4	61.5	57.0	°C/W	2 PCB layers
θ_{jc}	Thermal resistance from junction to case	17.1			°C/W	2 PCB layers
Ψ_{jt}	Junction to top characterization parameter	0.93			°C/W	2 PCB layers

6 ELECTRICAL CHARACTERISTICS

6.1 Test Conditions

Unless otherwise stated, the Min and Max values in Section 6.3 represent operation for 0C ≤ T_a ≤ 70C within the min/max voltage ranges listed. Where included, typical conditions reflect T_a = 25°C± 5°C, ambient humidity = 65% ± 10%, VDDIO = 3.3 V, ADC_AVDDC, PLL_AVDDC, and VDDC = 1.2 V.

6.2 Absolute Maximum Ratings[1]

Table 6-1 - Limiting Values

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDDC	Digital core supply voltage	-0.3	+1.32	V
VDDIO	Digital I/O supply voltage	-0.3	+3.6	V
ADC_AVDDC	ADC Analog core supply voltage	-0.3	+1.32	V
PLL_AVDDC	PLL Analog core supply voltage	-0.3	+1.32	V
V_i	Digital input voltage	-0.3	+3.6	V
VA_i	Analog input voltage	-0.3	+1.32	V
T_a	Ambient temperature	-10	+70	°C
T_j	Junction temperature	-40	+125	°C
T_s	Storage Temperature	-65	+150	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

6.3 Characteristics

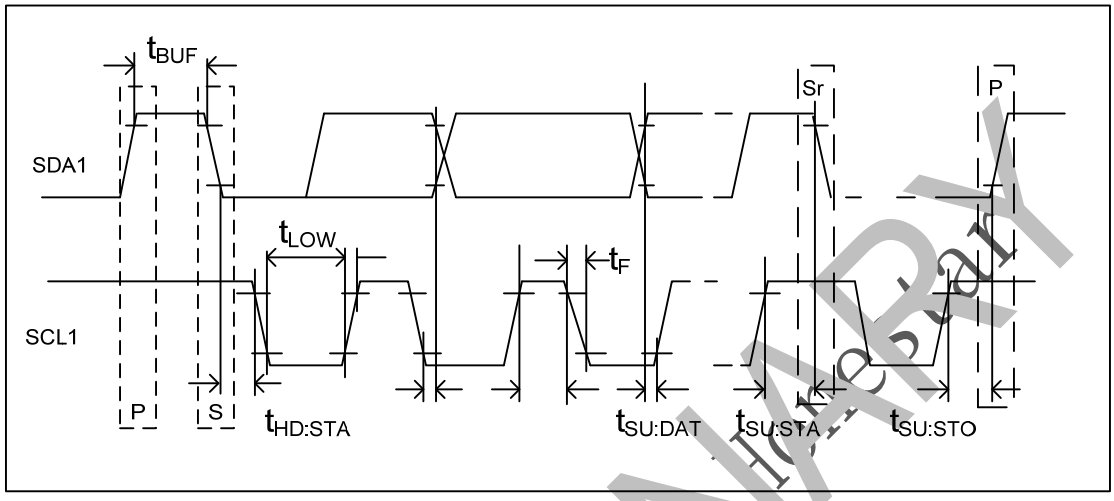
Table 6-2 - Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
VDDC	Digital core supply voltage		1.08	1.2	1.32	V
VDDIO	Digital I/O supply voltage		3.0	3.3	3.6	V
ADC_AVDD	ADC Analog core supply voltage		1.08	1.2	1.32	V
PLL_AVDD	PLL Analog core supply voltage		1.08	1.2	1.32	V
I_{DDC}	Digital core peak current			275		mA
I_{DDIO}	Digital I/O current			8		mA
$I_{ADC} + I_{PLL}$	1.2V Analog core current			111		mA
P_{SLEEP}	Average power in sleep mode			166		mW
$P_{INACTIVE}$	Average power inactive mode (RST_B held low)			54		mW
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
V_{OL}	Low level output voltage				0.4	V
V_{OH}	High level output voltage		2.4			V
Reference Clock Frequency						
f_{REF}	Reference clock frequency		4	10	27	MHz
ADC						
V_{FSR}	Analog input differential voltage range	FSCTRL Register = 00		±750		mV
V_{FSR}	Analog input differential voltage range	FSCTRL Register = 11		±375		mV
	Input impedance, differential					pF
	Input resistance, differential (Excluding ESD protection and package)			10		kΩ

6.4 Timing Characteristics

6.4.1 Host 2-Wire Bus Timing

Figure 6-1 - Host 2-Wire Bus Timing



Where: S = Start
Sr = Restart, i.e., Start without stopping first.
P = Stop

Table 6-3 - Host 2-Wire Bus Timing

Parameter: Host 2-wire bus only	Symbol	Value		Unit
		Min.	Max.	
SCL1 clock frequency	f_{CLK}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1300		ns
Hold time (repeated) START condition	$t_{HD:STA}$	600		ns
LOW period of SCL1 clock	t_{LOW}	1300		ns
HIGH period of SCL1 clock	t_{HIGH}	600		ns
Set-up time for a repeated START condition	$t_{SU:STA}$	600		ns
Data hold time (when input)	$t_{HD:DAT}$	0		ns
Data set-up time	$t_{SU:DAT}$	100		ns
Rise time of both SCL1 and SDA1 signals	t_R	20+0.1Cb[2]	300[3]	ns
Fall time of both SCL1 and SDA1 signals, (100pF to ground)	t_F	20+0.1Cb[2]	300[3]	ns
Set-up time for a STOP condition	$t_{SU:STO}$	600		ns

[2] Cb = the total capacitance on either clock or data line in pF.
[3] The rise time depends on the external bus pull-up resistor and bus capacitance.

6.4.2 MPEG Interface Timing

Figure 6-2 - MPEG Interface Timing In Parallel Mode with Falling Edge Clock

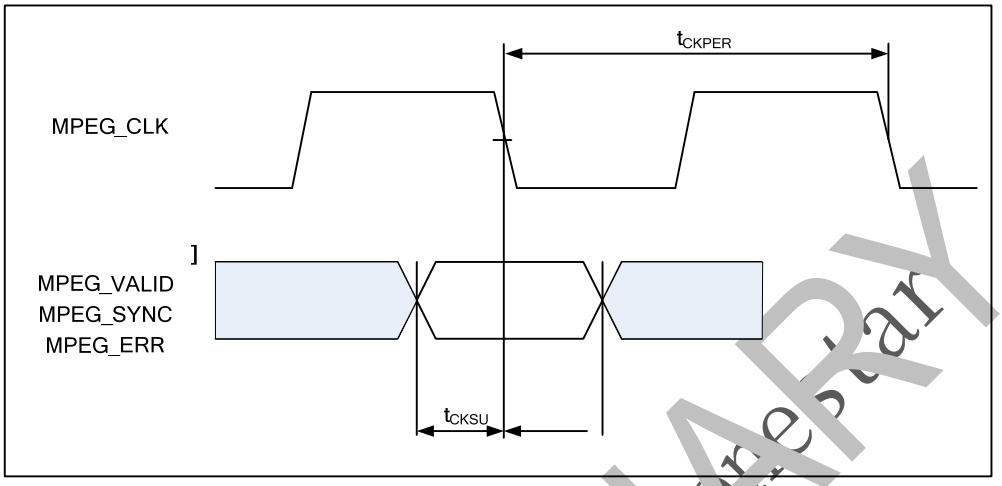


Table 6-4 - MPEG Interface Timing In Parallel Mode with Falling Edge Clock Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK falling edge	t_{CKSU}	28		ns
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK falling edge	t_{CKH}	28		ns
MPEG_CLK Parallel Mode Edge to Edge Time	t_{CKPER}	60		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. t_{CKPER} represents the minimum MPEG_CLK period in parallel mode in 8PSK modes with pilot on and all QPSK modes.

Figure 6-3 - MPEG Interface Timing In Parallel Mode with Rising Edge Clock

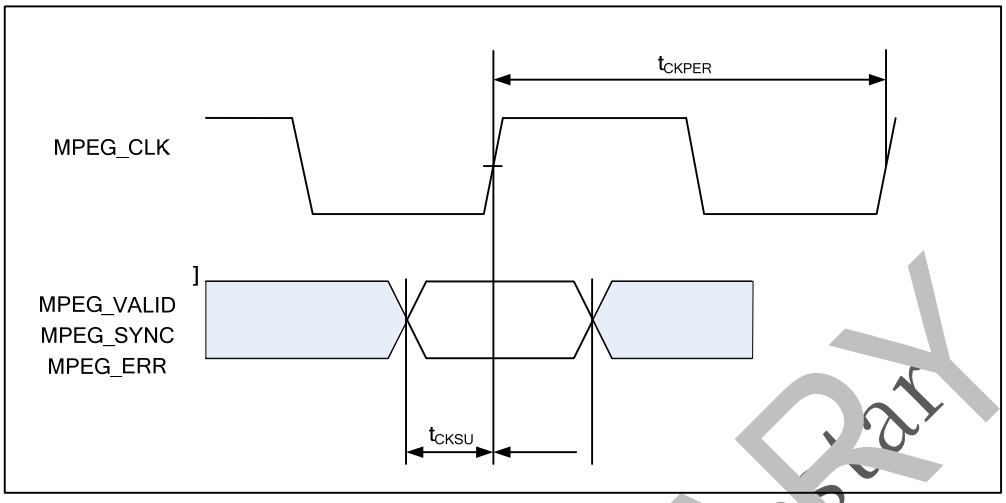


Table 6-5 - MPEG Interface Timing In Parallel Mode with Rising Edge Clock Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK rising edge	t_{CKSU}	28		ns
MPEG_DATA_[7:0], MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK rising edge	t_{CKH}	28		ns
MPEG_CLK Parallel Mode Edge to Edge Time	t_{CKPER}	60		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. t_{CKPER} represents the minimum MPEG_CLK period in parallel mode in 8PSK modes with pilot on and all QPSK modes.

Figure 6-4 - MPEG Interface Timing In Serial Mode with Falling Edge Clock

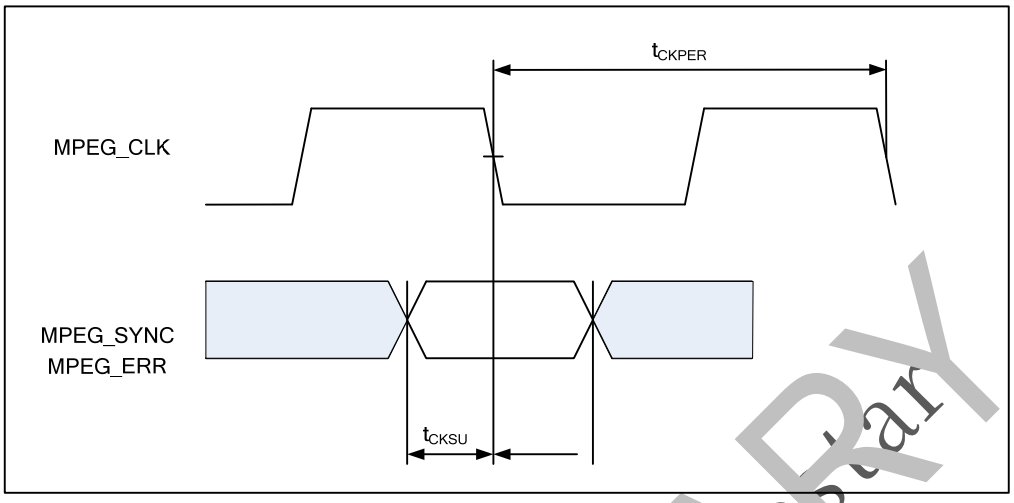


Table 6-6 - MPEG Interface Timing In Serial Mode with Falling Edge Clock Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK falling edge	t_{CKSU}	2.0		ns
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK falling edge	t_{CKH}	0.4		ns
MPEG_CLK Serial Mode Edge to Edge Time	t_{CKPER}	7.4		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. Serial mode limits the transport stream to 135 Mbps.

Figure 6-5 - MPEG Interface Timing In Serial Mode with Rising Edge Clock

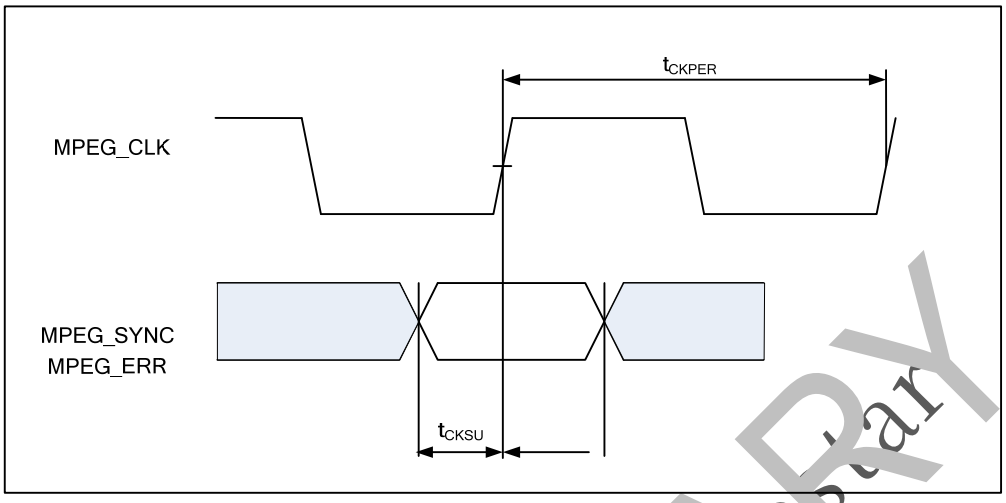


Table 6-7 - MPEG Interface Timing In Serial Mode with Rising Edge Clock Timing

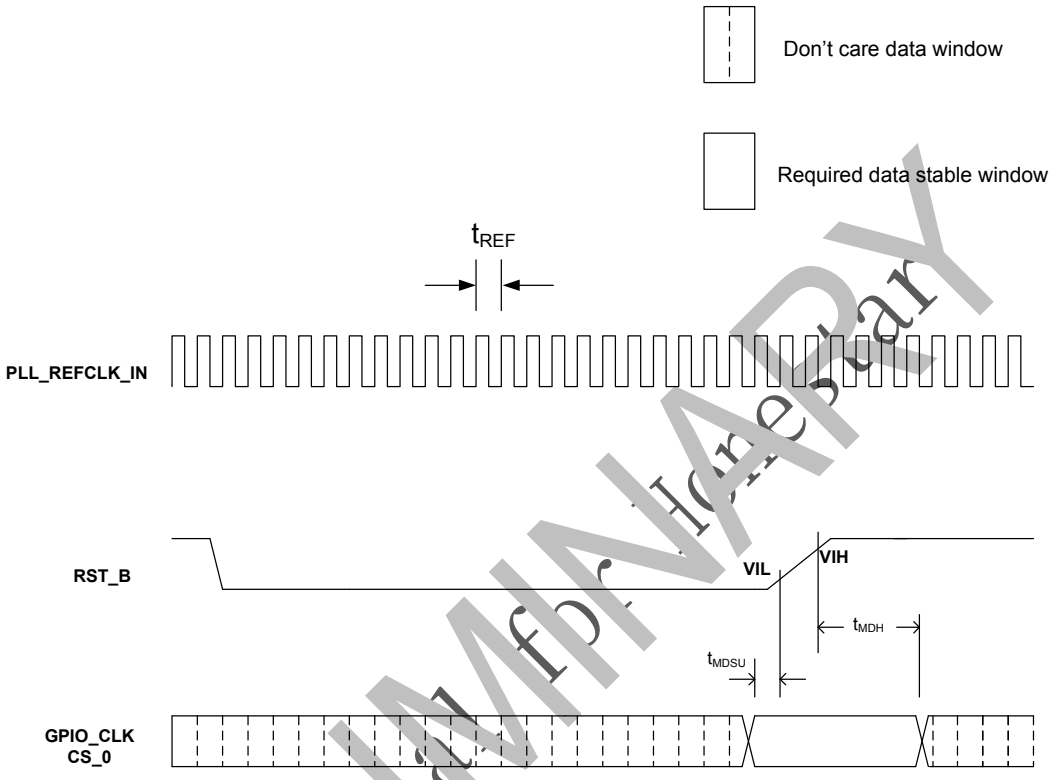
Parameter	Symbol	Value		Unit
		Min.	Max.	
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable before MPEG_CLK rising edge	t_{CKSU}	2.1		ns
MPEG_DATA_7, MPEG_VALID, MPEG_SYNC, MPEG_ERR stable after MPEG_CLK rising edge	t_{CKH}	0.4		ns
MPEG_CLK Serial Mode Edge to Edge Time[2]	t_{CKPER}	7.4		ns

Notes on Timing

1. t_{CKSU} and t_{CKH} are measured from the 1.5 Volt point of the MPEG_CLK to the 30%/70% level of the output swing with a load of 12 pF.
2. Serial mode limits the transport stream to 135 Mbps.

6.4.3 Reset and Mode Signal Timing

Figure 6-6 - Reset and Mode Signal Timing



Note: RST_B must be asserted for > 18 t_{REF} cycles

Table 6-8 - Reset and Mode Signal Timing

Parameter	Symbol	Value					Unit
PLL_REFCLK_IN Clock Frequency		4	4.5	10	16	27	MHz
PLL_REFCLK_IN Clock Period	t_{REF}	250	222	100	63	37	ns
Minimum GPIO_CLK and CS_0 stable before RST_B rising edge	t_{MDSU}	250	222	100	63	37	ns
Minimum GPIO_CLK and CS_0 stable after RST_B rising edge	t_{MDH}	1000	888	400	252	148	ns

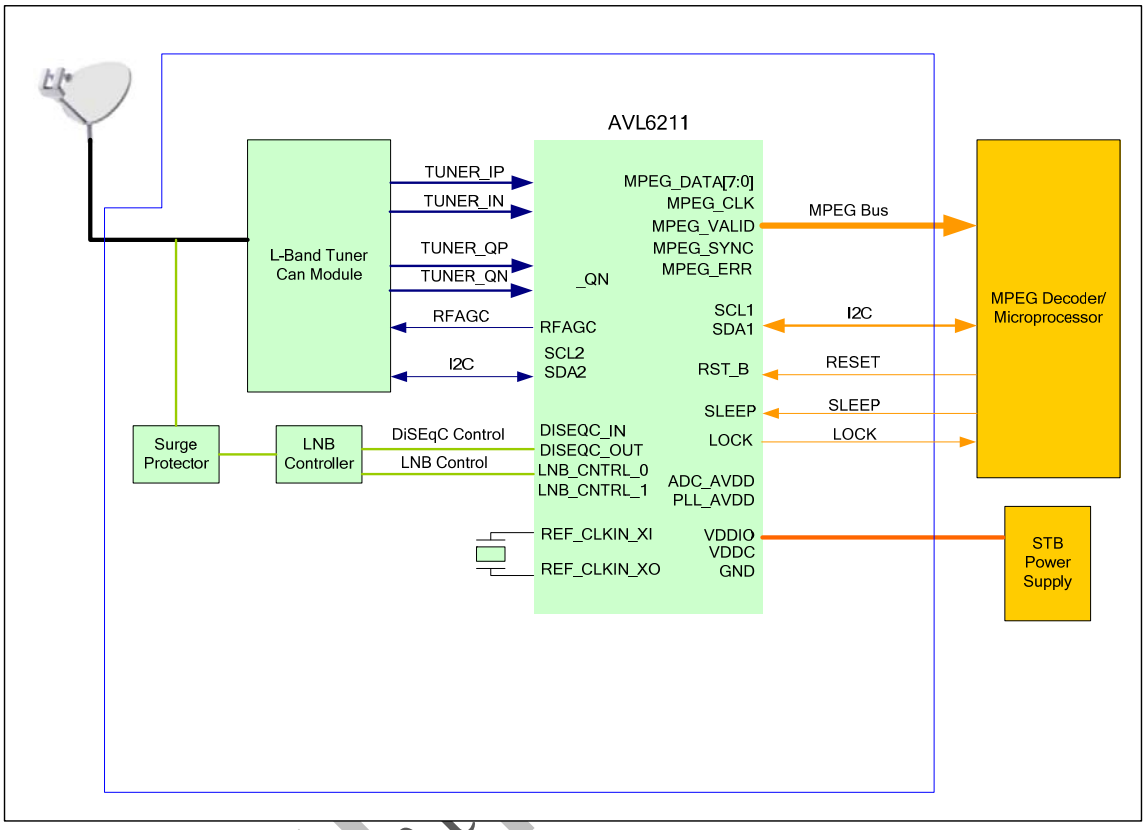
7 TYPICAL PERFORMANCE CHARACTERISTICS

Table 7-1 - AVL6211 Average Power, DVB-S2

Symbol Rate (Msps)	Clear Sky SNR (mW)	Threshold SNR (mW)
30	250 - 270	330 - 460
45	280 - 310	340 - 480

8 APPLICATION INFORMATION

Figure 8-1 - Typical Application



As shown in Figure 8-1, the AVL6211 device communicates with an L-Band Tuner intended for DVB-S2 set top box (STB) applications. The Tuner outputs a differential I/Q pair of signals which are then sampled within the AVL6211 device. The AVL6211 demodulates the signal and applies an advanced FEC algorithm on the data. The device then forwards an MPEG data stream to the adjacent MPEG decoder chip. The STB host controls the AVL6211 device and Tuner IC via an I2C Bus interface.

Availink Application Engineers can provide support and a sample reference design to assist the board designer with their specific application. In addition the following sub-sections provide the designer with guidelines to help construct their application schematic.

8.1 AVL6211 Device Interface

As shown in Figure 8-1 the AVL6211 device communicates and connects to a variety of other devices.

- The Tuner IC's differential inputs connect to ADC_IP/IN and ADC_QP/QN input pins. RFAGC output signal is connected to the Tuner. An I2C bus interfaces between the Tuner and the AVL6211 device.

- A host processor and video device connect to the AVL6211 device's I2C bus and MPEG bus respectively.
- The SLEEP, RESET and LOCK pins are connected to a host processor and used as control/status to/from the AVL6211 device.
- After reset, the CS_0 pin can serve as general purpose IOs. However when RST_B is asserted, CS_0 serves as input signal. The input signal represents the LSb of the I2C seven bit address bus.

8.1.1 RF AGC Filter Circuitry

Figure 8-2 - RFAGC Filter Circuitry

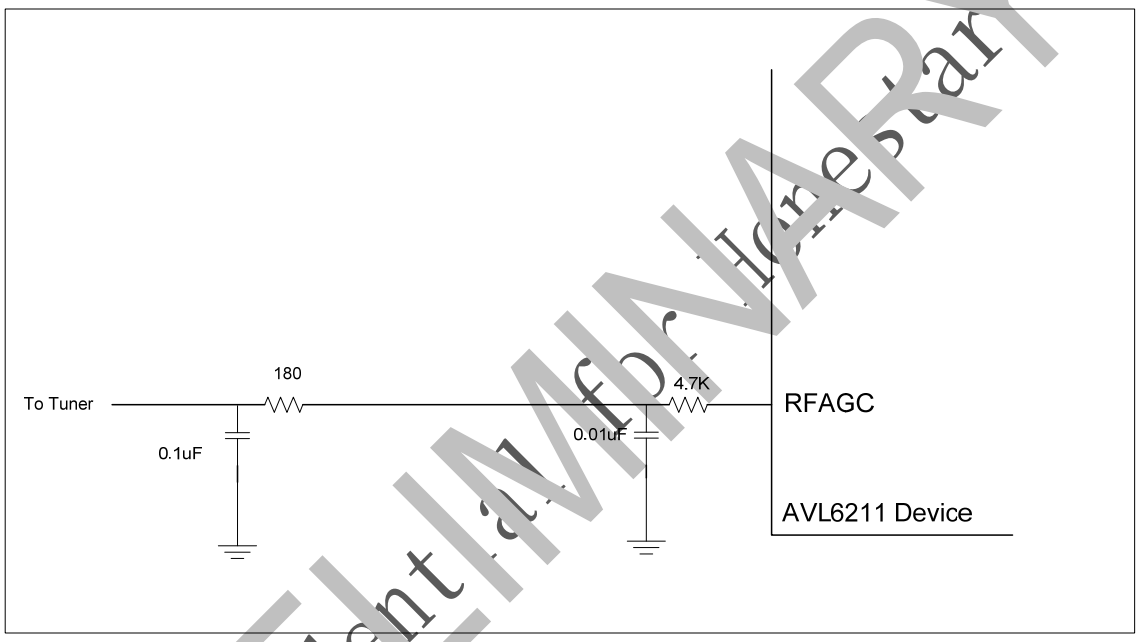


Figure 8-2 shows the RF AGC output signal passing through two RC filters before connecting to the Tuner IC. The RFAGC output signal is a digital pulse-width modulated signal and requires the low pass filters depicted in Figure 8-2 to convert the digital signal to an analog signal. It is advisable that the board designer adhere to the following rules when implementing the RC AGC filter circuitry:

- Place the first RC filter components, 4.7k ohm and 0.01uF, close to the AVL6211 part.
- Place the second RC filter components, 180 ohm and 0.1uF, close to the Tuner IC.
- Use ground shielding on the RFAGC trace to reduce the interference from other signals.
- If possible, avoid the use of vias when routing the RFAGC trace.

In addition the AVL6211 device supports a tri-state RFAGC output interface that is controlled by software. The tri-state RFAGC output feature allows tuner sharing among different demodulator devices.

The RFAGC signal defaults to tri-state during and after a chip reset event. After RST_B is de-asserted, the RFAGC output remains in tri-state until software programs the RFAGC pin as an output.

Note: The user should ensure that one and only one of the devices on the shared RFAGC bus drives at all times or the bus is pulled up or down. The shared bus should not be left floating between V_{IH} and V_{IL} or excess current draw may occur on the AVL6211 or the connected devices.

8.2 AVL6211 Clock Options

The AVL6211 device can accommodate three different clock circuit options. The board designer must be aware that it is important for overall chip performance to select a low jitter clock source. The designer can select from one of the following three clock sources:

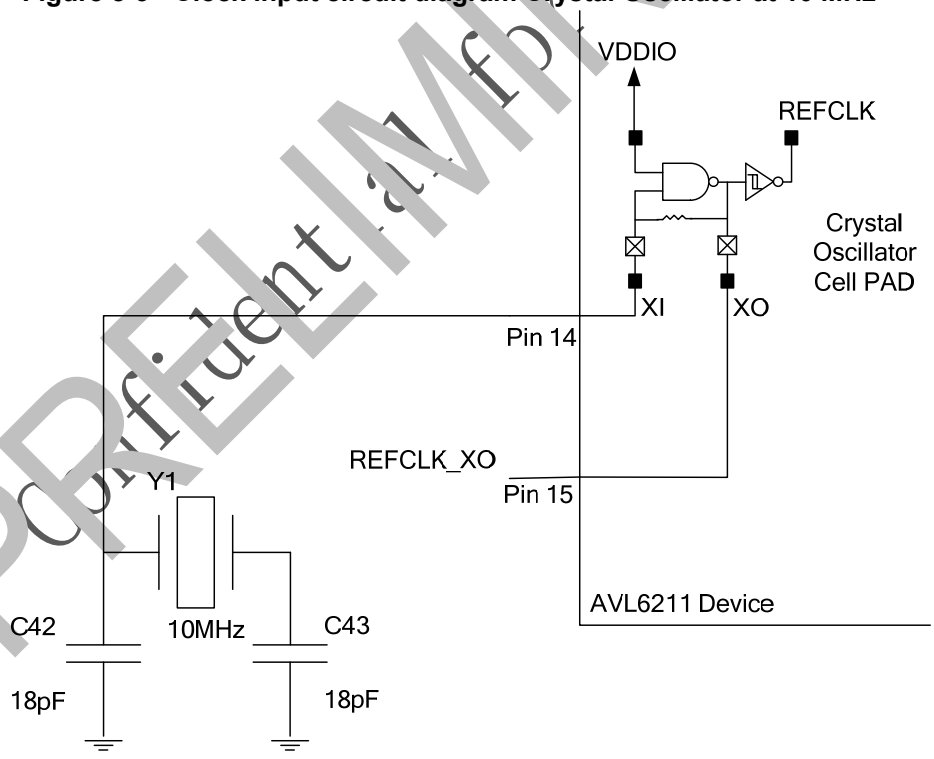
- Clock input using a crystal
- Use an external digital input clock
- Clock input using an external sine wave

The following sub-sections describe in detail each clock circuit option, clock frequency selection and tolerances.

8.2.1 Clock Input Using a Crystal

The AVL6211, PLL_REFCLK_XI input pin can be driven using a crystal oscillator source. The diagram below shows how such a circuit is implemented and connected to the AVL6211 device.

Figure 8-3 - Clock input circuit diagram Crystal Oscillator at 10 MHz



The clock circuit diagram shown in Figure 8-3 is used in the sample reference design. The crystal should meet the following specifications:

- Tolerance overall: ±50 ppm

- Nominal load capacitance: 12 pF
- Maximum equivalent series resistance: 160 ohms

Select from one of the following crystal resonant frequencies:

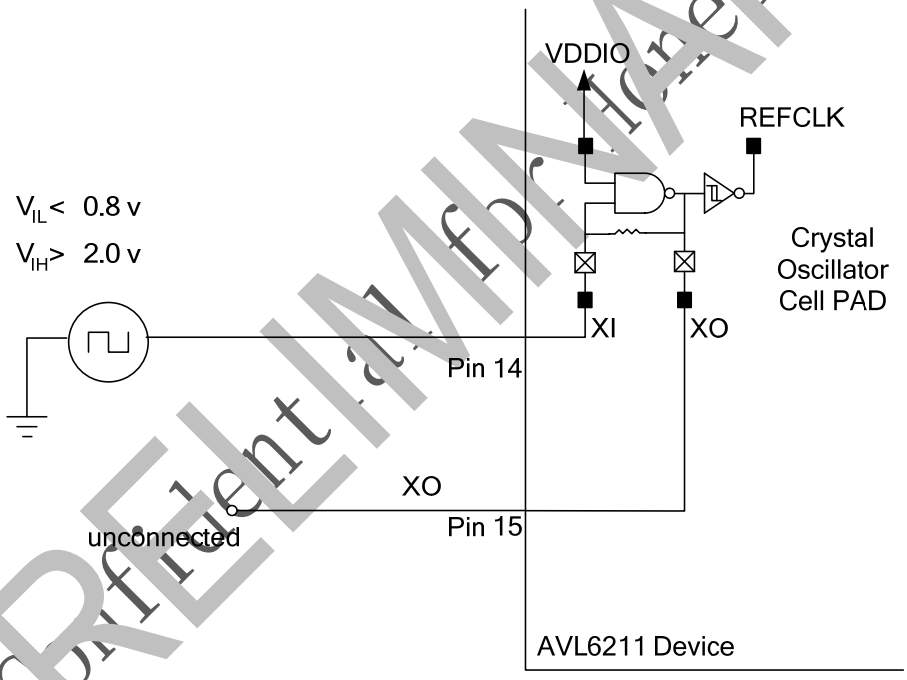
- Parallel resonant fundamental frequency: 4 MHz, 4.5 MHz, 10 MHz, 16 MHz, or 27 MHz.

After selecting a clock frequency the designer must configure the AVL6211 GPIO_CLK pin, as specified in Table 4-1. For example, selecting a 10 MHz crystal, the GPIO_CLK pin requires a 10k ohm pull down resistor to ground.

8.2.2 External Digital Input Clock

PLL_REFCLK_XI input pin can be driven by an external LVTTL level square wave clock. The diagram below shows how a LVTTL level square wave clock source is implemented and connected to the AVL6211 device.

Figure 8-4 - Square Wave Clock Input Source Circuit



The clock source should meet the following specifications:

- For LVTTL level square wave clock, it must meet V_{IL} and V_{IH} defined in Table 6-2.
- Tolerance overall: ±50 ppm

Select from one of the following frequencies:

- Frequency: 4 MHz, 4.5 MHz, 10 MHz, 16 MHz, or 27 MHz.

For this clock circuit option, the PLL_REFCLK_XO pin, (Pin 15), is left unconnected.

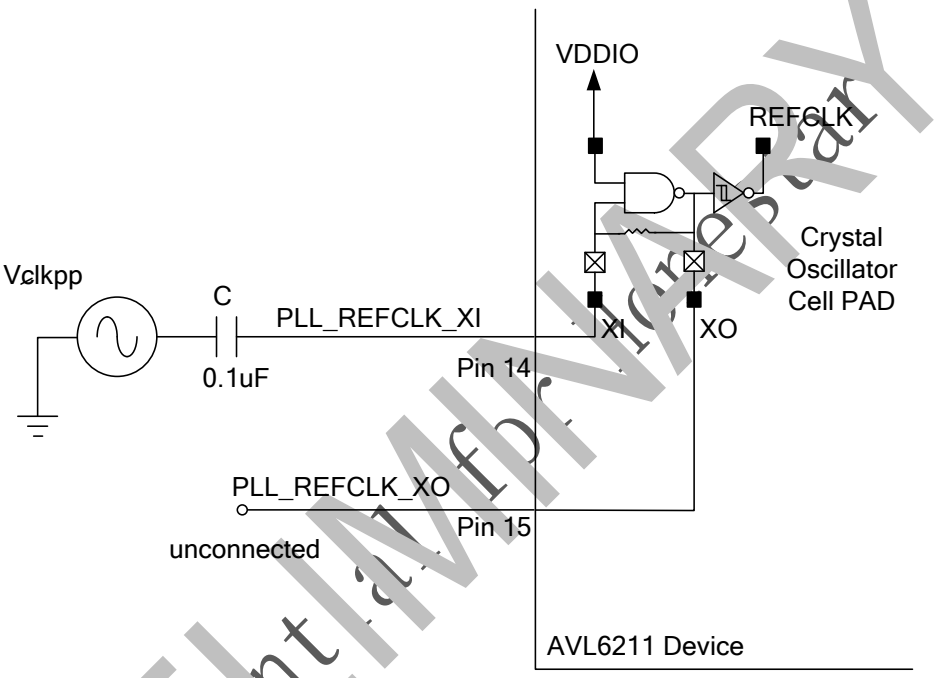
Note: If the clock source is from a Tuner device, then the Tuner device must be properly configured from the power-on-reset event. The AVL6211 device requires a stable clock in order to boot up and in turn communicate to the Tuner device via the I2C interface.

Finally after selecting a clock frequency the designer must configure the AVL6211 GPIO_CLK pin, as specified in Table 4-1. For example, selecting a 27 MHz fundamental frequency, the GPIO_CLK pin requires a 10k ohm pull up resistor to digital IO supply voltage.

8.2.3 External Clock Using Sine Wave Source

The AVL6211, PLL_REFCLK_XI input pin can be driven from the tuner crystal output. The tuner crystal output is a sine wave source. The diagram below shows how this clock source is connected to the AVL6211 device.

Figure 8-5 - Sine Wave Clock Input Source Circuit



The Sine Wave clock source should meet the following specifications:

- Tolerance overall: ±50 ppm
- Vclkpp ≥ 200mVpp

Select from one of the following frequencies:

- Frequency: 4 MHz, 4.5 MHz, 10 MHz, 16 MHz, or 27 MHz.

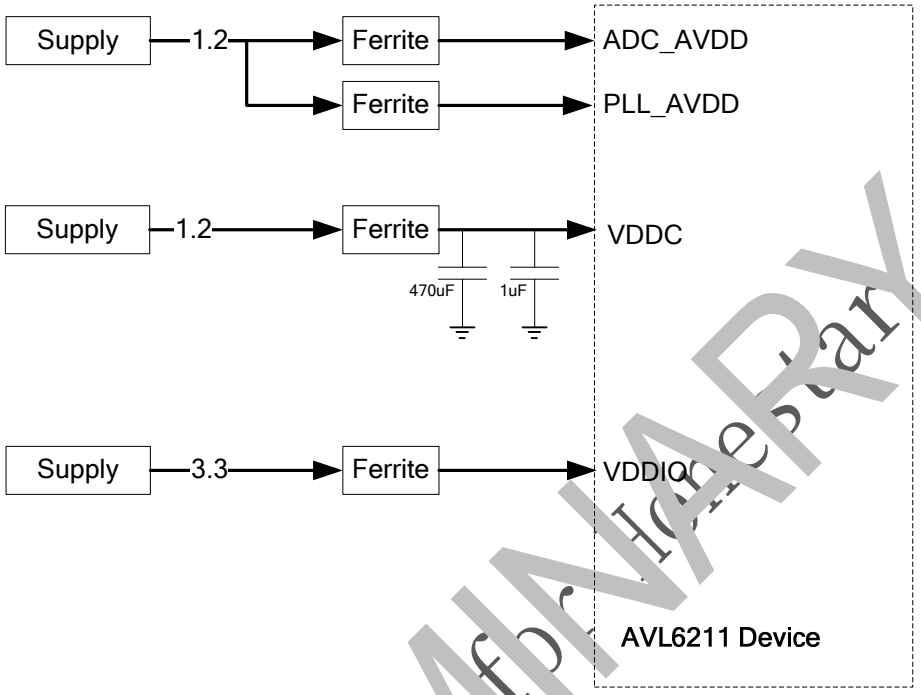
For this clock circuit option, the PLL_REFCLK_XO pin, (Pin 15), is left unconnected.

Note: If the clock source is from a Tuner device, then the Tuner device must be properly configured from the power-on-reset event. The AVL6211 device requires a stable clock in order to boot up and in turn communicate to the Tuner device via the I2C interface.

Finally after selecting a clock frequency the designer must configure the AVL6211 GPIO_CLK pin, as specified in Table 4-1.

8.3 Power Supply Circuitry

Figure 8-6 - Power Supply Circuitry



Each power pin requires a 0.1uF decoupling capacitor, which is not shown in above figure. In addition to the decoupling capacitor, in order to achieve superior AVL6211 device performance it is important to select a minimum 470uF capacitor and a minimum 1uF capacitor for VDDC. Both capacitors reside on the 1.2V digital supply and help prevent VDDC dropping below minimum levels during device step current transients. For best performance, it is recommended to place both 470uF and 1uF capacitors as close as possible to the AVL6211 device.

8.4 Power Decoupling Capacitors

Figure 8-7 - Power Decoupling Capacitors

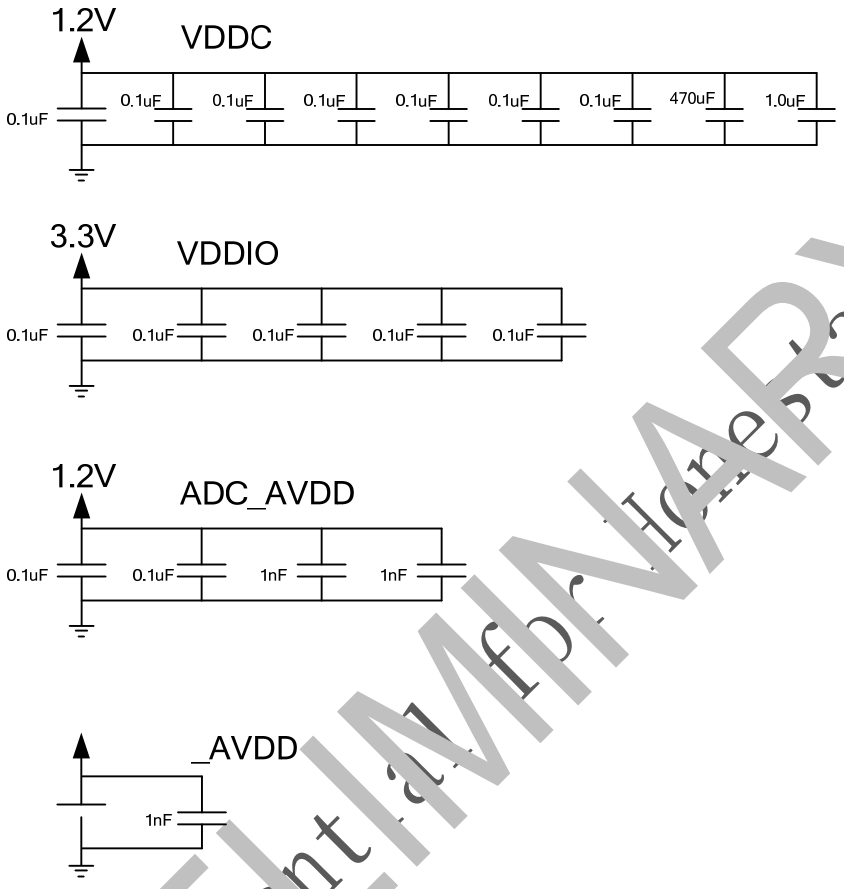


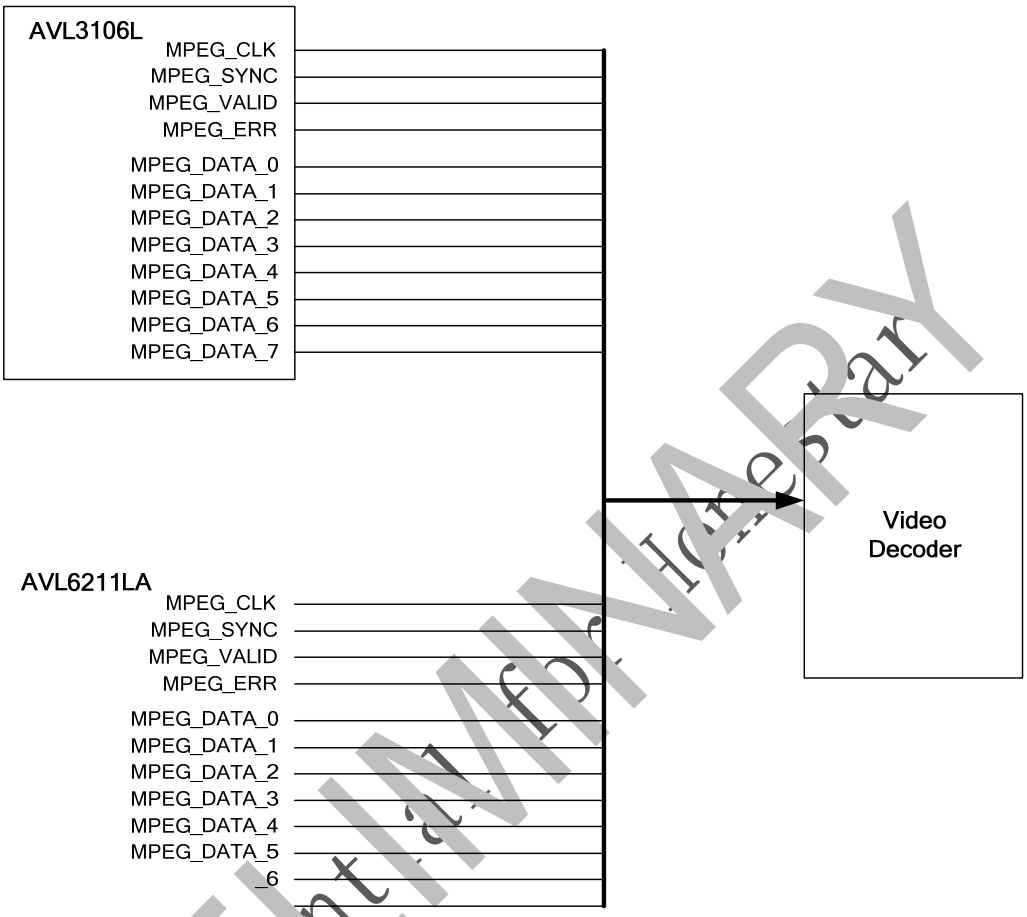
Figure 8-7 shows the recommended number and size of the power decoupling capacitors to be implemented on each power supply:

In addition, in order to achieve superior AVL6211 device performance it is important to select a minimum 470uF capacitor and a minimum 1uF capacitor to reside on the 1.2V digital supply. This will help prevent VDDC dropping below minimum levels during device step current transients. Figure 8-6 shows where the 470uF and 1uF capacitors are to be implemented.

8.5 MPEG Output Interface

The AVL6211 device supports a tri-state MPEG output interface that is controlled by software. The tri-state MPEG output feature allows MPEG bus sharing as shown in the diagram below. This enables two demodulator devices to share a common MPEG bus to a video decoder.

Figure 8-8 - AVL6211LA Shared MPEG Bus Configuration



The MPEG interface defaults to pull-down state during and after a chip reset event. When RST_B is asserted, the AVL6211 MPEG outputs are pulled low by an internal pull-down resistor. After RST_B is de-asserted the AVL6211 MPEG outputs remain in pull-down state until software programs the MPEG outputs to one of three states:

1. Configure to tri-state
2. Configure to output state
3. Configure to pull-down state

Note: The user should ensure that one and only one of the devices on the shared MPEG bus drives at all times or the bus is pulled up or down. The shared bus should not be left floating between V_{IH} and V_{IL} or excess current draw may occur on the AVL6211 or the connected devices.

8.6 PCB Routing Guidelines

This section provides the board designer with trace width and length guidelines for the wires that connect to/from the AVL6211 device.

8.6.1 Tuner Differential Signal Routing

- Pair width, based on the tuner output impedance.
- I/Q pair spacing: >24 mils
- I/Q pair length matching: ± 200 mils.
- Differential pair, (i.e. IP/IN) length matching: ± 50 mils.
- Route differential pair, (i.e. IP/IN), close together to help maximize common-mode rejection.
- Use ground shielding for I and Q traces to prevent signal interference from surrounding traces.
- If possible, avoid use of via to route signal.

For more detailed PCB routing guidelines, refer to the 6211 evaluation board.

9 MECHANICAL SPECIFICATION

9.1 Mass

Total package weight at 0.370 ± 5% gram.

9.2 Package Outline

Figure 9-1 - 64 Pin LQFP

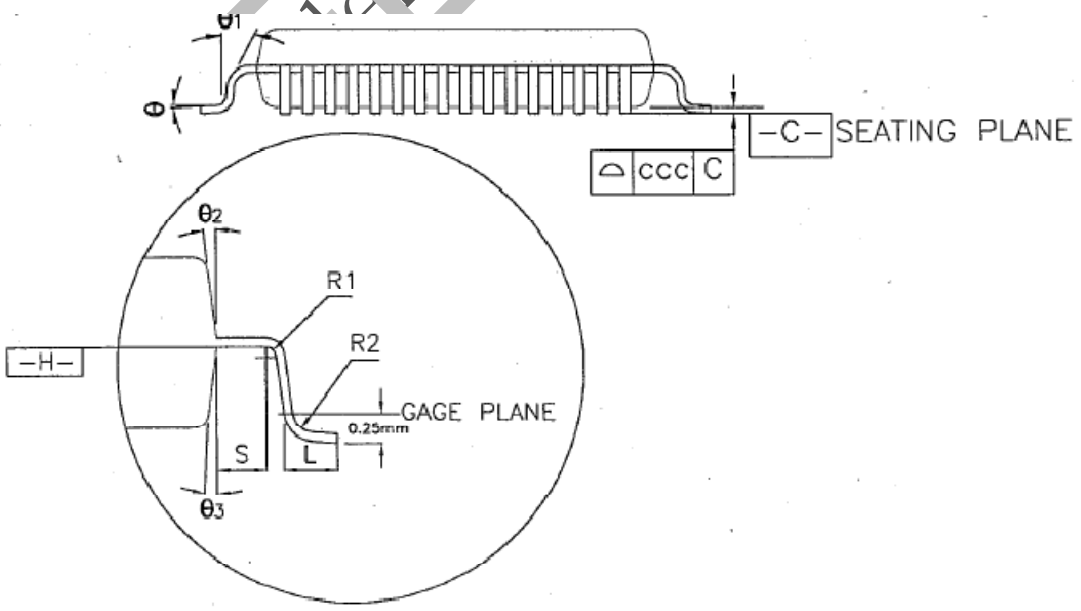


Table 9-1 - 64 Pin LQFP Dimension

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	-	0.20	0.003	-	0.008
R1	0.08	-	-	0.003	-	-
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	-	-	0.008	-	-
b	0.13	0.18	0.23	0.005	0.007	0.009
e	0.40 BSC.			0.016 BSC.		
D2	6.0			0.236		
E2	6.0			0.236		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Notes:

1. **DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.**
2. **DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 mm AND 0.5 mm PITCH PACKAGES.**

3. ALL DIMENSION OF 44L WERE BASE ON THOSE OF 48L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026

9.3 Moisture Sensitivity

The package is compliant with Moisture Sensitivity Level 3 defined by IPC/JEDEC Standard J-STD-020C, July 2004, which means the maximum allowed floor life before soldering is 168 hours. Once this time is exceeded, a 24-hour bake at 125 °C is recommended to avoid the potential for structural damage during high temperature excursions due to residual moisture present in the package (popcorning).

9.4 Storage Condition

Calculated shelf life in sealed bag: 12 months at < 40 °C and < 90% Relative Humidity (RH)

10 ORDERING INFORMATION

Table 10-1 - Ordering Information

PART NUMBER	DESCRIPTION
AVL6211LA	64 pin LQFP (Pb-free/RoHS Compliant) (trays).