AW-NH387

IEEE 802.11 b/g/n Wireless LAN & Bluetooth & FM Combo Module IC

For Mobile Phones, DSCs, PMPs and Gaming Devices

Datasheet

Version 0.5

Document release	Date	Modification	Initials	Approved
Version0.1	2010/01/04	Initial version	Max Huang	Ivan Chen
Version0.2	2010/02/09	Modify Sleep Clock description Add Power up timing sequence	Max Huang	Ivan Chen
Version0.3	2010/04/16	Modify Specification table and pin description	Max. Huang	Ivan Chen
Version0.4	2010/05/21	Modify output power of WiFi & BT	Max. Huang	Ivan Chen
Version0.5	2010/05/24	Define HT20&HT40 output power	Max. Huang	Ivan Chen

1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the first IEEE 802.11b/g/n WLAN & Bluetooth & FM combo module IC---**AW-NH387**. The module IC is targeted to mobile devices including **Mobile Phones, Digital Still Cameras (DSCs), Portable Media Players (PMPs), Personal Digital Assistants (PDAs), and Gaming Devices** which need small footprint package, low power consumption, multiple interfaces and OS support. By using AW-NH387, the customers can easily enable the Wi-Fi , BT and FM embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11b/g/n standard, the AW-NH387 uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-NH387. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-NH387 also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy(**WEP)** with Temporal Key Integrity Protocol(**TKIP**),Advanced Encryption Standard(**AES**)/Cipher-Based Message Authentication Code(**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-NH387 support **802.11e Quality of Service** (**QoS).**

For Bluetooth operation, AW-NH387 is **Bluetooth 3.0 + High Speed (HS) also complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR). Bluetooth 3.0 + HS** can make it **easier to connect devices, lower power consumption and improved security**.

AW-NH387 provides FM TX/RX function locating on 76-108MHz worldwide. FM bands supported and supports the **European Radio Data Systems (RDS)** and the **North American Radio Broadcast Data System (RBDS)** modulations

The AW-NH387 supports **SDIO** and **G-SPI** for WLAN to the host processor. **High speed UART, SDIO, PCM/Inter-IC Sound(I^{2}S)** interface are available to connect the BT core the host processor**.** For FM TX/RX, the device supports **I^{2}S**/analog stereo audio interfaces**.** An **I^{2}C**-compatible interface is available to connect FM Tx/Rx to the host processor, as well. FM Tx/Rx can also share the host interface with Bluetooth.

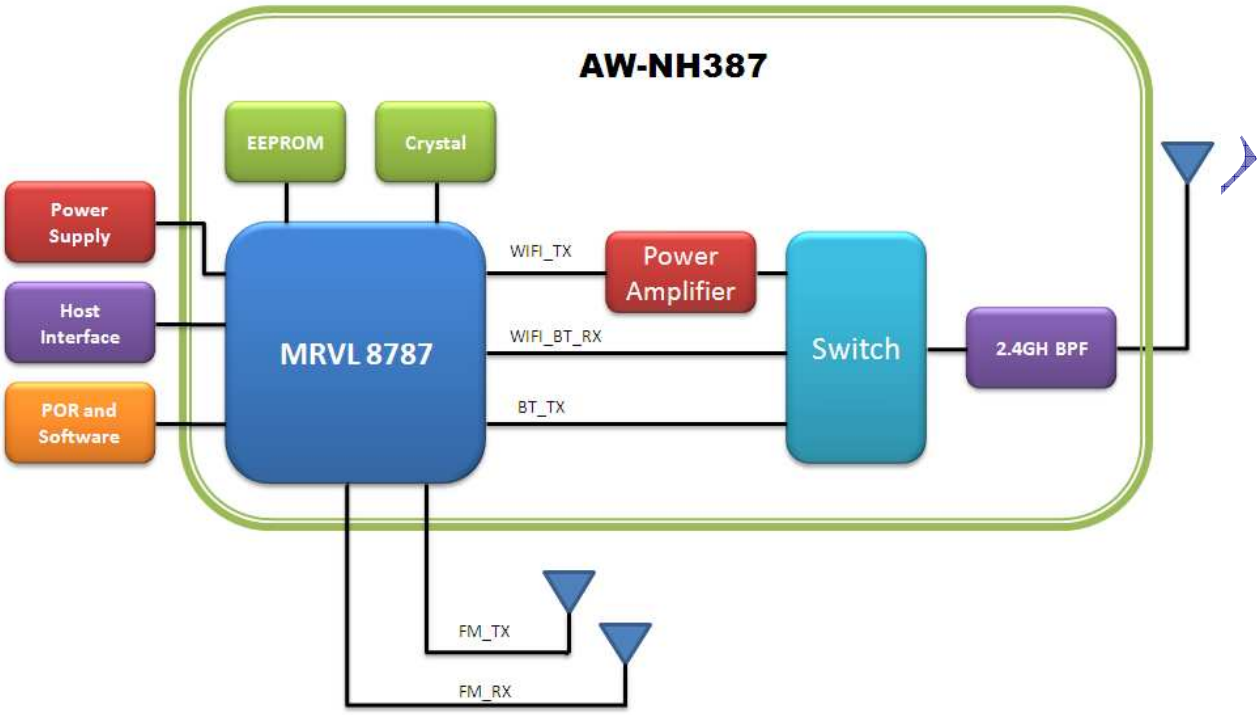
AW-NH387 is suitable for multiple mobile processors for different applications. With the support **cellular phone co-existence**, the AW-NH387 is also the best solution for mobile phones and PDA phones applications.

AW-NH387 module adopts Marvell's latest highly-integrated WLAN & Bluetooth SoC---**88W8787**. All the other components are implemented by all means to reach the mechanical specification required. AW-NH387 uses **IC module integration package** technology that provides customers mounting mechanism to secure the AW-NH387 module against vibration and shock on the host system. AW-NH387 uses module IC integration package technology can provide more **reliable** and **strong** electrical and mechanical performance.

1-2. Key Features

- **Small footprint: 9.6mm(L) x 9.6mm(W) x 1.2 mm(H)**
- **SDIO, G-SPI interfaces support for WLAN**
- **High speed UART,PCM/Inter-IC Sound(I^2S) and SDIO for Bluetooth**
- **SDIO, UART, GSPI and I2C for FM**
- **Bluetooth 3.0 + High Speed (HS) also complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR)**
- **Audio Codec interface support**
- **Cellular phone co-existence support**
- **Multiple power saving modes for low power consumption**
- **IEEE 802.11i for advanced security**
- **Quality of Service (QoS) support for multimedia applications**
- **Drip-in WLAN Linux drivers are Android ready and validated on Android based systems.**
- **Support for Linux kernel versions up to 2.6.32.**
- **Support for BlueZ v4.47 Bluetooth profiles stack used in Android Éclair**
- **Simultaneous AP-STA**
- **Support China WAPI**
- **Lead-free design**

A simplified block diagram of the AW-NH387 module is depicted in the figure below.



1-3. Specifications Table

Model Name	AW-NH387
Product Description	**Wireless LAN &Bluetooth & FM Combo Module IC**
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Bluetooth Standard	Bluetooth 3.0 +high speed complaint with Bluetooth 2.1+Enhanced Data Rate (EDR)
Host Interface	SDIO/G-SPI for WLAN UART,PCM/Inter-IC Sound(I^2S) and SDIO for Bluetooth SDIO/UART/I2C for FM
Major Chipset	Marvell 8787
Dimension	9.6mm x 9.6mm x 1.2mm
Weight	Less than 10 grams
Package	LGA
Operating Conditions	
Voltage	3.3V/2.6V/1.8V+/- 10%
Temperature	Operating: -20 ~ 70°C ; Storage: -40 ~ 85°C
Electrical Specifications	
Frequency Range	2.4 GHz ISM radio band
Number of Channels	802.11b: USA, Canada and Taiwan – 11 Most European Countries – 13 France – 4, Japan – 14 802.11g: USA, Canada and Taiwan – 11 Most European Countries – 13 Japan – 13 802.11n(HT20): Channel 1~14(2412~2484) 802.11n(HT40): Channel 1~7(2422~2472)
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM for WLAN GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth
Output Power	WLAN: 802.11b(Ch1~13): typical 17dBm +/- 2dBm 802.11b(Ch14): typical 10dBm +/- 2dBm 802.11g: typical 14dBm +/- 2dBm 802.11n: typical HT20 13dBm +/- 2dBm HT40 12dBm +/- 2dBm Typical power: Bluetooth Bluetooth Class 1.5>1dBm
Antenna	One WLAN/BT RF on pad One FM TX on pad One FM RX on pad
Receive Sensitivity	WLAN: 802.11b: Minimum -87dBm at 11Mbps 802.11g: Minimum -72dBm at 54Mbps 802.11n: Minimum -69dBm at HT20 MCS7 Minimum -66dBm at HT40 MCS7 Bluetooth: GFSK: typical -87dBm Π/4 DQPSK: typical -88dBm 8DPSK: typical -81dBm

Medium Access Protocol	**CSMA/CA with ACK**
Data Rates	**WLAN** **802.11b: 1, 2, 5.5, 11Mbps** **802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps** **802.11n up to 150Mbps** **Bluetooth** **Bluetooth 2.1+EDR data rates of 1,2, and 3Mbps**
Power Consumption	**Please reference Azurewave AW-NH387 power consumption test report**
Operating Range	**Open Space: ~300m ; Indoor: ~100m for WLAN** **Minimum 10 m indoor for Bluetooth** **The transmission speed may vary according to the environment)**
Security	◆ **WAPI** ◆ **WEP 64-bit and 128-bit encryption with H/W TKIP processing** ◆ **WPA/WPA2 (Wi-Fi Protected Access)** ◆ **AES-CCMP hardware implementation as part of 802.11i security standard**
Operating System Compatibility	**Win CE 5.0, Win Mobile 5.0/6.0, Linux, Pocket PC 2004/2005**
Co-Existence	**Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence**

2. Electrical Characteristics

2-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
3.3V_PA	PA power supply			3.3	4.6	V
VIO_X1	Host I/O power supply			1.8	2.3	V
				2.6	3.1	
				3.3	4.2	
VDD18_X3	Digital Signal power supply			1.8	1.98	V
VDD18A	Analog I/O power supply			1.8	2.3	V
VBAT	Internal voltage power supply			3.3	5.6	V

2-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
3.3V_PA	PA power supply		3	3.3	3.6	V
VIO_X1	Host I/O power supply		1.62	1.8	1.98	V
			2.5	2.6	2.7	
			2.97	3.3	3.63	
VDD18_X3	Digital Signal power supply		1.62	1.8	1.98	V
VDD18A	Analog I/O power supply		1.7	1.8	1.9	V
VBAT	Internal voltage power supply		2.3	3.3	4.8	V

2-3. Clock Specifications

AW-NH387 has internal reference clock source. The customer doesn't need to use external CLK.

2-3.1 External Sleep Clock Timing

External Sleep Clock is necessary for two reasons:

1. Auto frequency Detection.
   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 8787 what the ref clock input is.
2. Allow low current modes for BT to enter sleep modes such as sniff modes. Also provide optimized low power mode for FM Radio.

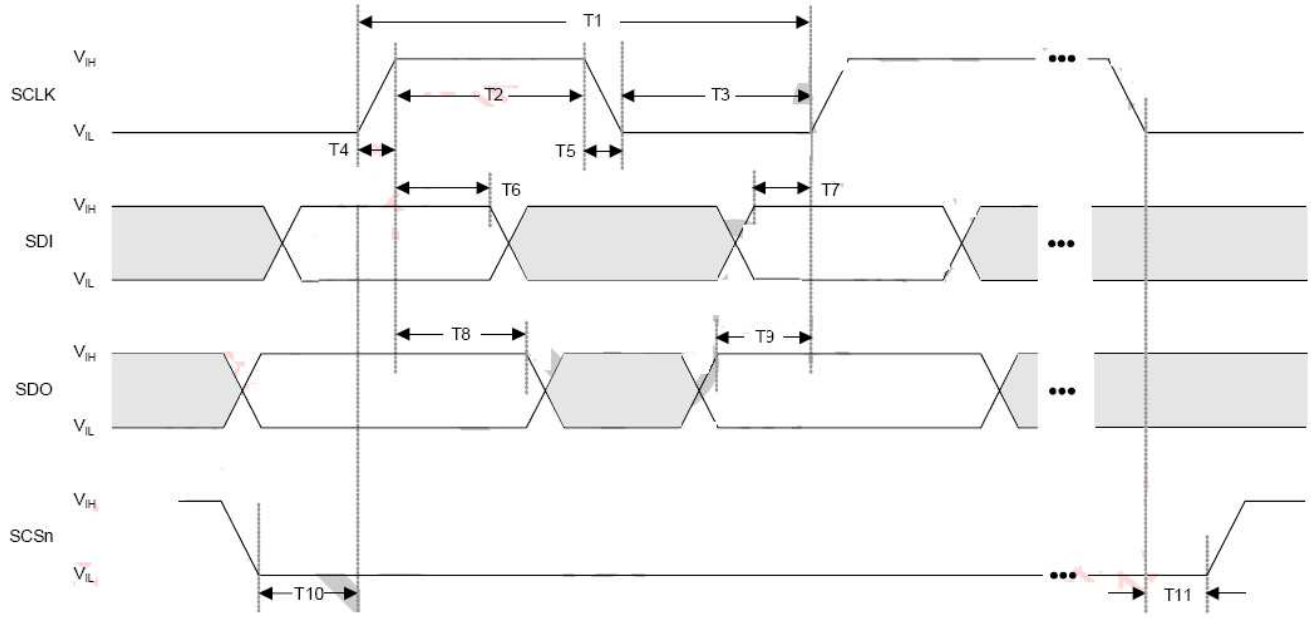
The AW-NH387 external sleep clock pin is powered from the 1.8V voltage supply.

Symbol	Parameter	Min	Typical	Max	Units
CLK	Clock Frequency Range	32 or 32.768 -50ppm	32 or 32.768	32 or 32.768 +50ppm	kHz
T_{HIGH}	Clock high time	40	--	--	ns
T_{LOW}	Clock low time	40	--	--	ns
T_{RISE}	Clock rise time	--	--	5	ns
T_{FALL}	Clock fall time	--	--	5	ns

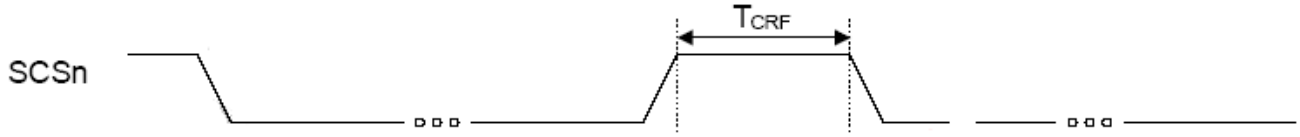
2-4. G-SPI Host Interface Specifications

Referred from Marvell hardware specifications

G-SPI Host Interface Transaction Timing



G-SPI Host Interface Inter-Transaction Timing

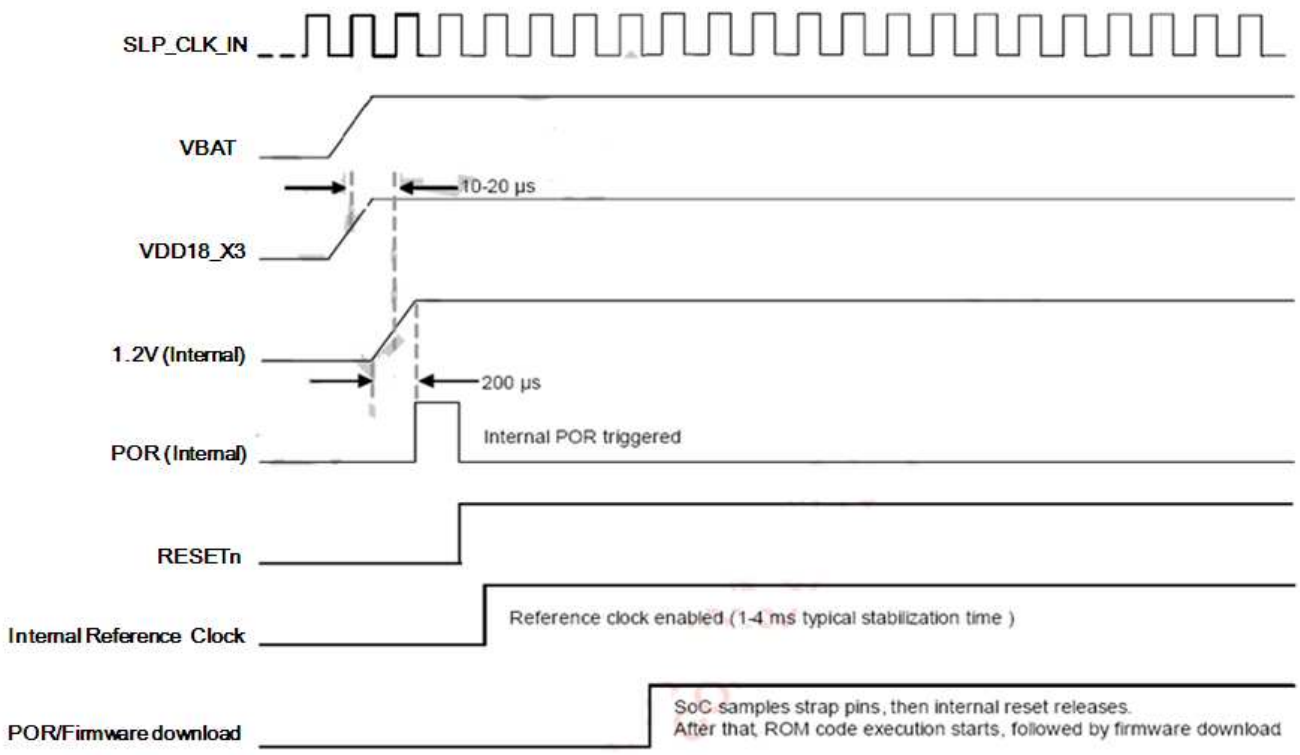


SPI Host Interface Timing Data

Over full range of values specified in the recommended operating conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T1	Clock Period		20			
T2	Clock high		5			
T3	Clock Low		9			
T4	Clock Rise Time				1	
T5	Clock Fall Time				1	
T6	SDI Hold Time		2.5			ns
T7	SDI Setup Time		2.5			
T8	SDO Hold Time		1			
T9	SCSn Fall to Clock		5			
T10	Clock to SCSn Rise		0			
T11	SCSn Rise to SCSn Fall	Delay Between transaction	4GBCLK/ HCLK^2			

2-5. Power Up Timing Sequence



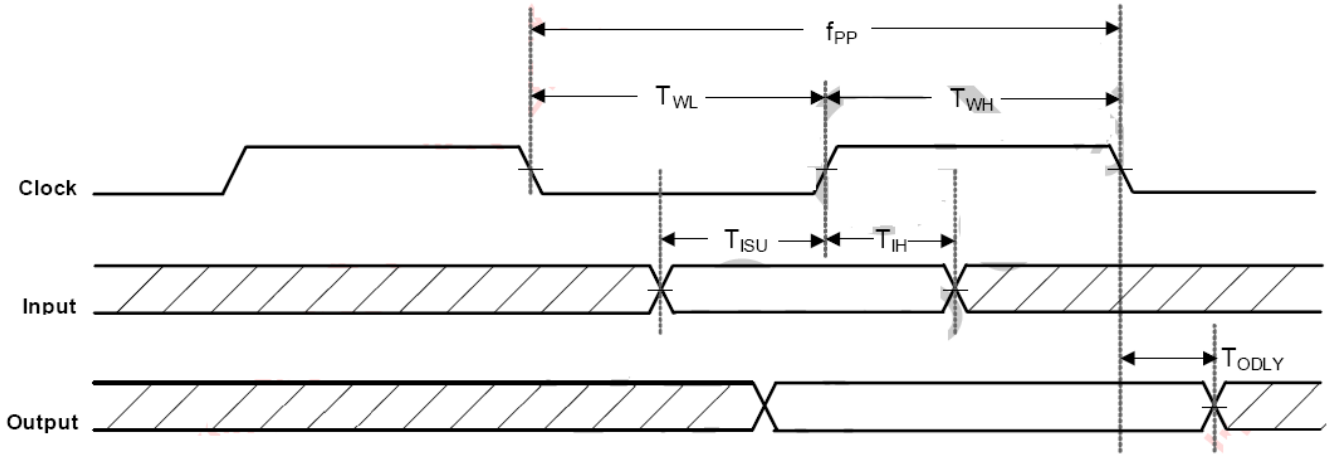
Note:

- For The auto reference clock calibration (frequency detection) to function properly. VBAT, VDD18_X3 and SLP_CLK_IN must be stable before 1.2V(Internal) is stable.
- The external sleep clock of 32.768 KHz must be used for reference clock calibration and low power applications.
- RESETn should be held asserted until all the power rails and SLP_CLK_IN are stable

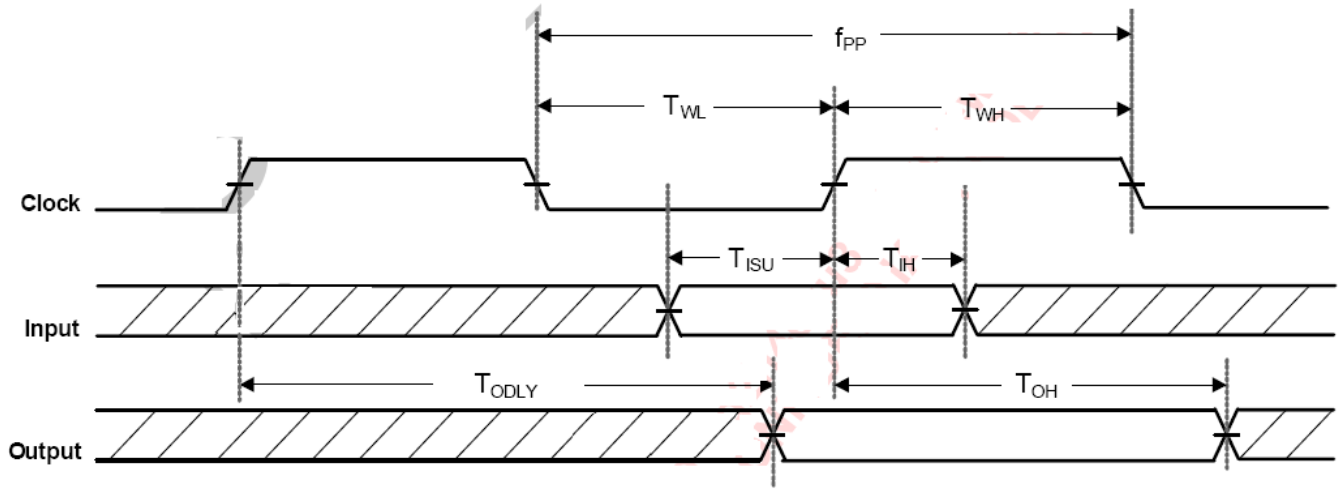
2-6. SDIO Host Interface Specifications

Referred from Marvell hardware specifications

SDIO Protocol Timing Diagram



SDIO Protocol Timing Diagram—High Speed Mode



SDIO Timing Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	Normal	0		25	MHz
		High Speed	0		75	
T_{WH}	CLK High Time	Normal	10			ns
		High Speed	7			
T_{WL}	CLK Low Time	Normal	10			
		High Speed	7			
T_{ISU}	Input Setup Time	Normal	5			
		High Speed	6			
T_{IH}	Input Hold Time	Normal	5			
		High Speed	2			
T_{ODLY}	Output Delay Time		0		7.33	
T_{OH}	Output Hold Time	High Speed	2.5			

2-7. UART Host Interface

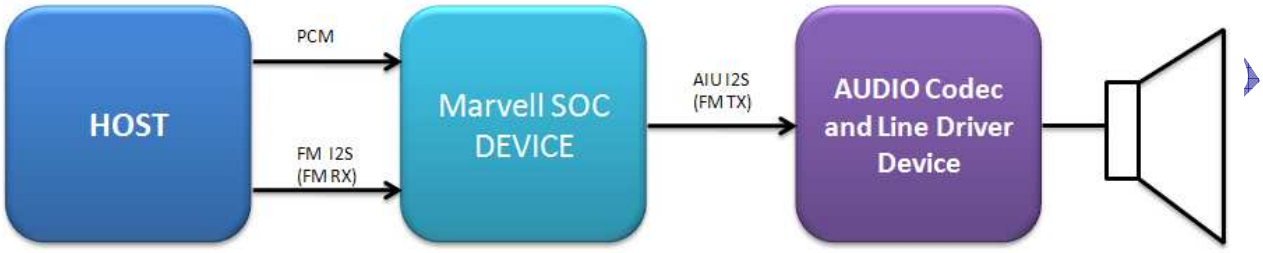
The AW-NH387 supports a high speed Universal Asynchronous Receiver/Transmitter (UART) interface. High speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. The table as below shows the rates supported.

UART baud rates supported

Baud Rate	UART Divisor
1200	1024
2400	512
4800	256
9600	128
19200	64
38400	32
57600	32
76800	16
115200	16
230400	8
460800	4
500000	4
921600	2
1000000	2
1382400	1
1500000	1
1843200	1
2000000	1
2100000	1
2764800	1
3000000	1
3250000	1
3692300	1
4000000	1

2-8. Audio CODEC Interface

The AW-NH387 supports two audio interfaces for simultaneous Bluetooth and FM audio traffic. Each interface can be programmed as I2S or PCM interface.



For applications in which the host connects both PCM and I2S on the same lines, the I2S and PCM interfaces share the same pins. In this case, either the PCM or the I2S interface may be used at a time. Please refer the below tables:

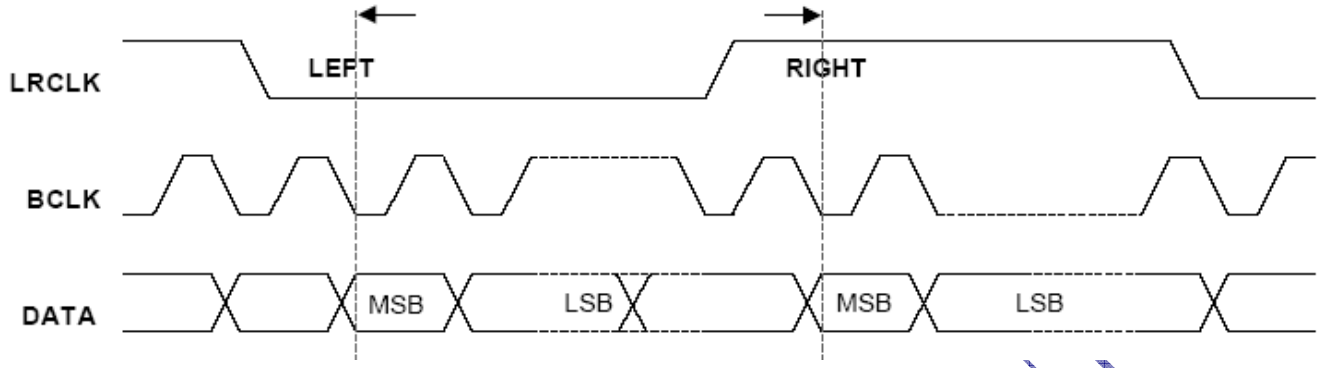
Pin Number	Pin Name	PCM Interface	AIU I2S Shared Interface	FM I2S Interface Shared with PCM
71	GPIO[15]	PCM_MCLK	I2S_CCLK	FM_I2S_CCLK
69	GPIO[14]	PCM_SYNC	I2S_LRCLK	FM_I2S_LRCLK
66	GPIO[13]	PCM_CLK	I2S_BCLK	FM_I2S_BCLK
28	GPIO[12]	PCM_DOUT	I2S_DOUT	FM_I2S_DOUT
73	GPIO[11]	PCM_DIN	I2S_DIN	FM_I2S_DIN

The I2S interface pins are also provided on the GPIO[23:20] pins for applications using PCM for voice and I2S for FM at the same time which shows in below table:

Pin Number	Pin Name	AIU I2S Shared Interface	FM I2S Separate
67	GPIO[23]	I2S_LRCLK	FM_I2S_LRCLK
5	GPIO[22]	I2S_DOUT	FM_I2S_DOUT
20	GPIO[21]	I2S_DIN	FM_I2S_DIN
23	GPIO[20]	I2S_BCLK	FM_I2S_BCLK

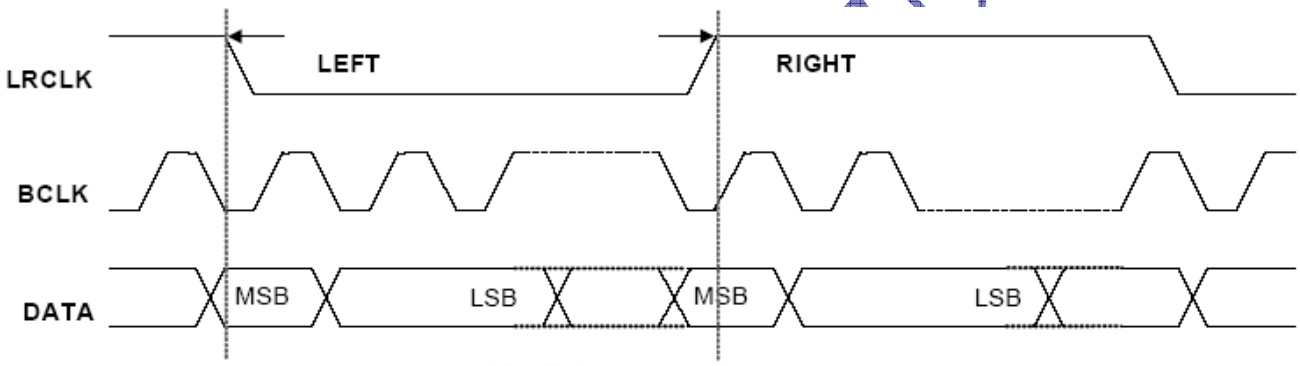
2-8-1.2 Protocol Description

2-8-1.2 .1 I²S interface Protocol

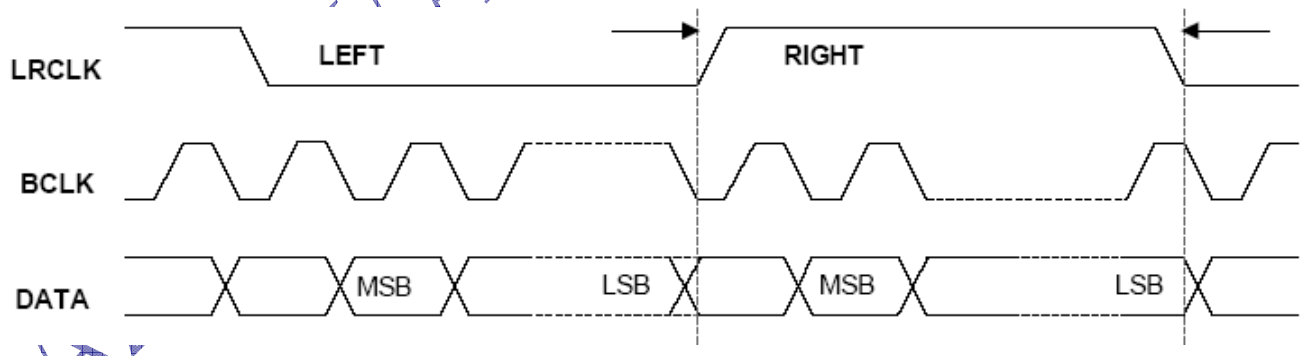


2-8-1.2 .2 Justified Protocol

MSB-Justified Protocol

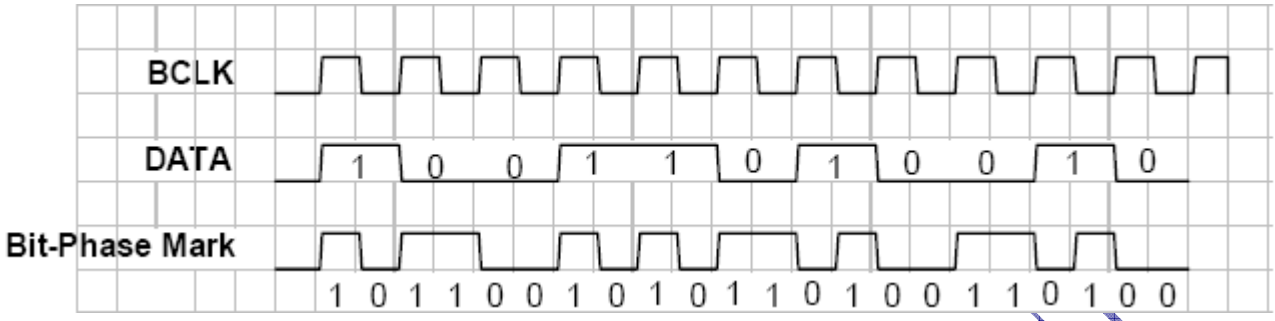


LSB-Justified Protocol

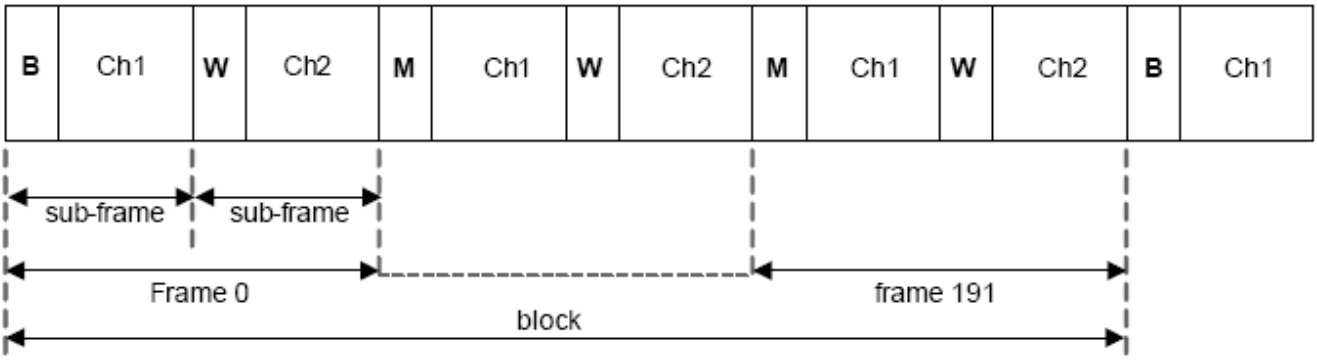


2-8-1.2 .3 IEC60958 Compatible Audio CODEC Interface Protocol

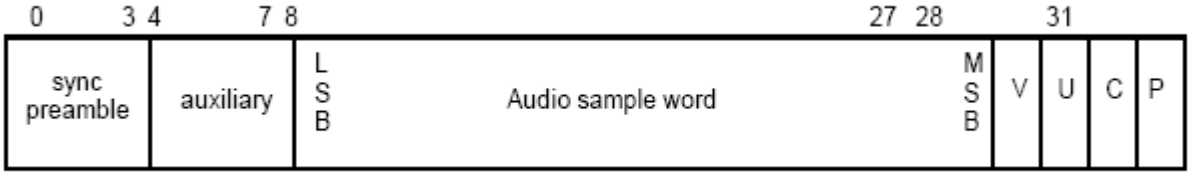
IEC60958 Compatible Audio CODEC Interface Encoding



IEC60958 Compatible Audio CODEC Interface Format Signal



IEC60958 Compatible Audio CODEC Interface Sub-Frame Format



IEC60958 Compatible Audio CODEC Interface Preambles

Preceding State	Channel Coding
B	11101000
M	11100010
W	11100100

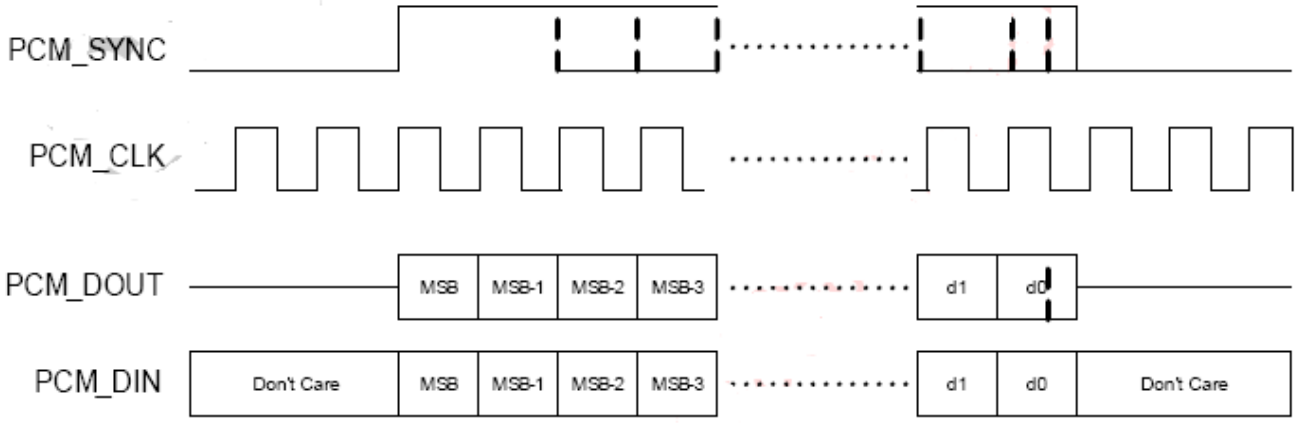
2-8-1.3 Clock Frequency and Audio Data Resolution.

Audio Data may arrive with different input data formats with different sampling rates. The AIU uses an audio input clock of 22.5792MHz, 24.576MHz, 11.285MHz, or 12.288MHz to provide the appropriate CCLK and BCLK frequency to match sampling rates of each audio data format.

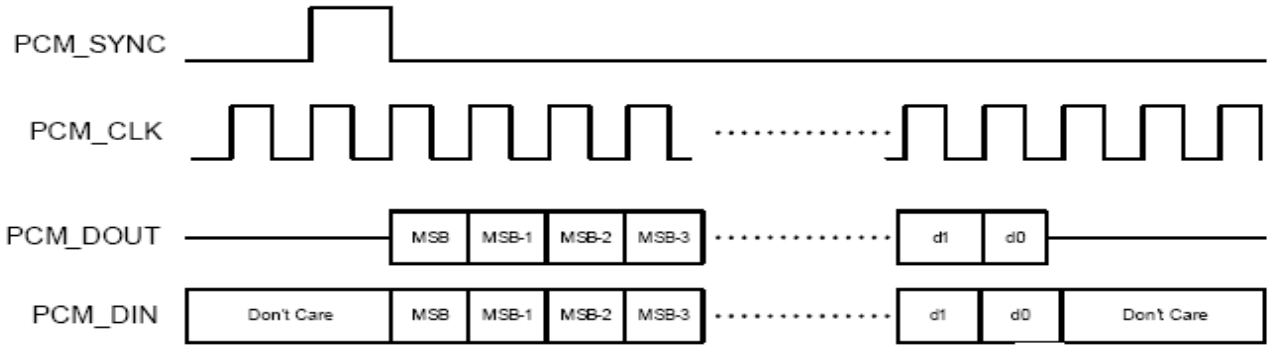
2-8-2.2.1 PCM Protocol Description

The PCM interface supports long and short frame sync.

PCM Long Frame Sync



PCM Short Frame Sync



2-8-2.2.1 Modes of Operation

The PCM interface supports two modes of operation:

- PCM master
- PCM slave

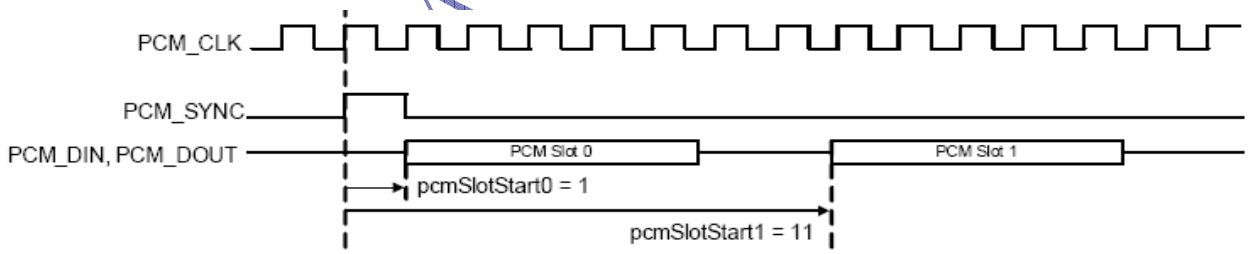
When in PCM master mode, the interface generates a 2MHz or a 2.048MHz PCM_CLK and 8kHz PCM_SYNC signal. An alternative PCM master mode is available that uses an externally generated PCM_CLK, but still generated the 8kHz PCM_SYNC. The external PCM_CLK must have a frequency that is an integer multiple of 8kHz. Supported frequencies are in the 512kH to 4MHz range.

When in PCM slave mode, the interface has both PCM_CLK and PCM_SYNC as inputs, thereby letting another unit on the PCM bus generate the signals.

The PCM Interface consists of up to four PCM slots(time divided) preceded by a PCM sync signal. Each PCM slot can be either 8 or 16 bits wide. The slots can be separated in times, but are not required to follow immediately after one other. The timing is relative to PCM_CLK.

This picture shows an example of a PCM burst with two slots. The burst starts with a PCM_SYNC and then follows the PCM burst. In the example, the PCM burst consists of two PCM slots(first one is 8 bites wide, second is 16 bits wide) separated with two PCM_CLK clock cycles. The PCM slots can be configured to start at an arbitrary point in time, and the start value is given relative to the tart of the PCM_SYNC. The timing of the four PCM slots must be such that slot 0 is always located before slot 1, slot 1 before slot 2, etc, It is possible to only use for example slot 1 and not slot 0.

PCM Burst with Two PCM Slots(example)

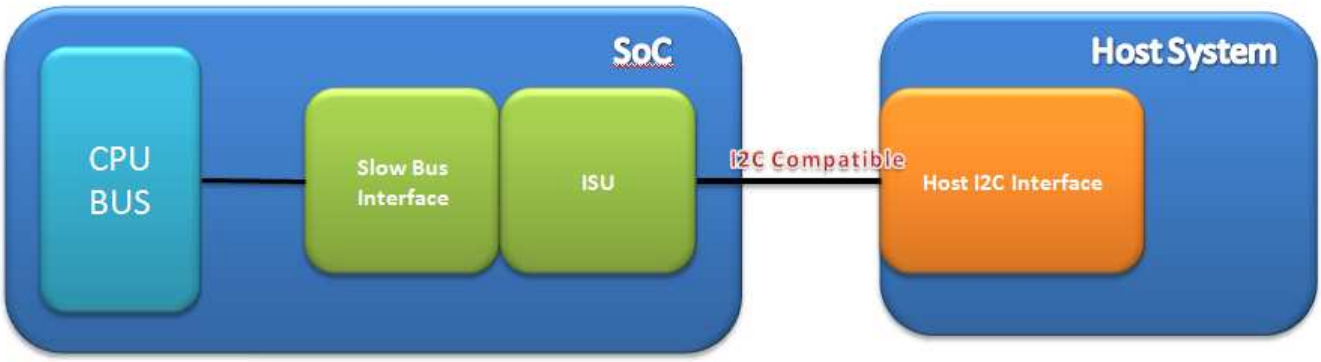


2-9. I2C-Compatible Slave Interface for FM control.

AW-NH387 I2C Slave Interface Unit (ISU) provides and I2C-compatible slave interface for communication between the internal CPU and an external host. This interface can be used for FM control. Device interface main features include:

- Complies with I2C bus standard v2.1, January 2000
  - Standard mode up to 100 kbps
  - Fast mode up to 400 kbps
- Supports 7-bit and 10-bit slave addressing (salve address is programmable)
- Optional wait cycle generation I2C bus when ISU cannot transmit/receive data.
- TX and RX FIFO for efficient communication between host and CPU (reduces CPU latency)
  - 16-byte RX FIFO depth
  - 16-byte TX FIFO depth
- Interface operates fully on SCLK input for wakeup operation (I2C access when SoC asleep)
- Generates dedicates interrupt host and handles interrupt masking and clearing
- Generic functionality to support other host interface functions besides FM control

ISU Interface Block Diagram



ISU Interface Signal Description

Pin Number	Pin Name	Type	Description
76	FM_TWSI_DATA	I/O	Serial data input/output
74	FM_TWSI_SCLK	I/O	Serial clock input/output
87	FM_HOSTIREQ	O	Interrupt to host from slave

2-10. Pin Out Power Supply Use

VIO_X1	VDD18_X3
RESETn	FM_AUDIO_OUT_L
PDn	FM_AUDIO_OUT_R
SD_CLK	FM_AUDIO_IN_L
SD_CMD	FM_AUDIO_IN_R
SD_DAT[1]	
SD_DAT[2]	
SD_DAT[3]	
GPIO[23:0]	
TCK	
TDI	
TDO	
TMS	
W1_CNTL	

3. Pin Definition

3-1. Pin Assignment

Pin No	Definition	Basic Description	Type	
1	GND			
2	RF 2G_IN/OUT	RF port for antenna or RF connector(Please keep matching circuit)		50Ohm @2.4GHz
3	GND			
4	GND			
5	I2S_DOUT	GPIO Mode: GPIO[22] I2S mode: I2S_DOUT(O) FM I2S Mode: FM_I2S_LRCLK(O) NOTE:GPIO[23:20]-separate I2S interface	O	
6	UART_DSR/ GPIO(3)/	UART DSR input: Data terminal ready output to the modem, data set, or peripheral device.	I	
7	GPIO(0)	External Oscillator control/Power management IC sleep mode	I/O	
8	FM_RX	FM RF receiver antenna or connector. 270nH indictor for module matching is necessary		
9	3.3V_PA	3.3V PA power supply	P	
10	GPIO(4)/	BT/WLAN/G-SPI host wake up	O	
11	LED OUT/GPIO(1)	WLAN transmit power or receive ready LED.	O	
12	GND			
13	SD_DAT[1]/ SPI_SDOn	SDIO 4-bit Mode: Data line bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Reserved G-SPI Mode: G-SPI Data Output(active low)	I/O	Note2
14	SD_DAT[3]	SDIO 4-bit Mode: Data line bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select(active low)	I/O	Note2
15	FM_TX	FM RF transceiver antenna or port.		
16	UART DTR/ GPIO(5)/	UART DTR out: Clear to send input from the modem data set, or peripheral device.	O	
17	UART SINT/ GPIO(7)	UART SINT input: Serial data input from the modem, data set or peripheral device.	I	
18	PDn	Full Power Down(active low as long as system need) 0=power down mode 1=normal mode (1)Connect to power down pin of host (2)Serial 100K ohm to VIO Note: Needs the external host to driver this pin high for normal operation. No internal pull-up on this pin.	I	
19	VBAT	3.3V digital I/O power supply	P	
20	I2S_DIN	GPIO Mode: GPIO[21] I2S mode: I2S_DIN(I) FM I2S Mode: FM_I2S_LRCLK(I) NOTE:GPIO[23:20]-separate I2S interface	I	
21	UART CTS/GPIO(8)	UART CTS input: Clear to send input from the modem, data set, or peripheral device.	I	
22	SLEEP_CLK	Clock input for external sleep clock **Note:** SLEEP_CLK is used by the WLAN MAC. The input clock frequency is typically 32kHz/32.768kHz/3.2kHz.The Bluetooth radio chip supply is 3.2kH.The WLAN requires 32kHz. External Sleep CLK is necessary for AW-NH387	I	
23	I2S_BCLK	GPIO Mode: GPIO[20] I2S mode: I2S_BCLK(I/O) ● Output if master ● Input if slave FM I2S Mode: FM_I2S_BCLK(I/O) ● Output if master ● Input if slave NOTE:GPIO[23:20]-separate I2S interface	I/O	

Pin No	Definition	Basic Description	Type	
24	GND			
25	SD_DAT[2]/ SPI_SINTn	SDIO4-bit Mode: Data line bit[2]or Read Wait(optional) SDIO 1-bit Mode: Read Wait(optional) SDIO SPI Mode: Reserved G-SPI Mode: Active G-SPI Interrupt Output(active low)	I/O	Note2
26	SD_DAT[0]/ SPI_SCSn	SDIO 4-bit Mode: Data line bit[0] SDIO 1-bit Mode:Data line SDIO SPI Mode: Data output G-SPI Mode: G-SPI Chip Select Input(active low)	I/O	Note2
27	SD_CLK/ SPI_CLK	SDIO 4-bit Mode: Clock Input SDIO 1-bit Mode: Clock Input SDIO SPI Mode: Clock Input G-SPI Mode:G-SPI Clock Input	I/O	Note2
28	BT_PCM_DOUT/ I2S_DOUT/ GPIO(12)	GPIO Mode:GPIO[12] I2S mode: I2S_DOUT FM I2S Mode: FM_I2S_DOUT PCM Mode: PCM_DOUT NOTE:GPIO[14:11]-shared I2S/PCM interface	O	
29	SD_CMD/ SPI_SDI	SDIO 4-bit Mode: Command/Response SDIO 1-bit Mode: Command Line SDIO SPI Mode: Data Input G-SPI Mode: G-SPI Data Input	I/O	Note2
30	UART SOUT/ GPIO(6)	UART SOUT out: Serial data output to the modem, data set, or peripheral device.	O	
31	NC			
32	TDO	JTAG Test Mode: JTAG test data(O) Coexistence Mode: BT_REQ (I)	I/O	
33	Host interface select[2]	Host Interface Select, see Note1.	O	*
34	RES_K3	Please left test point.		
35	VIO_X1	1.8V/2.6V/3.3V SDIO and UART host supply	P	
36	GND			
37	VDD18_X3	1.8V digital I/O and internal voltage regulator power supply	P	
38	VIO_X1	1.8V/2.6V/3.3V SDIO and UART host supply	P	
39	RESETn	RESETn: Reset(active low at least 10ns) (1)When the customer uses the RESETn mode, the SDIO/SPI interface must reboot. (2)Serial 100K ohm to VIO	I	
40	1.2V_Internal	Internal 1.2V power supply. Only for Monitor voltage.	P	
41	VDD18A	1.8V analog I/O power supply	P	
42	SW_RX2	For Monitor IC function. Left NC.		
43	Host interface select [1]	Host Interface Select, see Note1.	O	Note1
44	GPIO(17)	BT transmits power or receives ready LED.	I/O	
45	Host interface select [0]	Host Interface Select , see Note1	O	Note1
46	GND			
47	GND			
48	GND			
49	GND			
50	SW_BT	For Monitor IC function. Left NC.		

Pin No	Definition	Basic Description	Type	
51	GND			
52	GPIO(16)	WLAN host wake up	O	
53~57	GND			
58	GND			
59	GND			
60	GND			
61	GND			
62	GND			
63	GND			
64	GND			
65	GND			
66	BT_PCM_CLK/ I2S_BCLK/ GPIO(13)	GPIO Mode:GPIO[13] I2S mode: I2S_BCLK ● Output if master ● Input if slave FM I2S Mode: FM_I2S_BCLK ● Output if master ● Input if slave PCM Mode: PCM_CLK ● Output if master ● Input if slave NOTE:GPIO[14:11]-shared I2S/PCM interface	I/O	
67	I2S_LRCLK	GPIO Mode: GPIO[23] I2S mode: I2S_LRCLK(I/O) ● Output if master ● Input if slave FM I2S Mode: FM_I2S_LRCLK(I/O) ● Output if master ● Input if slave NOTE:GPIO[23:20]-separate I2S interface	I/O	
68	GND			
69	BT_PCM_SYNC/ I2S_LRCLK/ GPIO(14)	GPIO Mode:GPIO[14] I2S mode: I2S_LRCLK ● Output if master ● Input if slave FM I2S Mode: FM_I2S_LRCLK ● Output if master ● Input if slave PCM Mode: PCM_SYNC ● Output if master ● Input if slave NOTE:GPIO[14:11]-shared I2S/PCM interface	I/O	
70	TMS	JTAG Test Mode: JTAG controller select Coexistence: BT_FREQ	I	
71	BT_PCM_MCLK/ I2S_CCLK/ GPIO(15)	GPIO Mode:GPIO[15] I2S mode: I2S_CCLK ● Output if master ● Input if slave FM I2S Mode: FM_I2S_CCLK ● Output if master ● Input if slave PCM Mode: PCM_MCLK ● Output if master ● Input if slave Optional clock used for some codecs	I/O	
72	TCK	JTAG Test Mode: JTAG test clock Coexistence: BT_GRANTn	I/O	

Pin No	Definition	Basic Description	Type	
73	BT_PCM_DIN/ I2S_DIN/ GPIO(11)	GPIO Mode:GPIO[11] I2S mode: I2S_DIN FM I2S Mode: FM_I2S_DIN PCM Mode: PCM_MCLK NOTE:GPIO[14:11]-shared I2S/PCM interface	I/OI	
74	I2C_CLK/GPIO(9)	GPIO Mode: GPIO[9] I2C-Compatible Slave Interface: FM_TWSI_SCLK Serial data input/output I2C slave-compatible interface clock signal	I/O	
75	GND			
76	I2C_DAT/GPIO(10)	GPIO Mode: GPIO[10] I2C-Compatible Slave Interface: FM_TWSI_DATA Serial data input/output I2C slave-compatible interface clock signal	I/O	
77	FM_AUDIO_IN_L	FM Audio Input Left	I	
78	FM_AUDIO_OUT_L	FM Audio Output Left	I	
79	GND			
80	GND			
81	W1_CTRL	External power management IC program pin	O	
82	GND			
83	GND			
84	FM_AUDIO_IN_R	FM Audio Input Right	I	
85	FM_AUDIO_OUT_R	FM Audio Output Right	I	
86	TDI	JTAG Test Mode: JTAG test data Coexistence: BT_STATE	I	
87	GPIO(18)	FM host wake up	O	
88	UART RTS/ GPIO(2)	UART RTS output: Request to send output to the modem, data set, or peripheral device	I/O	

Note1: **Host Interface select define table**

Pin No	Definition	Basic Description
45	Host interface select [0]	
43	Host interface select [1]	
33	Host interface select [2]	

CON[2]	CON[1]	CON[0]	FW BOOT	WLAN	BT	FM
1	0	0	GSPI/UART	GSPI	UART	UART/I2C
1	0	1	SDIO	SDIO	SDIO	SDIO/I2C
1	1	0	SDIO/GSPI	SDIO	GSPI	GSPI/I2C
1	**1**	**1**	**SDIO/UART**	**SDIO**	**UART**	**UART/I2C**

Bolt is default setting

Note2: SDIO/G-SPI interface Pin

Pin No	Definition	Basic Description	Type	
13	SD_DAT[1]/ SPI_SDOn	SDIO 4-bit Mode: Data line bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Reserved G-SPI Mode: G-SPI Data Output(active low)	I/O	
14	SD_DAT[3]	SDIO 4-bit Mode: Data line bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select(active low)	I/O	
25	SD_DAT[2]/ SPI_SINTn	SDIO4-bit Mode: Data line bit[2]or Read Wait(optional) SDIO 1-bit Mode: Read Wait(optional) SDIO SPI Mode: Reserved G-SPI Mode: Active G-SPI Interrupt Output(active low)	I/O	
26	SD_DAT[0]/ SPI_SCSn	SDIO 4-bit Mode: Data line bit[0] SDIO 1-bit Mode:Data line SDIO SPI Mode: Data output G-SPI Mode: G-SPI Chip Select Input(active low)	I	
27	SD_CLK/ SPI_CLK	SDIO 4-bit Mode: Clock Input SDIO 1-bit Mode: Clock Input SDIO SPI Mode: Clock Input G-SPI Mode:G-SPI Clock Input	I/O	
29	SD_CMD/ SPI_SDI	SDIO 4-bit Mode: Command/Response SDIO 1-bit Mode: Command Line SDIO SPI Mode: Data Input G-SPI Mode: G-SPI Data Input	I/O	

UART Interface

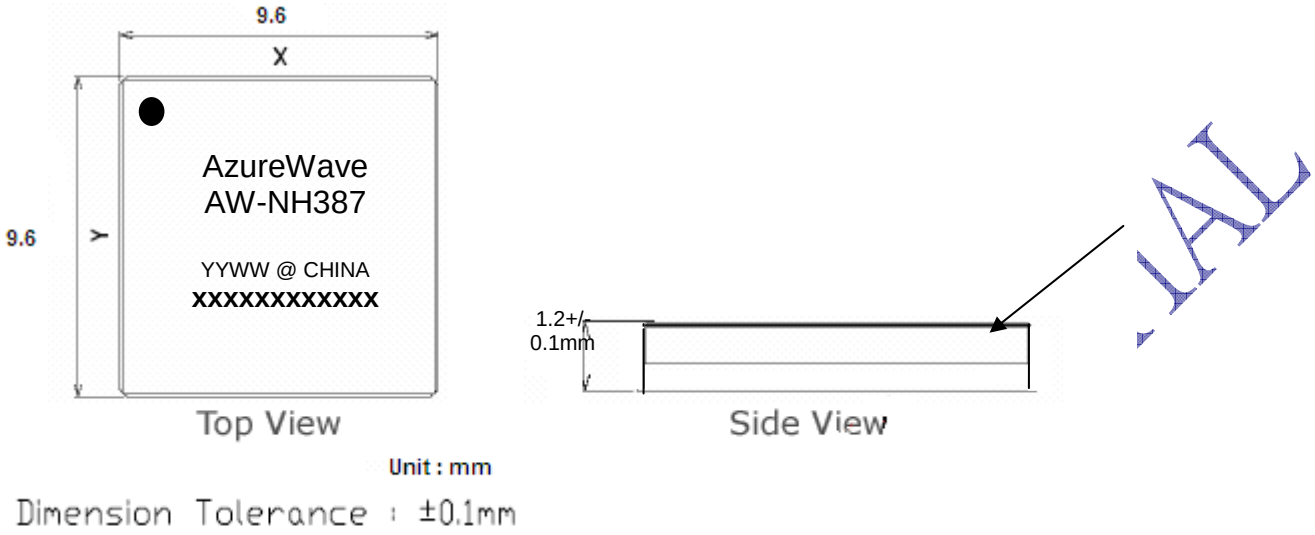
Pin No	Definition	Basic Description	Type	
Data Bus				
17	UART SINT/GPIO(7)	UART SINT input: Serial data input from the modem, data set or peripheral device.	I	
30	UART SOUT/ GPIO(6)	UART SOUT out: Serial data output to the modem, data set, or peripheral device.	O	
Modem Control				
6	UART_DSR/ GPIO(3)	UART DSR input: Data terminal ready output to the modem, data set, or peripheral device.	I	
16	UART DTR/ GPIO(5)/	UART DTR out:Clear to send input from the modem data set, or peripheral device.	O	
21	UART CTS/GPIO(8)	UART CTS input: Clear to send input from the modem, data set, or peripheral device.	I	
63	UART RTS/ GPIO(2)	UART RTS output: Request to send output to the modem, data set, or peripheral device	O	

Wake up function

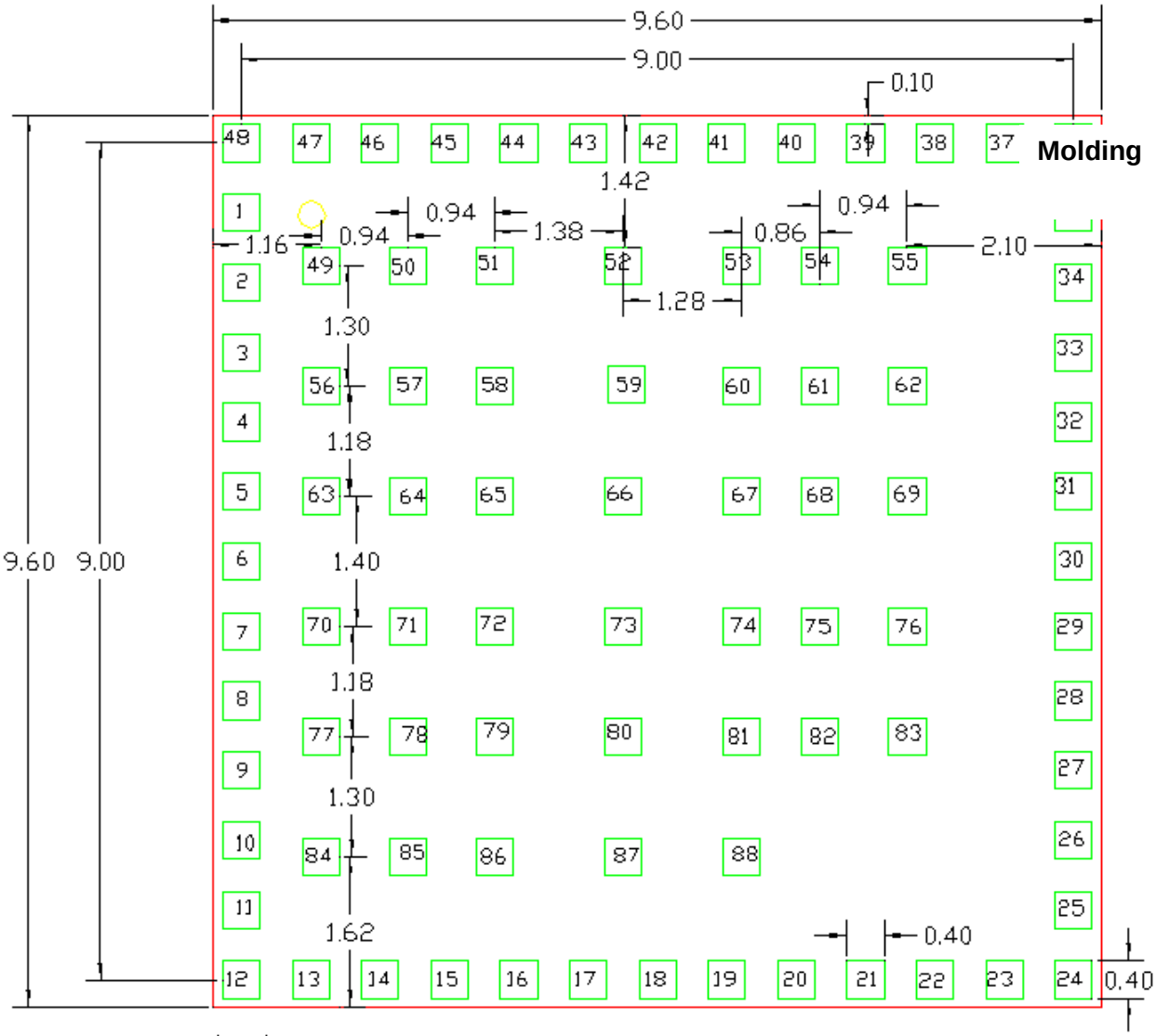
Pin No	Definition	Basic Description	Type	
87	GPIO18	FM host wake up	O	
52	GPIO16	WLAN host wake up	O	
10	GPIO4	BT/WLAN/G-SPI host wake up	O	

4. Mechanical Characteristics

The size and thickness of the AW-NH387 LGA package module is listed below:



AW-NH387 Top View PCB Layout FootPrint

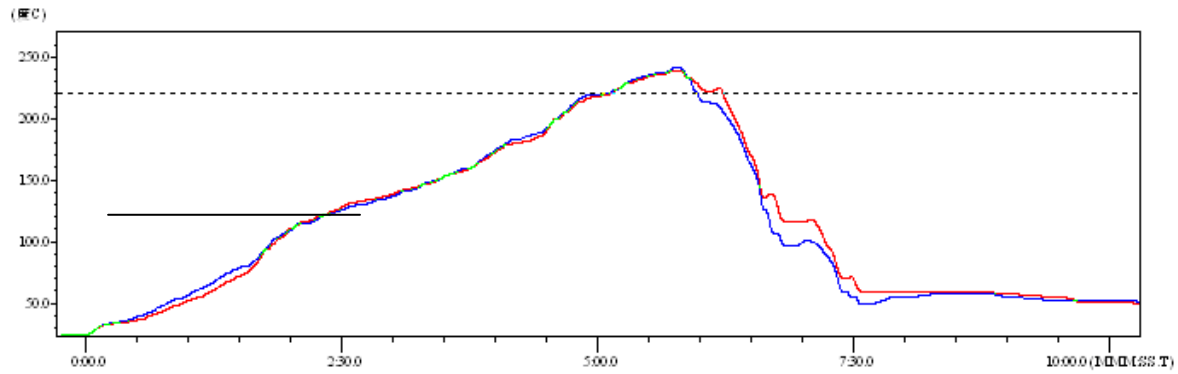


Note: AzurWave will provide AW-NH387 Top View FootPrint DXF file for customer reference.

5. Package Information

5-1. Recommended Reflow Profile

Reflow Soldering Profile



No	Item	Temperature(℃)	Time(sec)
1	Reflow Time	Time of above 220℃	40~60sec
2	Peak-Temp	245℃ max	

Note: 1. Recommend to supply N_2 for reflow oven

2. N_2 atmosphere during reflow (O_2<300ppm)

5-2. Device Handling Instruction(Module IC SMT Preparation)

5-2-1. Shelf life in sealed bag:12 months, At<30℃ and <60% relative humidity(RH)

5-2-2. After bag is opened, devices that will be

5-2-2-1. Baked for 24 hours at 125+-5℃ with tray

5-2-2-2. Re-baked required after last baked with window time 24 hours

5-2-3. Recommend to Oven bake with N2 supplied

5-2-4. Recommend end to Reflow Oven with N2 supplied

5-2-5. Baked required with 24 hours at 125+-5℃ before rework process for two modules, one is new module and two is board with module

5-2-6. Recommend to store at ≦10% RH with vacuum packing

5-2-7. If SMT process needs twice reflow:

5-2-7-1. Process flow: (1) Top side SMT and reflow → (2) Bottom side SMT and reflow

5-2-7-1-1. Case 1: Wifi module mound on Top side. Need to bake when bottom side process over 24 hours window time, no need to bake within 24 hours

5-2-7-1-2. Case 2: Wifi module mound on bottom side, follow normal bake rule before process

Note: Window time means from last bake end to next reflow start that has 24 hours space.