

## Over-Voltage Protection Load Switch with Surge Protection

### FEATURES

- Surge protection
  - IEC 61000-4-5: > 100V
- Integrated low  $R_{dson}$  nFET switch: typical 24m $\Omega$
- 5A continuous current capability
- Default Over-Voltage Protection (OVP) threshold
  - AW32705: 6.8V
  - AW32710: 10.5V
- OVP threshold adjustable range: 4V to 20V
- Input system ESD protection
  - IEC 61000-4-2 Contact discharge:  $\pm 8kV$
  - IEC 61000-4-2 Air gap discharge:  $\pm 15kV$
- Input maximum voltage rating: 35V<sub>DC</sub>
- Fast turn-off response: typical 50ns
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)
- WLCSP 1.17x1.57-12B package

### APPLICATIONS

- Smartphones
- Tablets
- Charging Ports

### GENERAL DESCRIPTION

The AW327XX family OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to 100V.

The AW327XX features an ultra-low 24m $\Omega$  (typ.)  $R_{dson}$  nFET load switch. When input voltage exceeds the OVP threshold, the switch is turned off very fast to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to 35V<sub>DC</sub>.

The default OVP threshold is 6.8V (AW32705) and 10.5V (AW32710), the OVP threshold can be adjusted from 4V to 20V through external OVLO pin.

The device features an open-drain output  $\overline{ACOK}$ , when  $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$  and the switch is on,  $\overline{ACOK}$  will be driven low to indicate a good power input, otherwise it is high impedance.

This device features over-temperature protection that prevents itself from thermal damaging.

The AW327XX is available in a RoHS compliant WLCSP 1.17x1.57-12B package.

### TYPICAL APPLICATION CIRCUIT

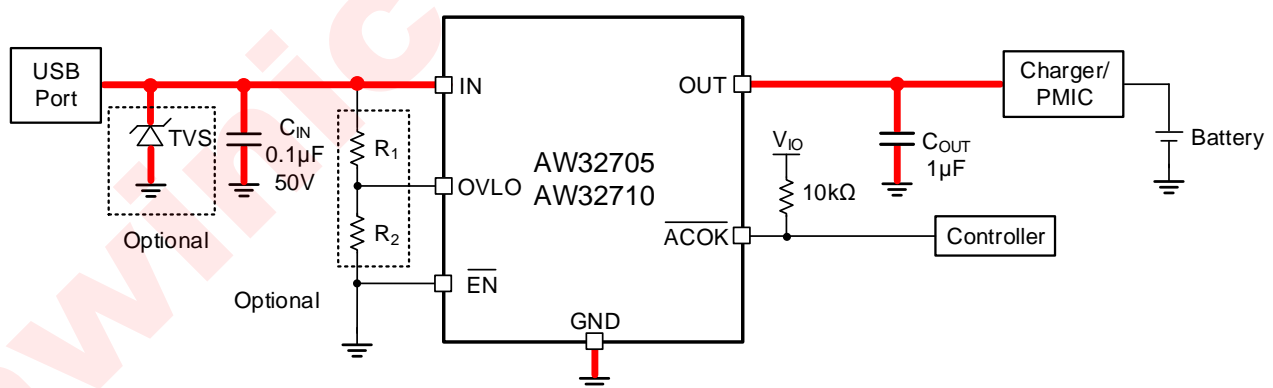


Figure 1 AW327XX typical application circuit

$R_1$  and  $R_2$  are used for OVP threshold adjustment, to use default OVP threshold, connect OVLO to ground.

All the trademarks mentioned in the document are the property of their owners.

## DEVICE COMPARISON TABLE

Device	$V_{IN\_OVLO}$ (V)				$V_{IN\_OVLO}$ hysteresis (mV)
	Condition	Min.	Typ.	Max.	
AW32705	$V_{IN}$ rising	6.66	6.80	6.94	140
AW32710	$V_{IN}$ rising	10.29	10.50	10.71	210

## PIN CONFIGURATION AND TOP MARK

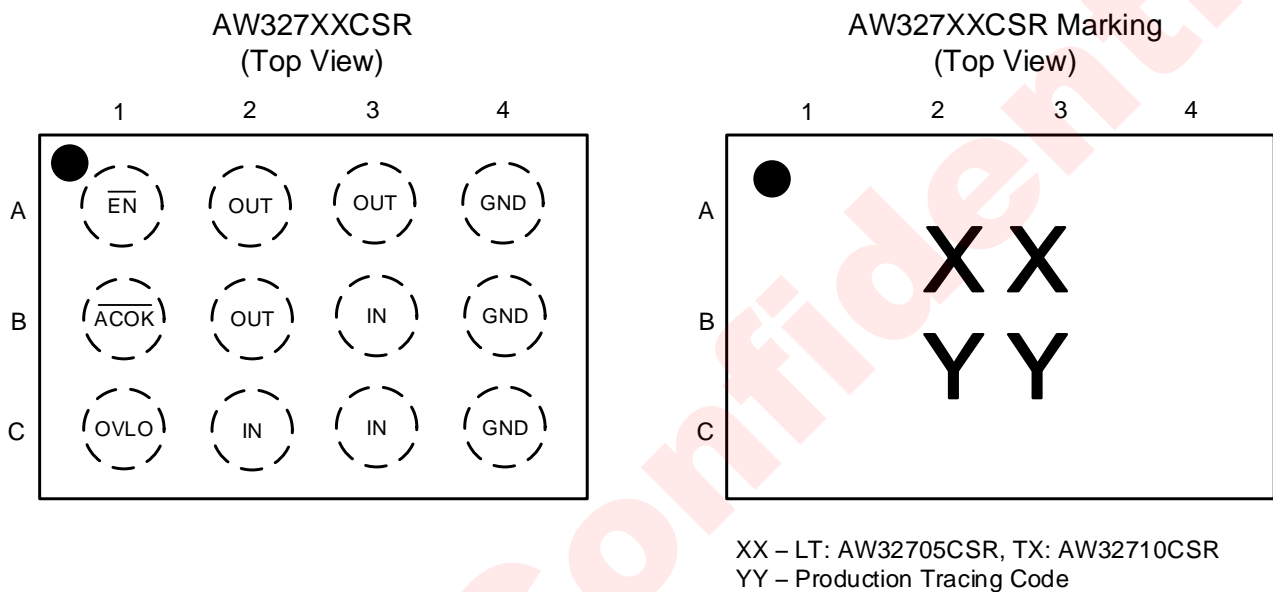


Figure 2 Pin Configuration and Top Mark

## PIN DEFINITION

Pin	Name	Description
A1	$\overline{EN}$	Enable pin, active low
B1	$\overline{ACOK}$	Power good flag, active-low, open-drain
C1	OVLO	OVP threshold adjustment pin
C2, C3, B3	IN	Switch input and device power supply
A2, A3, B2	OUT	Switch output
A4, B4, C4	GND	Device ground

## FUNCTIONAL BLOCK DIAGRAM

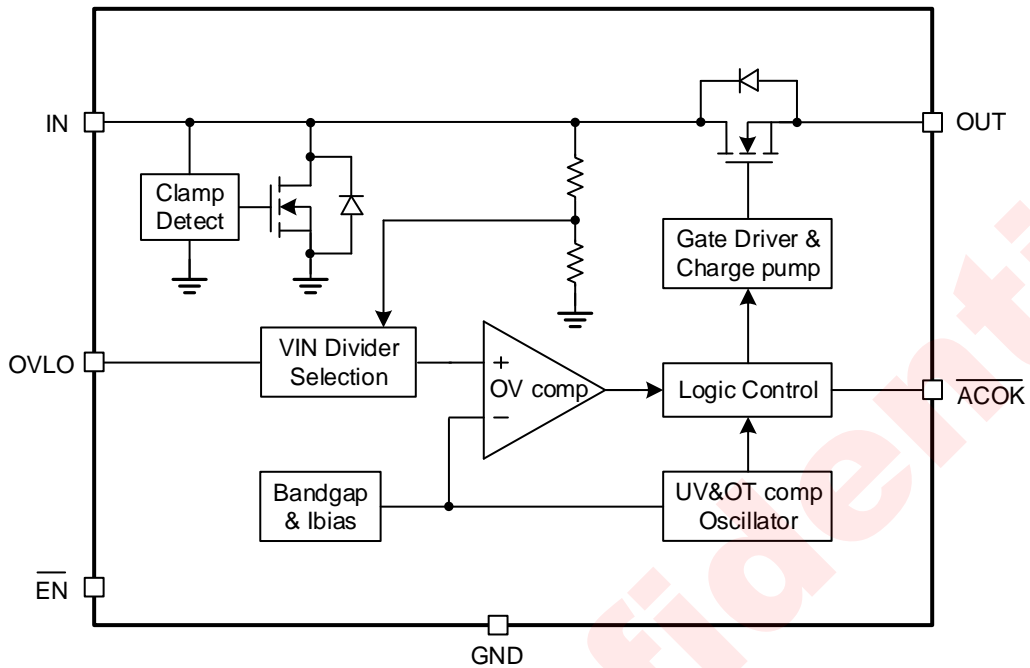


Figure 3 Functional Block Diagram

## TYPICAL APPLICATION CIRCUITS

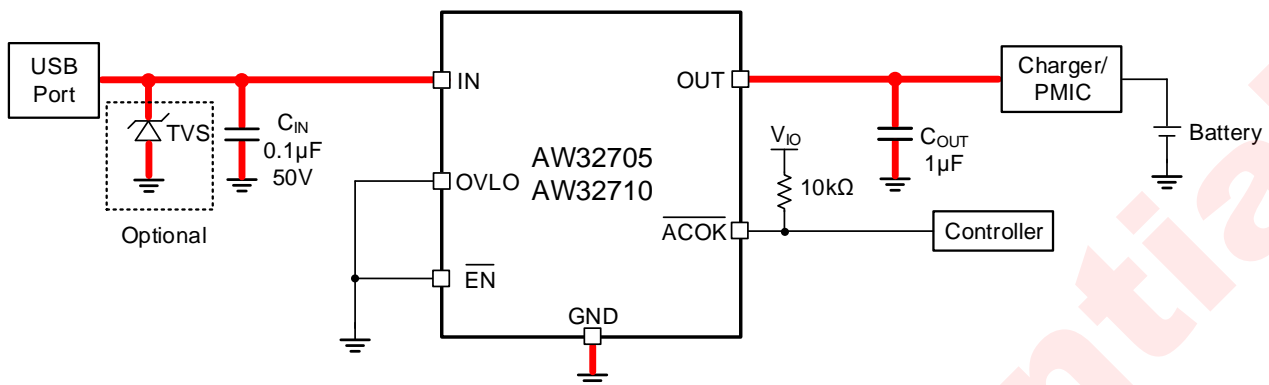


Figure 4 AW327XX typical application circuit(using default OVP threshold)

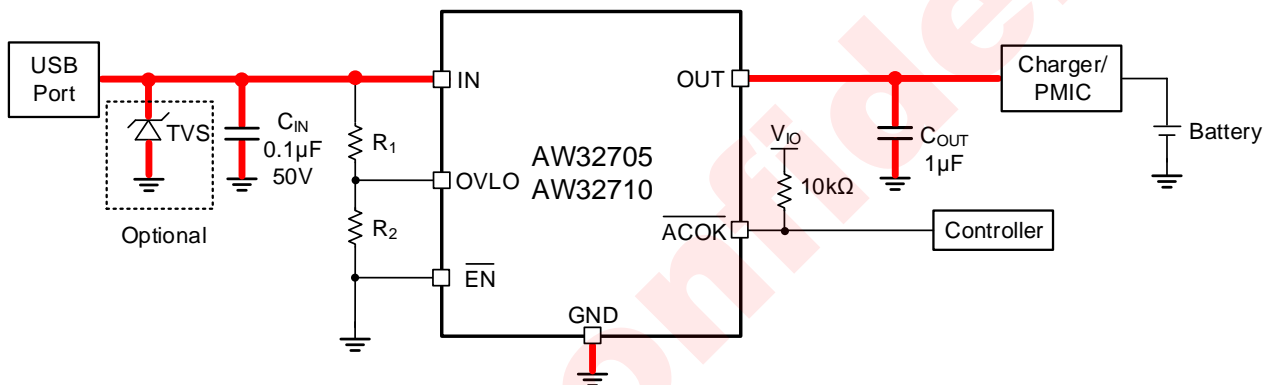


Figure 5 AW327XX typical application circuit(using external resistors set OVP threshold)

### Notice for Typical Application Circuits:

1. If VBUS is required to pass surge voltage greater than 100V, external TVS is needed, the maximum clamping voltage of the TVS should be below 37V.
2. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. OVLO pin cannot be left floating.
3. If R<sub>1</sub> and R<sub>2</sub> are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
4. If  $\overline{\text{ACOK}}$  is not used, it can be left floating, or short to GND.
5. C<sub>IN</sub> = 0.1µF is recommended for typical application, larger C<sub>IN</sub> is also acceptable. The rated voltage of C<sub>IN</sub> should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW327XX is used, the rated voltage of C<sub>IN</sub> should be 50V.
6. C<sub>OUT</sub> = 1µF is recommended for typical application, larger C<sub>OUT</sub> is also acceptable. The rated voltage of C<sub>OUT</sub> should be larger than the OVP threshold. For example, if the OVP threshold is 6.8V, the rated voltage of C<sub>OUT</sub> should be 10V or higher.

## ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32705CSR	-40°C~85°C	WLCSP 1.17mmx1.57mm-12B	LT	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW32710CSR	-40°C~85°C	WLCSP 1.17mmx1.57mm-12B	TX	MSL1	ROHS+HF	3000 units/ Tape and Reel

## ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Symbol	Parameter	Condition	Min.	Max.	Unit
$V_{IN}$	Input voltage		-0.3	35	V
$V_{OUT}$	Output voltage		-0.3	See(NOTE 2)	V
$V_{OVLO}$	OVLO voltage		-0.3	6	V
$V_{\overline{ACOK}}$	$\overline{ACOK}$ voltage		-0.3	6	V
$V_{\overline{EN}}$	$\overline{EN}$ voltage		-0.3	6	V
$I_{SW}$	Continuous current of switch IN-OUT(NOTE 3)	Continuous current on IN and OUT pin		5	A
$I_{PEAK}$	Peak current	Peak input and output current on IN and OUT pin(10ms)		8	A
$I_{DIODE}$	Continuous diode current	Continuous forward current through the nFET body diode		1.5	A
$T_A$	Ambient temperature		-40	85	°C
$T_J$	Junction temperature		-40	150	°C
$T_{STG}$	Storage temperature		-65	150	°C
$T_{LEAD}$	Soldering temperature	At leads, 10 seconds		260	°C
Surge	Input surge protection	IEC61000-4-5 test with 2Ω equivalent series resistance	100		V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: 29V or  $V_{IN}+0.3V$ , whichever is smaller.

NOTE3: Limited by thermal design.

## THERMAL INFORMATION

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Thermal resistance from junction to ambient (NOTE 1)	In free air	90	$^{\circ}\text{C/W}$

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

## ESD AND LATCH-UP RATINGS

Symbol	Parameter	Condition	Value	Unit
$V_{ESD}$	IEC61000-4-2 system ESD on IN pin	Contact discharge	$\pm 8$	kV
		Air gap discharge	$\pm 15$	kV
	Human Body Model	ANSI/ESDA/JEDEC JS-001	$\pm 2$	kV
	Charged Device Model	JESD22-C101	$\pm 1.5$	kV
	Machine Model	JESD22-A115C	$\pm 200$	V
$I_{Latch-up}$	Latch-up	JEDEC78	$\pm 200$	mA

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IN}$	Input DC voltage	3		30	V
$C_{IN}$	Input capacitance		0.1		$\mu\text{F}$
$C_{OUT}$	Output load capacitance		1		$\mu\text{F}$

## ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise noted. Typical values are guaranteed for  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 0.1\mu\text{F}$ ,  $I_{IN} \leq 5\text{A}$  and  $T_A = 25^{\circ}\text{C}$ .

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units	
$V_{IN\_CLAMP}$	Input clamp voltage	$I_{IN} = 10\text{mA}$		36.3		V	
$R_{dson}$	Switch on resistance	$V_{IN} = 5\text{V}$ , $I_{OUT} = 1\text{A}$ , $T_A = 25^{\circ}\text{C}$		24	35	m $\Omega$	
$I_Q$	Input quiescent current	$V_{IN} = 5\text{V}$ , $V_{OVLO}=0\text{V}$ , $I_{OUT} = 0\text{A}$		70	140	$\mu\text{A}$	
$I_{IN\_OVLO}$	Input current at over-voltage condition	$V_{IN} = 5\text{V}$ , $V_{OVLO}=3\text{V}$ , $V_{OUT} = 0\text{V}$		67	130	$\mu\text{A}$	
$V_{OVLO\_TH}$	OVLO set threshold		1.16	1.20	1.24	V	
$V_{OVLO\_RNG}$	OVP threshold adjustable range		4		20	V	
$V_{OVLO\_SEL}$	External OVLO select threshold	OVLO rising	0.19	0.26	0.33	V	
		Hysteresis		0.06		V	
$I_{OVLO}$	OVLO pin leakage current	$V_{OVLO}=V_{OVLO\_TH}$	-0.2		0.2	$\mu\text{A}$	
<b>Protection</b>							
$V_{IN\_OVLO}$	OVP trip level	AW32705	$V_{IN}$ rising	6.66	6.80	6.94	V
			Hysteresis		0.14		
		AW32710	$V_{IN}$ rising	10.29	10.50	10.71	
			Hysteresis		0.21		
$V_{IN\_UVLO}$	UVLO trip level	$V_{IN}$ rising			2.9	3.0	V
		Hysteresis			0.1		
$T_{SDN}$	Shutdown temperature			150		$^{\circ}\text{C}$	
$T_{SDN\_HYS}$	Shutdown temperature hysteresis			20		$^{\circ}\text{C}$	
$R_{DCHG}$	Output discharge resistance	$V_{OUT}=7\text{V}$ , $V_{OVLO}=3\text{V}$		50		$\Omega$	

## ELECTRICAL CHARACTERISTICS (CONTINUED)

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise noted. Typical values are guaranteed for  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 0.1\mu\text{F}$ ,  $I_{IN} \leq 5\text{A}$  and  $T_A = 25^{\circ}\text{C}$ .

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
<b>Digital Logical Interface</b>						
$V_{OL}$	$\overline{ACOK}$ output low voltage	$I_{SINK}=1\text{mA}$			0.4	V
$I_{LEAK\_ACOK}$	$\overline{ACOK}$ leakage current	$V_{IO}=5\text{V}$ , $\overline{ACOK}$ de-asserted	-0.5		0.5	$\mu\text{A}$
$V_{IH}$	$\overline{EN}$ input high voltage		1.2			V
$V_{IL}$	$\overline{EN}$ input low voltage				0.5	V
$I_{LEAK\_EN}$	$\overline{EN}$ leakage current	$V_{\overline{EN}} = 5\text{V}$	0		2	$\mu\text{A}$
<b>Timing Characteristics (Figure 6)</b>						
$t_{DEB}$	Debounce time	From $V_{IN} > V_{IN\_UVLO}$ to 10% $V_{OUT}$		15		ms
$t_{START}$	Start-up time	From $V_{IN} > V_{IN\_UVLO}$ to $\overline{ACOK}$ low		30		ms
$t_{ON}$	Switch turn-on time	$R_L = 100\Omega$ , $C_L = 22\mu\text{F}$ , $V_{OUT}$ from 10% $V_{IN}$ to 90% $V_{IN}$		2		ms
$t_{OFF}$	Switch turn-off time	$C_L = 0\mu\text{F}$ , $R_L = 100\Omega$ , $V_{IN} > V_{IN\_OVLO}$ to $V_{OUT}$ stop rising, $V_{IN}$ rise at $10\text{V}/\mu\text{s}$		50		ns

## TIMING DIAGRAM

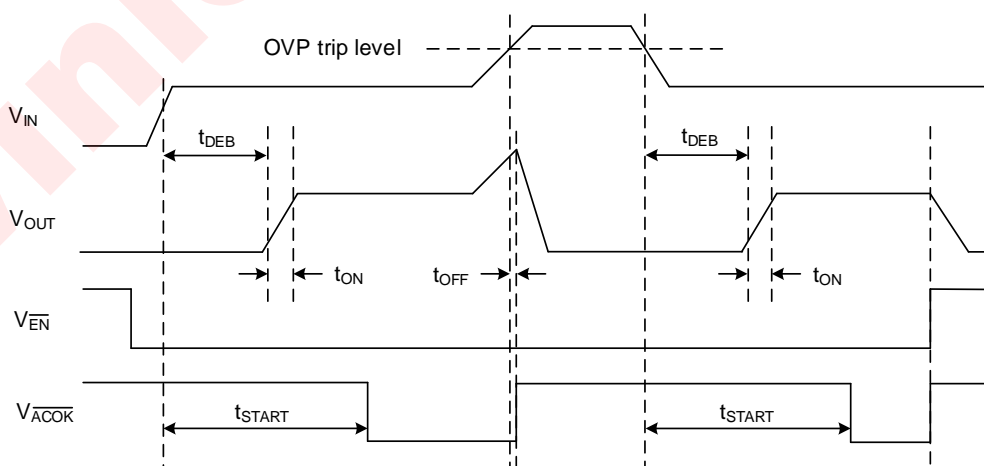


Figure 6 Timing diagram



## TYPICAL CHARACTERISTICS

$V_{IN} = 5V$ ,  $V_{EN} = 0V$ ,  $V_{OVLO} = 0V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , and  $T_A = 25^\circ C$  unless otherwise specified.

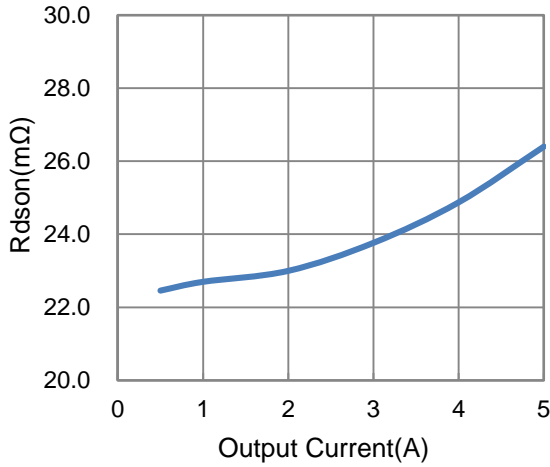


Figure 7 R<sub>ds(on)</sub> vs. Output Current

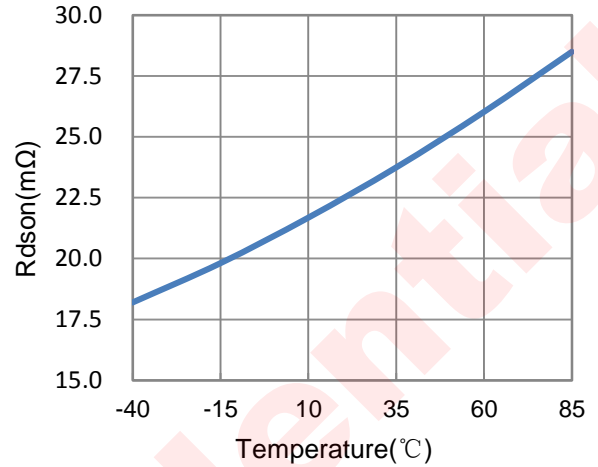


Figure 8 R<sub>ds(on)</sub> vs. Temp. (I<sub>out</sub> = 1A)

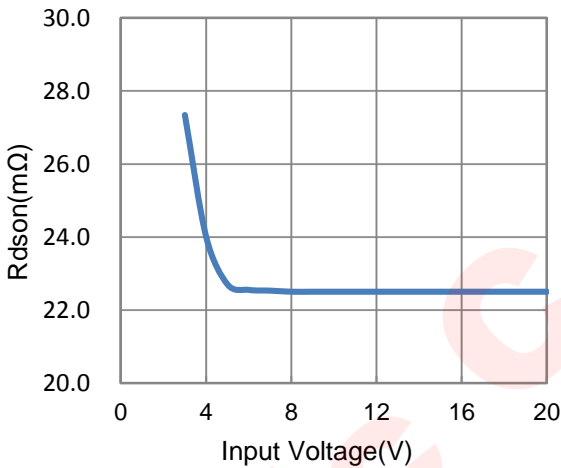


Figure 9 R<sub>ds(on)</sub> vs. Input Voltage (I<sub>out</sub> = 1A)

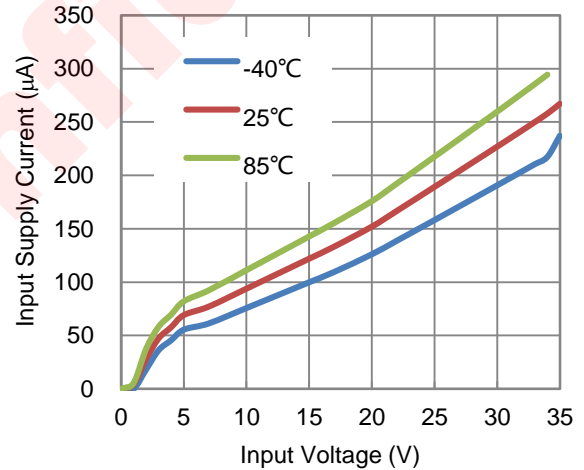


Figure 10 Input Supply Current vs. Supply Voltage

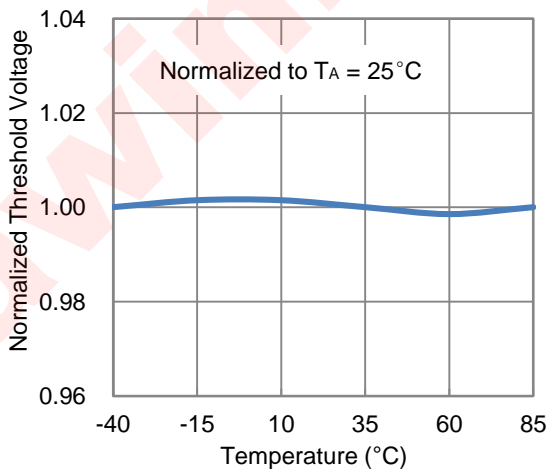


Figure 11 Normalized Internal OVP Threshold vs. Temp.

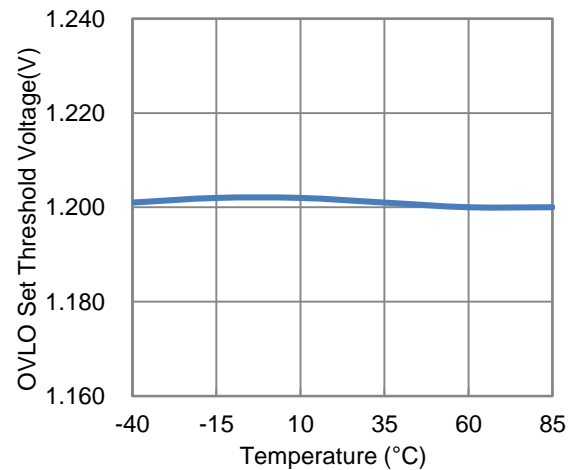


Figure 12 OVLO set threshold vs. Temp.

## TYPICAL CHARACTERISTICS (CONTINUED)

$V_{IN} = 5V$ ,  $V_{EN} = 0V$ ,  $V_{OVLO} = 0V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , and  $T_A = 25^\circ C$  unless otherwise specified.

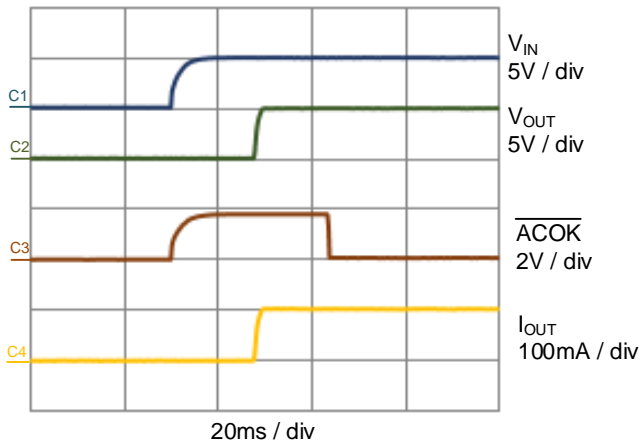


Figure 13 Power-up ( $C_{OUT} = 1\mu F$ , 100mA load).

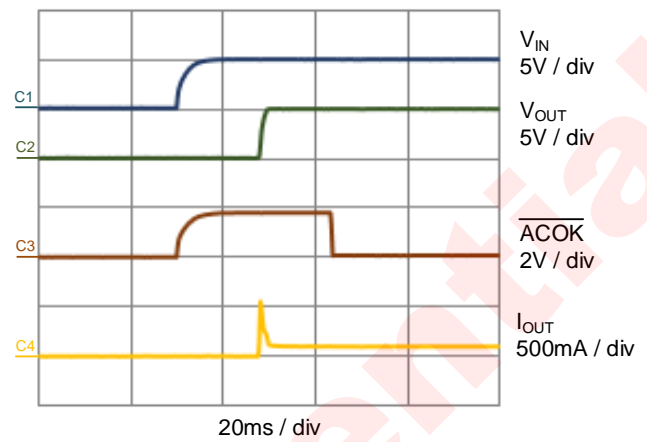


Figure 14 Power-up ( $C_{OUT} = 100\mu F$ , 100mA load)

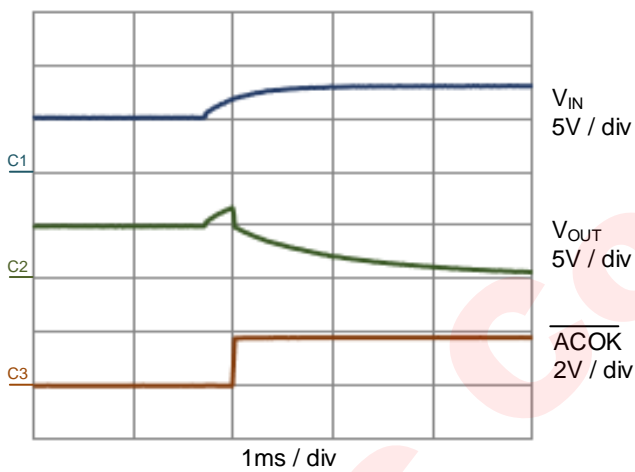


Figure 15 OVP Response (AW32705)

## DETAILED FUNCTIONAL DESCRIPTION

### Device Operation

If the AW327XX is enabled and the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on.  $\overline{ACOK}$  will be driven low about 30ms after  $V_{IN}$  valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 50ns. If  $\overline{EN}$  is pulled high, or input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

### Surge Protection

The AW327XX integrates a clamp circuit to suppress input surge voltage. For surge voltages between  $V_{IN\_OVLO}$  and  $V_{IN\_CLAMP}$ , the switch will be turned off but the clamp circuit will not work. For surge voltages greater than  $V_{IN\_CLAMP}$ , the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

### Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until  $V_{IN}$  falls below the OVP falling trip level.

### OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

For example, if we select  $R_1 = 1M\Omega$  and  $R_2 = 100k\Omega$ , then the new OVP threshold calculated from the above formula is 13.2V. The OVP threshold adjustment range is from 4V to 20V. When the OVLO pin voltage  $V_{OVLO}$  exceeds  $V_{OVLO\_SEL}$  (0.26V typical),  $V_{OVLO}$  is compared with the reference voltage  $V_{OVLO\_TH}$  (1.2V typical) to judge whether input supply is over-voltage.

### $\overline{ACOK}$ Output

The device features an open-drain output  $\overline{ACOK}$ , it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and  $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$ ,  $\overline{ACOK}$  will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, or  $\overline{EN}$  is pulled high, the switch will be turned off and  $\overline{ACOK}$  will be pulled high.

### USB On-The-Go (OTG) Operation

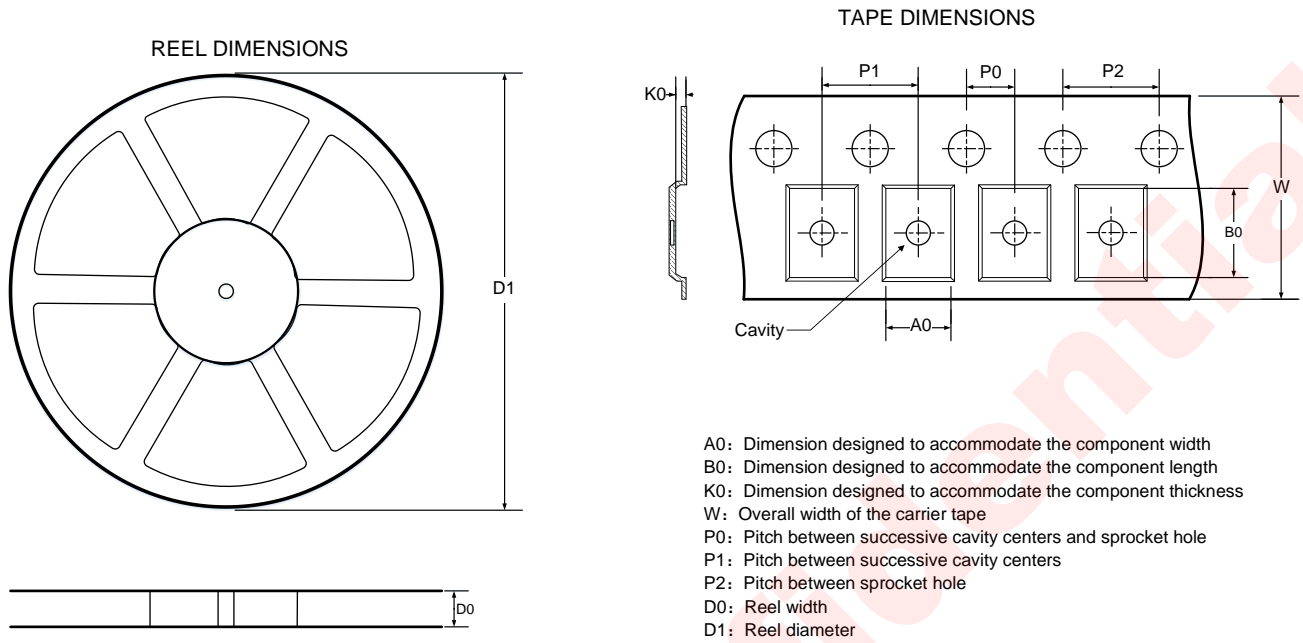
If  $V_{IN} = 0V$  and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When  $V_{IN} > V_{IN\_UVLO}$ , internal charge pump begins to open the load switch after debounce time (about 15ms). After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

## PCB LAYOUT CONSIDERATION

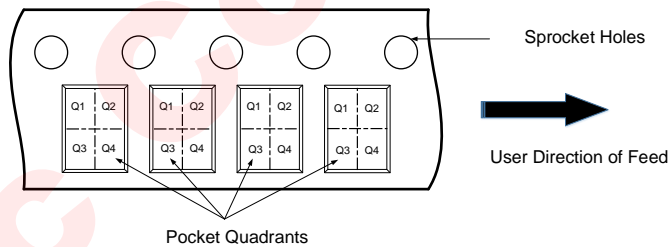
To obtain the optimal performance of AW327XX, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor  $C_{IN}$  on the top layer (same layer as the AW327XX) and close to IN pin, and place the output capacitor  $C_{OUT}$  on the top layer (same layer as the AW327XX) and close to OUT pin.
2. If external TVS is used, IN pin routing passes through the external TVS firstly, and then connect AW327XX.
3. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.
4. The path from device ground pins to the system ground plane must be as short as possible.
5. If  $R_1$  and  $R_2$  are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.
6. The power trace from USB connector to AW327XX may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.
7. Use rounded corners on the power trace from USB connector to AW327XX to decrease EMI coupling.

## TAPE AND REEL INFORMATION



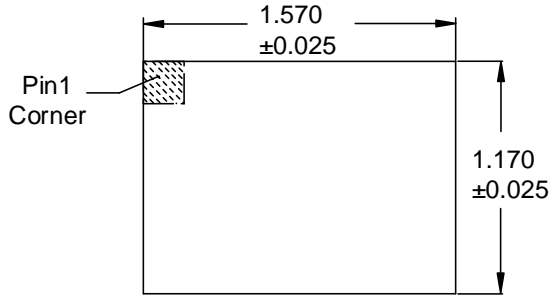
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



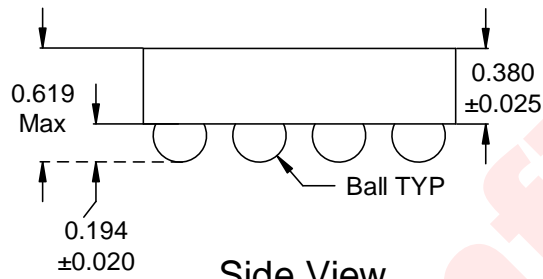
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.29	1.69	0.73	2.00	4.00	4.00	8.00	Q2

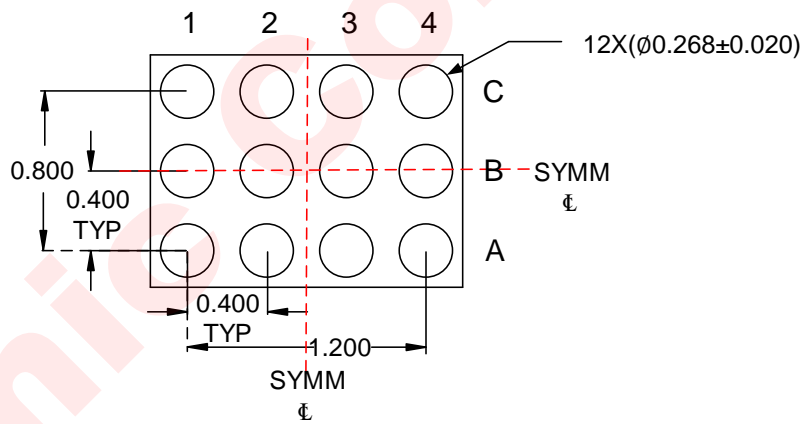
PACKAGE DESCRIPTION



Top View



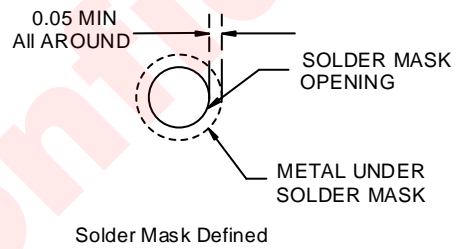
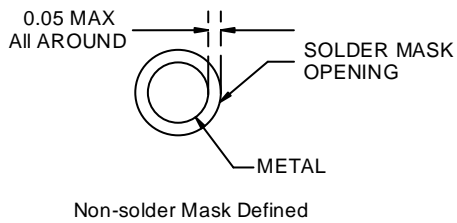
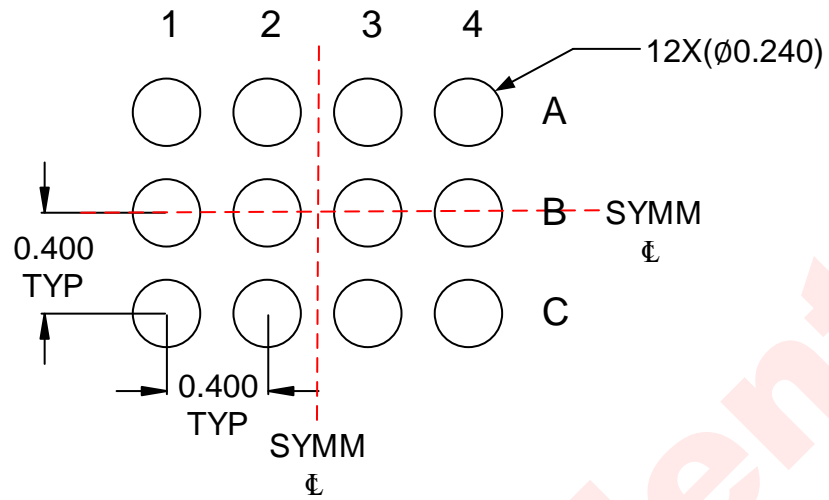
Side View



Bottom View

Unit: mm

LAND PATTERN DATA



Unit: mm

## REVISION HISTORY

Vision	Date	Change Record
V1.0	October 2018	Datasheet V1.0 Released

awinic Confidential



## DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.