

## USB Type-C Low Speed Ports Protection IC

### FEATURES

- IEC61000-4-5 surge protection
  - $\pm 80\text{V}$  surge protection on CON\_LSP1/2
- USB Type-C LSP1/2 DC protection
  - CON\_LSP1/CON\_LSP2: 16V DC
- Dead battery circuits in CON\_LSP1/CON\_LSP2
- Integrated low  $R_{\text{dson}}$  switch
  - LSP switch: 340m $\Omega$  typical
- IEC61000-4-2 ESD protection for CON\_LSP1/2
  - Contact discharge:  $\pm 12\text{kV}$
  - Air discharge:  $\pm 16\text{kV}$
- Default Over-Voltage Protection (OVP) threshold
  - CON\_LSP1/CON\_LSP2: 5.8V typical
- Low supply current: 20 $\mu\text{A}$  typical
- LSP1/2 leakage current: 0.5 $\mu\text{A}$  typical
- Fast OVP turn off time: 70ns typical
- Over-temperature protection (OTP)
- Under-voltage lockout (UVLO)
- WLCSP 1.82mm $\times$ 1.27mm-12B package

### APPLICATIONS

- Smartphones
- Tablets
- Laptop

### GENERAL DESCRIPTION

AW35611 is a single chip USB Type-C port protection solution, it integrates two channels of switches with OVP protection. CON\_LSP1/2 pins can tolerate up to 16V DC. LSP switch can be used to protect CC of Type-C.

AW35611 will disconnect both two channels of switches when any pin of CON\_LSP1/2 is above the OVP threshold, LSP1, LSP2 in system side are protected from the high voltage.

AW35611 integrates dead battery circuits in CON\_LSP1 and CON\_LSP2.

AW35611 integrates  $\pm 80\text{V}$  IEC61000-4-5 surge protection on CON\_LSP1 and CON\_LSP2, and also provides  $\pm 12\text{kV}$  contact discharge and  $\pm 16\text{kV}$  air discharge IEC61000-4-2 ESD protection on CON\_LSP1 and CON\_LSP2.

### TYPICAL APPLICATION CIRCUIT

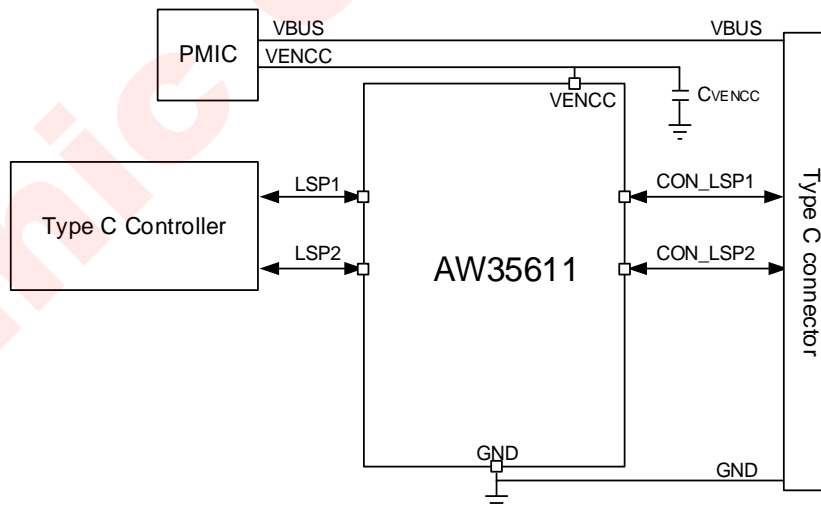


Figure 1 AW35611 typical application circuit

All the trademarks mentioned in the document are the property of their owners.

## PIN CONFIGURATION

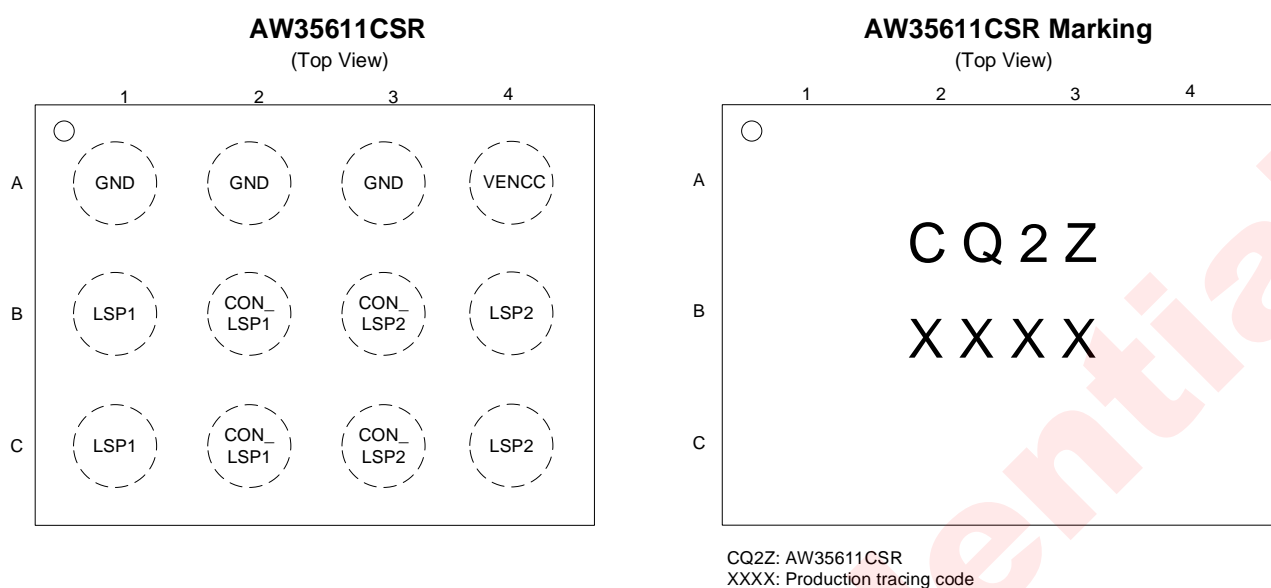


Figure 2 Pin Configuration

## PIN DEFINITION

Pin	Name	Description
A1,A2,A3	GND	Ground.
A4	VENCC	2.7V to 5.5V power supply.
B1,C1	LSP1	System side of the LSP1 OVP FET.
B2,C2	CON_LSP1	Connector side of the LSP1 OVP FET.
B3,C3	CON_LSP2	Connector side of the LSP2 OVP FET.
B4,C4	LSP2	System side of the LSP2 OVP FET.

FUNCTIONAL BLOCK DIAGRAM

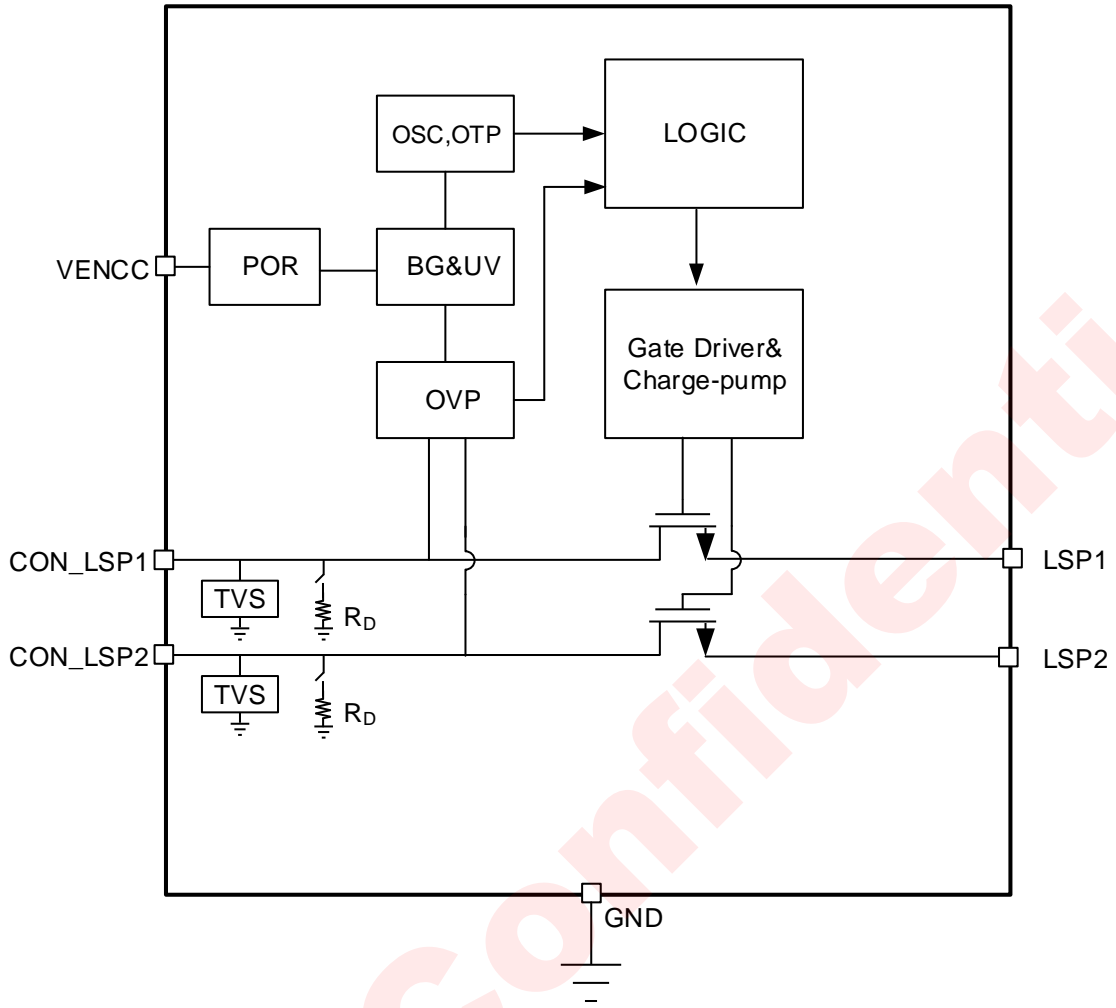


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

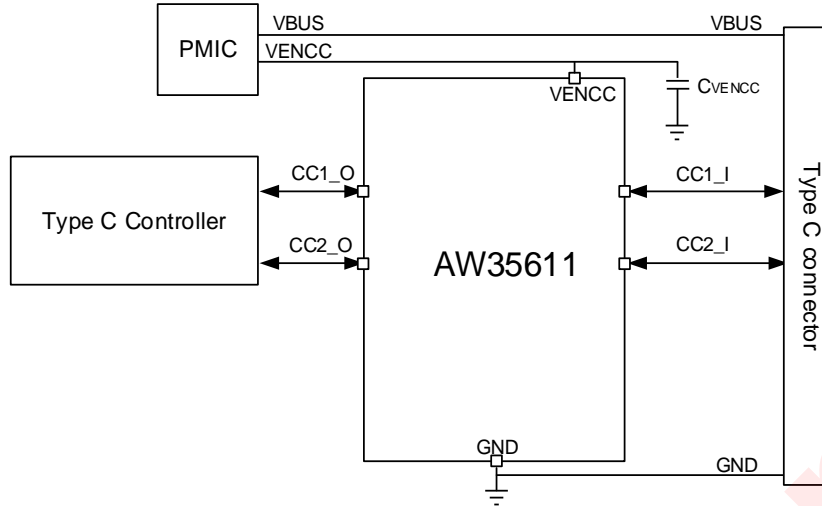


Figure 4 AW35611 application circuit (LSP switch used for CC switch)

Notice for Typical Application Circuits:

1. Place  $C_{VENCC}$  as close to the chip as possible.
2. CC1, CC2 channels support  $\pm 1A$  current, route the lines according to application current value.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35611CSR	-40°C ~ 85°C	WLCSP 1.82mm×1.27mm-12B	CQ2Z	MSL1	ROHS+HF	3000 units/ Tape and Reel

## ABSOLUTE MAXIMUM RATINGS <sup>(NOTE 1)</sup>

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>VENCC</sub>	Power voltage		-0.3	6	V
V <sub>CON_LSPX</sub>	CON_LSP1, CON_LSP2 input voltage		-0.3	16	V
V <sub>LSPX</sub>	LSP1, LSP2 output voltage		-0.3	6	V
I <sub>CON_LSPX</sub>	CON_LSP1, CON_LSP2 DC current		-1	1	A
T <sub>JMAX</sub>	Maximum operating junction temperature			150	°C
T <sub>STG</sub>	Storage temperature		-65	150	°C
T <sub>LEAD</sub>	Soldering temperature	At leads, 10 seconds		260	°C
CON_LSPX Surge	CON_LSP1, CON_LSP2 surge immunity	IEC61000-4-5 test with 2Ω equivalent series resistance	-80	80	V

NOTE1: Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

## THERMAL INFORMATION

Symbol	Parameter	Condition	Value	Unit
R <sub>θJA</sub>	Thermal resistance from junction to ambient <sup>(NOTE 1)</sup>	In free air	90	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

## ESD AND LATCH-UP RATINGS

Symbol	Parameter	Condition	Value	Unit
V <sub>ESD</sub>	IEC61000-4-2 system ESD on CON_LSP1,CON_LSP2	Contact discharge	±12	kV
		Air gap discharge	±16	kV
	Human body model	ANSI/ESDA/JEDEC JS-001	±2	kV
	Charged device model	JESD22-C101	±1.5	kV
I <sub>Latch-up</sub>	Latch up	JEDEC78	±200	mA

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>VENCC</sub>	Input DC voltage	2.7		5.5	V
V <sub>CON_LSPX</sub> , V <sub>LSPX</sub>	CON_LSP1,CON_LSP2,LSP1,LSP2 voltage	0		5.5	V
T <sub>A</sub>	Ambient temperature	-40		85	°C

## ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V<sub>VENCC</sub> = 3.3V, C<sub>VENCC</sub> = 1μF, T<sub>A</sub> = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
<b>Power supply and leakage current</b>						
V <sub>UVLO</sub>	Power under voltage lockout	V <sub>ENCC</sub> rising	2.30	2.50	2.70	V
V <sub>UVLO_HYS</sub>	Power under voltage lockout hysteresis			100		mV
I <sub>VENCC</sub>	VENCC supply current	V <sub>VENCC</sub> =3.3V, CON_LSPX floating, LSPX floating		20	60	μA
I <sub>LSP_Leak</sub>	Leakage current for LSP pins	V <sub>VENCC</sub> =3.3V, V <sub>LSPX</sub> =3.3V, CON_LSPX floating		0.5	3	μA
<b>LSP switches</b>						
R <sub>ON</sub>	Switch on resistance	V <sub>VENCC</sub> =3.3V, V <sub>LSPX</sub> =3.3V, I <sub>OUT</sub> = 100mA, T <sub>A</sub> = 25°C		340	600	mΩ
R <sub>ON_Flat</sub>	On resistance flatness	CON_LSPX input 100mA, sweep LSPX voltage between 0V and 3.3V, T <sub>A</sub> = 25°C		1	5	mΩ
R <sub>D</sub>	Dead battery pull-down resistance	V <sub>CON_LSPX</sub> =3.3V	4.1	5.1	6.1	kΩ
V <sub>CLAMPH</sub>	CON_LSPX clamp voltage	External current 330μA in CON_LSPX	0.85	1.80	2.45	V
V <sub>CLAMPM</sub>	CON_LSPX clamp voltage	External current 180μA in CON_LSPX	0.45	1.20	1.50	V
V <sub>CLAMPL</sub>	CON_LSPX clamp voltage	External current 80μA in CON_LSPX	0.25	1.10	1.50	V
V <sub>OVPLSP</sub>	OVP threshold on CON_LSPX	CON_LSPX rising	5.5	5.8	6.0	V
V <sub>OVPLSP_HYS</sub>	OVP threshold hysteresis			100		mV
CON_LSP	Equivalent on capacitance	Capacitance from CON_LSPX or LSPX to GND when device is powered. V <sub>C_LSPX</sub> /V <sub>LSPX</sub> = 0V to 1.2V, f = 240kHz		200		pF
BW <sub>LSP</sub>	Single ended on bandwidth (-3dB)	R <sub>L</sub> =50Ω, V <sub>LSPX</sub> =0.1V to 1.2V		20		MHz
V <sub>CLAMPLSP</sub>	Maximum clamp voltage on system side	8/20μs surge, V <sub>surge</sub> =+80V		7		V
<b>Thermal shutdown</b>						
T <sub>SDN</sub>	Shutdown temperature	Temperature rising		135		°C
T <sub>SDN_HYS</sub>	Shutdown temperature hysteresis			10		°C

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

T<sub>A</sub> = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V<sub>VENCC</sub> = 3.3V, C<sub>VENCC</sub> = 1μF, T<sub>A</sub> = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
<b>Timings requirements</b>						
t <sub>ON_FET</sub>	Power on delay time	Time from VENCC valid to LSP OVP FETs are on.		2.4		ms
t <sub>ON_FET_DB</sub>	Dead battery resistors valid time	Time from VENCC valid to the internal dead battery resistors are turned off		4.5		ms
t <sub>ovp_res</sub>	OVP response time	Time from crossing rising CON_LSPX at OVP voltage until LSPX stop rising. Rising rate is 70V/μs		70		ns
t <sub>ovp_deb_LSP</sub>	LSP switch recovery time after OVP removed			50		μs
t <sub>off_thermal</sub>	Time to shut down from over-temperature			20		μs
t <sub>OTP_deb</sub>	OTP recovery time			20		ms



TIMING DIAGRAM

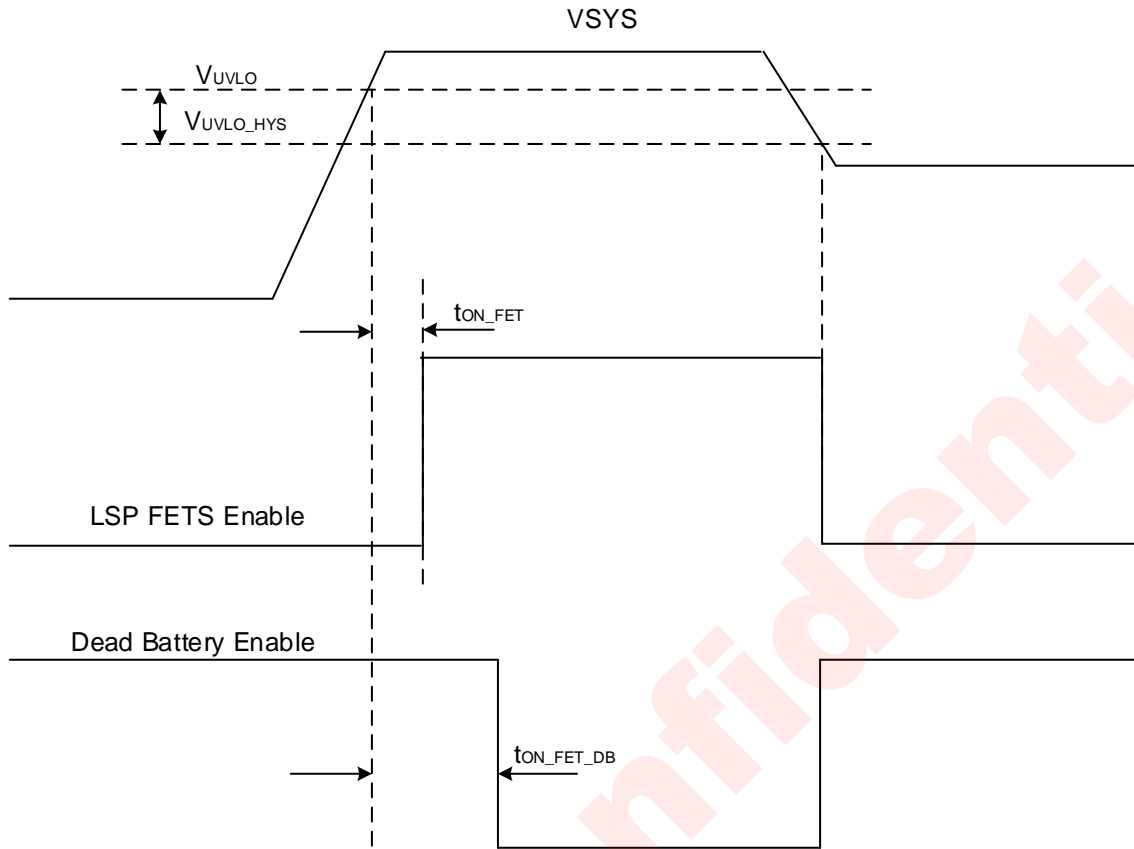


Figure 5 Power on and off Timing diagram

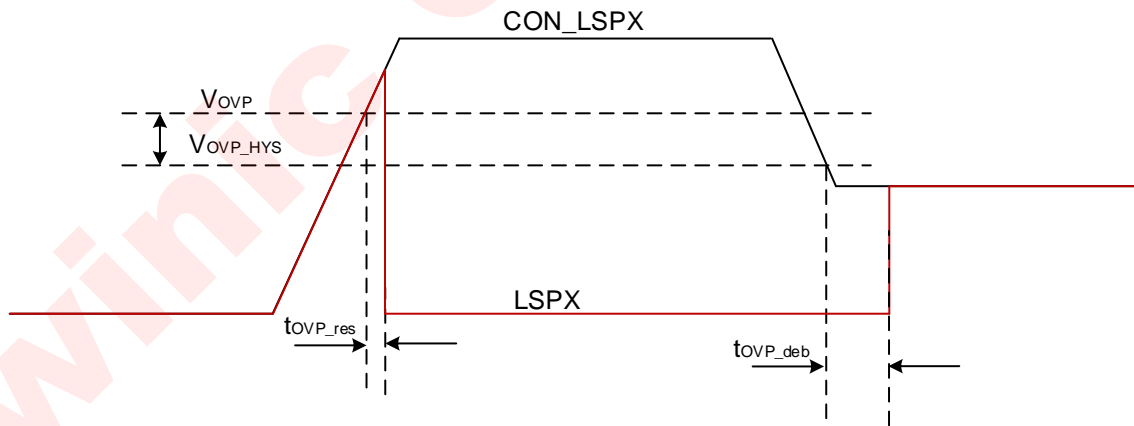
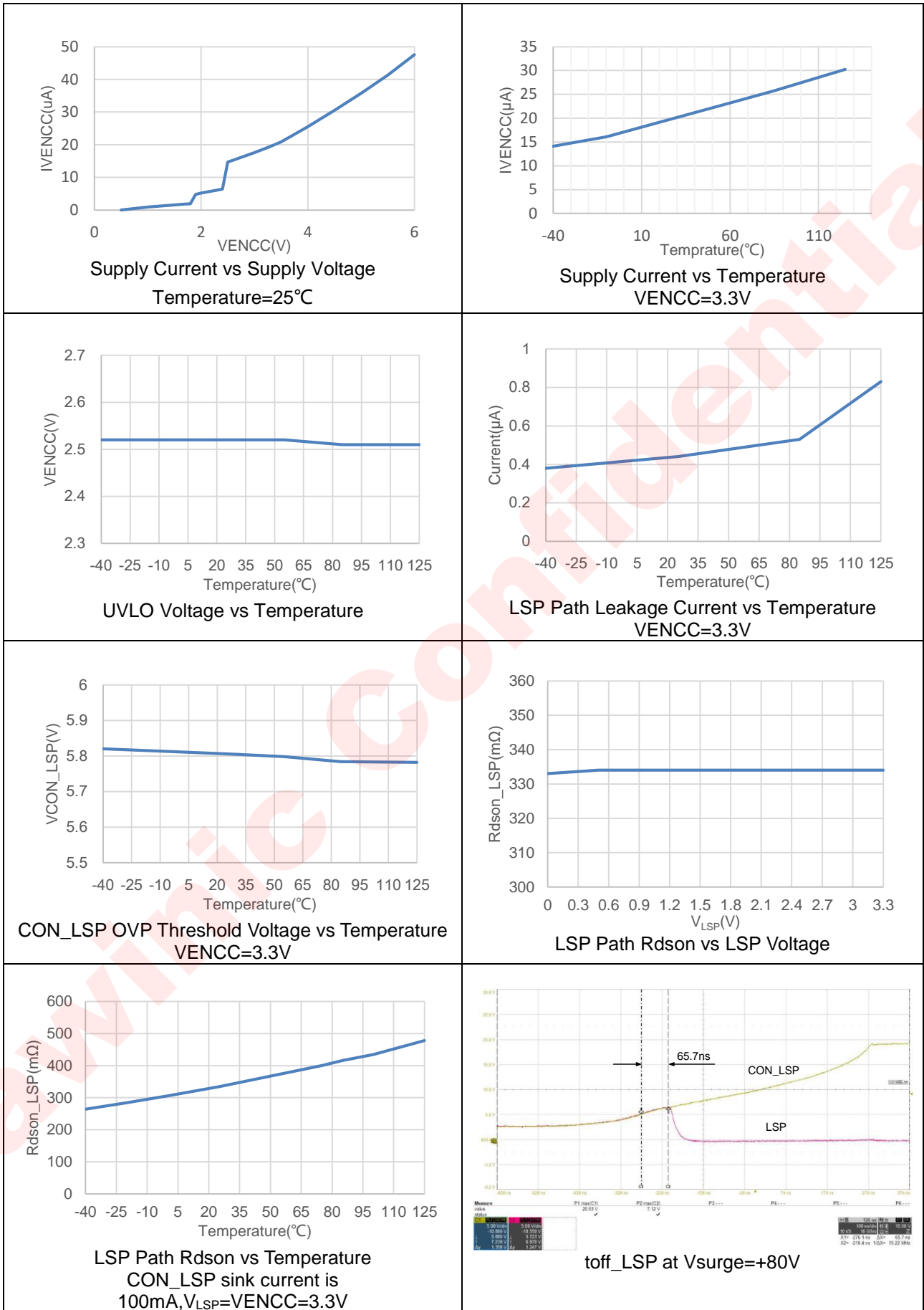


Figure 6 Over Voltage Protection Timing diagram

TYPICAL CHARACTERISTICS



## DETAILED FUNCTIONAL DESCRIPTION

The AW35611 is a single chip USB Type-C port protection solution, it integrates two channels of switches with over-voltage protection function that protect LSP1 and LSP2. The CON\_LSP1 and CON\_LSP2 pins of AW35611 are 16V DC tolerant, so they can be well protected if they are shorted to USB VBUS by accident or moisture.

### Surge and ESD Protection

AW35611 integrates  $\pm 80\text{V}$  IEC61000-4-5 surge protection on CON\_LSP1 and CON\_LSP2, and also provides  $\pm 12\text{kV}$  contact discharge and  $\pm 16\text{kV}$  air discharge IEC61000-4-2 ESD protection on CON\_LSP1 and CON\_LSP2, so no external TVS are needed on these two pins, which helps to reduce external BOM cost.

### LSP Switch Power Delivery

The typical on-resistance of the integrated switches of LSP1 and LSP2 is  $340\text{m}\Omega$ , the two switches are both able to deliver 1A DC current, which is compliant with the USB Type-C specification.

### LSP Dead Battery Resistors

AW35611 integrates dead battery pull-down resistors on CON\_LSP1 and CON\_LSP2 pins to allow dead battery charging. In dead battery condition, the AW35611 is unpowered, the pull-up resistor from a power adaptor will activate the pull-down resistor inside the AW35611. Once power delivery is established from power adaptor to the system and AW35611 has power supply on its VENC pin, after about 2.4ms the AW35611 turns on its LSP switches and after about another 2.1ms it removes its  $R_D$  pull-down resistors.

### Over-Voltage Protection

The two channels of integrated switches of AW35611 all have over-voltage protection function, when over-voltage event is detected on any pin of CON\_LSP1, CON\_LSP2, device will shut off all the switches within 70ns (typical). The typical OVP threshold voltage of CON\_LSP1 and CON\_LSP2 is 5.8V.

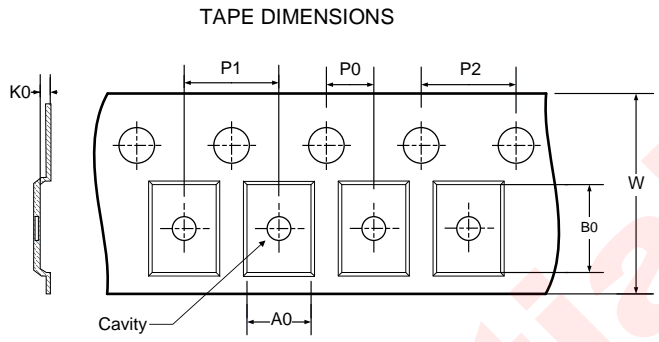
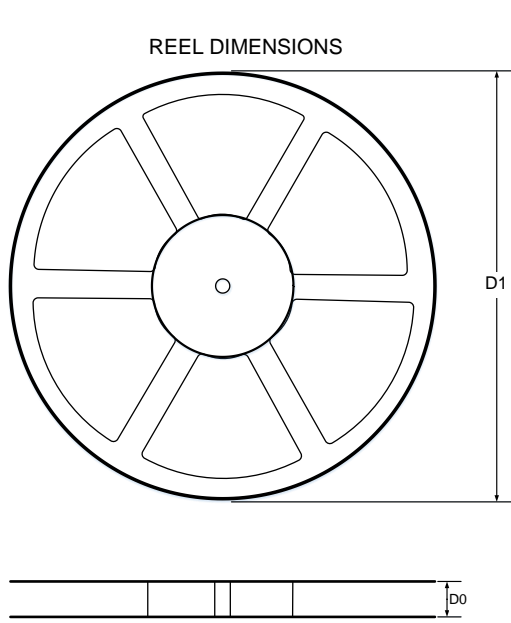
## PCB LAYOUT CONSIDERATION

To obtain the optimal performance of AW35611, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to VENCC pin as possible.
2. LSP1, LSP2 channels support  $\pm 1\text{A}$  current, route the lines according to application current value.

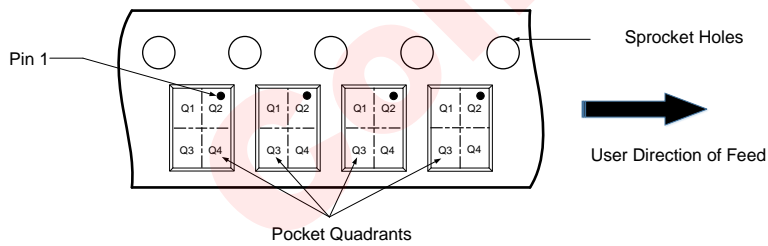
awinic Confidential

TAPE AND REEL INFORMATION



- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width

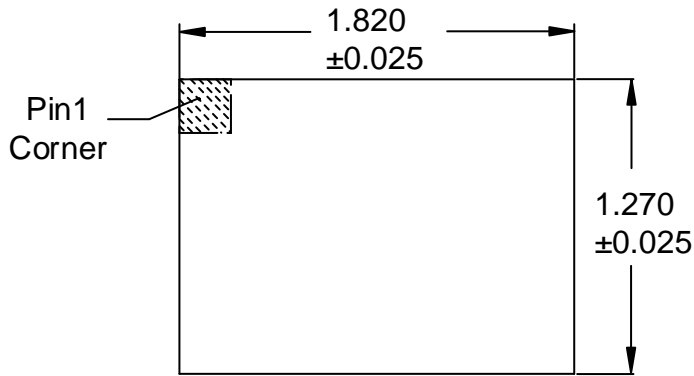
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



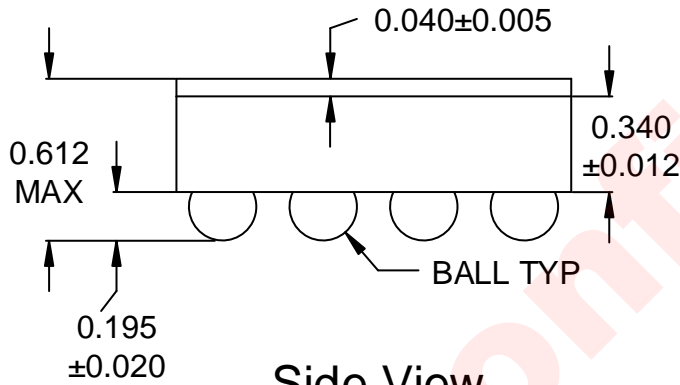
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.37	1.94	0.69	2.00	4.00	4.00	8.00	Q2

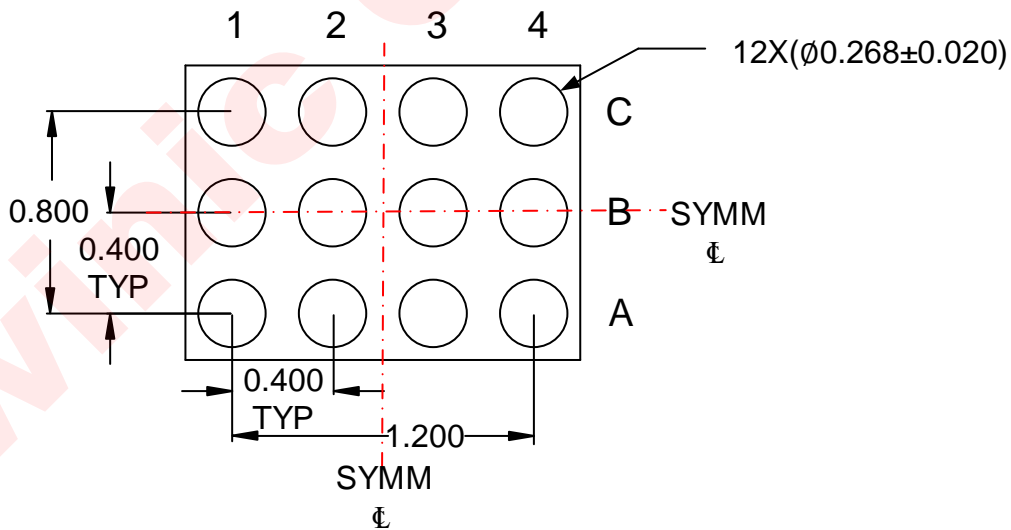
PACKAGE DESCRIPTION



Top View



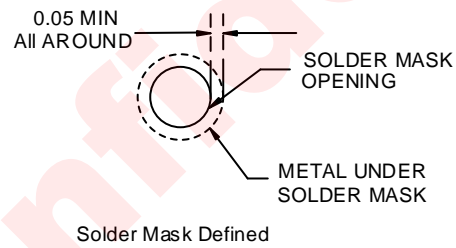
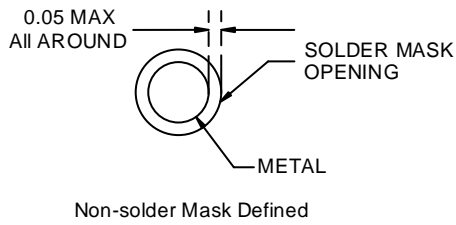
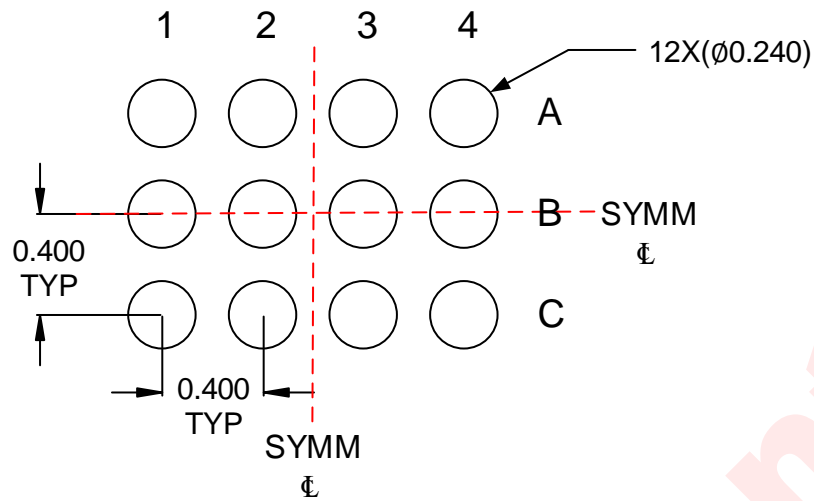
Side View



Bottom View

Unit: mm

LAND PATTERN DATA



Unit: mm

**REVISION HISTORY**

<b>Version</b>	<b>Date</b>	<b>Change Record</b>
V1.0	Jan.2019	First version

awinic Confidential



**DISCLAIMER**

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.