DPDT USB Switch With Over Voltage Protection

Features

- USB 2.0 Hi-speed DPDT switch
- Typical -3dB bandwidth: 1.0 GHz
- Over voltage protection : 4.8V typical
- 16V DC protection on D+ and D- Ports
- +25V surge protection on D+ and D-
- Supply voltage range: 2.7V to 5.5V
- 5Ω switch on-resistance typical
- C_{ON}: 6pF typical
- I_{CC}: 35μA typical
- FCQFN 1.5mm X2.0mm X0.55mm-10L package

General Description

The AW35742 is a Hi-Speed USB 2.0(480Mbps) DPDT (Double Pole Double Throw) switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch.

The AW35742 protection on the D+/D- pins can tolerate up to 16V DC, when D+ or D- voltage is greater than the OVP(Over-Voltage Protection) threshold, the switch will be automatically shutoff to protect downstream devices.

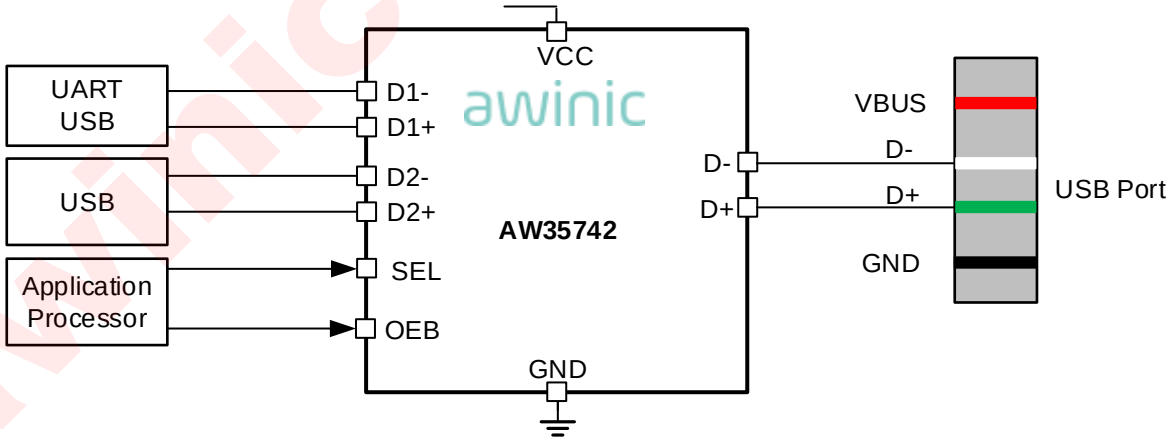
The device operates over 2.7V to 5.5V supply range.

The AW35742 is available in an FCQFN 1.5mm X2.0mm X0.55mm-10L package.

Applications

- Smartphones
- Tablets

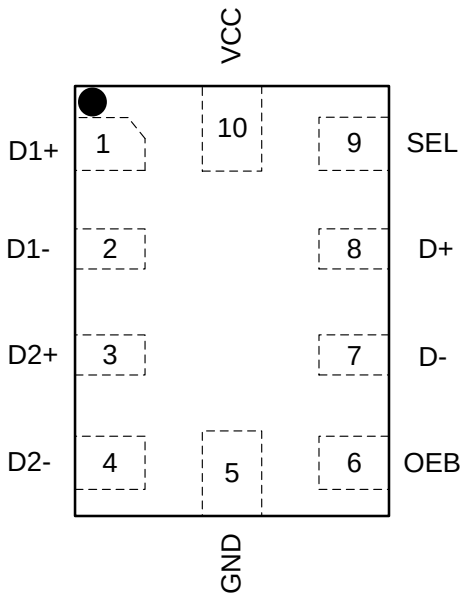
Typical Application Circuit



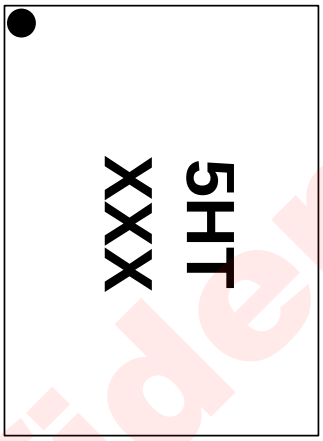
Typical Application Circuit of AW35742

Pin Configuration And Top Mark

AW35742FCR
（Top View）



AW35742FCR Marking
（Top View）



5HT – AW35742FCR
XXX – Production Tracing Code

Pin Configuration And Top Mark

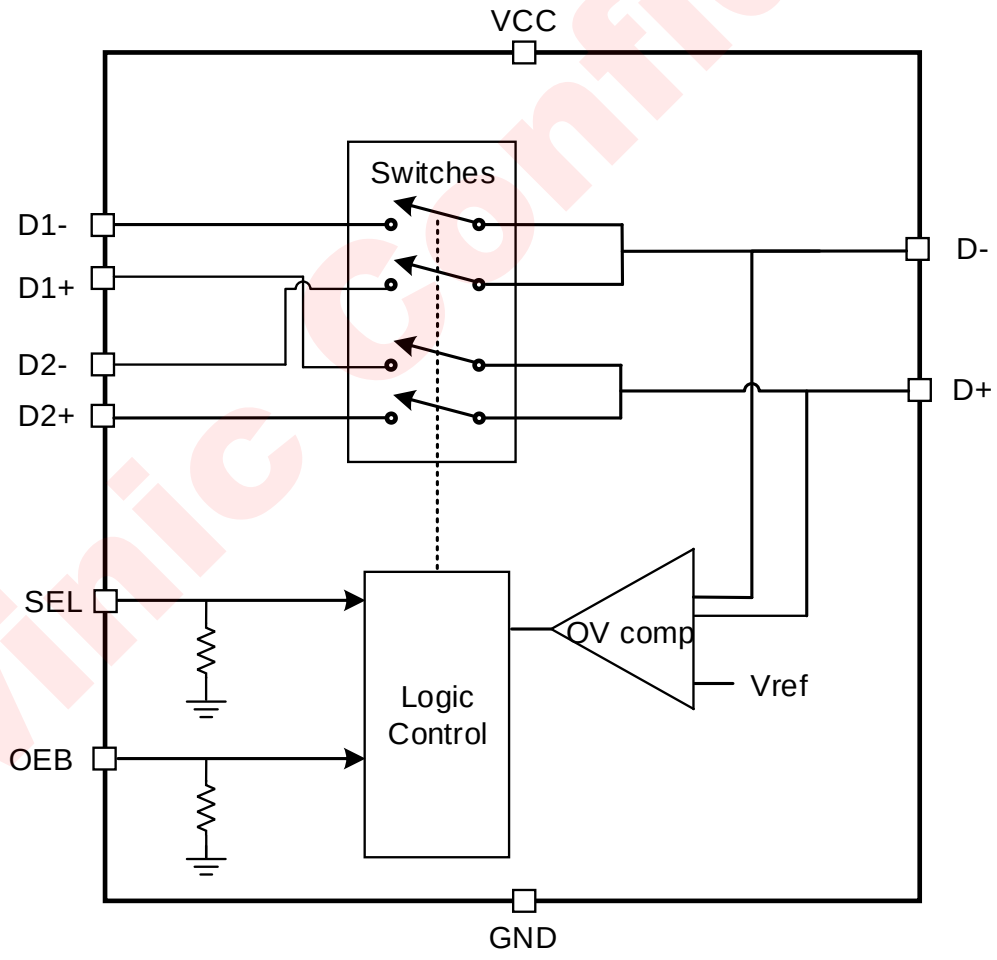
Pin Definition

No.	NAME	DESCRIPTION
1	D1+	Multiplexed high speed data port1, differential +
2	D1-	Multiplexed high speed data port1, differential -
3	D2+	Multiplexed high speed data port2, differential +
4	D2-	Multiplexed high speed data port2, differential -
5	GND	Ground
6	OEB	Output enable, active low
7	D-	Common high speed data port, differential -
8	D+	Common high speed data port, differential +
9	SEL	Switch select, active high
10	VCC	Supply voltage

Pin Functions

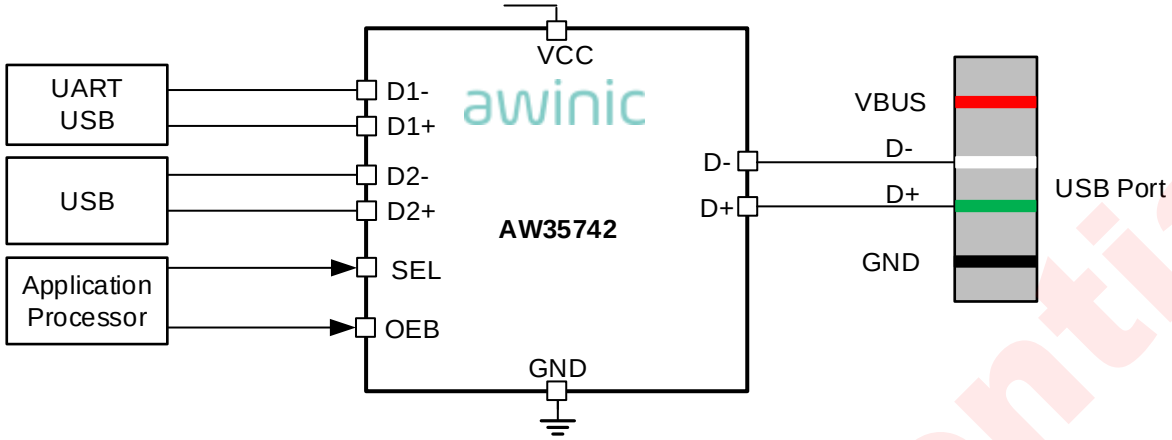
OEB	SEL	D- CONNECTION	D+ CONNECTION
H	X	High-Z	High-Z
L	L	D- to D1-	D+ to D1+
L	H	D- to D2-	D+ to D2+

Functional Block Diagram



Functional Block Diagram

Typical Application Circuits



Typical Application Circuit of AW35742

Notice for Typical Application Circuits:

1. The AW35742 has internal 7-MΩ pull down resistors on SEL and OEB, so no external resistors are required on the logic pins.
2. Internal pull-down resistor on SEL pins ensures the D1+ and D1- channels are selected by default.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35742FCR	-40°C～85°C	FCQFN 1.5mm X2.0mm -10L	5HT	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.3V to 6V
Input/Output DC voltage(D+, D-)		-0.3V to 16V
Input/Output DC voltage(D1+, D1-, D2+, D2-)		-0.3V to 6V
Input voltage range	SEL, OEB	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		95°C/W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
Human Body Model (All pins, per ANSI/ESDA/JEDEC JS-001)		±2kV
Charged Device Model (All pins, per JESD22-C101)		±1.5kV
Latch-Up		
Test condition: JEDEC78		±200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

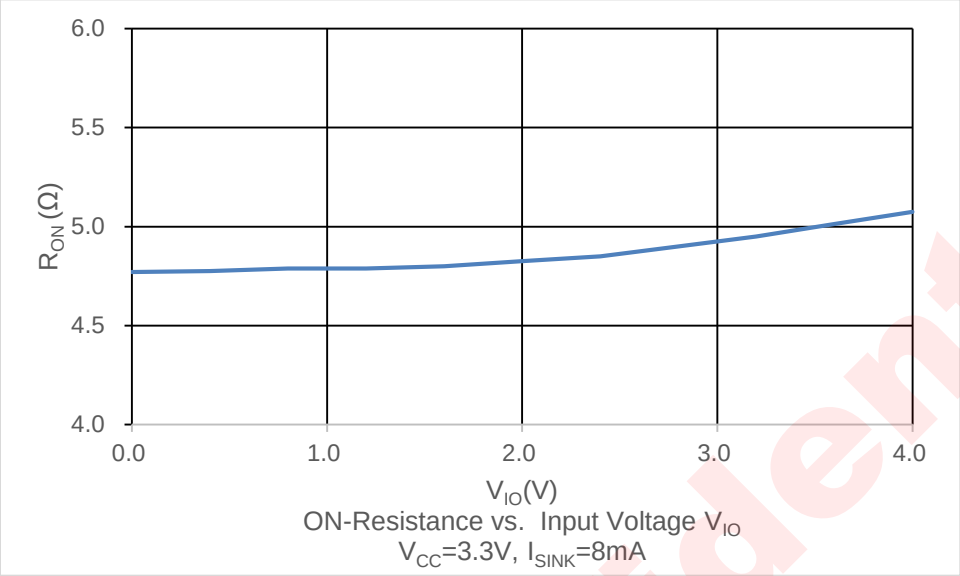
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	5.5	V
I_{CC}	Active supply current	OEB=0V SEL =0V 0V< $V_{D\pm}$<3.6V		35	50	μA
I_{CC_PD}	Standby supply current	OEB= V_{CC} SEL= 0V		9.5		μA
DC Characteristics						
R_{ON}	On-state resistance	$V_{I/O}$=0.4V, I_{SINK}=8mA		5		Ω
ΔR_{ON}	On-state resistance match between channels	$V_{I/O}$=0.4V, I_{SINK}=8mA		0.1		Ω
$R_{ON(FLAT)}$	ON-state resistance flatness	$V_{I/O}$=0V to 0.4V, I_{SINK}=8mA		0.1		Ω
I_{OFF}	I/O pin OFF leakage current on D+/D-	$V_{D\pm}$ = 0 V or 3.6 V $V_{D1\pm}$ or $V_{D2\pm}$ = 3.6 V or 0 V			10	μA
I_{ON}	ON leakage current on D+/D-	$V_{D\pm}$ = 0 V or 3.6 V $V_{D1\pm}$ and $V_{D2\pm}$ = high-Z		2	10	μA
Digital Characteristics						
V_{IH}	Input logic high	SEL, OEB	1.4		V_{CC}	V
V_{IL}	Input logic low	SEL, OEB			0.4	V
R_{PD}	Internal pull-down resistor on digital input pins			7		MΩ
Protection						
V_{OVP_TH}	OVP threshold	D+/D- rising	4.4	4.8	5.4	V
V_{OVP_HYST}	OVP threshold hysteresis			60		mV
V_{CLAMP_V}	Clamping voltage on $D_{1\pm}$ and $D_{2\pm}$ pins during surge	8/20 μs surge test, OEB=0V, R_L = open			9	V
t_{CLAMP}	Clamp time during OVP	8/20 μs surge test, OEB=0V, R_L = open		2	5	μs

Electrical Characteristics (Continued)

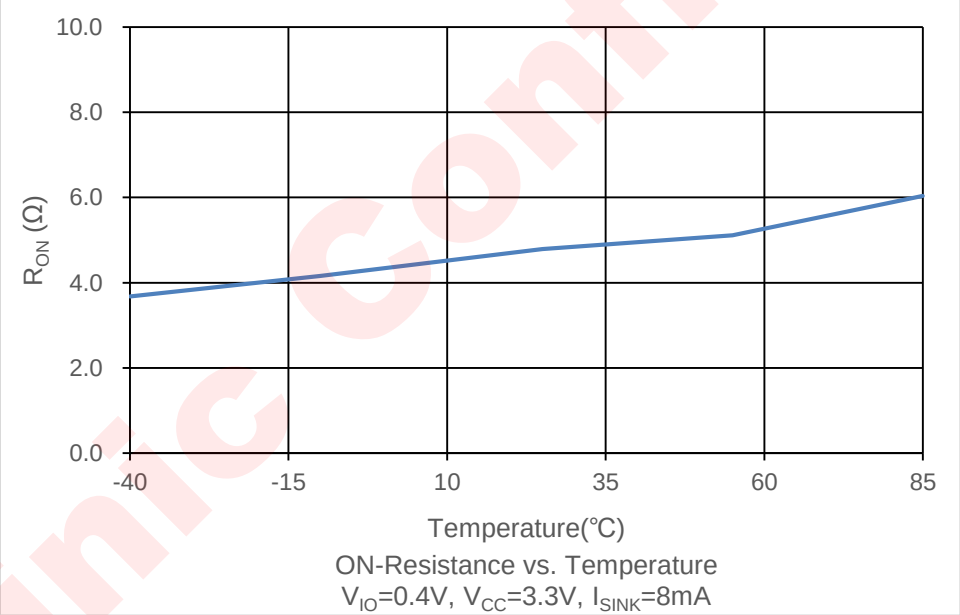
T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Dynamic Characteristics						
C_{ON}	IO pins ON capacitance	$V_{D±}$= 0 or 3.3 V, f = 240 MHz, switch ON		6		pF
O_{ISO}	Differential off isolation	R_L = 50 Ω C_L = 5 pF f = 100 kHz, switch OFF		-60		dB
		R_L = 50 Ω C_L = 5 pF f = 240MHz, switch OFF		-20		dB
X_{TALK}	Channel to channel crosstalk	R_L = 50 Ω C_L = 5 pF f = 100 kHz, switch ON		-60		dB
BW	-3dB bandwidth	R_L = 50 Ω, switch ON		1.0		GHz
t_{switch}	Switching time between channels (SEL1, SEL2 to output)	$V_{D±}$ = 0.8 V R_L = 50 Ω C_L = 5 pF, V_{CC} = 2.7 V to 5.5 V		1.5	5	μs
t_{on}	Device turn on time (OEB to output)			15		μs
t_{off}	Device turn off time (OEB to output)			1.5		μs
t_{pd}	Propagation delay	$V_{D±}$ = 0.4 V R_L = 50 Ω,C_L = 5 pF, V_{CC} = 2.7 V to 5.5 V		200		ps

Typical Characteristics



ON-Resistance vs. Input Voltage V_{IO}
V_{CC}=3.3V, I_{SINK}=8mA



ON-Resistance vs. Temperature
V_{IO}=0.4V, V_{CC}=3.3V, I_{SINK}=8mA

Detailed Functional Description

The AW35742 is a Hi-Speed USB 2.0 DPDT switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch. The AW35742 will protect D+ and D- pins when stressed with voltages up to 16V. The device can pass signals with bandwidth 1GHz to maintain signal integrity and eye compliance.

Over-Voltage Protection

AW35742 is designed to protect the system from damage. Over-voltage event happens when voltage on D+/D- exceeds 4.8V(typ.), and device will activate OVP to disconnect the switches.

High Impedance Mode

When OEB is logic high, the AW35742 is in high impedance mode, all the signal paths are in Hi-Z state.

OEB	SEL	D- Connection	D+ Connection
H	X	High-Z	High-Z
L	L	D- to D1-	D+ to D1+
L	H	D- to D2-	D+ to D2+

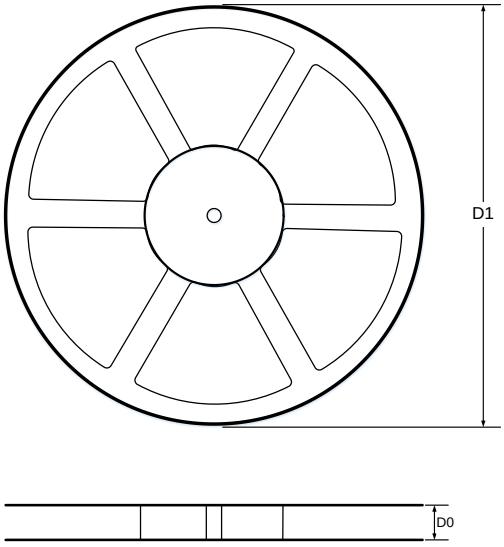
PCB Layout Consideration

To obtain the optimal performance of AW35742, PCB layout should be considered carefully. Here are some guidelines:

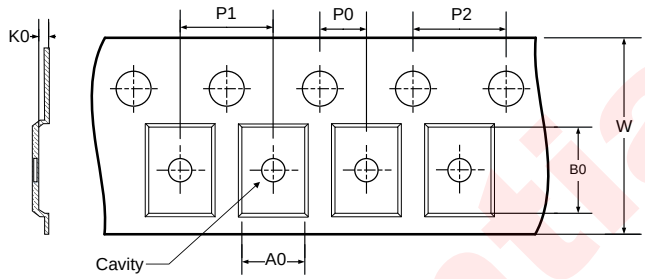
1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass capacitors near the D+/D- traces.
2. The differential characteristic impedance of D+ and D- traces is suggested to be 90Ω, and it's better to shield D+ and D- traces by ground planes.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals because they cause signal reflections.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Tape And Reel Information

REEL DIMENSIONS

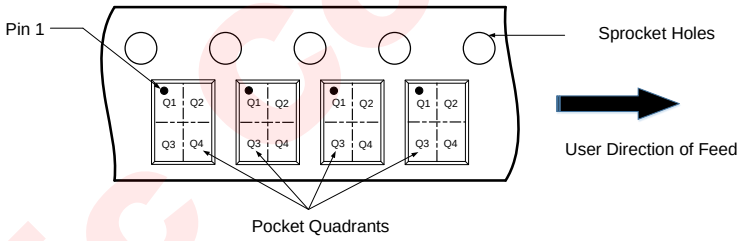


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

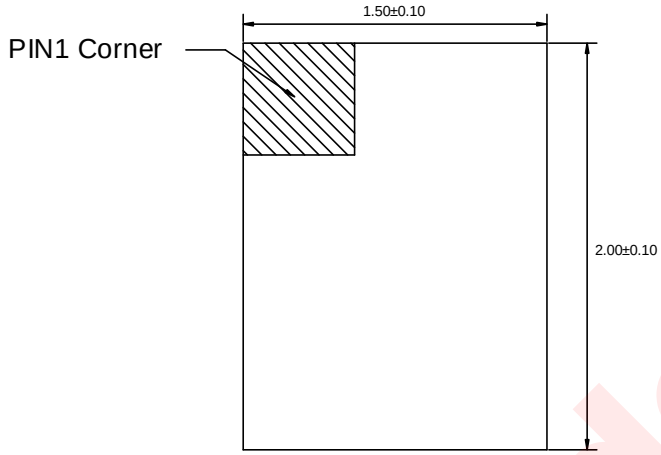
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



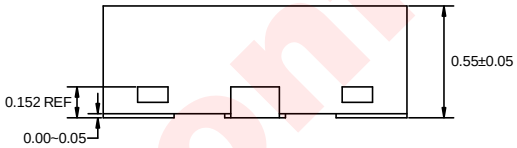
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.40	1.75	2.30	0.75	2	4	4	8	Q1

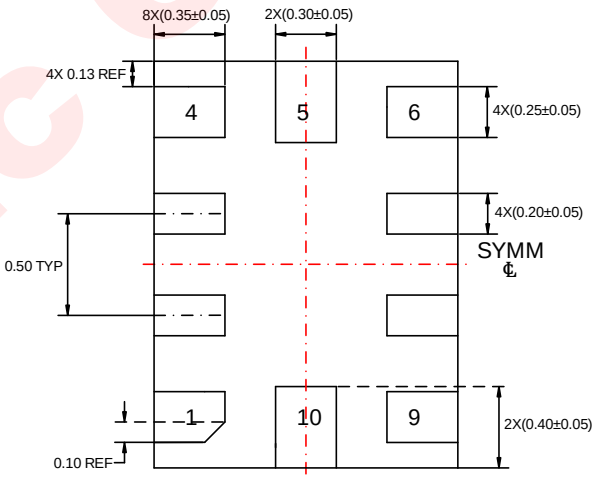
Package Description



Top View



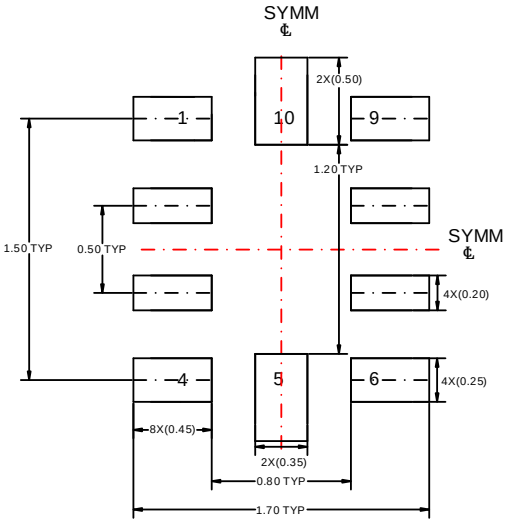
Side View

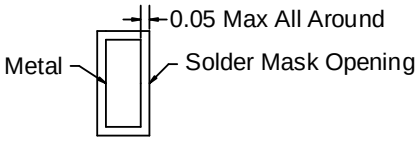


Bottom View

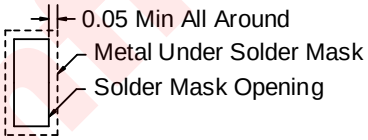
Unit: mm

Land Pattern Data





Non-solder Mask Defined



Solder Mask Defined

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Feb 2019	Datasheet V1.0 released

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