High Efficiency, 1.5A Flash LED Driver

FEATURES

- 1.5A Accurate and Programmable LED Current Source
  - Flash:23.4mA~1.5A，64 levels 23.44mA/level
  - Torch:5.4mA~376mA，64 levels 5.88mA/level
  - Flash Timeout：40ms~1.6s，16 levels
  - Flash/Torch/IR Mode
- High Efficiency: 85%
- Optimized Flash LED Current During Low Battery Conditions (IVFM)
- Hardware Strobe Enable (STROBE)
- Synchronization Input for RF Power Amplifier Pulse Events (TX)
- 400kHz I^2C:AW3642（I^2C Address=0x63）
- 0.5mm Pitch, CSP-9 Package

APPLICATION

Smartphone Camera Flash

GENERAL DESCRIPTION

The AW3642 is a LED flash driver that provides a high level of adjustability within a small solution size. The AW3642 utilizes a 2MHz or 4MHz fixed-frequency synchronous boost converter to provide power to the 1.5A constant current LED sources. The 64 levels current source provides the flexibility to adjust the current of LED in Flash/Torch/IR modes. The AW3642 provides three IVFM protection modes to prevent system reset or shutdown under low battery condition.

The AW3642 is controlled via an I^2C-compatible interface. The main features of the AW3642 include: flash/torch current, flash timeout duration, IVFM, TX interrupt. The AW3642 also provides hardware flash pins (STROBE) to control flash events.

The 2MHz or 4MHz switching frequency options, overvoltage protection (OVP), and adjustable current limit allow for the use of tiny, low-profile inductors and 10-µF ceramic capacitors. The device operates over a –40°C to +85°C ambient temperature range.

The AW3642 is available in small 0.5mm pitch 1.630mm×1.330mm CSP-9 package.

TYPICAL APPLICATION CIRCUIT

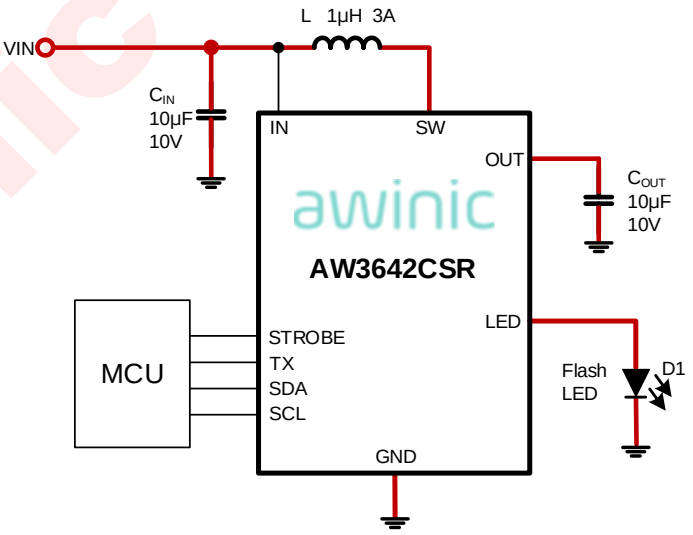
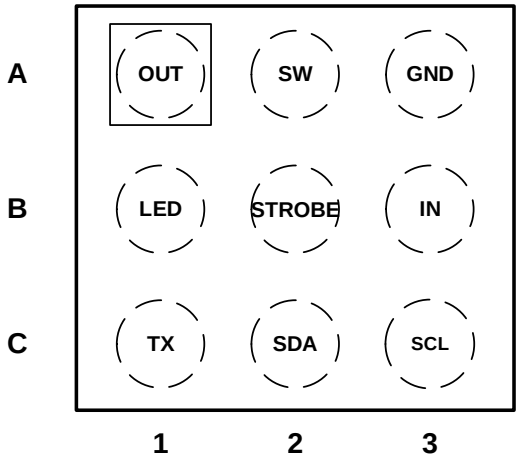


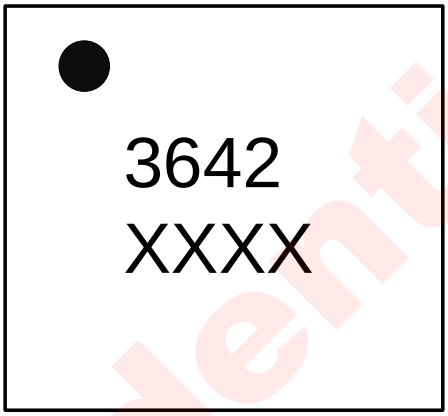
Fig 1 Typical Application Circuit of AW3642

PIN CONFIGURATION AND TOP MARK

AW3642CSR Pin Configuration (Top View)



AW3642CSR Top Mark (Top View)



3642 – AW3642CSR
XXXX – Manufacture Tracking Code

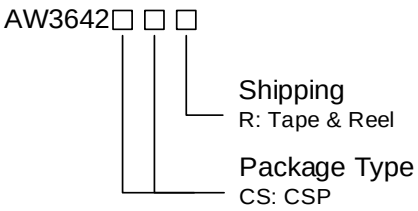
Fig 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	TYPE	DESCRIPTION
A1	OUT	Power	Step-up DC-DC converter output. Connect a 10μF ceramic capacitor between OUT and GND.
A2	SW	Power	Switch pin of the step-up DC-DC convertor.
A3	GND	Ground	Ground
B1	LED	Power	High-side current source output for flash LED.
B2	STROBE	I/O	Active high hardware flash enable. Drive STROBE high to turn on Flash pulse. Internal pull down resistor of 300kΩ between STROBE and GND.
B3	IN	Power	Input voltage connection. Connect IN to GND with a 10μF or larger ceramic capacitor.
C1	TX	I/O	Power amplifier synchronization input. Internal pull down resistor of 300kΩ between TX and GND.
C2	SDA	I/O	Serial data input/output of the I^2C interface.
C3	SCL	I/O	Serial clock input of the I^2C interface.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW3642 CSR	-40°C～85°C	1.630mm×1.330mm CSP-9	3642 XXXX	MSL1	ROHS+HF	3000 units/ Tape and Reel



AWINIC FLASH LED DRIVER SERIES

Product	Channels	Type	Description	Package
AW3644	2	Boost	High Efficiency, Dual Independent 1.5A Flash LED Driver	CSP-12
AW36414	2	Boost	High Efficiency, Dual Independent 1.5A Flash LED Driver	CSP-12
AW3643	2	Boost	High Efficiency, Dual 1.5A Flash LED Driver	CSP-12
AW36413	2	Boost	High Efficiency, Dual 1.5A Flash LED Driver	CSP-12
AW3648	1	Boost	High Efficiency, 1.5A Flash LED Driver	CSP-12
AW3642	1	Boost	High Efficiency, 1.5A Flash LED Driver	CSP-9
AW3641E	1	Charge Pump	Flash Current & Flash Timer Programmable 1A Flash LED Driver	DFN-10L
AW36402	1	Current Sink	200mA 1-wire Configurable Front Flash LED Driver with Ultra Small Package	DFN-6L
AW36404	1	Current Sink	400mA 1-wire Configurable Front Flash LED Driver with Ultra Small Package	DFN-8L
AW36406	1	Current Sink	600mA PWM Configurable Front Flash LED Driver with Ultra Small Package	DFN-8L

TYPICAL APPLICATION CIRCUITS

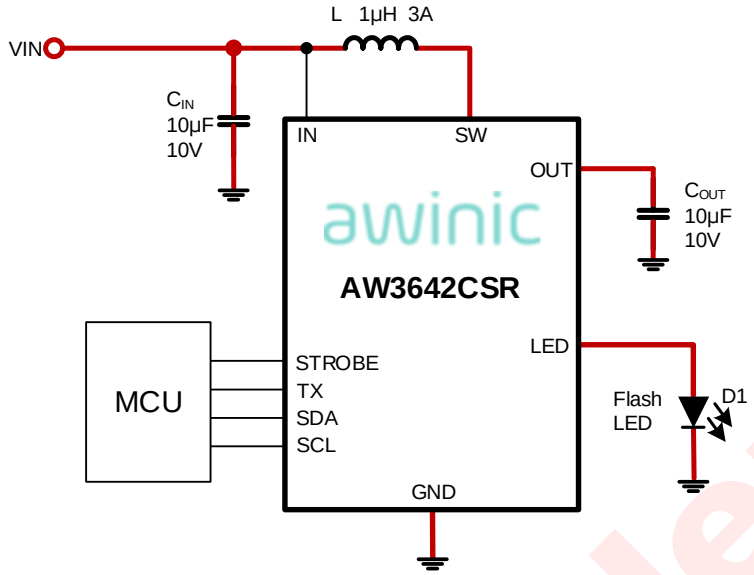


Fig 3 AW3642 Application Circuit

Notice for Typical Application Circuits:

1: Please place C_{IN}, C_{OUT} as close to the chip as possible.

2: Connect the inductor on the top layer close to the SW pin.

3: For the sake of driving capability, the power lines, output lines, and the connection lines of L and LED should be short and wide as possible.

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		Range	Unit
IN, SW, OUT, LED		-0.3 to 6	V
SCL, SDA, STROBE, TX		−0.3 to (VIN+0.3)	V
Continuous power dissipation		Internally limited	
Max Junction Temperature T_{JMAX}		155	°C
Storage Temperature T_{STG}		-65 to 150	°C
Maximum lead temperature (soldering)		260	°C
Junction to Ambient Thermal Resistance θ_{JA}		90.2	°C /W
ESD, All Pins(NOTE2)	HBM	±2000	V
	MM	±200	V
	CDM	±2000	V
Latch-Up JEDEC STANDARD NO.78B DECEMBER 2008		+IT：+350 -IT：-350	mA

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	Range	Unit
V_{IN}	2.7 to 5.5	V
Junction temperature (T_J)	-40 to 125	°C
Ambient temperature (T_A)	-40 to 85	°C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

ELECTRICAL CHARACTERISTICS

Typical limits tested at T_A=25℃. Minimum and maximum limits apply over the full operating ambient temperature range(-40℃≤T_A≤85℃). Unless otherwise specified, V_{IN}=3.6V.

Symbol	Description	Test Condition	Min	Typ	Max	Unit
Vin Supply						
V_{IN}	Input operating range		2.7		5.5	V
I_Q	Quiescent supply current	Device not switching, pass mode		0.4	0.8	mA
I_{SB}	Standby supply current	Device disabled, 2.7V≤VIN≤5.5V		1.5	10	μA
UVLO	Under voltage lockout threshold	Falling V_{IN}		2.5		V
		Rising V_{IN}		2.6		V
Current Source Specifications						
I_{LED}	Current source accuracy	V_{OUT}=4V, flash code=0x3F=1.5A	-7%	1.5	7%	A
		V_{OUT}=4V, torch code=0x1F=188mA	-10%	188	10%	mA
V_{OVP}	V_{OUT} over-voltage protect threshold	ON threshold	4.85	5	5.15	V
		OFF threshold	4.75	4.9	5.05	
Boost Converter Specifications						
R_{PMOS}	PMOS switch on-resistance			85		mΩ
R_{NMOS}	NMOS switch on-resistance			60		mΩ
I_{CL}	Switch current limit	Reg 0x07, bit[0]=0	-12%	1.9	12%	A
		Reg 0x07, bit[0]=1	-12%	2.8	12%	
F_{SW}	Switching frequency	Reg 0x07, bit[1]=0	-6%	2	6%	MHz
		Reg 0x07, bit[1]=1	-6%	4	6%	
V_{IVFM}	Input voltage flash monitor trip threshold	Reg 0x02, bits[3:1]=”000”	-3%	2.9	3%	V
T_{SD}	Thermal shutdown threshold			155		℃
	Thermal shutdown hysteresis			20		
I^2C-Compatible Interface Specifications(SCL,SDA)						
V_{IL}	Input logic low		0		0.4	V
V_{IH}	Input logic high		1.2		V_{IN}	V
V_{OL}	Output logic low	I_{LOAD}=3mA			0.4	V

STROBE, TX Voltage Specifications						
V_{IL}	Input logic low		0		0.4	V
V_{IH}	Input logic high		1.2		V_{IN}	V
R_{PD}	Internal pull down resistors			300		kΩ

I²C INTERFACE TIMING

Symbol	Description		Min	Typ	Max	Units
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

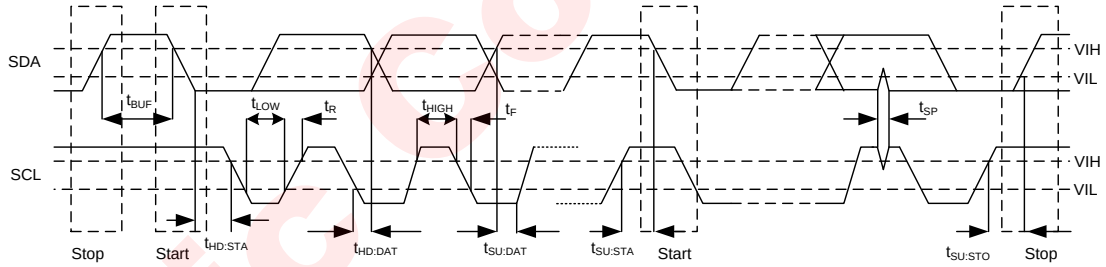


Fig 4 I²C INTERFACE TIMING

TYPICAL CHARACTERISTICS

Ambient temperature is 25°C, input voltage is 3.6 V, C_{IN} = C_{OUT} = 2×10 μF and L=1 μH, unless otherwise noted .

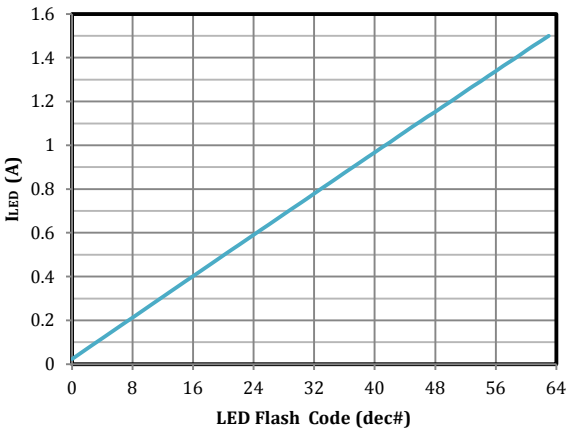


Fig 5. LED Flash Current vs Brightness Code

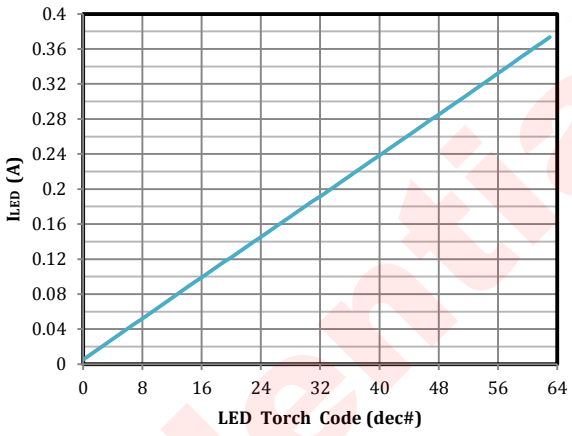


Fig 6. LED Torch Current vs Brightness Code

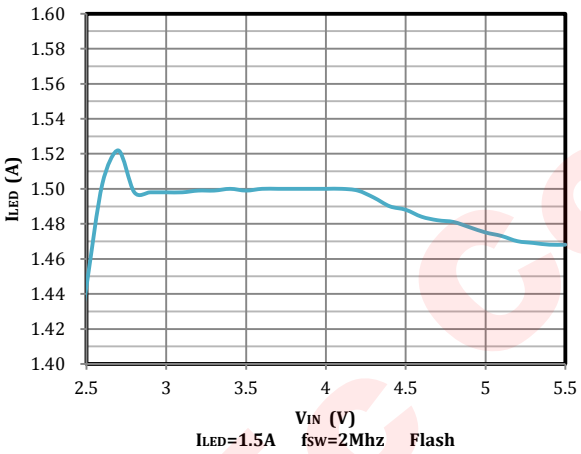


Fig 7. LED Flash Current vs Input Voltage

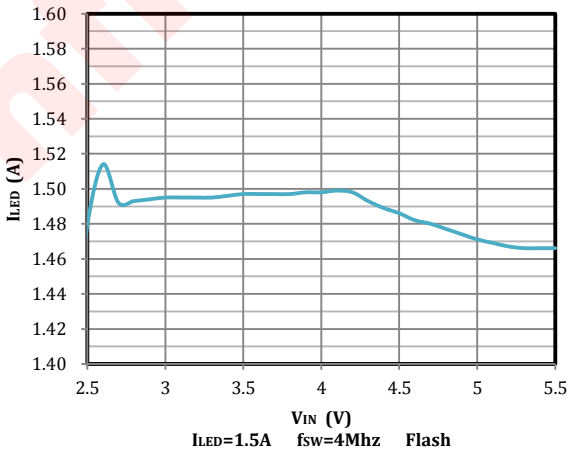


Fig 8. LED Flash Current vs Input Voltage

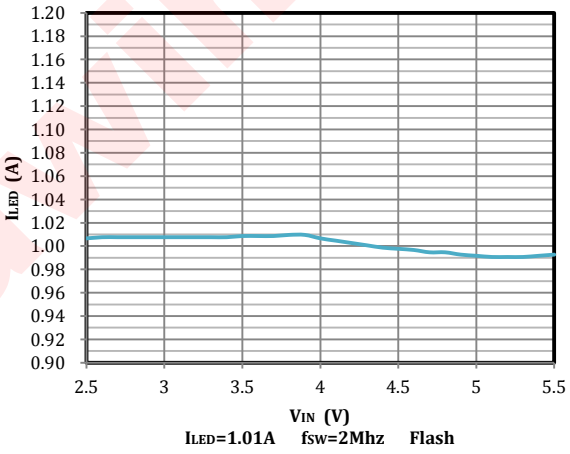


Fig9. LED Flash Current vs Input Voltage

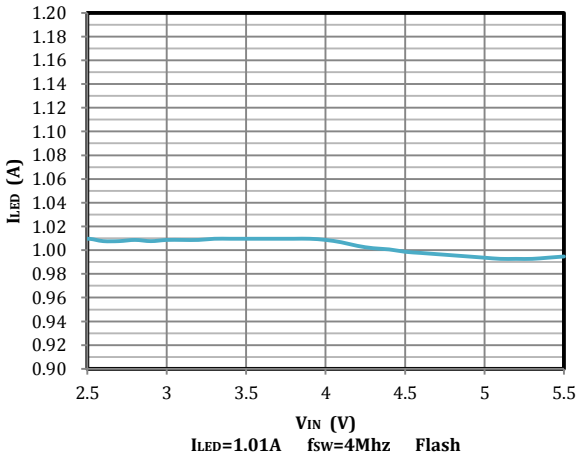


Fig10. LED Flash Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, C_{IN} = C_{OUT} = 2×10 μF and L=1 μH, unless otherwise noted .

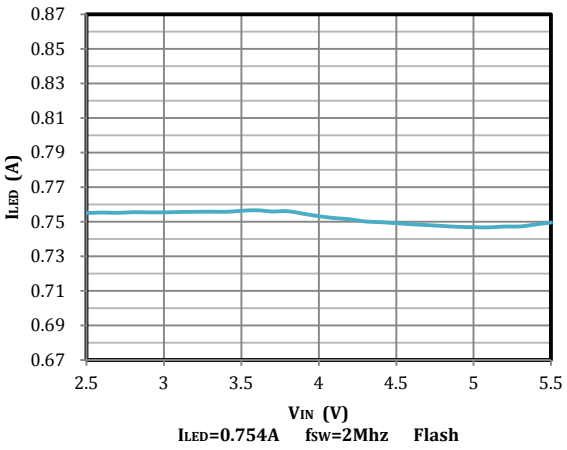


Fig11. LED Flash Current vs Input Voltage

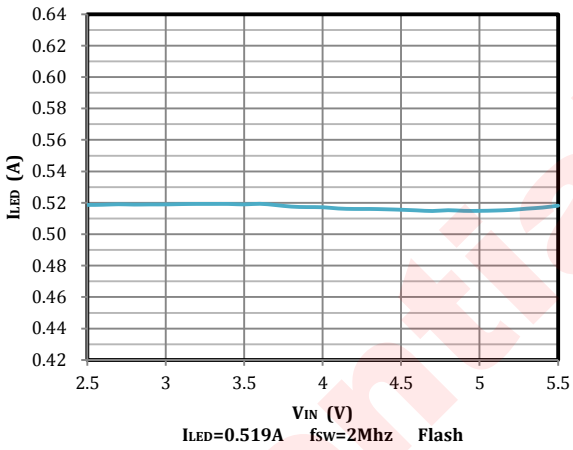


Fig12. LED Flash Current vs Input Voltage

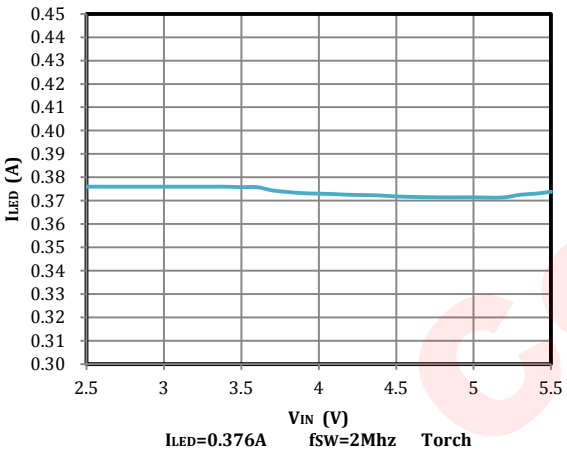


Fig13. LED Torch Current vs Input Voltage

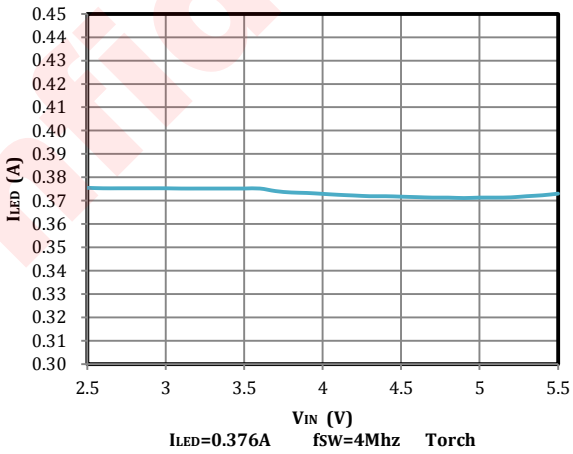


Fig14. LED Torch Current vs Input Voltage

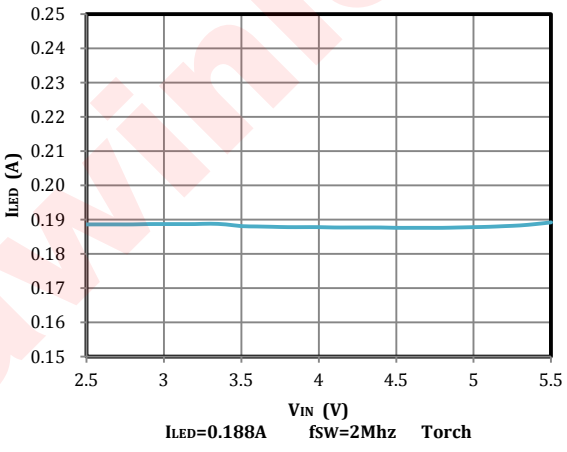


Fig15. LED Torch Current vs Input Voltage

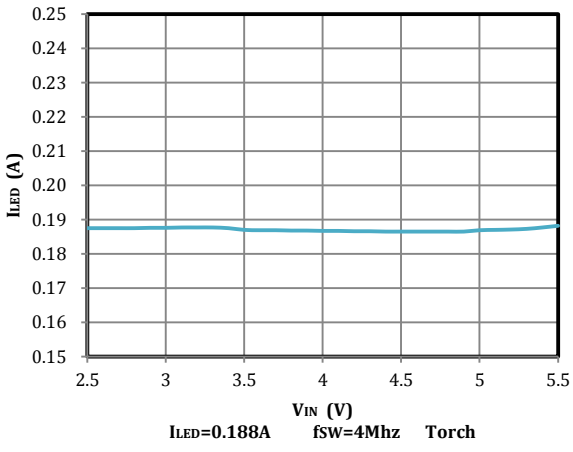


Fig16. LED Torch Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, C_{IN} = C_{OUT} = 2×10 μF and L=1 μH, unless otherwise noted .

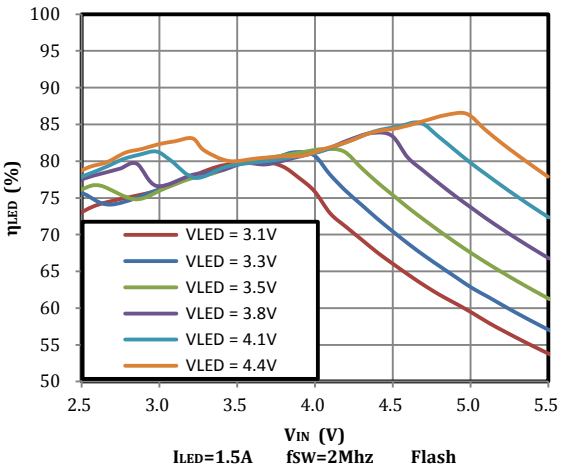


Fig17. LED Efficiency vs Input Voltage

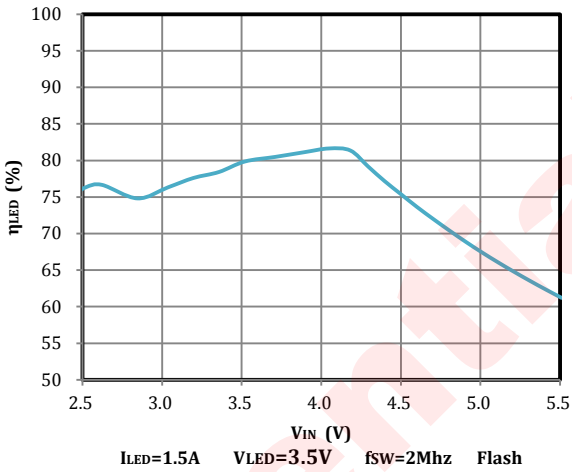


Fig18. LED Efficiency vs Input Voltage

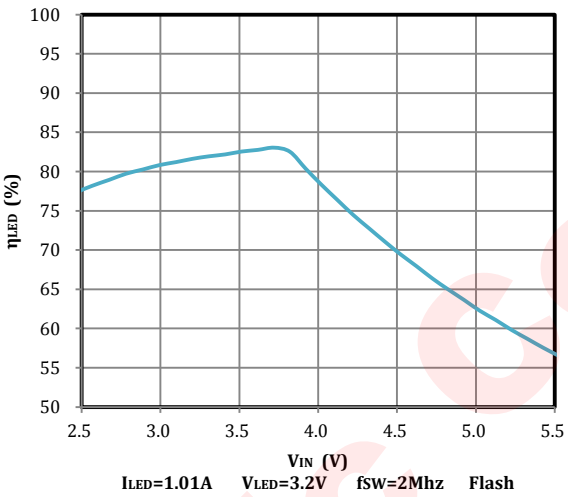


Fig19. LED Efficiency vs Input Voltage

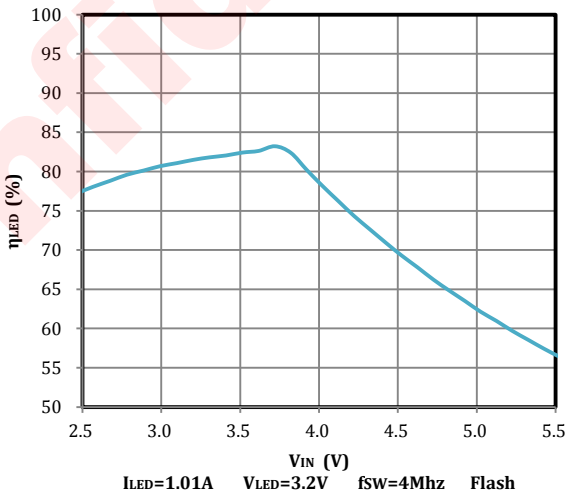


Fig20. LED Efficiency vs Input Voltage

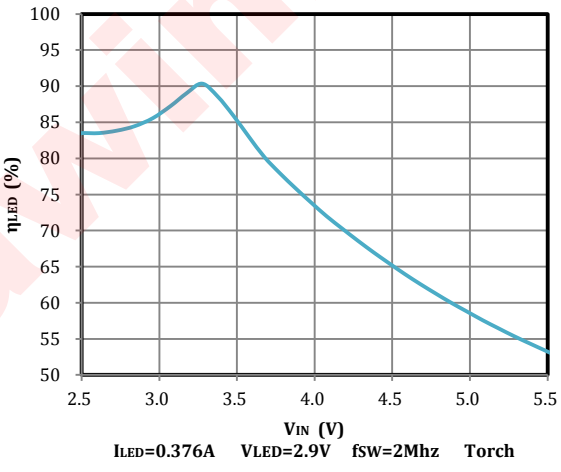


Fig21. LED Efficiency vs Input Voltage

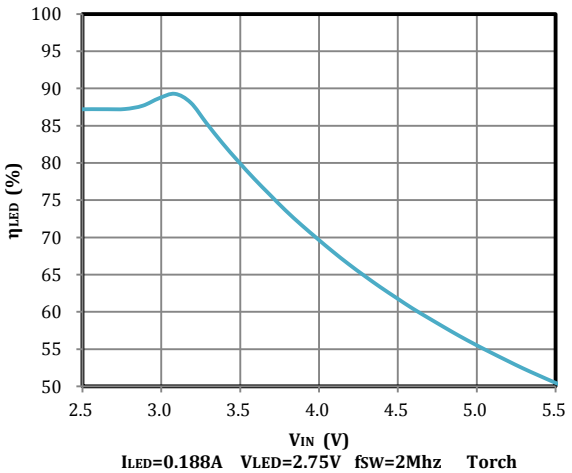


Fig22. LED Efficiency vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, C_{IN} = C_{OUT} = 2×10 μF and L=1 μH, unless otherwise noted .

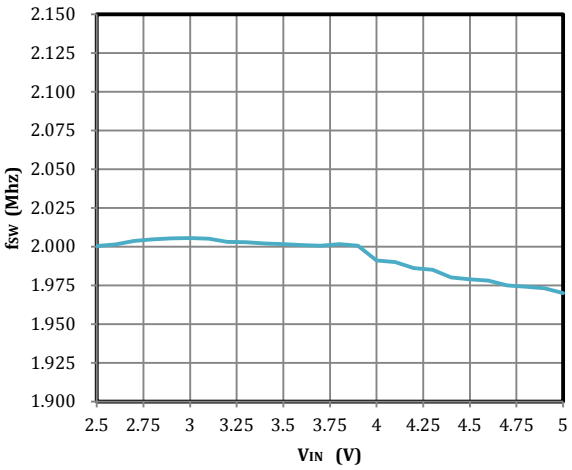


Fig 23. 2-Mhz Frequency vs Input Voltage

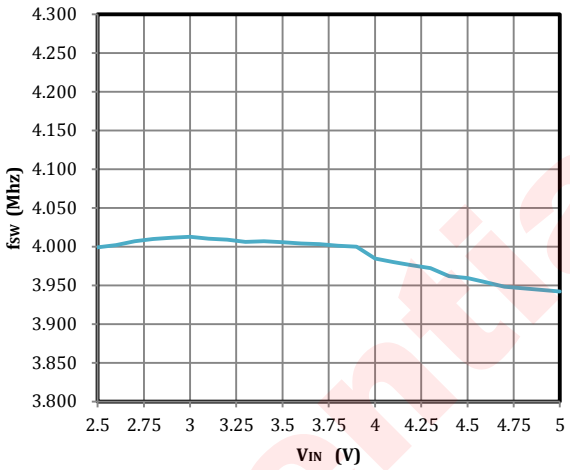


Fig 24. 4-Mhz Frequency vs Input Voltage

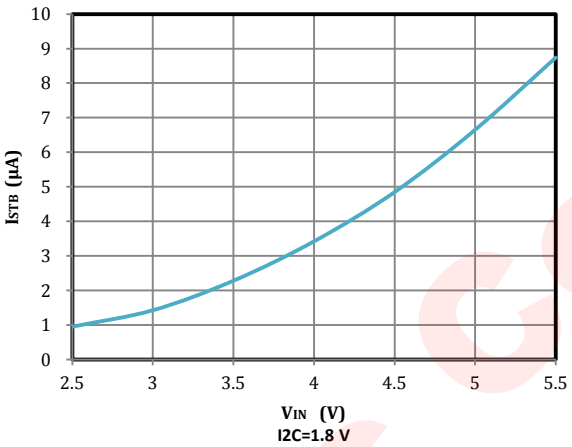


Fig 25. Standby Current vs Input Voltage

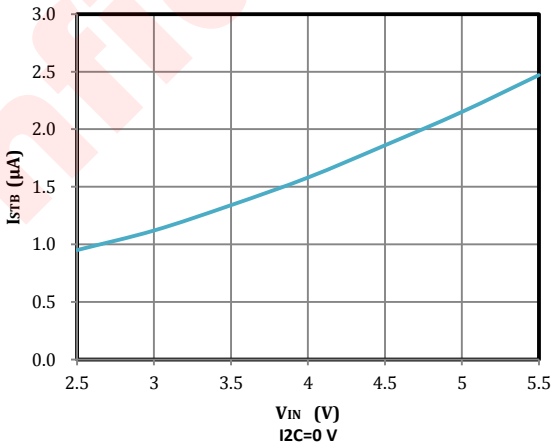


Fig 26. Standby Current vs Input Voltage

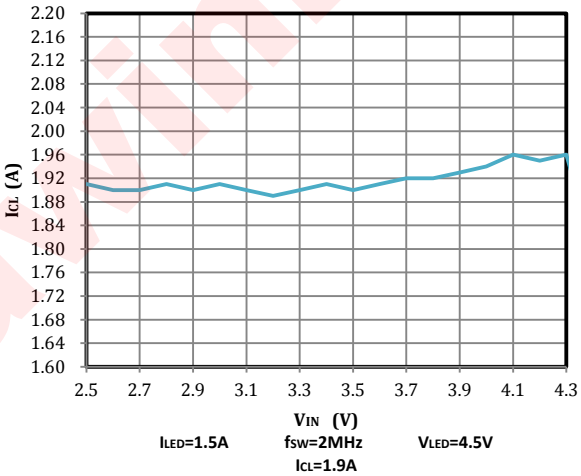


Fig 27. Inductor Current Limit vs Input Voltage

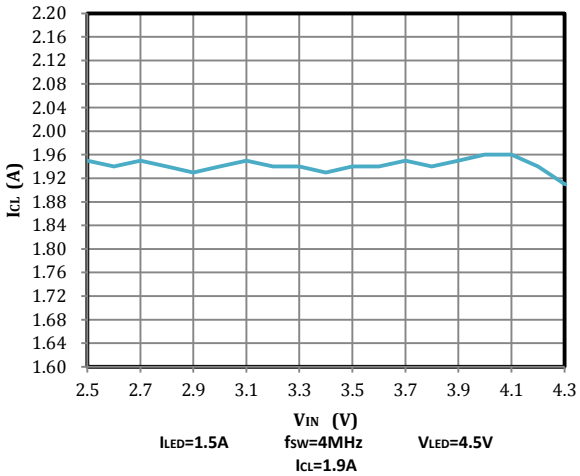


Fig 28. Inductor Current Limit vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, C_{IN} = C_{OUT} = 2×10 μF and L=1 μH, unless otherwise noted .

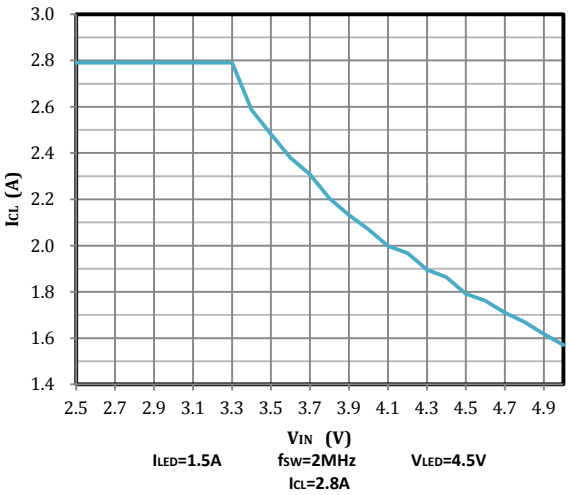


Fig 29. Inductor Current Limit vs Input Voltage

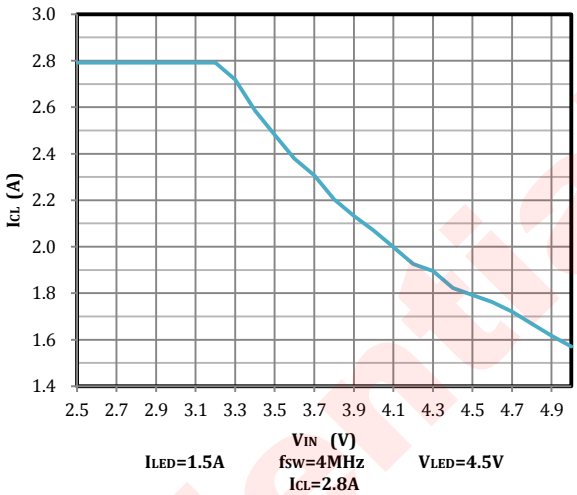


Fig 30. Inductor Current Limit vs Input Voltage

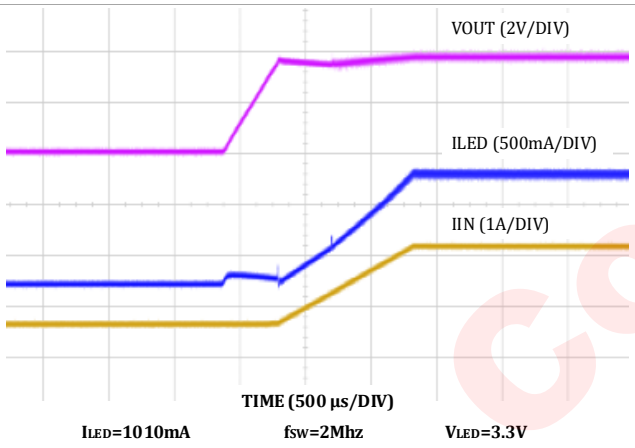


Fig 31. Ramp Up

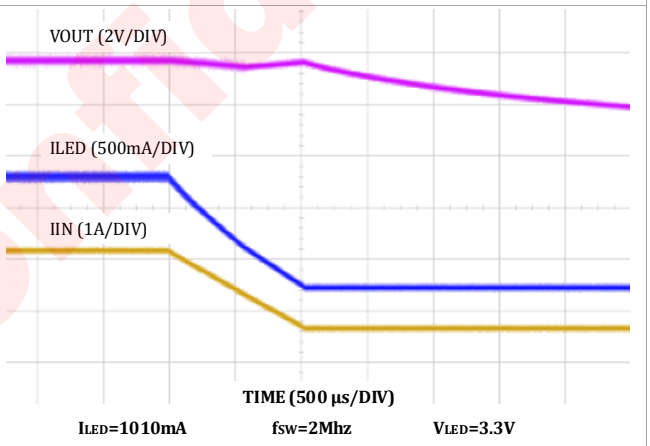


Fig 32. Ramp Down

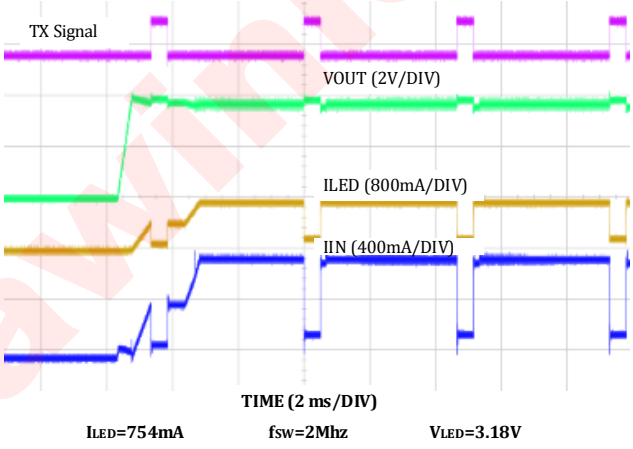


Fig 33. TX Interrupt

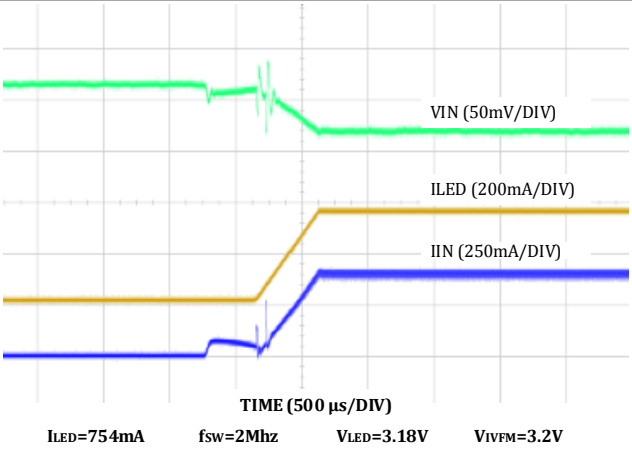


Fig 34. IVFM - Stop and Hold

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, C_{IN} = C_{OUT} = 2×10 µF and L=1 µH, unless otherwise noted .

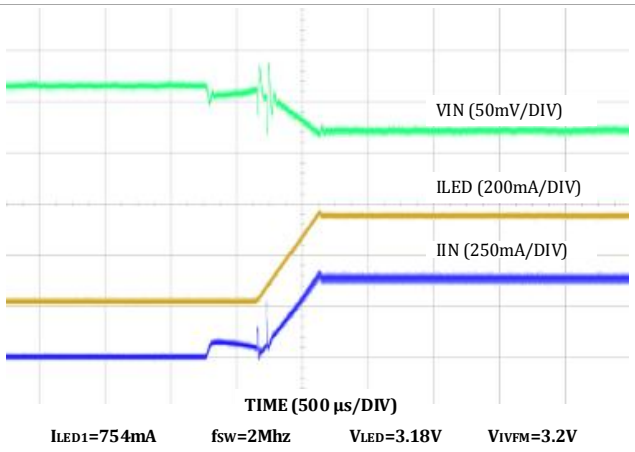


Fig 35. IVFM - Down

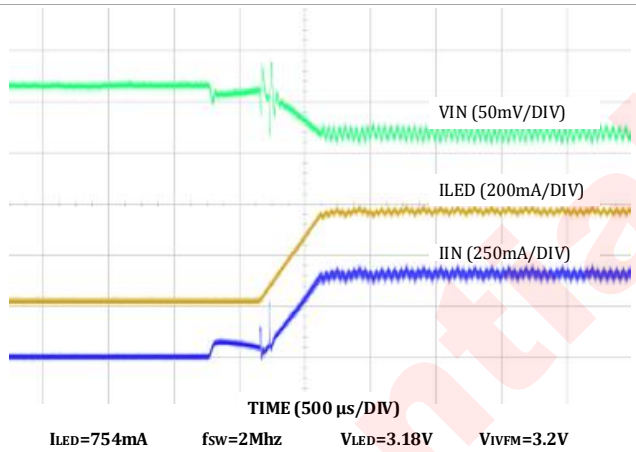


Fig 36. IVFM - Up and Down

DETAILED FUNCTIONAL DESCRIPTION

The AW3642 is a high-power white LED flash driver capable of delivering up to 1.5A to the LED. The device incorporates a 2MHz or 4MHz constant frequency-synchronous current-mode PWM boost converter and high-side current source to regulate the LED current over the 2.7V to 5.5V input voltage range.

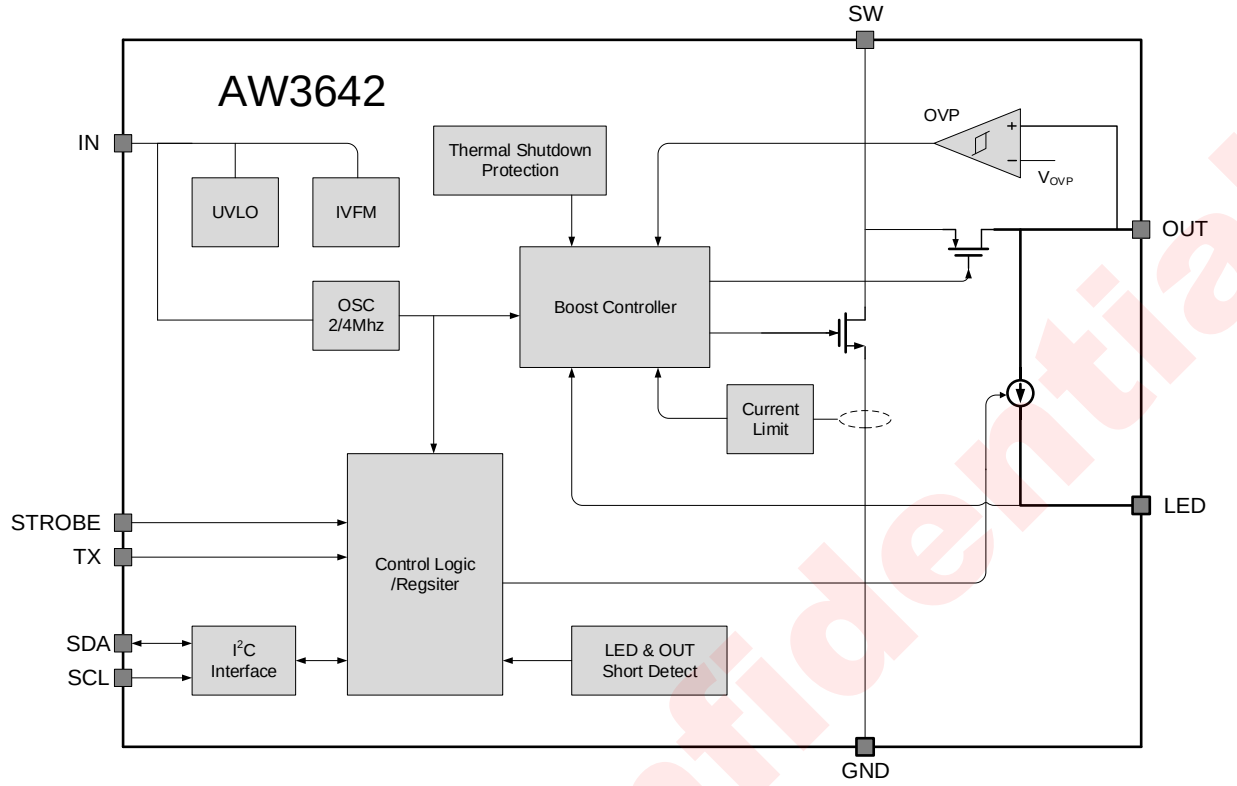
The AW3642 PWM DC-DC boost converter switches and boosts the output to maintain at least V_{HR} across the current source. This minimum headroom voltage ensures the current source remains in regulation. If the input voltage is above the LED voltage + current source headroom voltage, the device would not switch, but turns the PMOS on continuously (Pass mode). In Pass mode the difference between (V_{IN} − I_{LED} × R_{PMOS}) and the voltage across the LED is dropped across the current source.

The AW3642 has two logic inputs including a hardware Flash Enable (STROBE), and a Flash Interrupt input (TX) designed to interrupt the flash pulse during high battery-current conditions. Two logic inputs have internal 300kΩ (typ.) pull-down resistors to GND.

The AW3642 provides three IVFM protection modes to prevent system reset or shutdown under low battery condition.

Control is done via an I^2C-compatible interface. This includes adjustment of the Flash and Torch current levels, changing the Flash Timeout Duration, and changing the switch current limit. Additionally, there are flag and status bits that indicate flash current timeout, LED over-temperature condition, LED failure (open/short), device thermal shutdown, TX interrupt, and V_{IN} under-voltage conditions.

FUNCTIONAL BLOCK DIAGRAM



FEATURE DESCRIPTION

FLASH MODE

In Flash Mode, the LED current source provides 64 target current levels from 23.4mA to 1.5A. The Flash current are adjusted via the LED Flash Brightness Registers. Flash mode is activated by the Enable Register(setting M1, M0 to '11'), or by pulling the STROBE pin HIGH when the pin is enabled (Enable Register). Once the Flash sequence is activated the current source ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached.

When the device is enabled in Flash Mode through the Enable Register, all mode bits in the Enable Register are cleared after a flash timeout event.

TORCH MODE

In Torch mode, the LED current source provides 64 target current levels from 5.4mA to 376mA. The Torch currents are adjusted via the LED Torch Brightness Registers. Torch mode is activated by the Enable Register (setting M1, M0 to '10'). Once the Torch sequence is activated the active current source ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. The rate at which the current ramps is determined by the value chosen in the Timing Register.

Torch Mode is not affected by Flash Timeout or by a TX Interrupt event.

IR MODE

In IR Mode, the target LED current is equal to the value stored in the LED Flash Brightness Registers. When IR mode is enabled (setting M1, M0 to '01'), the boost converter turns on and set the output equal to the input (pass-mode). At this point, toggling the STROBE pin enables and disables the LED current source (if enabled). The strobe pin can only be set to be Level sensitive, meaning all timing of the IR pulse is externally controlled.

In IR Mode, the current sources do not ramp the LED outputs to the target. The current transitions immediately from off to on and then on to off.

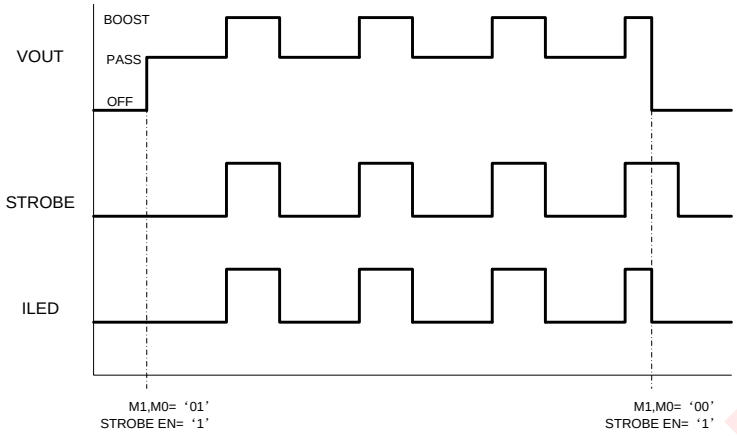


Fig 39 IR Mode with Boost

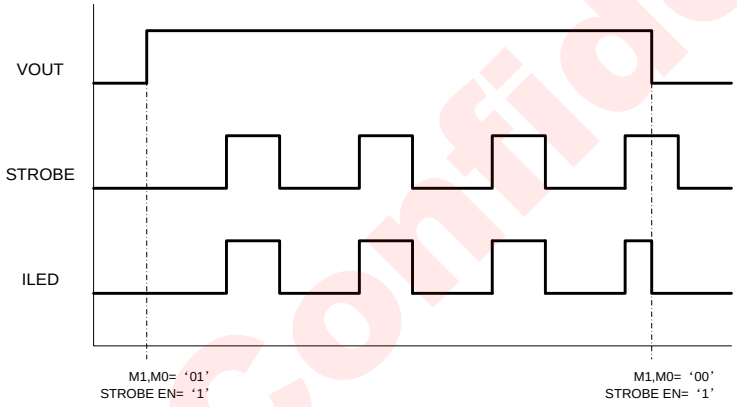


Fig 40 IR Mode Pass Only

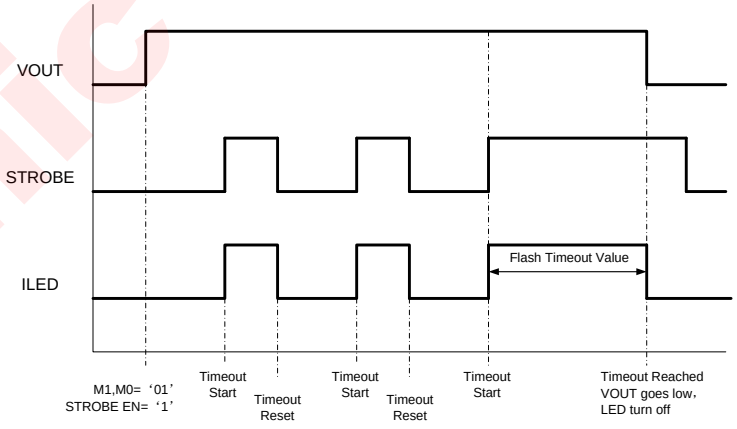


Fig 41 IR Mode Timeout

SOFT START-UP

Turn on of the AW3642 Torch and Flash modes can be done through the Enable Register. On start-up, when V_{OUT} is less than V_{IN} the internal synchronous PMOS turns on as a current source and delivers 200mA (typ.)

to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typ.) the current source turns on. At turn-on the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turn-on and limits inrush current from the V_{IN} supply.

PASS MODE

The AW3642 starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. In Pass Mode the boost converter does not switch, and the synchronous PMOS turns fully on bringing V_{OUT} up to $V_{IN} - I_{LED} \times R_{PMOS}$. In Pass Mode the inductor current is not limited by the peak current limit. If the voltage difference between V_{OUT} and V_{LED} falls below V_{HR}, the device switches to Boost Mode.

POWER AMPLIFIER SYNCHRONIZATION (TX)

The TX pin is a Power Amplifier Synchronization input. This is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. When the AW3642 is engaged in a Flash event, and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current returns to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current turns off.

The TX input can be disable by setting bit[7] (TX Enable) to a '0' in the Enable Register(0x01).

INPUT VOLTAGE FLASH MONITOR (IVFM)

The AW3642 has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing the Input Voltage Flash Monitor (IVFM). The adjustable threshold ranges from 2.9 V to 3.6 V in 100mV steps as well as adjustable hysteresis, with three different usage modes (Stop and Hold, Down, Up and Down). The IVFM threshold and hysteresis are controlled by bits[5:3] and bit[2] respectively, in the IVFM Register(0x02). The Flags2 Register has the IVFM flag bit set when the input voltage crosses the IVFM threshold value. Additionally, the IVFM threshold sets the input voltage boundary that forces the AW3642 to either stop ramping the flash current during startup in Stop and Hold Mode, or to actively adjust the LED current lower in Down Mode, or to continuously adjust the LED current up and down in Up & Down Mode.

- Stop and Hold Mode: Stops Current Ramp and holds the level for the remaining flash, If V_{IN} falls below the IVFM threshold value.
- Down Mode: Adjust current down if V_{IN} falls below the IVFM threshold value and stops decreasing once V_{IN} rises above the IVFM threshold (or plus a hysteresis). The AW3642 will decrease the current throughout the flash pulse anytime V_{IN} falls below the IVFM threshold, not just once. The flash current will not increase again until the next flash.
- Up & Down Mode: Adjust current down if V_{IN} falls below the IVFM threshold value and adjusts current up if V_{IN} rise above the IVFM threshold (or plus a hysteresis). In Up & Down mode, the LED current will continually adjust with the rising and falling of V_{IN} throughout the entire flash pulse.

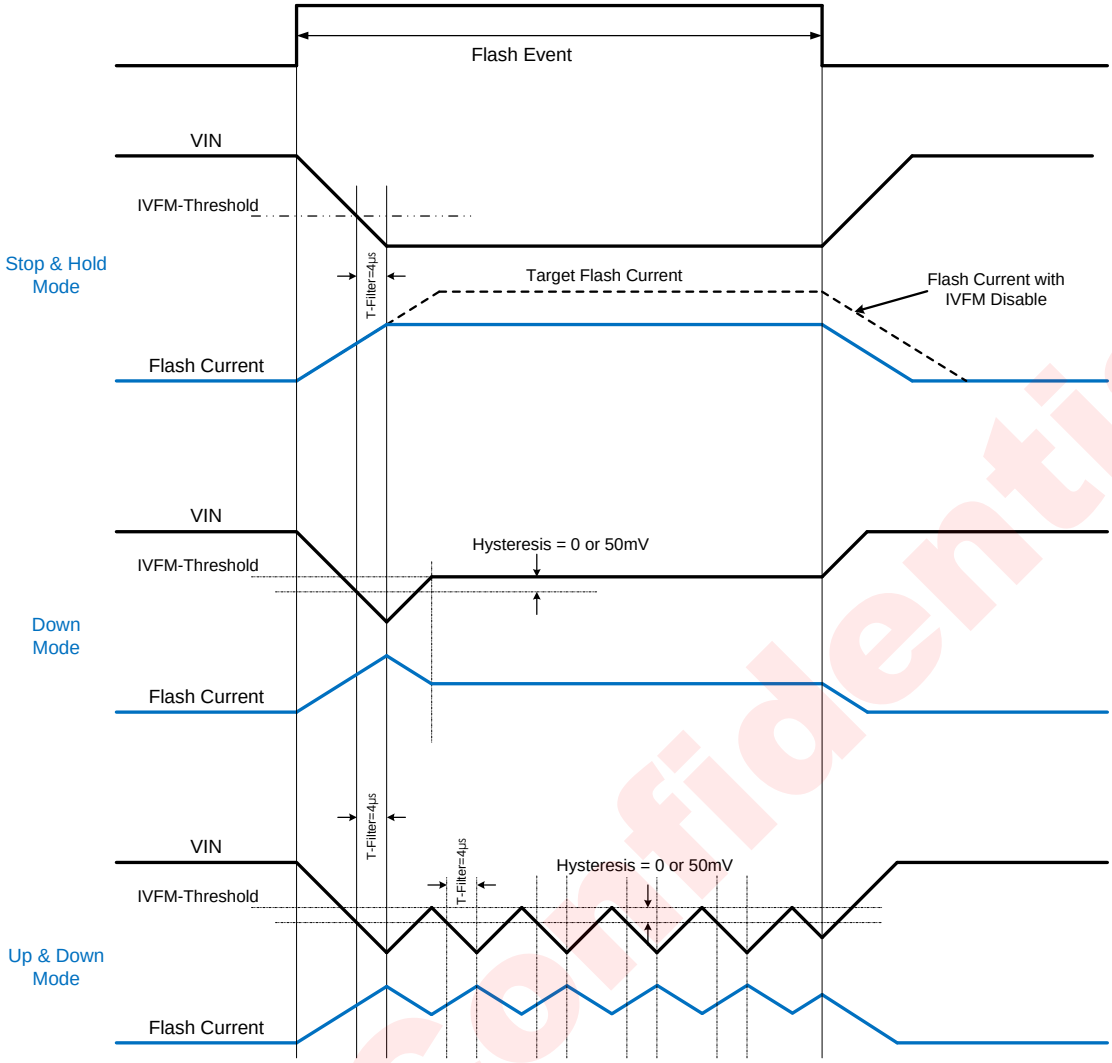


Fig 42 IVFM Modes

FLASH TIMEOUT

The Flash Timeout period sets the maximum time of one flash event, whether a flash stop command is received or not. The AW3642 has 16 timeout levels ranging from 40ms to 1.6s (see ***TIMING CONFIGURATION REGISTER (0X08)*** for more detail). Flash Timeout applies to both Flash and IR modes, and it continues to count when the Flash mode is forced into Torch mode during a TX high event. The mode bits are cleared and bit[0] is set in the Flags1 register(0x0A) upon a Flash Timeout. This fault flag can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting the SW RESET bit to a '1', or by removing power to the AW3642.

CURRENT LIMIT

When the inductor current limit is reached, the AW3642 terminates the charging phase of the switching cycle until the next switching period. If the over-current condition persists, the device operates continuously in current limit. The AW3642 features two selectable inductor current limits(1.9A and 2.8A) that are programmable by bit[0] in Boost configuration Register(0x07).

Since the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in Pass Mode (current does not flow through the NMOS in pass mode). The mode bits are not cleared upon a Current Limit event, but a flag bit[3] is set in the Flags1 register(0x0A).

This fault flag can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting the SW RESET bit to a '1', or by removing power to the AW3642.

UNDERVOLTAGE LOCKOUT (UVLO)

The AW3642 has an internal comparator that monitors the voltage at IN and forces the AW3642 into standby if the input voltage drops to 2.5 V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the Flags1 Register (0x0A). If the input voltage rises above 2.5 V, the AW3642 is not available for operation until there is an I^2C read of the Flags1 Register (0x0A). Upon a read, the Flags1 register is cleared, and normal operation can resume if the input voltage is greater than 2.5 V.

VOUT SHORT FAULT

The Output Short Fault flag reads back a '1' if the device is active in Flash or Torch mode and the boost output experiences a short condition. VOUT short condition occurs if the voltage at OUT goes below 2.3V (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 2.048ms before the VOUT Short flag is valid. The mode bits are cleared upon an the VOUT short fault. The AW3642 is not available for operation until VOUT Fault flags is cleared. The VOUT Short Faults can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting the SW RESET bit to a '1', or by removing power to the AW3642.

LED SHORT FAULT

The LED Short Fault flag read back a '1' if the device is active in Flash or Torch mode and the LED output experiences a short condition. An LED short condition is determined if the voltage at LED goes below 500mV (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 256μs before the LED Short Fault flag is valid. The mode bits are cleared upon an LED short fault. The AW3642 is not available for operation until the LED Fault Short flag is cleared. The LED Short Fault can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting the SW RESET bit to a '1', or by removing power to the AW3642.

OVERVOLTAGE PROTECTION (OVP)

The output voltage is limited to typically 5 V. In situations such as an open LED, the AW3642 raises the output voltage in order to try and keep the LED current at its target value. When VOUT reaches 5 V (typ.) the overvoltage comparator trips and turns off the internal NMOS. When VOUT falls below the "V_{OVP} Off Threshold", the AW3642 begins switching again. The mode bits are cleared, and the OVP Fault flag is set, when an OVP condition is present for three rising OVP edges. This prevents momentary OVP events from forcing the device to shut down. The AW3642 is not available for operation until the OVP Fault flag is cleared. The OVP Fault can be reset to '0' by reading back the Flags2 Register (0x0A), or by setting the SW RESET bit to a '1', or by removing power to the AW3642.

THERMAL SHUTDOWN (TSD)

When the AW3642 die temperature reaches 155°C, the thermal shutdown detection circuit trips, forcing the AW3642 into standby and writing a '1' to the Thermal Shutdown Fault flag of the Flags1 Register (0x0A) . The AW3642 is only allowed to restart after the Thermal Shutdown Fault flag is cleared. The Thermal Shutdown Faults can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting the SW RESET bit to a '1', or by removing power to the AW3642. Upon restart, if the die temperature is still above 155°C, the AW3642 resets the Fault flag and re-enters standby.

PROGRAMMING

CONTROL TRUTH TABLE

MODE1	MODE0	STROBE EN	STROBE PIN	ACTION
0	0	0	X	Standby
0	0	1	0	Standby
0	0	1	Pos edge	Ext Flash
1	0	X	X	Int Torch
1	1	X	X	Int Flash
0	1	0	X	IRLED Standby
0	1	1	0	IRLED Standby
0	1	1	Pos edge	IRLED Enabled

I²C INTERFACE

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

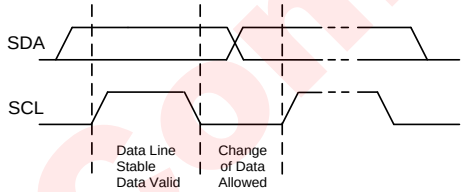


Fig 43 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

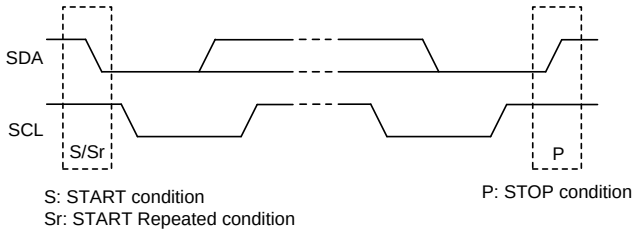


Fig 44 Start and Stop Conditions

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

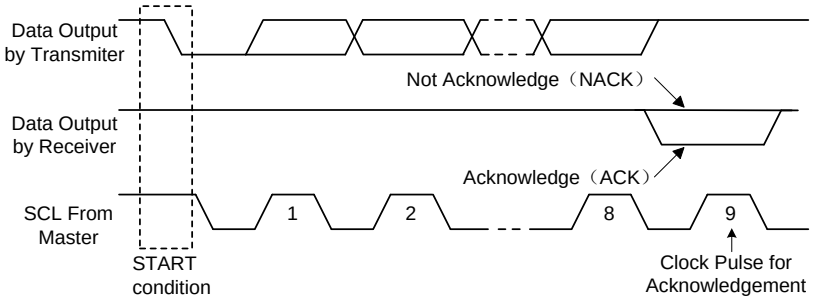


Fig 45 Acknowledgement Diagram

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6, 7)

i) Master generates STOP condition to indicate write cycle end

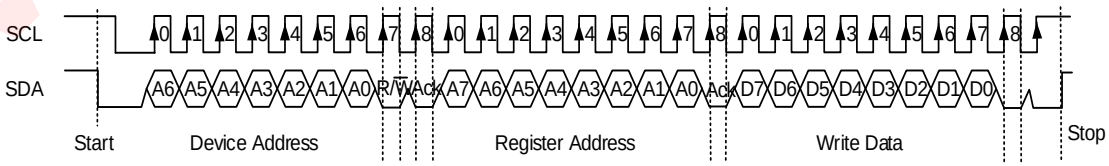


Fig 46 I²C Write Timing

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

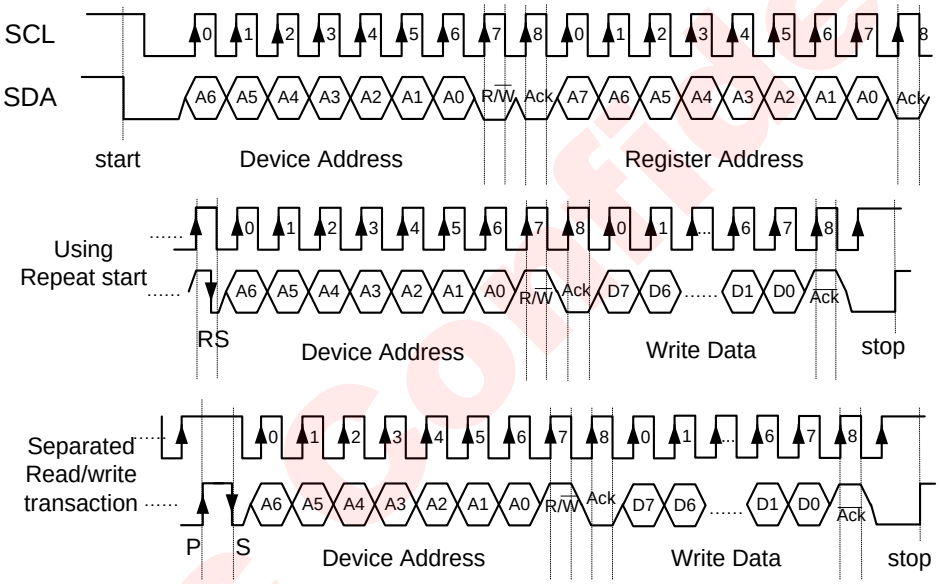


Fig 47 I²C Read Timing

REGISTER CONFIGURATION

REGISTER LIST

Register name	Address(HEX)	Read/Write	Default Value
Chip ID Register	0x00	Read	0x36
Enable Register	0x01	Read/Write	0x80
IVFM Register	0x02	Read/Write	0x01
LED Flash Brightness Register	0x03	Read/Write	0xBF
LED Torch Brightness Register	0x05	Read/Write	0xBF
Boost Configuration Register	0x07	Read/Write	0x09
Timing Configuration Register	0x08	Read/Write	0x1A
Flags1 Register	0x0A	Read	0x00
Flags2 Register	0x0B	Read	0x00
Device ID Register	0x0C	Read	0x0A
Last Flash Register	0x0D	Read	0x00

REGISTER DETAILED DESCRIPTION

✧ **Chip ID Register (0x00)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Chip ID: “00110110”							

✧ **Enable Register (0x01)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX Pin Enable 0=Disabled 1=Enabled (Default)	**Strobe Type** 0=Level Triggered (Default) 1=Edge Triggered	**Strobe Enable** 0=Disabled (Default) 1=Enabled	**RFU**	**Mode Bits: M1, M0** 00=Standby (Default) 01=IR Drive 10=Torch 11=Flash		**LED Enable** 00=OFF (Default) 11=ON 01 and 10 are not valid settings	

Note:

In Edge or Level Strobe Mode, it is recommended that the trigger pulse width be set greater than 1ms to ensure proper turn-on of the device.

✧ IVFM Register (0x02)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**UVLO Circuitry** 0=Disabled (Default) 1=Enabled	**IVFM Levels** 000=2.9 V (Default) 001=3.0 V 010=3.1 V 011=3.2 V 100=3.3 V 101=3.4 V 110=3.5 V 111=3.6 V			**IVFM Hysteresis** 0=0 mV (Default) 1=50 mV	**IVFM Mode Selection** 00=Disabled 01=Stop and Hold Mode (Default) 10=Down Mode 11=Up and Down Mode	

✧ LED Flash Brightness Register (0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUST BE SET TO '10' FOR PROPER OPERATION		**LED Flash Brightness Levels** I_{FLASH}(mA)≈(Brightness Code*23.44mA)+23.4mA 000000=23.4mA …… 011111=753.6mA …… 111111=1.5 A (Default)					

✧ LED Torch Brightness Register (0x05)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUST BE SET TO '10' FOR PROPER OPERATION		**LED Torch Brightness Levels** I_{TORCH}(mA)≈(Brightness Code*5.88mA)+5.4mA 000000=5.4mA …… 011111=188 mA …… 111111=376mA (Default)					

✧ Boost Configuration Register (0x07)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software Reset Bit 0=Not Reset (Default) 1=Reset	**RFU**	**RFU**	**RFU**	**LED Pin Short Fault Detect** 0=Disabled 1=Enabled (Default)	**Boost Mode** 0=Normal (Default) 1=Pass Mode Only	**Boost Frequency Select** 0=2 MHz (Default) 1=4 MHz	**Boost Current Limit** 0=1.9A 1=2.8A (Default)

✧ Timing Configuration Register (0x08)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**Torch Current Ramp time** 000=No Ramp 001=1 ms (Default) 010=32 ms 011=64 ms 100=128 ms 101=256 ms 110=512 ms 111=1024 ms			**Flash Time-out Duration** 0000=40 ms 0001=80 ms 0010=120 ms 0011=160 ms 0100=200 ms 0101=240 ms 0110=280 ms 0111=320 ms 1000=360 ms 1001=400 ms 1010=600 ms (Default) 1011=800 ms 1100=1000 ms 1101=1200 ms 1110=1400 ms 1111=1600 ms			

✧ Flags1 Register (0x0A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX Flag	**V_{OUT} Short Fault**	**LED Short Fault**	**LED Short Fault**	**Current Limit Flag**	**Thermal Shutdown (TSD) Fault**	**UVLO Fault**	**Flash Time-Out Flag**

✧ Flags2 Register (0x0B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**RFU**	**RFU**	**RFU**	**RFU**	**IVFM Trip Flag**	**OVP Fault**	**RFU**

✧ Device ID Register (0x0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**RFU**	**Device ID** “001”			**Silicon Revision Bits** “010”		

✧ Last Flash Register (0x0D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	The value stored is always the last current value the IVFM detection block set $I_{LED}=I_{FLASH-TARGET}*((code+1)/128)$						

APPLICATION INFORMATION

The AW3642 can drive a flash LED at currents up to 1.5A. The 2MHz/4MHz DC-DC boost regulator allows for the use of small value discrete external components. Below are some peripheral selection guidelines.

OUTPUT CAPACITOR SELECTION

The AW3642 is designed to operate with a 10μF ceramic output capacitor. When the boost converter is running, the output capacitor supplies the load current during the boost converter on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

Larger capacitors such as a 22μF or capacitors in parallel can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to the capacitors ESR (ΔV_{ESR}) use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{(V_{OUT} - V_{IN}) \times I_{LED}}{V_{OUT} \times f \times C_{OUT}}$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{V_{OUT} \times I_{LED}}{V_{IN}} + \frac{\Delta I_L}{2} \right)$$

Where $\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f \times L}$

In ceramic capacitors the ESR is very low so the assumption is that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 1 lists different manufacturers for various output capacitors and their case sizes suitable for use with the AW3642.

INPUT CAPACITOR SELECTION

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the AW3642 boost converter and reduce noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In the typical application circuit a 10-μF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the AW3642 input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 1 lists various input capacitors recommended for use with the AW3642.

Table 1 Recommended Input/ Output Capacitors (X5R/X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE	VOLTAGE RATING
TDK	C1608JB0J106M	10μF	0603	6.3V
TDK	C2012JB1A106M	10μF	0805	10V
Murata	GRM188R60J106M	10μF	0603	6.3V
Murata	GRM21BR61A106KE19	10μF	0805	10V

INDUCTOR SELECTION

The AW3642 is designed to use a 0.47μH or 1μH inductor. When the device is boosting (V_{OUT} > V_{IN}) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the AW3642. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the AW3642 are greater than I_{PEAK} in the following calculation:

$$I_{PEAK} = \frac{I_{LED} \times V_{OUT}}{\eta \times V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

And f_{SW} =2 or 4MHz.

Table 2 lists various inductors and their manufacturers that work well with the AW3642.

Table 2 Recommended Inductors

MANUFACTURER	L	PART NO.	SIZE	I_{SAT}	R_{DC}
TOKO	1μH	DFE201610P-1R0M	2.0 mm x 1.6 mm x 1.0 mm	3.7A	58mΩ
TOKO	0.47μH	DFE201610P-R470M	2.0 mm x 1.6 mm x 1.0 mm	4.1A	32mΩ
Sunlord	1μH	WPN252012H1R0MT	2.5mm × 2.0mm ×1.2mm	3.4A	48mΩ

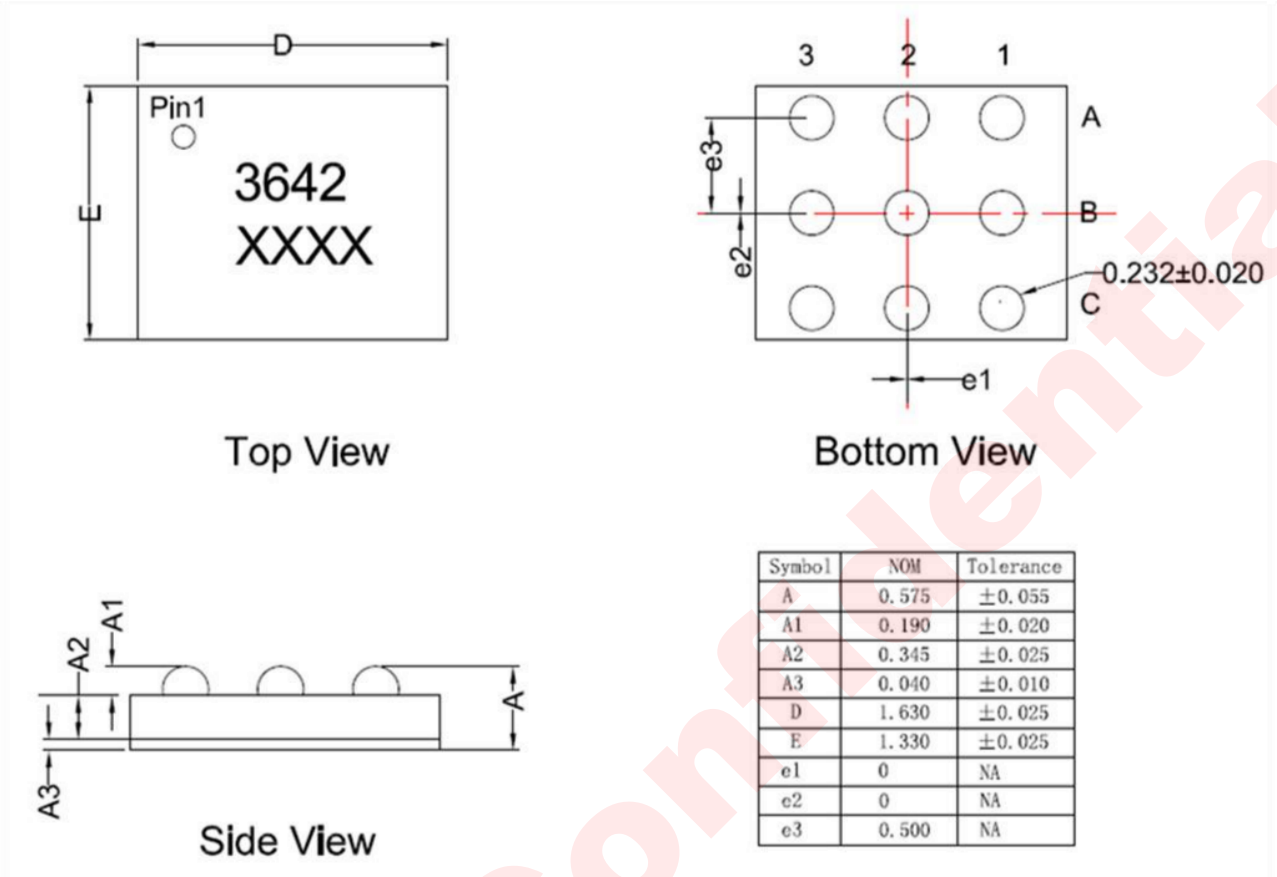
PCB LAYOUT

LAYOUT GUIDELINES

The high switching frequency and large switching currents of the AW3642 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

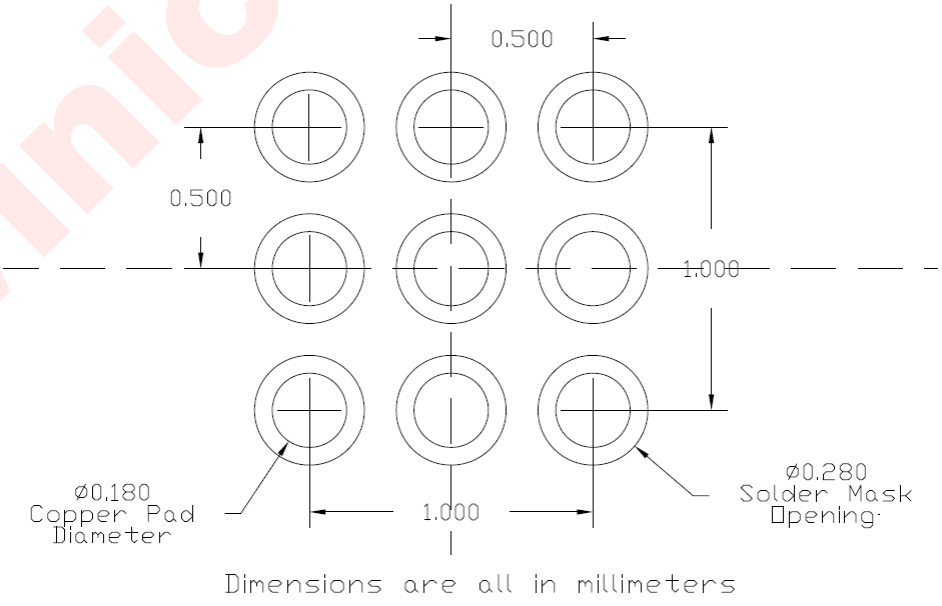
1. Place C_{IN} on the top layer (same layer as the AW3642) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turn-on and turn-off and can detect current spikes over 1 A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V_{IN} line.
2. Place C_{OUT} on the top layer (same layer as the AW3642) and as close as possible to the OUT and GND pin. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the VOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the high dV/dT present at SW that can couple into nearby traces.
4. Avoid routing logic traces near the SW node so as to avoid any capacitive coupling from SW onto any high-impedance logic lines such as STROBE, SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the Flash LED cathodes directly to the GND pin of the AW3642. If possible, route the LED returns with a dedicated path so as to keep the high amplitude LED currents out of the GND plane. For Flash LEDs that are routed relatively far away from the AW3642, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.

PACKAGE DESCRIPTION



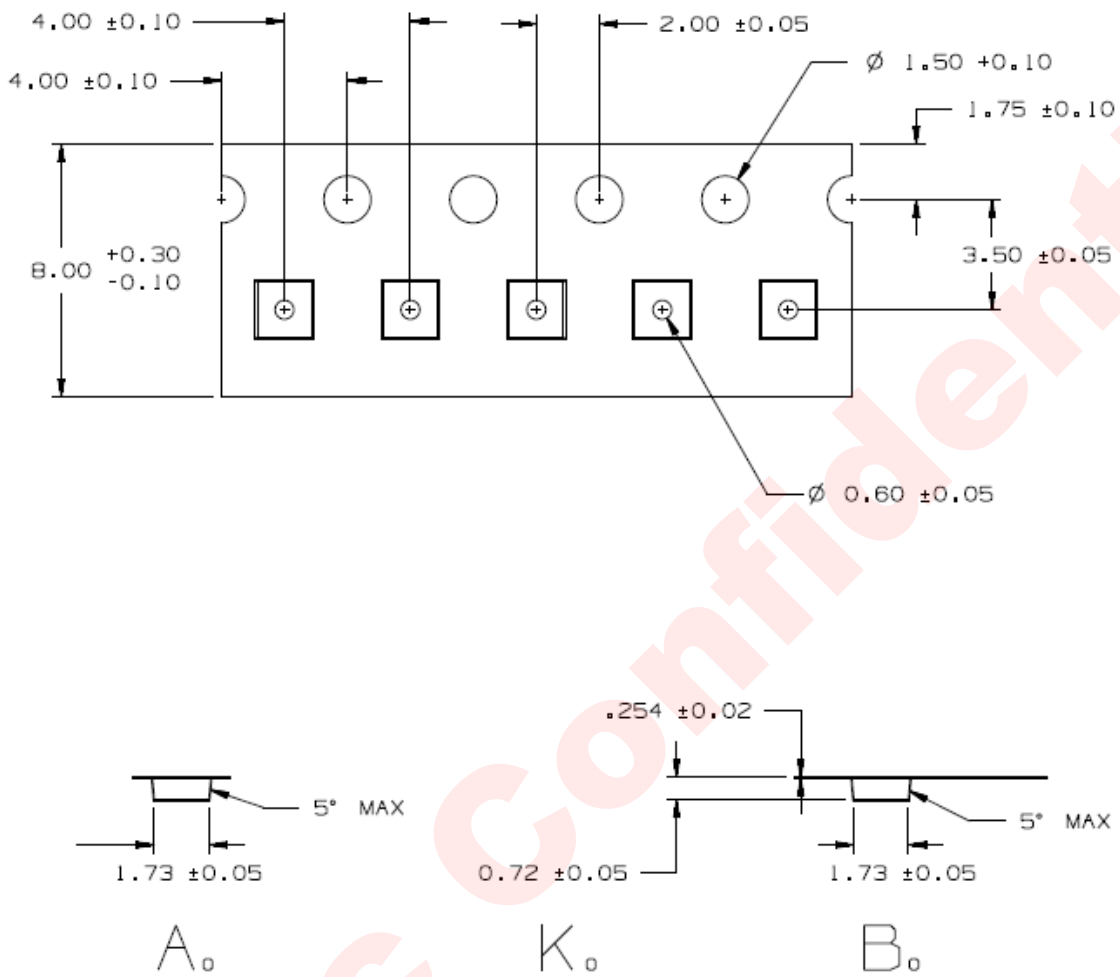
Symbol	NOM	Tolerance
A	0.575	±0.055
A1	0.190	±0.020
A2	0.345	±0.025
A3	0.040	±0.010
D	1.630	±0.025
E	1.330	±0.025
e1	0	NA
e2	0	NA
e3	0.500	NA

LAND PATTERN DATA

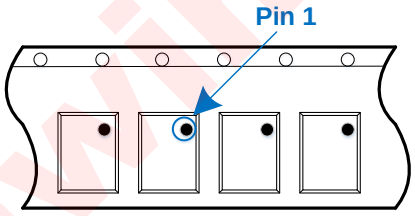


TAPE AND REEL INFORMATION

Carrier Tape

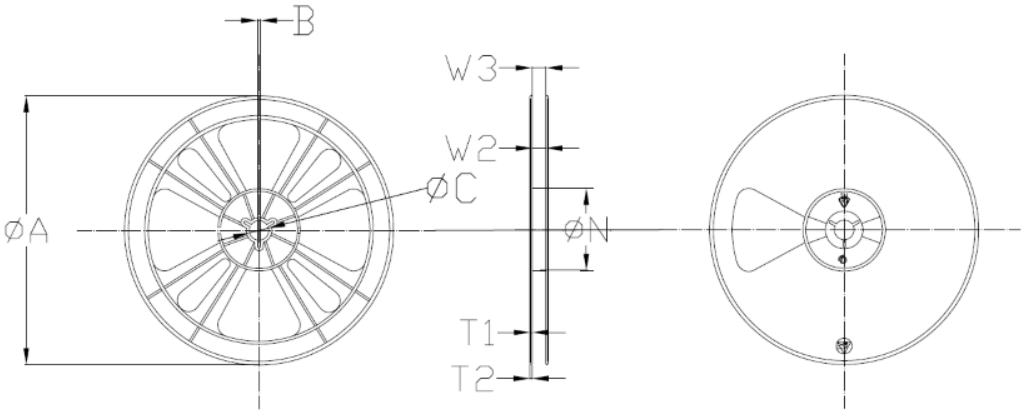


Pin 1 direction



User Direction of Feed

Reel

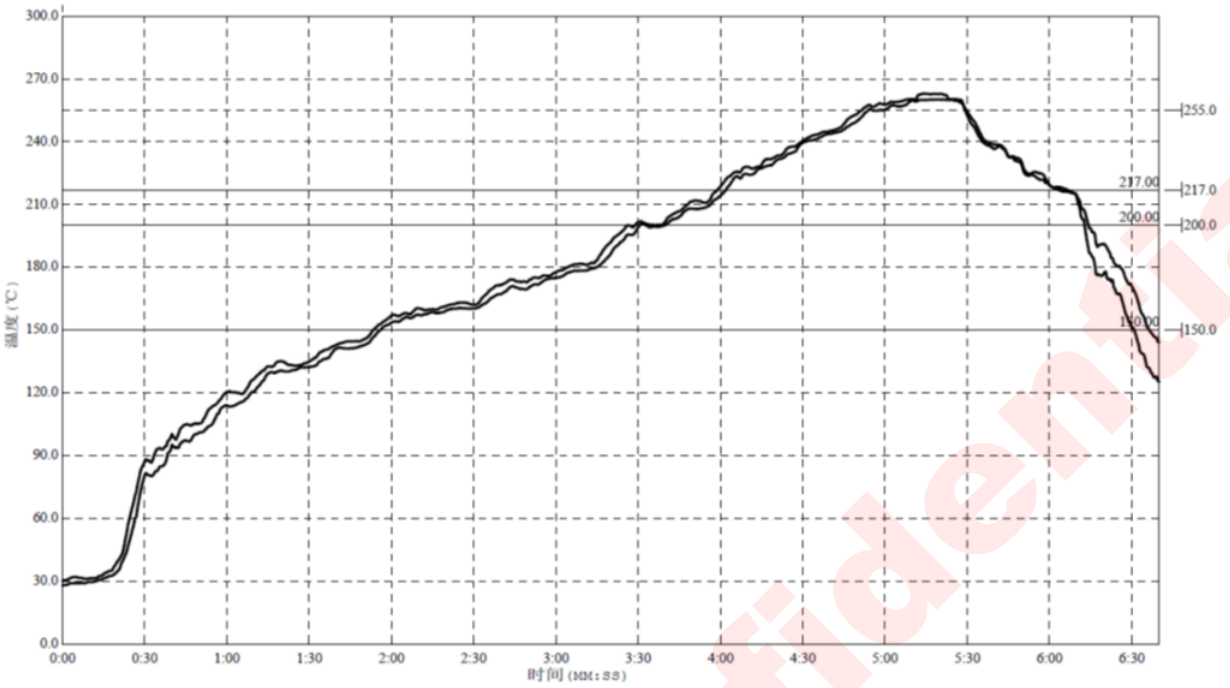


Item	Value&Tolerance
A	179±1.0
B	2.0±0.1
C	13.5±0.2
N	54.8±0.2
W2	9.0±0.2
W3	9.2+1.0
T1	1.2±0.2
T2	1.5±0.2

Note:

1. surface resistivity: 10^{5} to 10^{11} ohms/sq.
2. Restriction criterion of hazardous substance for packing material follow GP-M001.

REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW3642 adopted the Pb-Free assembly.

REVISION HISTORY

Vision	Date	Change Record
V1.0	Oct 2017	Product Datasheet V1.0 Released
V1.1	Jan 2018	Added the Moisture Sensitivity Level and Environmental Information. –page3
V1.2	Feb 2018	Added the Land Pattern Data. –page30
V1.3	Mar 2018	Modify the Pin Description of LED –page2
V1.4	Oct 2018	Correct the Carrier tape –page31

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