Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

FEATURES

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Ultra low noise figure(NF)=0.60dB;
- High power gain=18.5dB;
- High linearity IIP3oob=+3.6dBm;
- High input 1dB-compression point=-9.4dBm;
- Requires only one input matching inductor;
- RF output internally matched to 50 ohm;
- Supply voltage: 1.5V to 3.6V;
- Operating frequencies: 1550~1615MHz;
- Slim LGA-6L package:1.1mmX0.7mmX 0.42mm
- 3000V HBM ESD protection (including RFIN and RFOUT pin)

APPLICATIONS

- Smart phones, feature phones,
- Tablet PCs,
- Personal Navigation Devices,
- Digital Still Cameras, Digital Video Cam- eras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

GENERAL DESCRIPTION

- The AW5025 is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW5025 can be close to the antenna, requires only one external input matching inductor, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW5025 with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.6V. All these features make AW5025 an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.
- The AW5025 is available in a small lead-free, RoHS-Compliant, 1.1mm x 0.7mm x 0.42mm 6-pin LGA package.

TYPICAL APPLICATION CIRCUIT

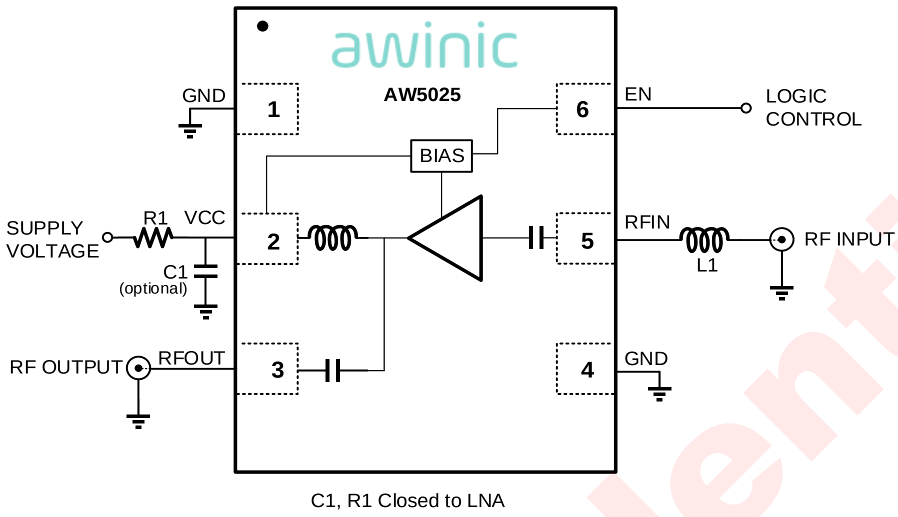

Figure 1(a) Typical Application Circuit of AW5025 for GNSS L1

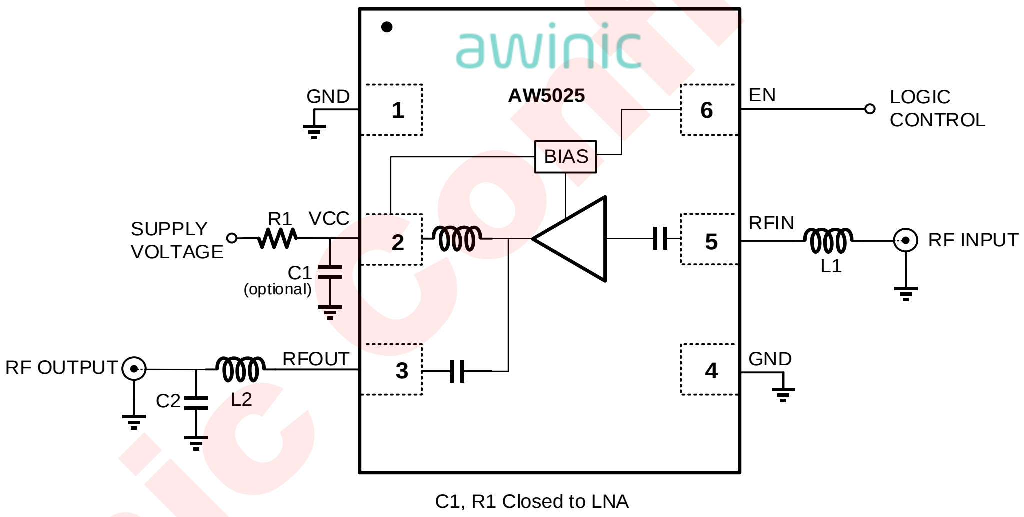

Figure 1(b) Typical Application Circuit of AW5025 for GNSS L2/L5

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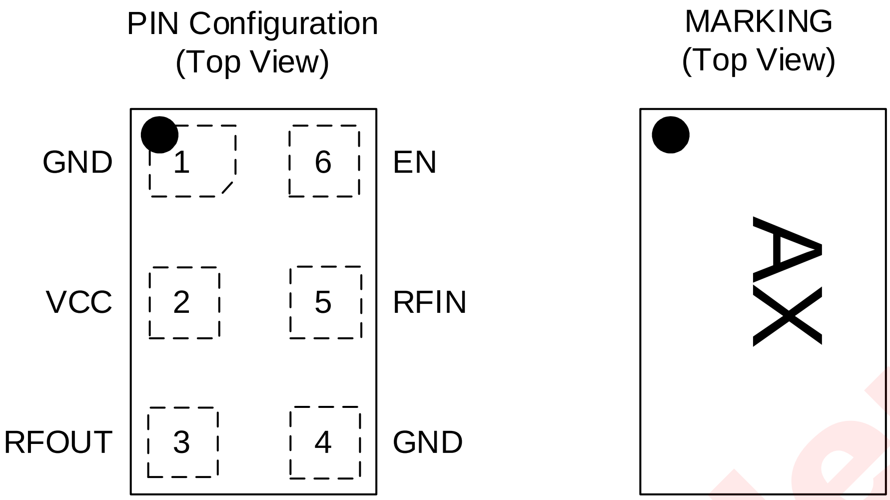
PIN CONFIGURATION AND TOP MARK



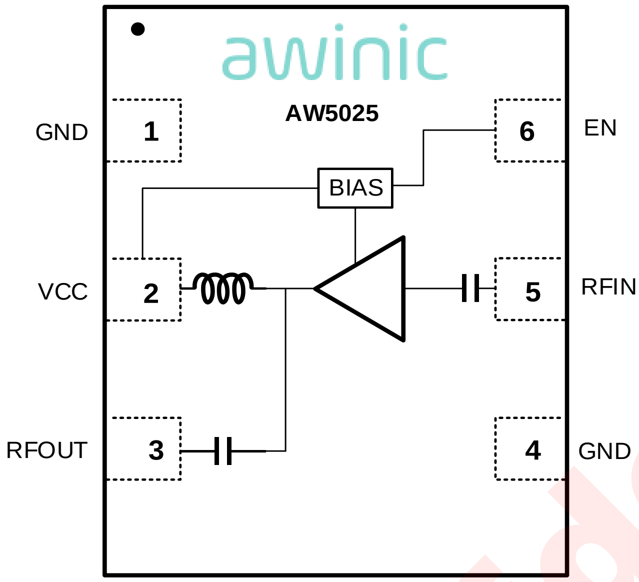
A – AW5025LGR
X – Production Trace Code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

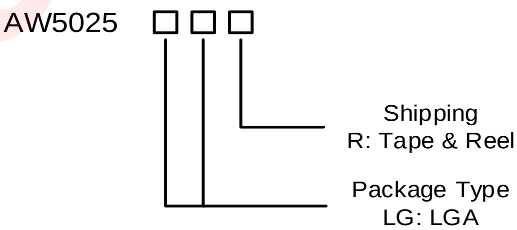
No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW5025LGR	-40°C ~ 85°C	LGA-1.1x0.7-6L	A	MSL3	ROHS+HF	6000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETERS	Symbol	Values			
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V_{CC}	-0.3	-	5	V
Voltage at pin EN [2]	V_{EN}	-0.3	-	5	V
Current into pin VCC	I_{CC}	-	-	30	mA
RF input power [3]	P_{IN}	-	-	10	dBm
Package thermal resistance	θ_{JA}	-	732	-	℃/W
Junction temperature	T_J	-	-	150	℃
Storage temperature range	T_{STG}	-65	-	150	℃
Ambient temperature range	T_{amb}	-40	-	85	℃
Solder temperature(10s)		-	260	-	℃
ESD range					
HBM [4]		±3000			V
Latch-up					
Standard: JEDEC STANDARD NO.78D NOVEMBER 2011		+IT: +400 -IT: -400			mA mA

***Note1**: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.*

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

***Note2:** Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 5.0V in order to avoid excess current.*

***Note3**: The RF input and RF output are AC coupled through internal DC blocking capacitor.*

***Note4**: HBM standard: MIL-STD-883H Method 3015.8.*

ELECTRICAL CHARACTERISTICS

(AW5025 EVB[1] ; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1550MHz to 1615MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1575.42MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.6	V
I_{SD}	Shut-Down Current	EN=Low			1	µA
I_{CC}	Supply Current	EN=High		6.9	15.0	mA
V_{EN}	Digital Input-Logic High		0.80			V
V_{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain			18.5		dB
RL_{in}	Input Return Loss			7.0		dB
RL_{out}	Output Return Loss			11.0		dB
ISL	Reverse Isolation			31.0		dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer		0.62		dB
Kf	Stability factor	f=20MHz…10GHz	1			
NF_j	Noise Figure with jammer	Pjam=-20dBm; fjam=850MHz		1.18		dB
		Pjam=-20dBm; fjam= 1850MHz		1.47		dB
		Pjam=-30dBm; fjam=850MHz		0.62		dB
		Pjam=-30dBm; fjam= 1850MHz		0.67		dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz		-9.4		dBm
$IIP3_{oob}$	Out-of-band input 3rd-order intercept point	f1=1712.7MHz; f2=1850MHz; Pin=-20dBm;		3.4		dBm
$IIP3_{oob}$	Out-of-band input 3rd-order intercept point	f1=1712.7MHz; f2=1850MHz; Pin=-30dBm;		3.6		dBm
$IIP2_{oob}$	Out-of-band input 2nd-order intercept point	f1=824.6MHz; f2=2400MHz; Pin=-20dBm		8.4		dBm
$IIP2_{oob}$	Out-of-band input 2nd-order intercept point	f1=824.6MHz; f2=2400MHz; Pin=-30dBm		8.7		dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
H2-input referred	LTE band-13 2^{nd} Harmonic	f=787.76MHz; Pin=-25dBm; fH2=1575.52MHz		-63.1		dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain		2.2		μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain		1.7		μs

Note1: *input matched to 50 ohm using a high quality-factor 9.1nH inductor.*

Note2: *0.08dB PCB losses are subtracted.*

(AW5025 EVB[1] ; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1550MHz to 1615MHz; Typical values are at VCC=1.8V and TA=+25°C, f=1575.42MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.6	V
I_{SD}	Shut-Down Current	EN=Low			1	μA
I_{CC}	Supply Current	EN=High		6.2	15.0	mA
V_{EN}	Digital Input-Logic High		0.80			V
V_{EN}	Digital Input-Logic Low				0.45	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain			18.0		dB
RL_{in}	Input Return Loss			6.5		dB
RL_{out}	Output Return Loss			14.0		dB
ISL	Reverse Isolation			30.0		dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer		0.62		dB
Kf	Stability factor	f=20MHz…10GHz	1			
NF_j	Noise Figure with jammer	Pjam=-20dBm; fjam=850MHz		1.23		dB
		Pjam=-20dBm; fjam= 1850MHz		1.51		dB
		Pjam=-30dBm; fjam=850MHz		0.65		dB
		Pjam=-30dBm; fjam= 1850MHz		0.69		dB
IP1dB	Inband input 1dB-compression point	f=1575.42MHz		-15.0		dBm
$IIP3_{oob}$	Out-of-band input 3rd-order intercept point	f1=1712.7MHz; f2=1850MHz; Pin=-20dBm;		-4.6		dBm
$IIP3_{oob}$	Out-of-band input 3rd-order intercept point	f1=1712.7MHz; f2=1850MHz; Pin=-30dBm;		-1.1		dBm
$IIP2_{oob}$	Out-of-band input 2nd-order intercept point	f1=824.6MHz; f2=2400MHz; Pin=-20dBm		7.0		dBm
$IIP2_{oob}$	Out-of-band input 2nd-order intercept point	f1=824.6MHz; f2=2400MHz; Pin=-30dBm		7.3		dBm
H2-input referred	LTE band-13 2nd Harmonic	f=787.76MHz; Pin=-25dBm;		-62.0		dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		fH2=1575.52MHz				
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain		2.2		μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain		1.7		μs

Note1: *input matched to 50 ohm using a high quality-factor 9.1nH inductor.*

Note2: *0.08dB PCB losses are subtracted.*

TYPICAL OPERATING CHARACTERISTICS

(AW5025 EVB; Typical values are at Vcc=2.8V and TA=+25°C, f_{RFIN}=1575.42MHz, unless otherwise noted.)

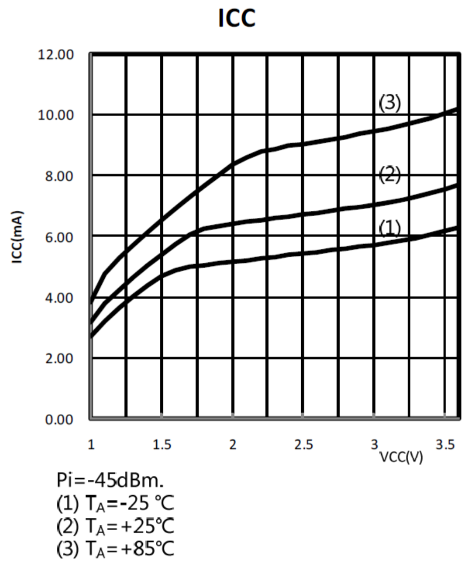


Figure 3. Supply current as a function of supply voltage; typical values

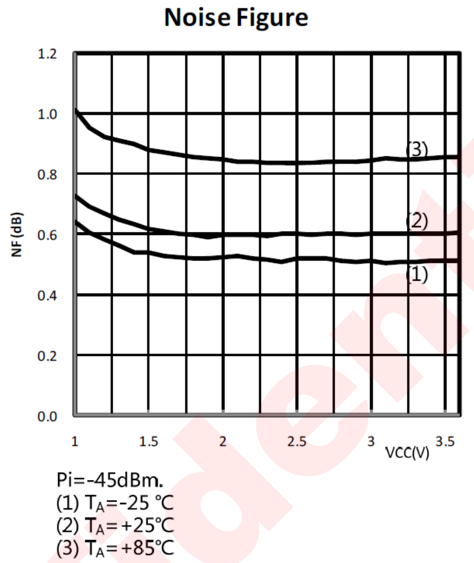


Figure 4. Noise Figure as a function of supply voltage; typical values

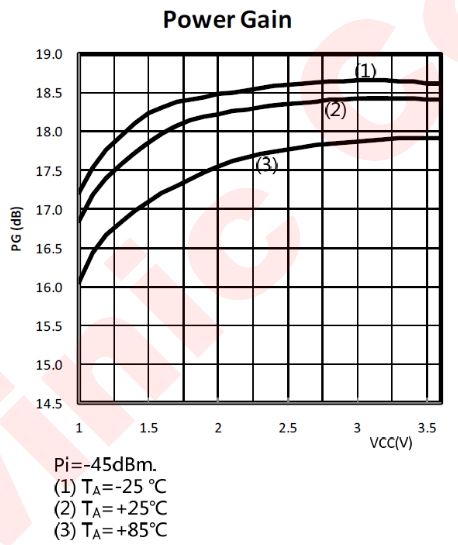


Figure 5. Power Gain as a function of supply voltage; typical values

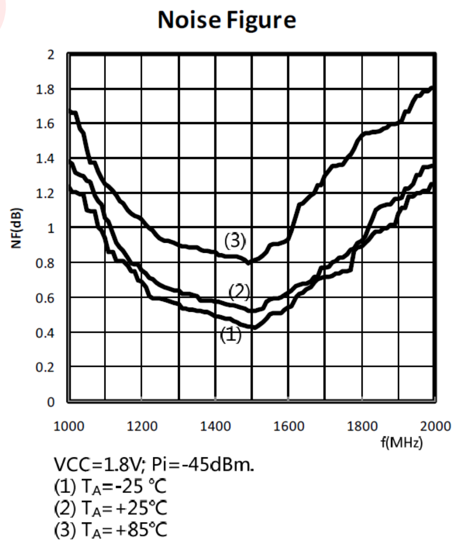


Figure 6. Noise Figure as a function of frequency; typical values

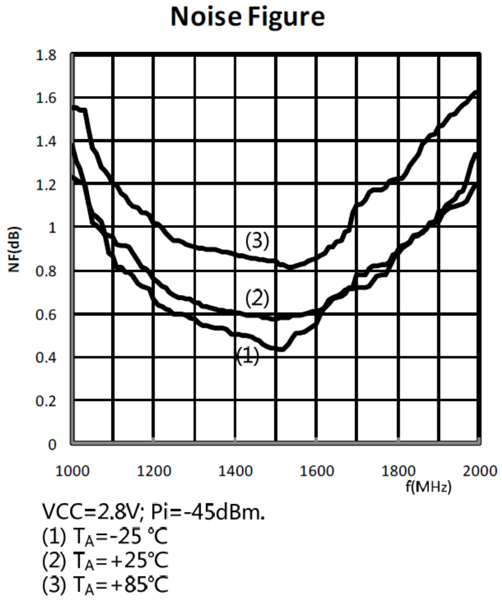


Figure 7. Noise Figure as a function of frequency; typical values

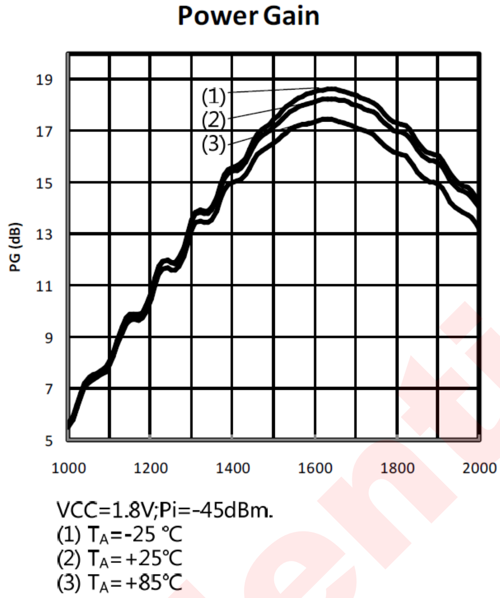


Figure 8. Power Gain as a function of frequency; typical values

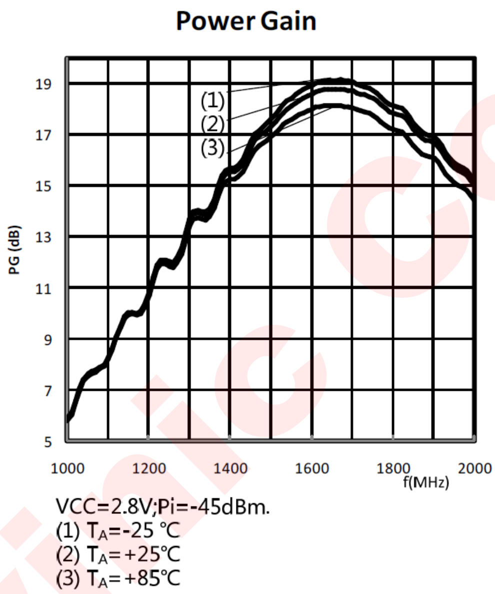


Figure 9. Power Gain as a function of frequency; typical values

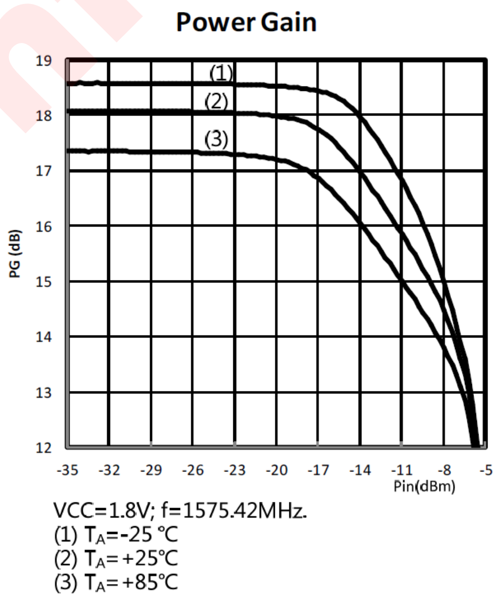


Figure 10. Power Gain as a function of input power; typical values

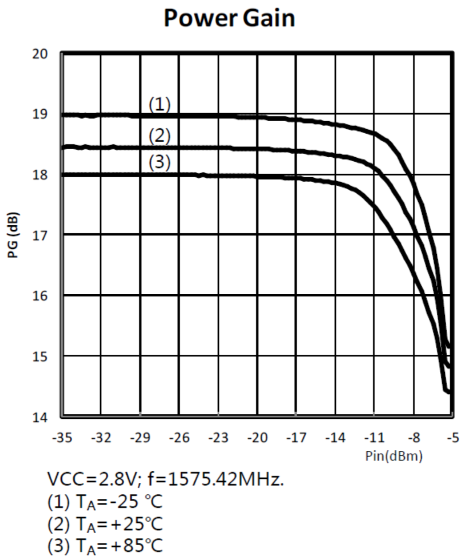


Figure 11. Power Gain as a function of input power; typical values

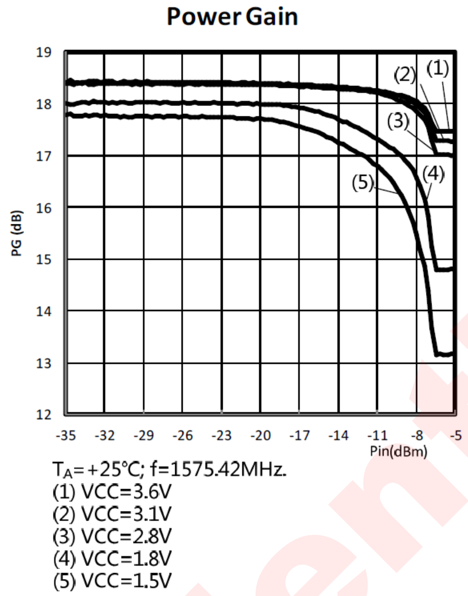


Figure 12. Power Gain as a function of input power; typical values

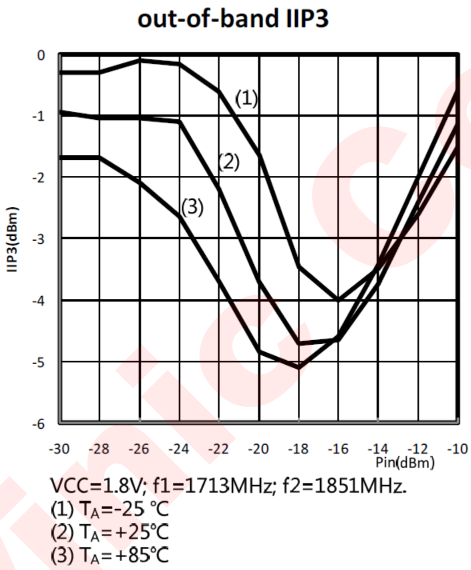


Figure 13. Out-of-band Input IP3 as a function of input power; typical values

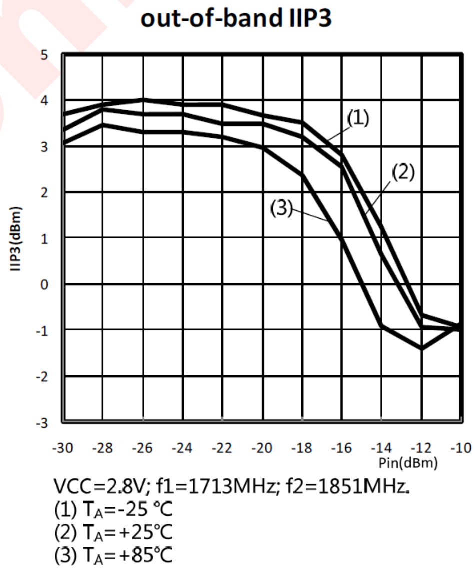


Figure 14. Out-of-band Input IP3 as a function of input power; typical values

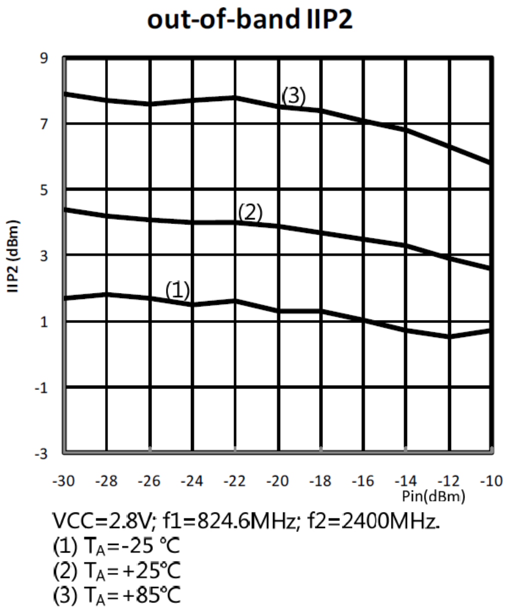


Figure 15. Out-of-band Input IP2 as a function of input power; typical values

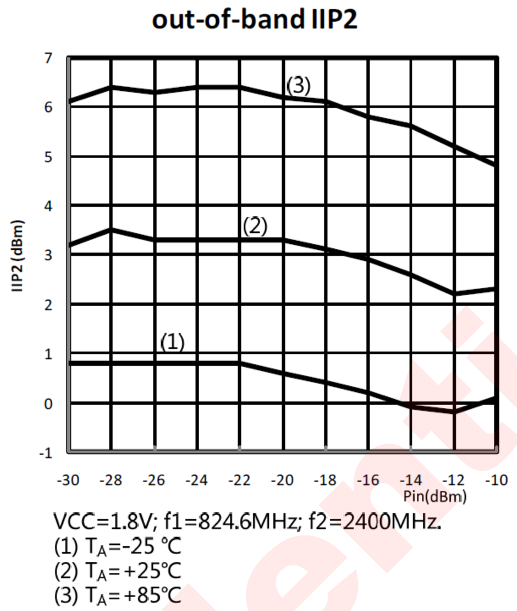


Figure 16. Out-of-band Input IP2 as a function of input power; typical values

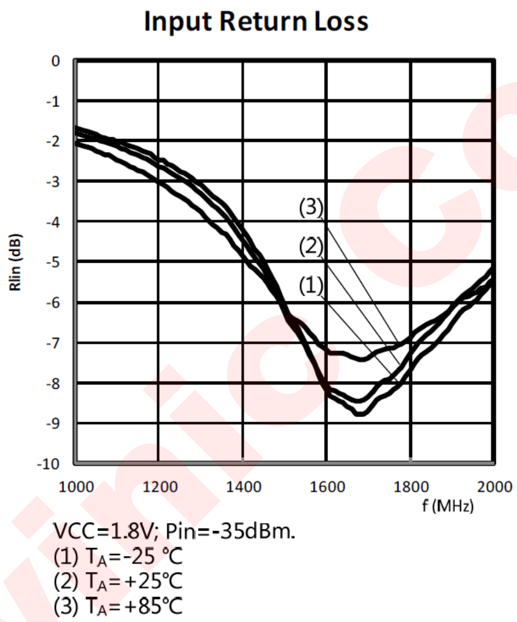


Figure 17. Input return loss as a function of frequency; typical values

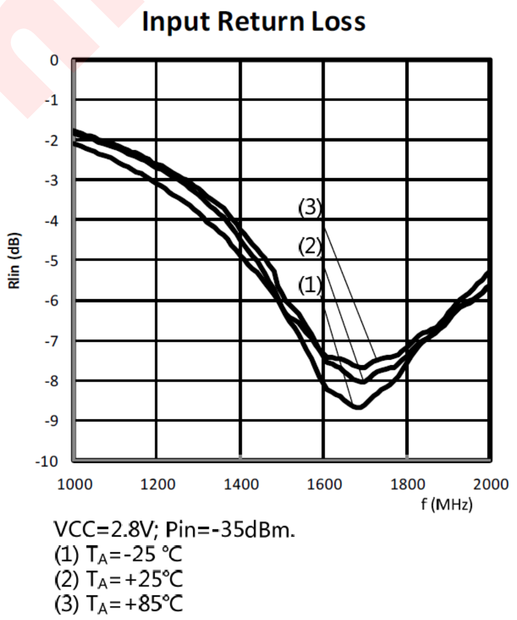
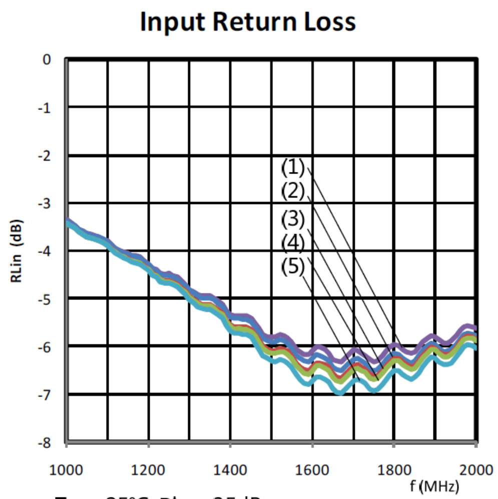
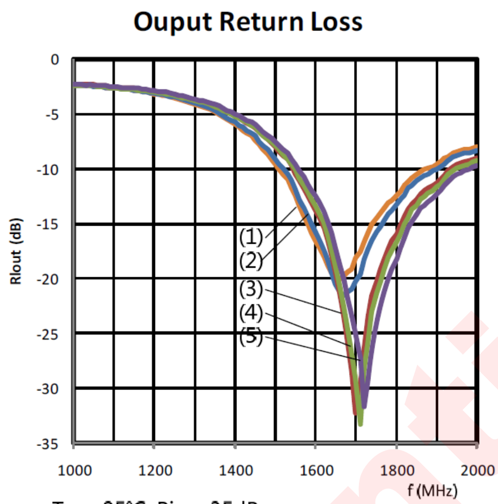


Figure 18. Input return loss as a function of frequency; typical values



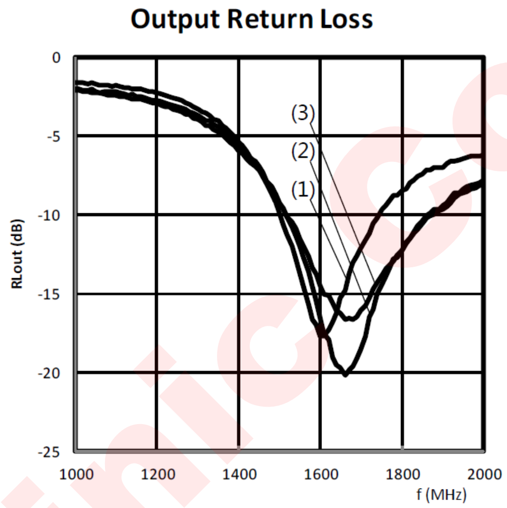
T_A=+25℃; Pin=-35dBm.
(1) VCC=1.5V
(2) VCC=1.8V
(3) VCC=2.8V
(4) VCC=3.1V
(5) VCC=3.6V

Figure 19. Input return loss as a function of frequency; typical values



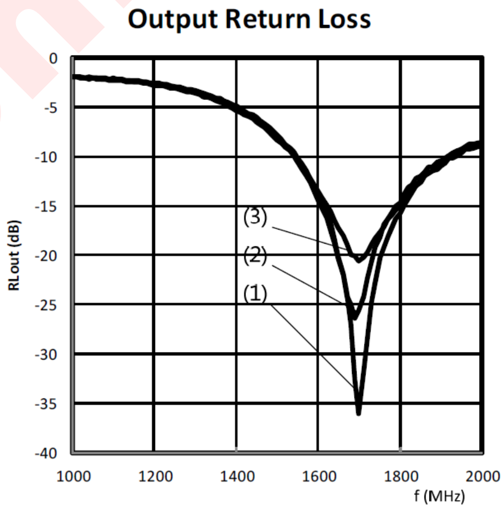
T_A=+25℃; Pin=-35dBm.
(1) VCC=1.5V
(2) VCC=1.8V
(3) VCC=2.8V
(4) VCC=3.1V
(5) VCC=3.6V

Figure 20. Output return loss as a function of frequency; typical values



VCC=1.8V; f=1575.42MHz.
(1) T_A=-25 ℃
(2) T_A=+25℃
(3) T_A=+85℃

Figure 21. Output return loss as a function of frequency; typical values



VCC=2.8V; f=1575.42MHz.
(1) T_A=-25 ℃
(2) T_A=+25℃
(3) T_A=+85℃

Figure 22. Output return loss as a function of frequency; typical values

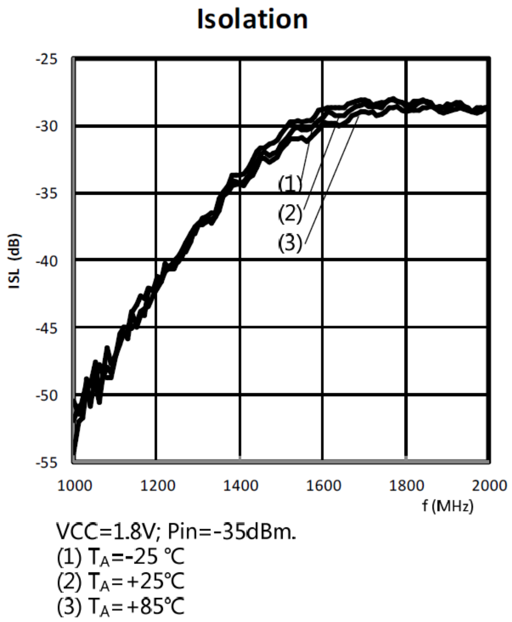


Figure 23. Isolation as a function of frequency; typical values

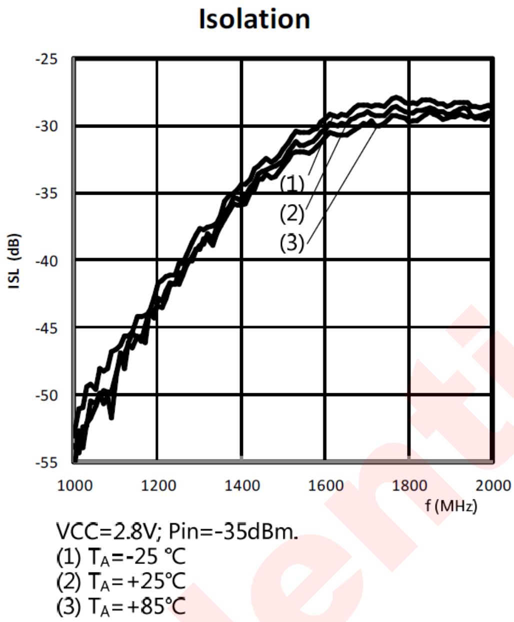


Figure 24. Isolation as a function of frequency; typical values

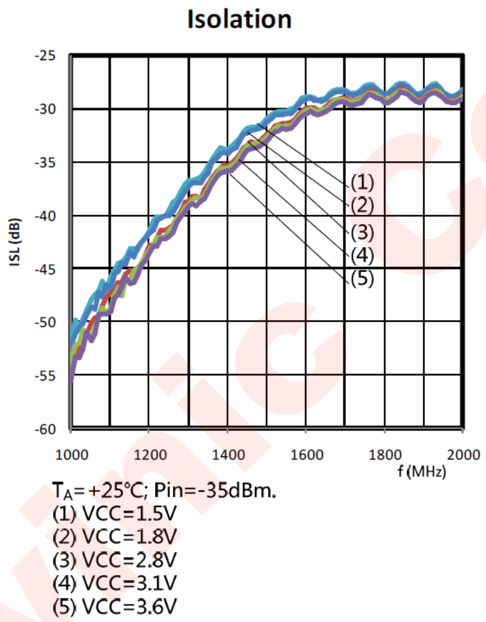


Figure 25. Isolation as a function of frequency; typical values

APPLICATION BOARD

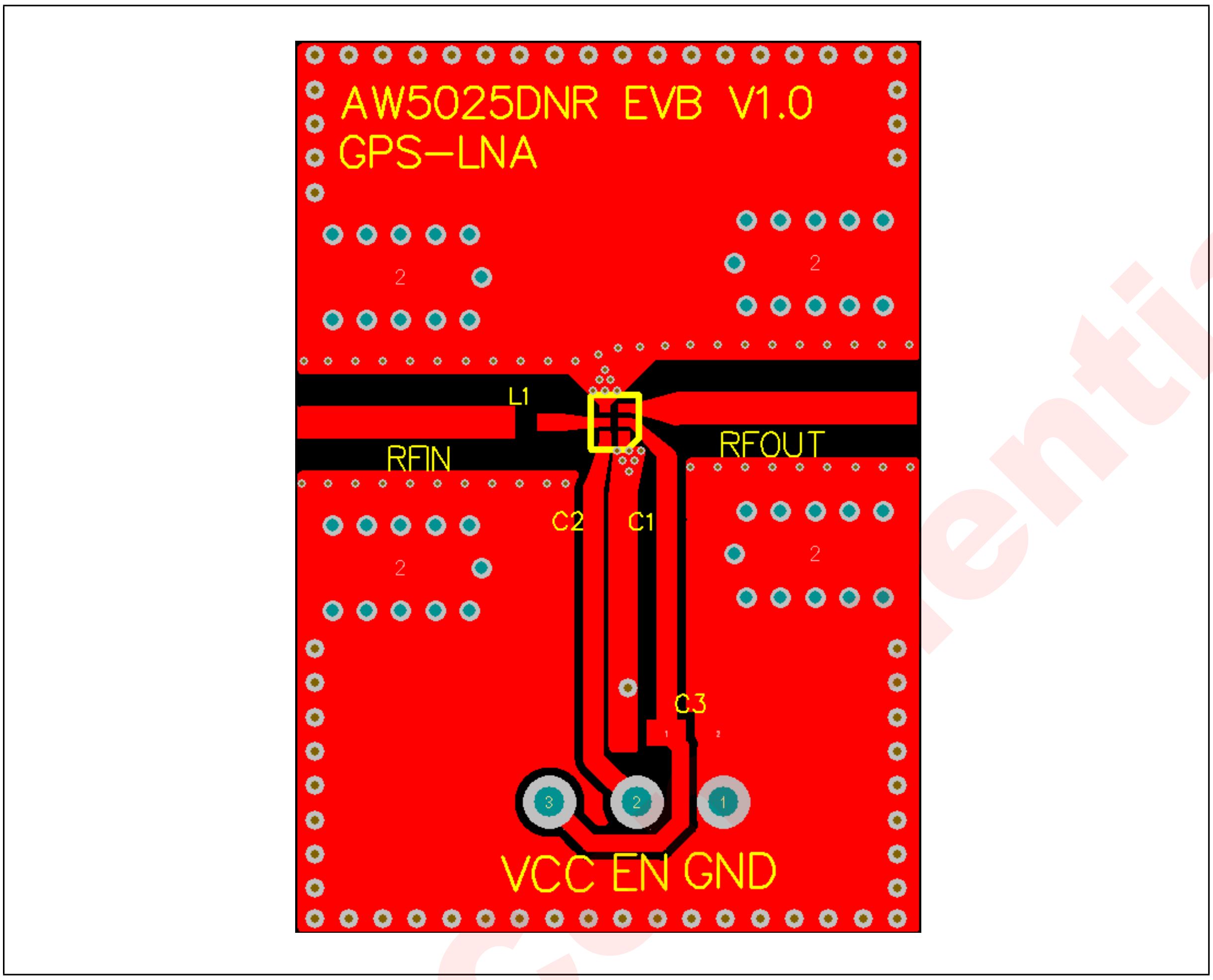


Figure 26. Drawing of Application Board

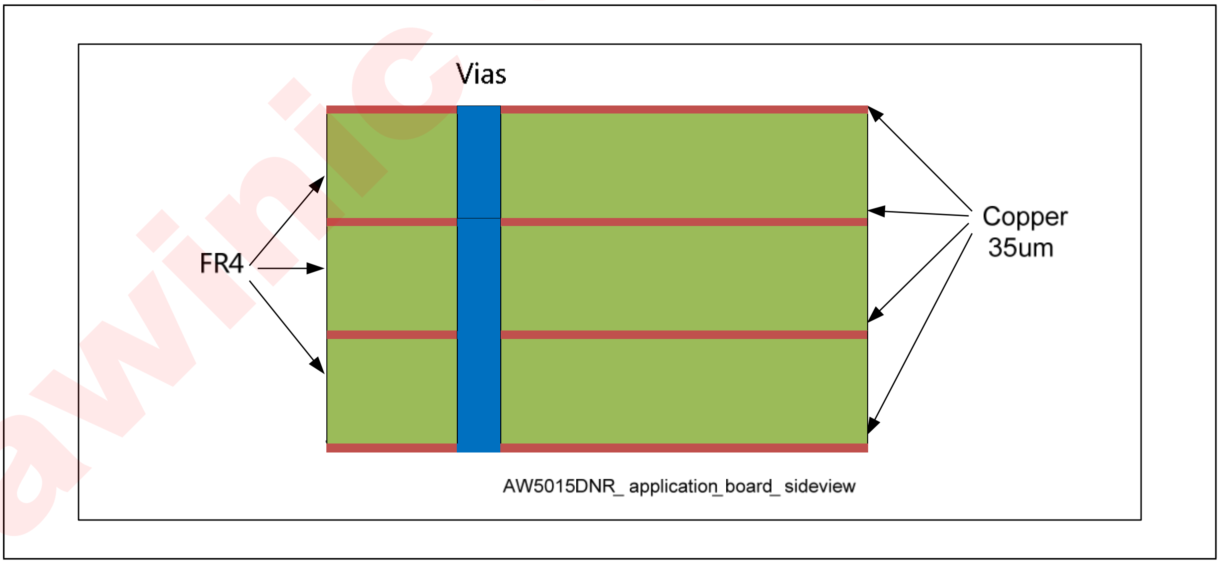
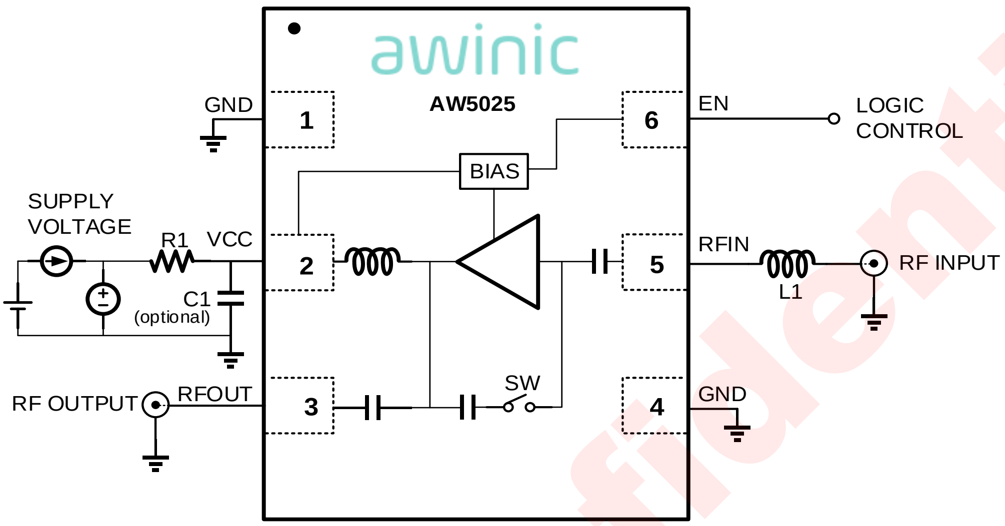


Figure 27. Application Board Cross-Section

TEST CIRCUITS

DC Characteristics

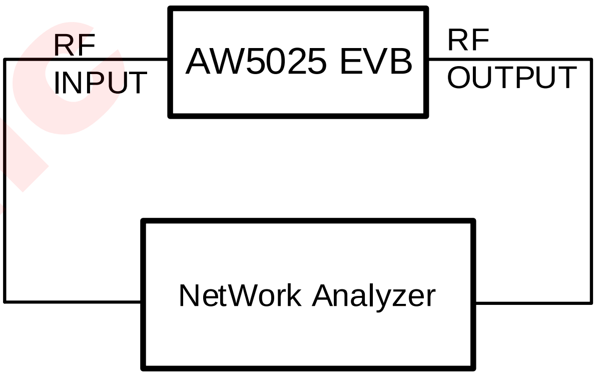
The following is the test bench for power supply, pin voltage, supply current, standby current



C1, R1 Closed to LNA

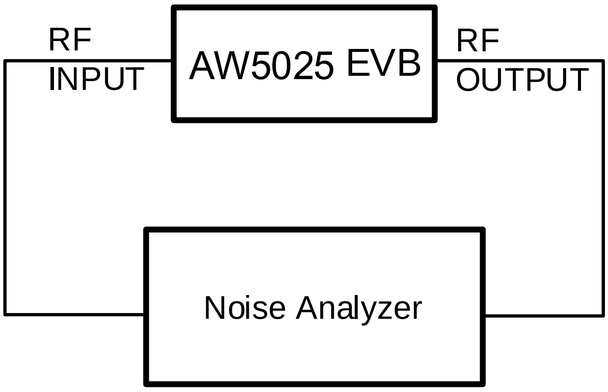
S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.



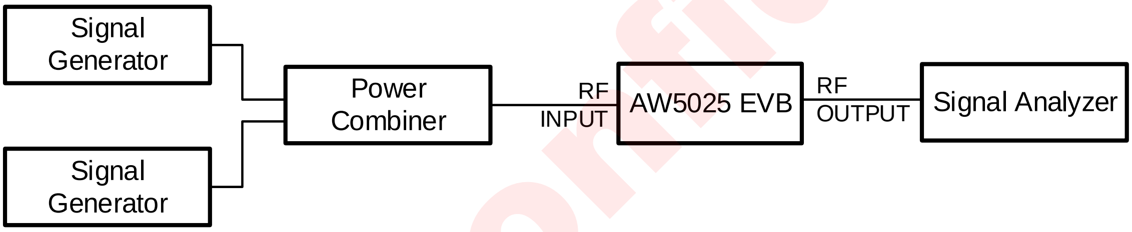
Noise Figure

The following is the test bench for noise figure, power gain.



Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.



Harmonic distortion

The following is the test bench for second-order harmonic distortion.

RECOMMENDED COMPONENTS LIST

Table1 and talble2 list the recommended inductor types and values; Table 3 lists the recommended capacitor types and values.

Table1: list of inductor for GNSS L1

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	9.1	25	250	Murata	0402
L1	SDWL1005C	9.1	24	250	Sunlord	0402

Table2: list of inductor for GNSS L2/L5

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	15/18	25	250	Murata	0402
L2	LQW15A	12	25	250	Murata	0402

Table3: list of capacitor

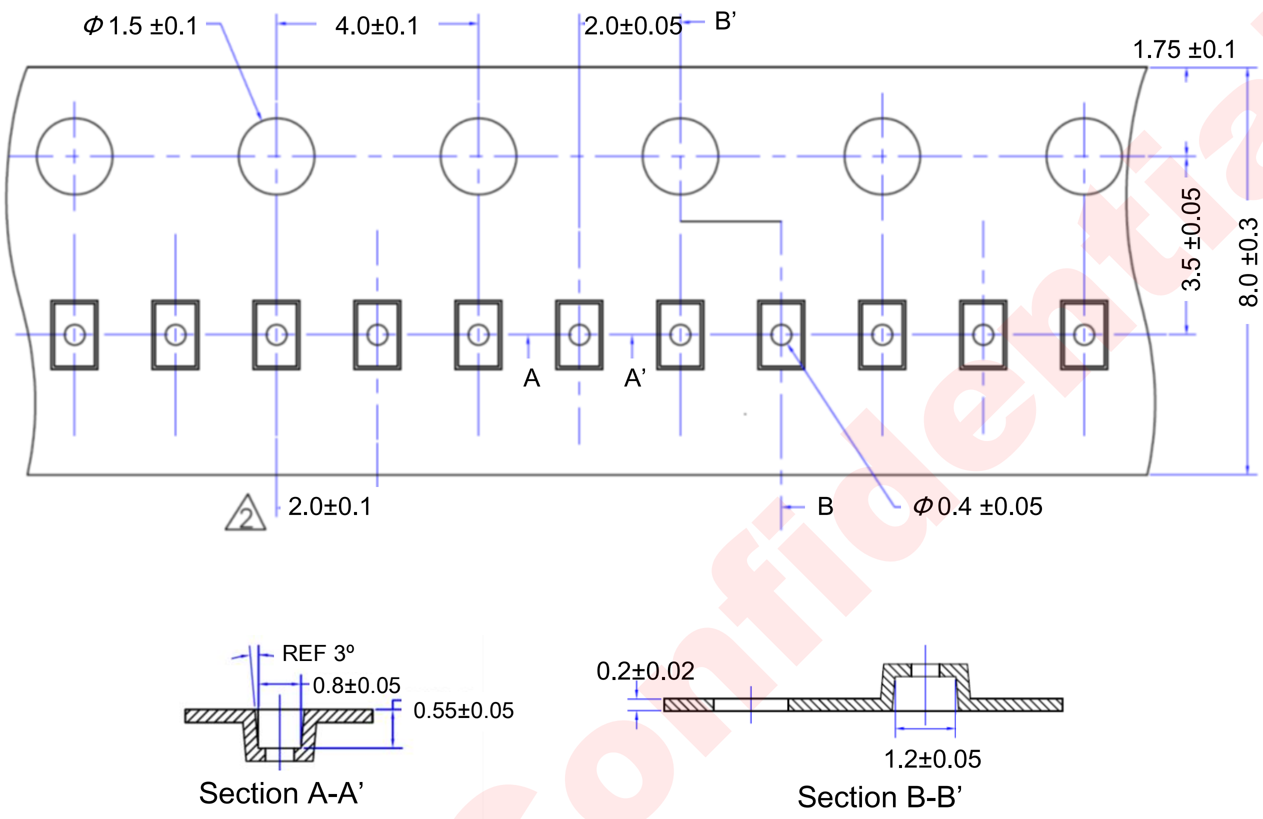
Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
	Units	pF	V		
C1	GRM155	1000	50	Murata	0402
C2	GRM155	1.8	50	Murata	0402

PCB LAYOUT CONSIDERATION

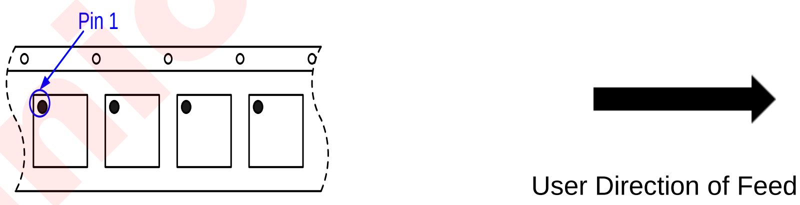
1. The AW5025 requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the capacitor we can get better performance like a little higher gain etc. The value is optimized for the best gain, noise figure, return loss performance. Typical value of inductor is 9.1nH, capacitor is 1nF. For schematics see Figure1.
2. The output of AW5025 is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.
3. The AW5025 should be placed close to the GPS antenna with the input-matching inductor. Use 50 ohm micro strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor should be located close to the device. For long VCC lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

TAPE AND REEL INFORMATION

Carrier Tape



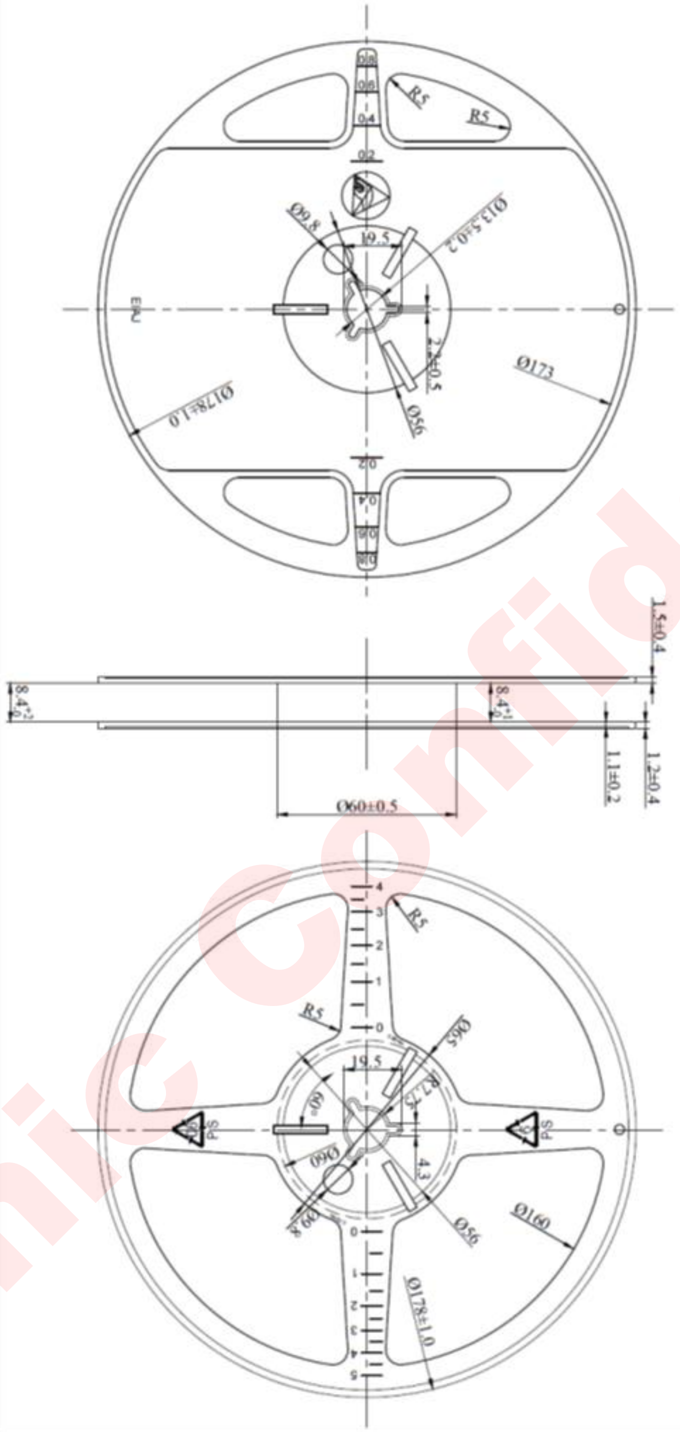
Pin 1 direction



NOTES:

1. ALL DIMS IN MM;

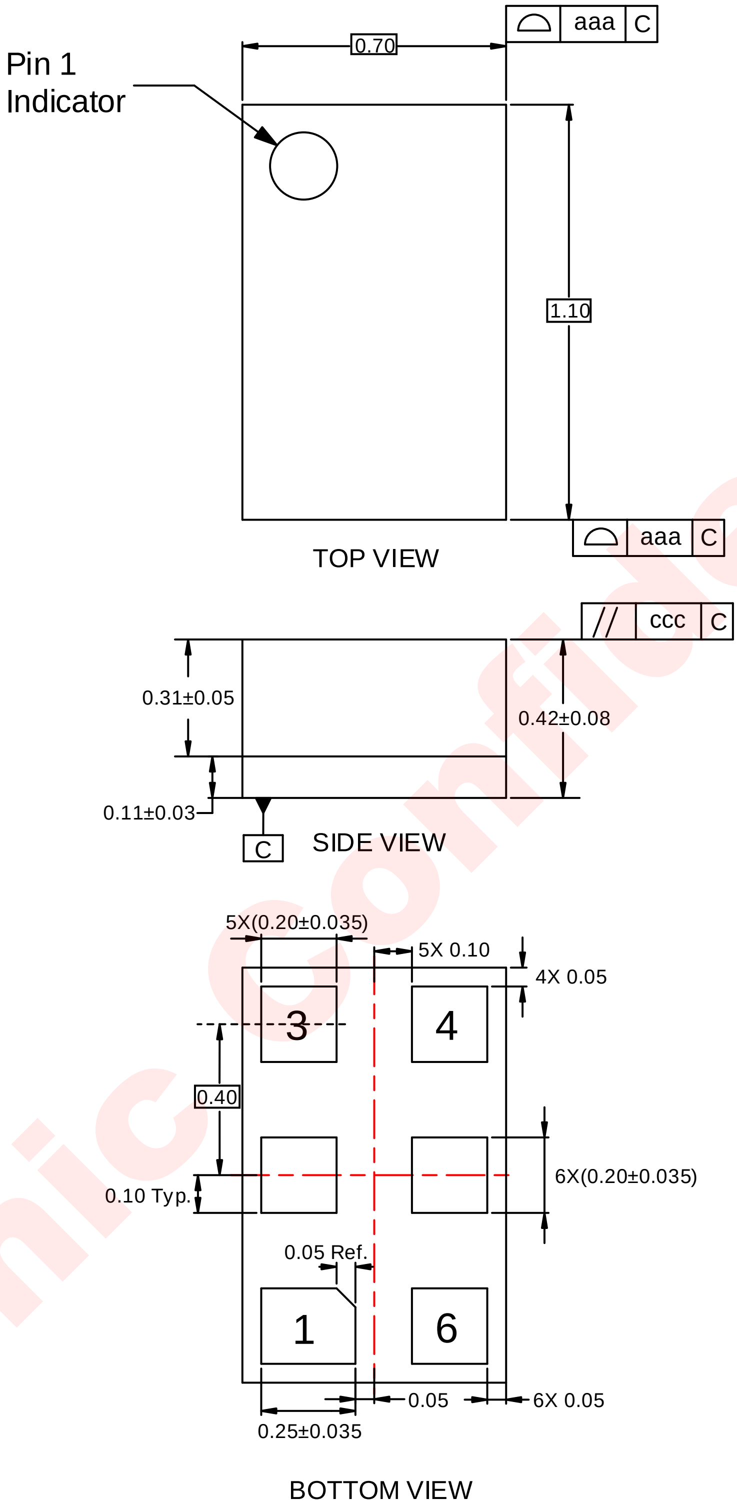
Reel



NOTES:

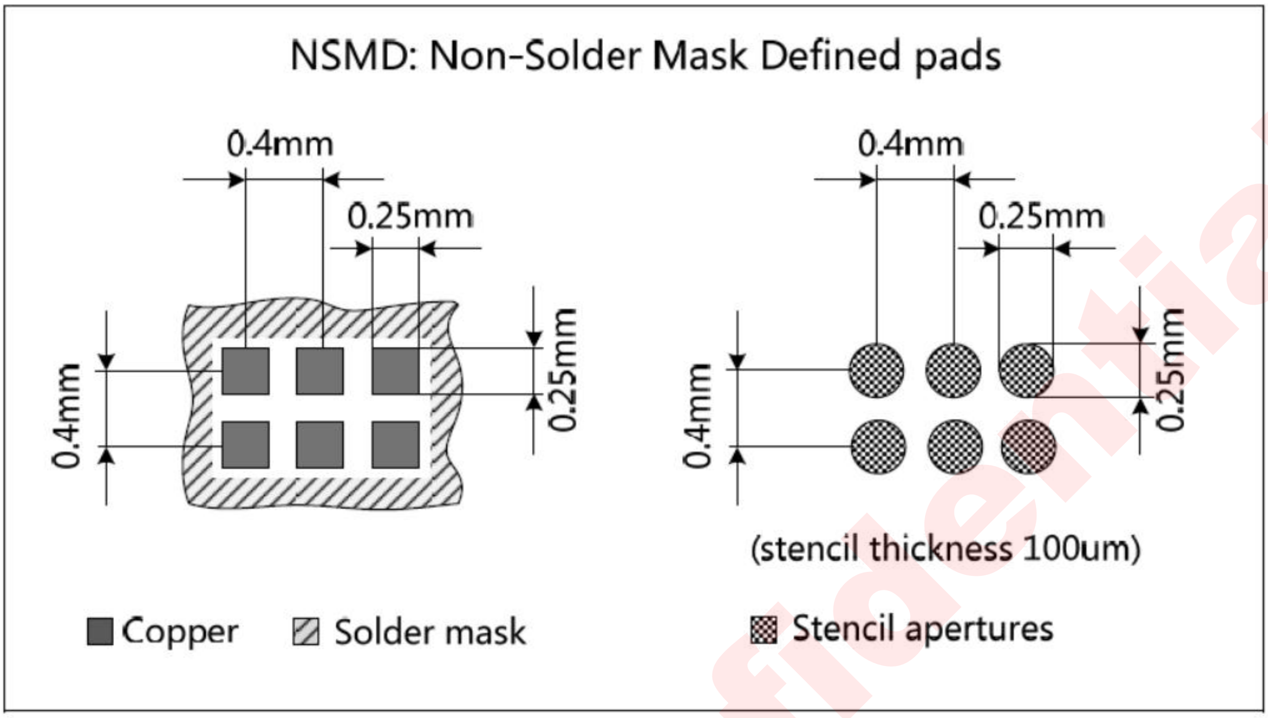
1. All dimensions in mm;
2. General Tolerance: ±0.25.

PACKAGE DESCRIPTION

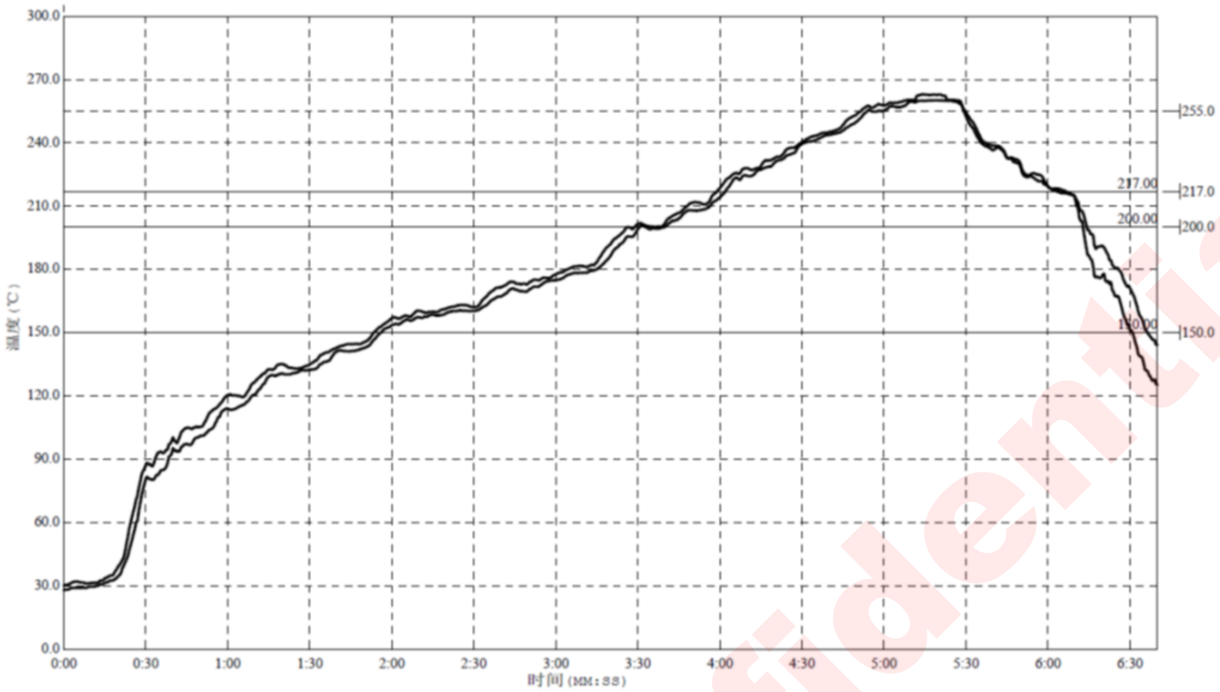


All measurements are in millimeters

LAND PATTERN DATA



REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

NOTES:

1: All data are compared with the package-top temperature, measured on the package surface;

2: AW5025 adopted the Pb-Free assembly.

REVISION HISTORY

Document ID	Release date	Change Record
AW5025_V1.5	2018-12	Updated Package thermal resistance.
AW5025_V1.4	2018-08	Added GNSS L2 and L5 application recommendation.
AW5025_V1.3	2016-04	Added Reflow notes
AW5025_V1.2	2016-01	Added Tape & Reel description and Corrected Pin 1 Marking
AW5025_V1.1	2015-05	Corrected PIN Configuration and Pack- age Information
AW5025_V1.0	2014-09	● Product data sheet ● Updated typical operating characteristics with temperature variation ● Added ESD characteristics ● Added jammed noise figure etc.
AW5025_V0.8	2014-05	Preliminary data sheet

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