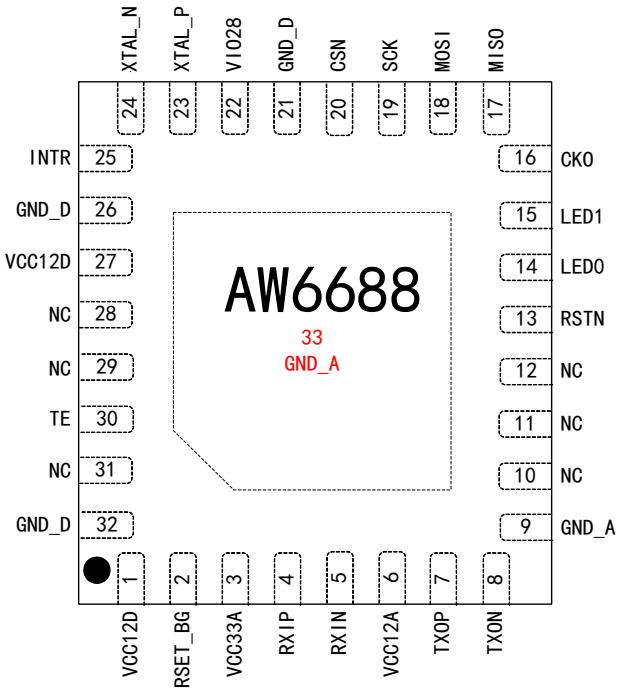
Stand-Alone Ethernet Controller

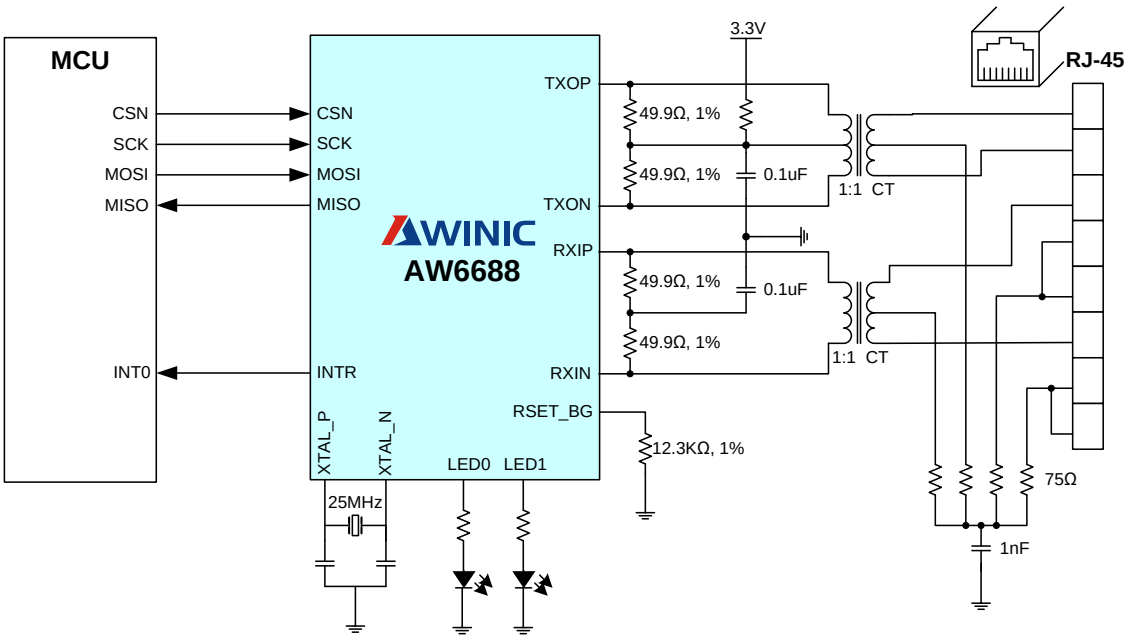
FEATURES

- 5X5 mm, 32-pin QFN
- Compatible with Motorola SPI SPEC
  - Input clock frequency up to 60MHz
  - Only support phase 0
  - Only support polarity 0
- IEEE 802.3 compatible Ethernet controller
- Fully compatible with 10/100 BASE-T networks
- Integrated MAC and 10/100 PHY
- Supports full and half duplex modes
- Programmable padding and CRC generation
- Programmable padding and CRC stripping
- Programmable flow control
- Supports Ethernet frame length up to 1522 bytes
- Flexible address filtering modes
- 8k byte receive buffer
- 4k byte transmit buffer
- Multi-function LED output
- 2.8V IO supply and 1.2V core supply
- CMOS process technology

The AW6688 adopts TRQ5x5-32L package:



1 APPLICATION



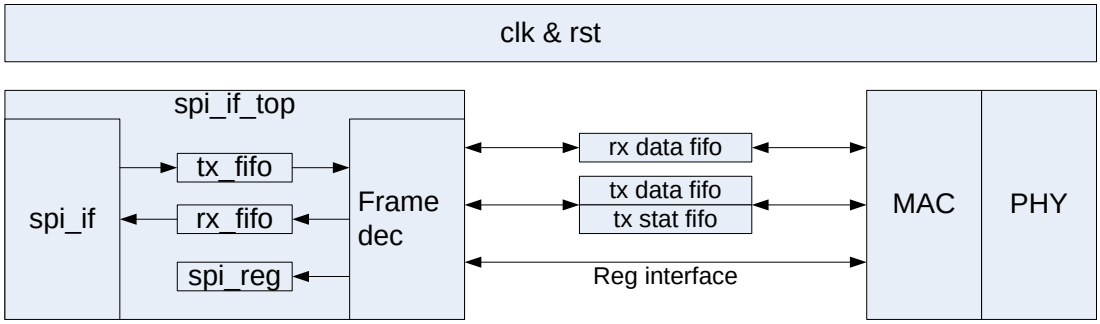
2 ORDER INFORMATION

Order Number	Temperature Range	Package	Marking	Packing Type
AW6688TQR	-40~85℃	TRQ5x5-32L	AW6688	Tape & Reel

3 OVERVIEW

AW6688 is a standalone SPI to Ethernet converter which serves as an Ethernet network interface for any controller with SPI master interface. The SPI interface is fully compatible with MOTO SPI interface SPEC and only supports phase 0 and polarity 0 of the SPI clock. The clock rate of the SPI interface is up to 60MHz. A dedicated interrupt output is used to communicate with the SPI master chip. The Ethernet interface of AW6688 is fully compatible with IEEE802.3 protocol. A number of embedded filters are used to limit the incoming Ethernet packets. Integrated hardware CRC calculator helps to release the CPU power of the master. A 4k byte transmit buffer and an 8k byte receive buffer is integrated. Stream mode of transferring the Ethernet packets through the SPI interface is supports under which the SPI transfer boundary can be at any word boundary of the Ethernet packets. The block diagram of the chip is shown below.

Figure 1 AW6688 block diagram



The function of the major block of AW6688 is listed below:

- SPI_IF: the SPI_IF serves as the SPI protocol decoder and serial to parallel converter.
- TX_FIFO, RX_FIFO: the FIFO servers as the synchronizer between the SPI clock domain and the system clock domain.
- FRAME_DEC: the FRAME_DEC decodes and encodes the SPI packet, performs the register programming, recognizes the Ethernet packets and performs the data transfer between the internal data FIFO.
- SPI_REG: all the SPI related registers and the interrupt related logic are implemented in the SPI_REG
- MAC: the MAC implements the IEEE802.3 compliant MAC logic.
- PHY: the PHY performs the data transfer between the analog interface and the MAC.

4 IO DESCRIPTION

Table 1 IO description

Name	Number	Type	Dir	Description
VCC12D	1	PWR		1.2V digital power supply
RSET_BG	2	ANA	I	Off-chip resistor, connect a resistor of 12.3 kΩ ±1% to the ground
VCC33A	3	PWR		3.3V analog power supply
RXIP	4	ANA	I	Differential received signal pair. The differential data from the media is received on the RXIP/RXIN signal pair in the MDI mode.
RXIN	5	ANA	I	
VCC12A	6	PWR		1.2V analog power supply
TXOP	7	ANA	O	Differential transmitted signal pair. The differential data is transmitted to the media on the TXOP/TXON signal pair in the MDI mode.
TXON	8	ANA	O	
GND_A	9	GND		Analog ground
NC	10	PD		
NC	11	PD		
NC	12	PD		
RSTN	13	PU	I	System reset input, low active
LED0	14	PD	O	LED output
LED1	15	PD	O	LED output
CKO	16		O	Clock output
MISO	17		O	SPI MISO
MOSI	18		I	SPI MOSI
SCK	19		I	SPI SCK
CSN	20	PU	I	SPI CSN
GND_D	21	GND		Digital ground
VIO28	22	PWR		2.8V digital IO power supply
XTAL_P	23	XTAL	I	25-MHz crystal input. A 25-MHz parallel-resonant crystal is used to connect these pins.
XTAL_N	24	XTAL	O	
INTR	25	PD	O	Interrupt output
GND_D	26	GND		Digital ground
VCC12D	27	PWR		1.2V digital power supply
NC	28	PD		
NC	29	PD		
TE	30		I	Test enable, high active

Name	Number	Type	Dir	Description
NC	31			
GND_D	32	GND		Digital ground
GND_A	33	GND		Analog ground, located at the centre of the bottom

Note:

PWR: power

GND: ground

ANA: analog function pin

PU: pull up digital function pin

PD: pull down digital function pin

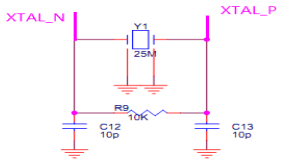
XTAL: crystal pin

5 EXTERNAL CONNECTIONS

5.1 Oscillator

AW6688 is designed to operate at 25MHz with an external crystal connected to XTAL_P and XTAL_N, To comply with IEEE 802.3 Ethernet timing requirements, the clock must have no more than ±50 ppm of total error;

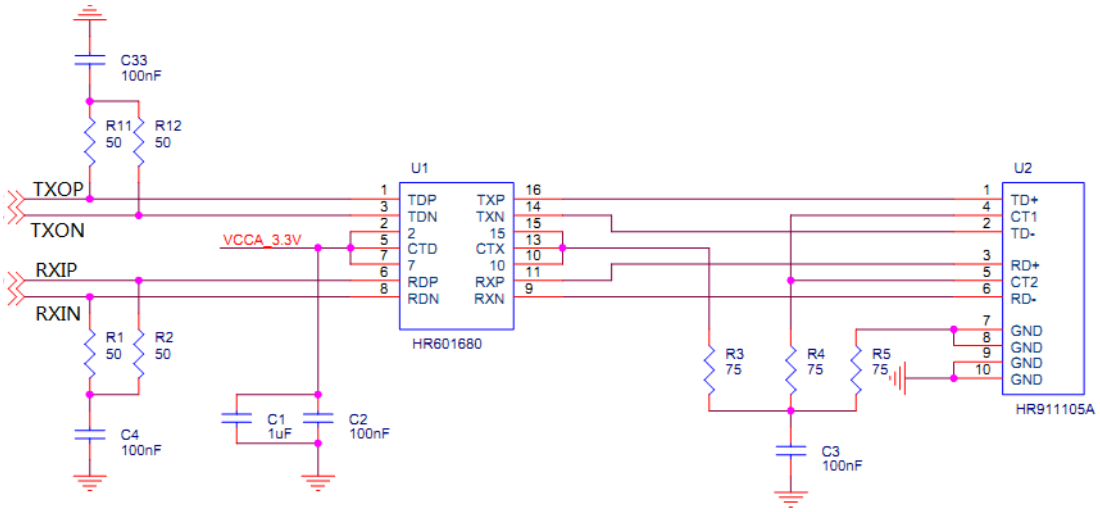
When clocking the device using a crystal, follow the connections shown in the following figure.



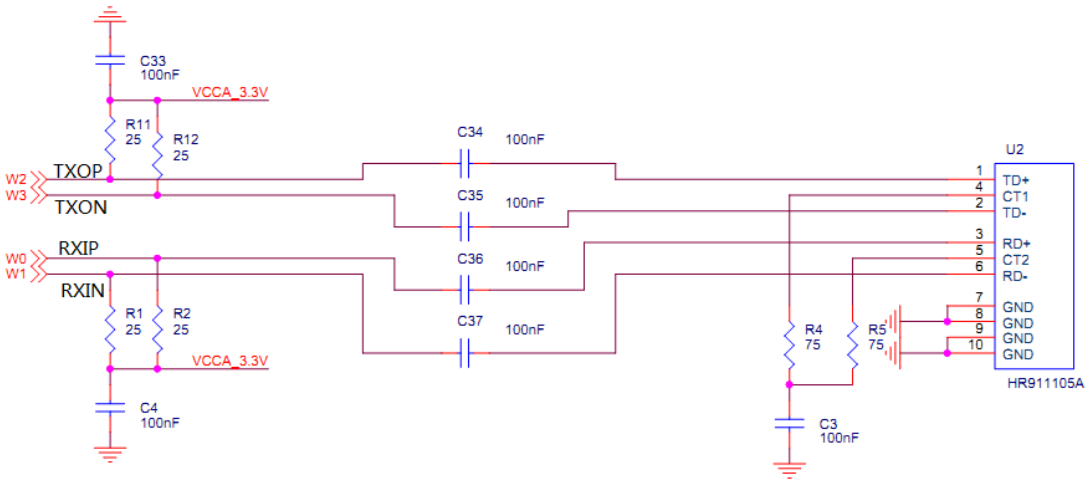
When using a CMOS clock oscillator or other external clock source, please connect the clock source directly to pin XTAL_P, and leave XTAL_N open.

5.2 Ethernet signal pins

Typical applications for AW6688 devices require an Ethernet transformer module, and a few resistors and capacitors to implement a complete IEEE 802.3 compliant 10/100 Ethernet interface, as shown in the following figure



For cost reduction purpose, following transformerless circuit also works with degraded signal quality.



5.3 SPI interface pin

There are four pins on the SPI interface: CSN, MISO, MOSI, and SCK. These pins will be connected to the SPI interface of external baseband or application processor chip. For example, in our demo cell phone chip based on MT6513/73, these pins are connected to MT6513/73's TDP1(B6), TDP0(B3), TCN(B5), TDN1(A6) respectively.

5.4 INTR pin

The INTR pin is interrupt pin of AW6688. It's connected to baseband or application processor's interrupt input or GPIO pin. For example, in our demo cell phone chip based on MT6513/73, the INTR is connected to MT6513/73's LSCE1B(P4) pin.

5.5 LED0 and LED1 pins

The LED0 and LED1 pins provide dedicated LED status indicator outputs. The LEDs are intended to display link status and TX/RX activity among other programmable options; a current-limiting resistor is generally required along with the LEDs.

5.6 Digital IO levels

The SPI interface and INTR digital IOs are characterized with central voltage at both 2.8V and 3.3V. So AW6688 can be connected directly to both baseband chips with 2.8V digital IO, such as MTK 6513/73, MT6515/75; and application processor chips with 3.3V digital IO.

5.7 Power supply pins

AW6688 has three group voltage supplies. 1.2V, 3.3V and 2.8V. All the powers can be supplied by baseband chip, such as MTK's MT6513/73. the power consumption under different operating condition is as following:

Current under different working conditions (mA)

Power Supply	100M	10M	PHY pwrdn	PHY/MAC down	chip pwrdn
3.3V Analog	53.4	23	0.9	0.9	0
2.8V Digital IO	4	4	3.9	0	0
1.2V Analog	37.7	0.006	0.003	0.003	0
1.2V PLL	3.7	1.7	0.015	0.015	0
1.2V Digital	15.9	3.8	1.7	0	0

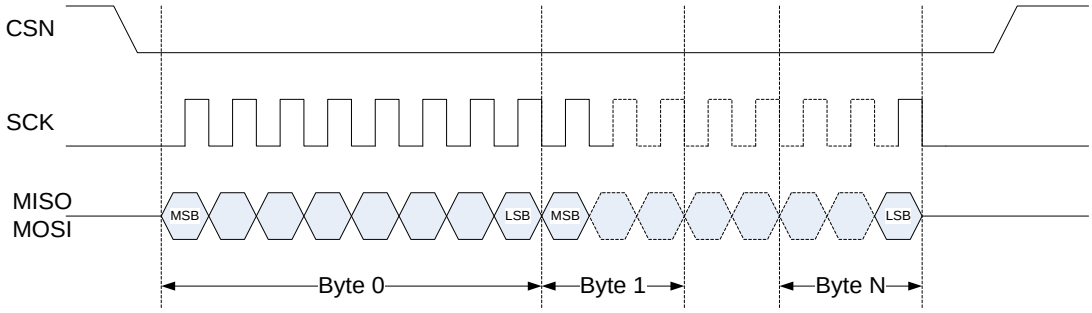
Specifically in 10M receiver mode, the overall current is only 16mA.

6 FUNCTIONAL DESCCRIPTION

6.1 SPI Interface

The SPI interface of the chip is compatible with the MOTO SPI protocol but only supports polarity 0 and phase 0. And the SPI transfer must be byte alignment. The SPI protocol supported by the chip is shown as below.

Figure 2 SPI timing



The first few bytes (byte 0 to byte3) after the negative edge of the SPI CSN on the SPI MOSI contain the SPI command which is defined as below. The bytes after the SPI command are the SPI payload which contains the data. The command ID is defined in bit 7 to bit 4 of the first byte of the SPI transfer which is shown in the second column of the table below.

Table 2 SPI command

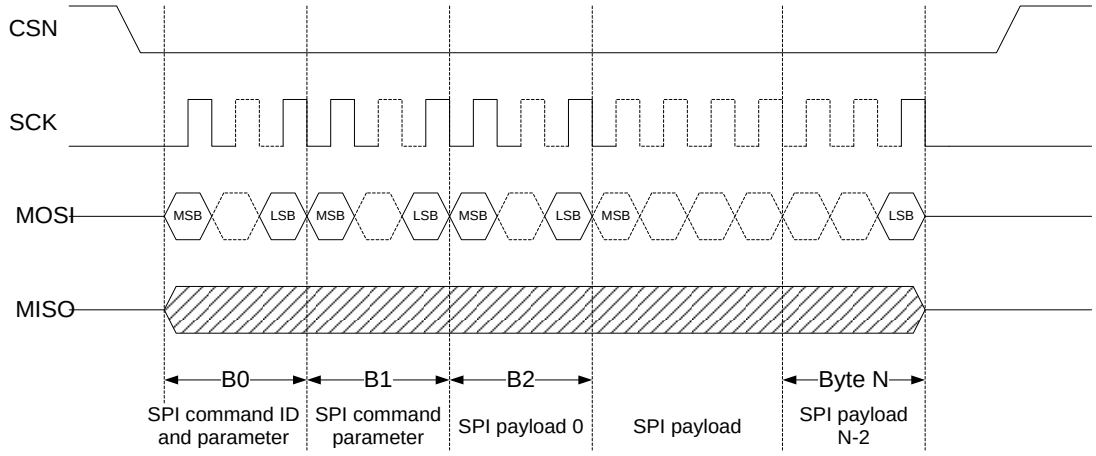
function	B0[7:4]	B0[3:0]	B1	B2	B3	B4	B5
write int reg	4'b0000	addr[11:8]	addr[7:0]	data0	data1	data2	data3
read int reg	4'b0001	addr[11:8]	addr[7:0]	dummy wait	dummy wait	data0	data1
write mac reg	4'b0010	addr[11:8]	addr[7:0]	data0	data1	data2	data3
read mac reg	4'b0011	addr[11:8]	addr[7:0]	dummy wait	dummy wait	data0	data1
write tx fifo	4'b0100	len[11:8]	len[7:0]	data0	data1	data2	data3
read rx fifo	4'b0101	len[11:8]	len[7:0]	dummy wait	dummy wait	data0	data1
fifo_rw	4'b0110	rx_len[11:8]	rx_len[7:0]	{4'b0,tx_len[11:8]}	tx_len[7:0]	data0	data1
read_tx_stat	4'b0111	8'b0	{3'b0,len[4:0]}	dummy wait	dummy wait	data0	data1
reset all	4'b1111	4'b1111	dummy wait				

6.1.1 Write INT REG Command

The command ID of the write INT REG command is 4’b0000. This command is used to write the internal control registers. The address in the command is the byte address of the first data byte in

the SPI command. The length of the command is unlimited. The address of the data byte following the first data byte of the SPI command is increased one by one.

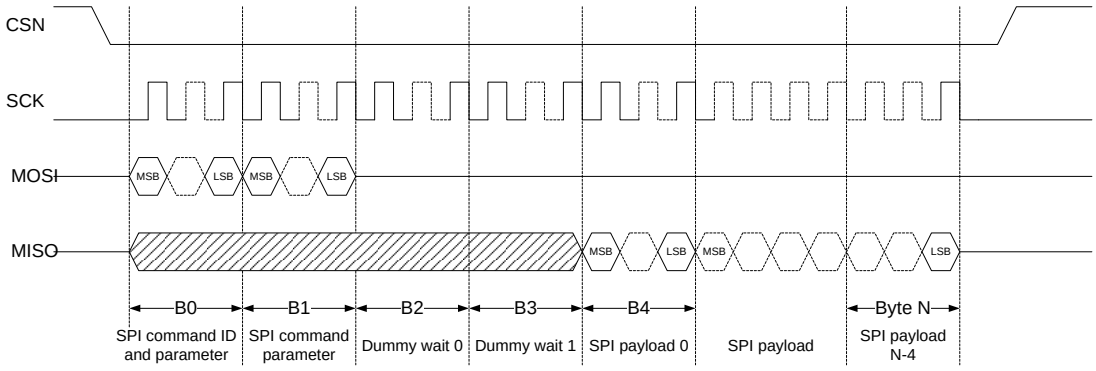
Figure 3 SPI write internal register command timing



6.1.2 Read INT REG Command

The command ID of the write INT REG command is 4'b0001. This command is used to read the internal control registers. The address in the command is the byte address of the first data byte in the SPI command. The two dummy wait bytes after the address are for the chip to get the read data ready. The length of the command is unlimited. The address of the data byte following the first data byte of the SPI command is increased one by one.

Figure 4 SPI read internal register timing

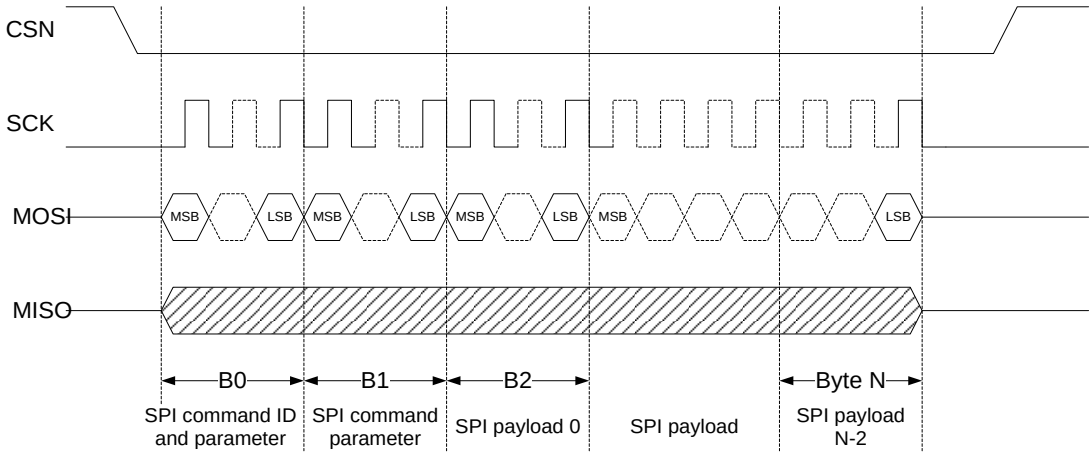


6.1.3 Write MAC REG Command

The command ID of the write MAC REG command is 4'b0010. This command is used to write the MAC control registers. The address in the command is the byte address of the first data byte

in the SPI command. The difference between this command and the write INT REG command is that the registers of the MAC written by the command will not cross the word (32 bit) boundary. For example if the address in the SPI command is point to 0x001, then only the first three data bytes will be written to address 0x001, 0x002 and 0x003. All the data bytes following will be dropped by the SPI interface. So the maximum number of the valid data byte is 4 in this SPI command.

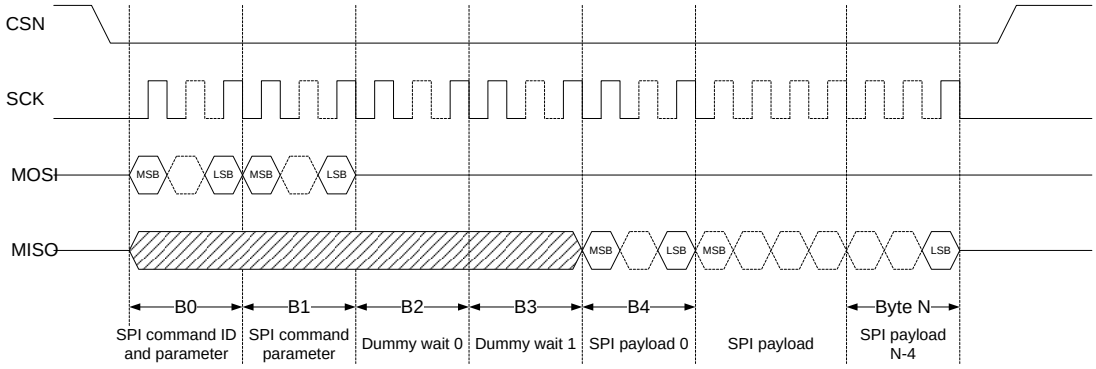
Figure 5 SPI write MAC register timing



6.1.4 Read MAC REG Command

The command ID of the write MAC REG command is 4'b0011. This command is used to read the MAC control registers. The address in the command is the byte address of the first data byte in the SPI command. The difference between this command and the read INT REG command is that the registers of the MAC read by the command will not cross the word (32 bit) boundary. For example if the address in the SPI command is point to 0x001, then only the first three data bytes will be valid and is read from the address 0x001, 0x002 and 0x003. All the data bytes following shall be dropped by the SPI master. So the maximum number of the valid data byte is 4 in this SPI command.

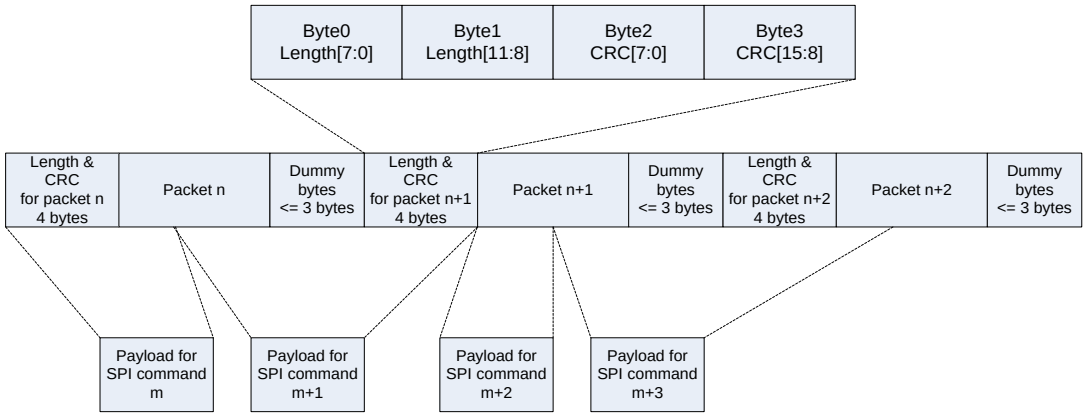
Figure 6 SPI read MAC register timing



6.1.5 Write TX FIFO Command

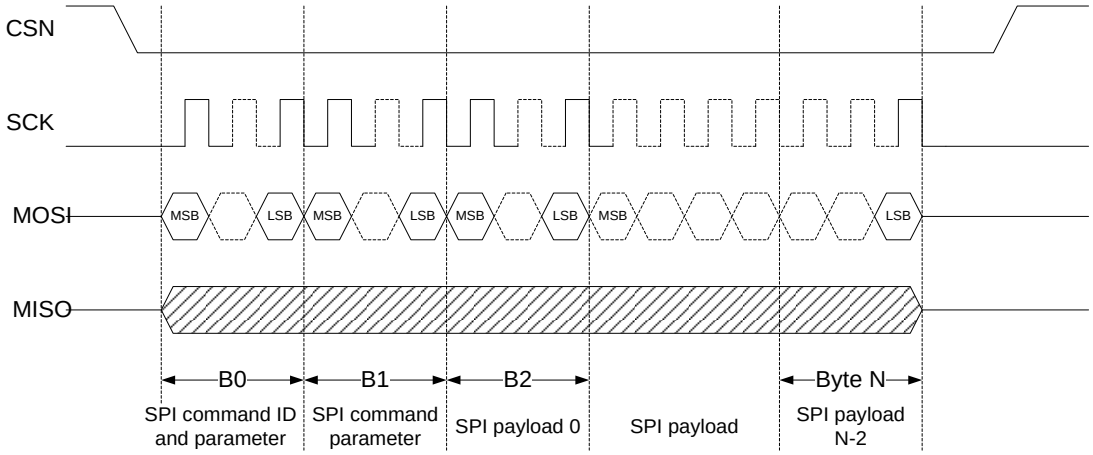
The command ID of the write TX FIFO command is 4'b0100. This command is used to write the data to the TX FIFO. The length in the command indicates the data number in word (32 bit) following. The data in the command is little endian which means that byte0 (bit 7 to bit0) of one word is transferred firstly and byte 3 (bit 31 to bit 24) is transferred last. The payload (data byte following the length) of the SPI command is continuous Ethernet packet separated by four bytes which contains the packet length of the following Ethernet packet and the CRC of the packet length and the dummy bytes which makes the overall length of one Ethernet packet including the length and CRC and raw packet and the dummy bytes to be multiply of 4 bytes. Also the number of byte of the payload of single SPI write TX FIFO command must be multiply of 4. The relationship of the Ethernet packet and the SPI command payload is shown as below.

Figure 7 SPI write TX FIFO payload



The CRC applied here is 16 bit CRC which the coordinates of the origin polynomial is 17'h18005.

Figure 8 SPI write TX FIFO timing



6.1.6 Read RX FIFO Command

The command ID of the read TX FIFO command is 4'b0101. This command is used to read the data to the RX FIFO. The length in the command indicates the data number in word (32 bit) following. The data in the command is little endian which means that byte0 (bit 7 to bit0) of one word is transferred firstly and byte 3 (bit 31 to bit 24) is transferred last. The two dummy wait bytes after the address are for the chip to get the read data ready. The payload (data byte following the dummy bytes) is almost the same as the payload of the write TX FIFO command except that the RX status is inserted between the dummy bytes of the current Ethernet packet and the length of the next Ethernet packet. The RX status is described in the table below. Also the number of byte of the payload of single SPI read RX FIFO command must be multiply of 4.

Figure 9 SPI read RX FIFO payload

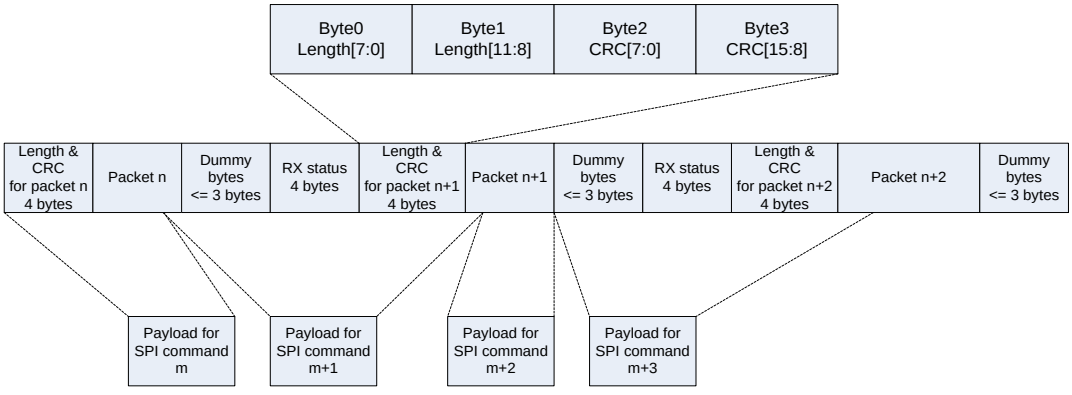
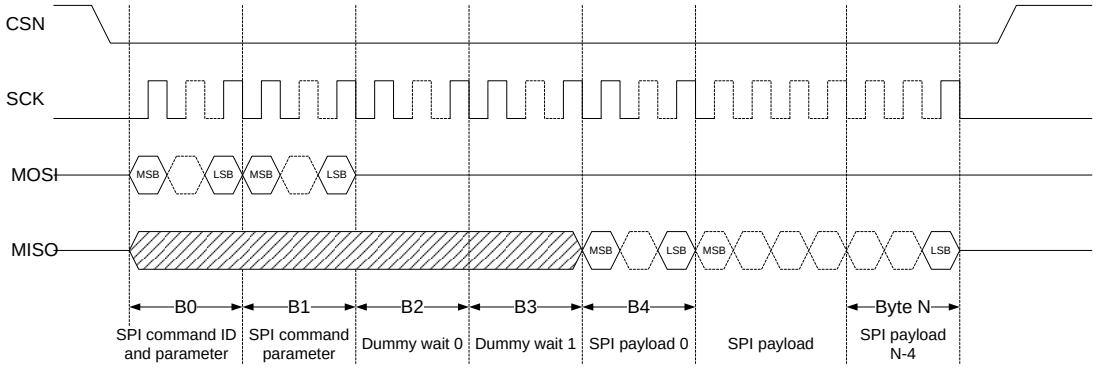


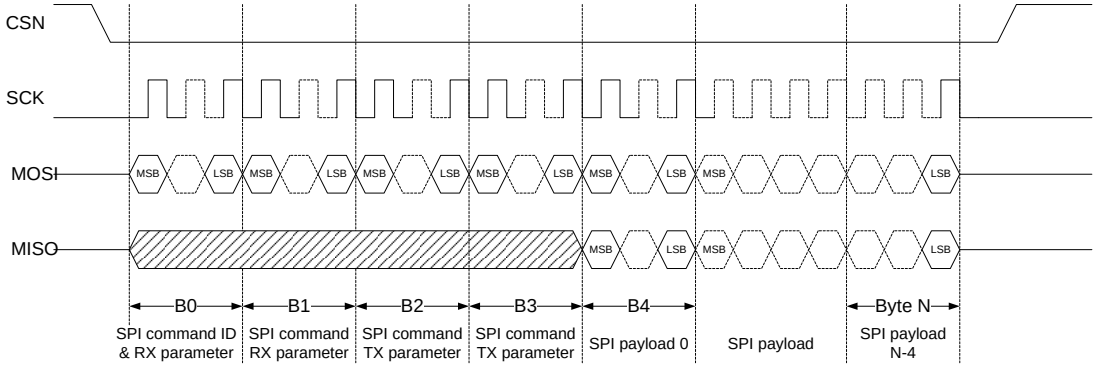
Figure 10 SPI read RX FIFO timing



6.1.7 Write TX FIFO and Read RX FIFO Command

The command ID of the command is 4'b0110. This command is used to write the TX FIFO and read the RX FIFO at the same time. The RX and TX length and payload are defined the same as the Write TX FIFO command and Read RX FIFO command.

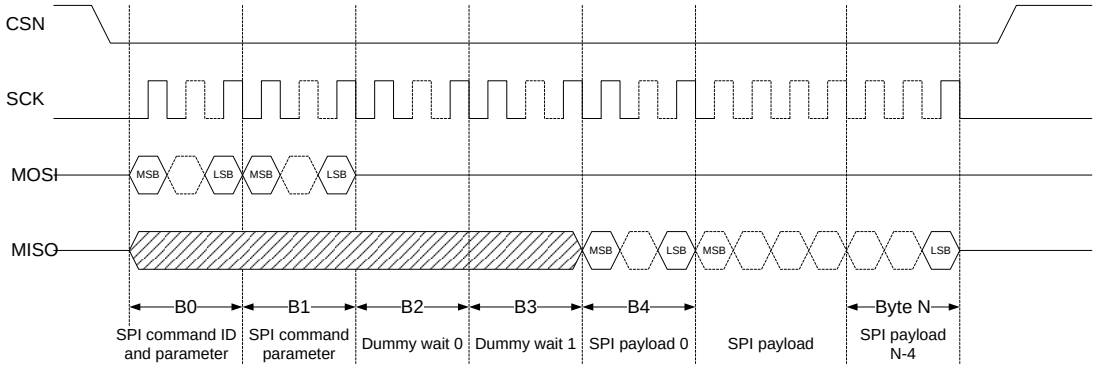
Figure 11 SPI write/read command timing



6.1.8 Read TX Status Command

The command ID of the read TX status command is 4'b0111. This command is used to read the TX status FIFO. The length of the command indicates the data number of the payload following in word (32 bit). The payload of the command is organized in word (32 bit). Each word is one TX status for one TX Ethernet packet. And the payload is little endian. Bit 24 of the word indicates whether current word is valid. And bit 23 to bit 0 of the word is the accrual TX status for the packet from the MAC. The TX status is described in the table below.

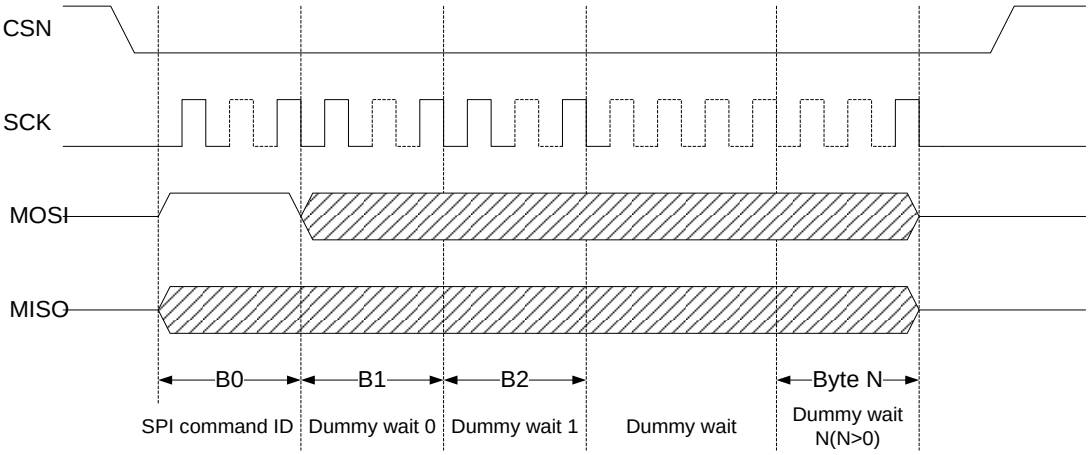
Figure 12 SPI read TX status timing



6.1.9 Reset Command

Any SPI transfer which the first byte is 8'hFF will be treated as SPI reset command. The SPI reset command is used to reset the whole chip.

Figure 13 SPI reset timing



6.2 MAC

Please refer to IEEE 802.3 protocol. All MAC related initialization and configuration are implemented in the device driver.

6.3 PHY

All PHY related initialization and configuration are implemented in device driver.

6.4 Interrupt

There is a dedicated pin on the chip to output the interrupt signal to communicate with the master chip. And there are three main interrupt sources: SPI controller, MAC and PHY. All the interrupts are high active and there is a group of registers which can be programmed to mask the

interrupts.

6.4.1 SPI Interrupt

Table 3 SPI interrupt

Name	Description
Rx_flen_fifo_th_intr	the frame number in the rx data fifo bigger than or equal to rx_flen_fifo_th
Rx_data_fifo_th_intr	the rx data fifo fill level bigger than or equal to rx_data_fifo_th
Rx_data_fifo_to_intr	the cycle number of continuous clock cycle that the rx data fifo is not empty and no read to the rx data fifo bigger than rx_data_fifo_to
Tx_data_fifo_th_intr	the tx data fifo empty level bigger than or equal to tx_data_fifo_th
Tx_stat_fifo_th_intr	the tx stat fifo fill level bigger than or equal to tx_stat_fifo_th
Spi_tx_len_l_intr	if the internal counter down count to 1'b0 and there are still un-transferred data in the spi module, then this intr will be triggered. It means that the transmit length in the first two byte of the spi transfer is less than the actual transmitted data by the spi host. this intr will not be triggerred in the spi RW command
Spi_tx_len_g_intr	if rising edge of the spi cs is encounterred and the the internal counter is not 0, then this intr will be triggered. It means that the transmit length in the first two byte of the spi transfer is bigger than the actual transmitted data by the spi host
Spi_rx_len_g_intr	if rising edge of the spi cs is encounterred and the the internal counter is not 0, then this intr will be triggered. It means that the transmit length in the first two byte of the spi transfer is bigger than the actual received data by the spi host
Spi_txf_ovr_intr	spi tx fifo over run
Spi_rxf_ndr_intr	spi rx fifo under run
Spi_tx_flen_crc_err_intr	tx frame length crc err
Spi_rx_flen_crc_err_intr	rx frame length crc err
Spi_stat_dead_intr	spi stat dead lock intr

6.4.2 MAC Interrupt

Please refer to the device driver

6.4.3 PHY Interrupt

Please refer to the device driver

6.5 Clock Output

There is a dedicated pin named CKO to output the muxed clock on the chip. The source of the muxed clock output can be: the system clock from the crystal input, the divided system clock, the TX clock of the Ethernet PHY and the RX clock of the Ethernet PHY. The divide parameter of the divided system clock is programmable and ranged from 2 to 512. Also the clock output pin can be programmed to be high-z.

6.6 LED Output

There are two dedicated pin named LED0 and LED1 to output the status of the Ethernet PHY. The source of the two LED output signal are the same and can be: PHY link done, PHY speed, PHY full duplex mode, PHY collision, PHY RX active, PHY TX active, PHY RX active and PHY TX active, PHY RX active or PHY TX active. And also the two LED output pin can be programmed to be high-z.

6.7 Data Transmit Flow

The host control flow of the Ethernet packet transmission is listed as below:

1. System initialization. Set the TX_DATA_FIFO_TH to some vale such as 512 which is the depth of the TX data FIFO. Set the internal TX empty level to 2048(512*4) byte.
2. If there is new data need to be transferred to the Ethernet and the data length is less than the internal TX empty level, then use write TX FIFO command or write/read FIFO command to transfer data to the SPI slave with the length of the new data. If there is new data need to be transferred to the Ethernet and the data length is bigger than the internal TX empty level, then use write TX FIFO command or write/read FIFO command to transfer data to the SPI slave with the length of the internal TX empty level. Then updates the internal TX empty level using the original empty level subscribes the transferred data length.
3. If the interrupt triggered, then read the interrupt status and also the FIFO status. Updates the internal TX empty level with the TX FIFO fill level read back. Then goes back to step 2.

6.8 Data Receive Flow

The host control flow of the Ethernet packet reception is listed as below:

1. System initialization. If the host uses RX_DATA_FIFO_TH_INTR to trigger the data reception transfer then the RX_DATA_FIFO_TH need to be set to some value such as 512 which is half of the RX data FIFO depth. Also the RX_DATA_FIFO_TO need to be set to some value to trigger the interrupt when some data is left in the RX data FIFO un-read for a long time which exceeds the limitation set by the host. If the host uses

RX_FLEN_FIFO_TH_INTR to trigger the data reception transfer then the RX_FLEN_FIFO_TH need to be set to some value such as 1 which means 1 Ethernet packet will trigger the interrupt.

2. If interrupt triggered, then read the interrupt status and also the FIFO status. If it is the RX_DATA_FIFO_TH_INTR or RX_DATA_FIFO_TO_INTR or RX_FLEN_FIFO_TO_INTR, then goes to step 3.
3. Use read RX FIFO command or write/read FIFO command to read the data back with the length read back in step 2. Then goes back to step 2.

7 REGISTER DESCRIPTION

The control registers in the chip are organized in three parts: the SPI control registers, the MAC control registers and the PHY control registers. All the configuration of the registers is implemented in the device driver.

8 ELECTRICAL CHARACTERISTICS

Table 4 Absolute ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage		-	-	5	V
Storage temperature		-40	-	150	℃
Digital input level	Functional pin	-0.3	-	3.6	V
Analog input level	Functional pin	-0.3	-	3.6	V

Table 5 AC characteristics

Parameter	Condition	Min	Typ	Max	Unit
Analog IO supply voltage	VCC33A	2.97	3.3	3.63	V
Analog core supply voltage	VCC12A	1.08	1.2	1.32	V
Digital IO supply voltage	VIO28	2.52	2.8	3.08	V
Digital core supply voltage	VCC12D	1.08	1.2	1.32	V
Operating temperature	Ambient temperature	-40	25	125	℃
Clock frequency		25-0.005%	25	25+0.005%	MHz
Clock duty cycle		40	50	60	%
Clock period jitter		-	-	120	ps
Clock cycle to cycle jitter		-	-	160	ps
Clock long term jitter		-	-	200	ps

Figure 14 SPI timing diagram

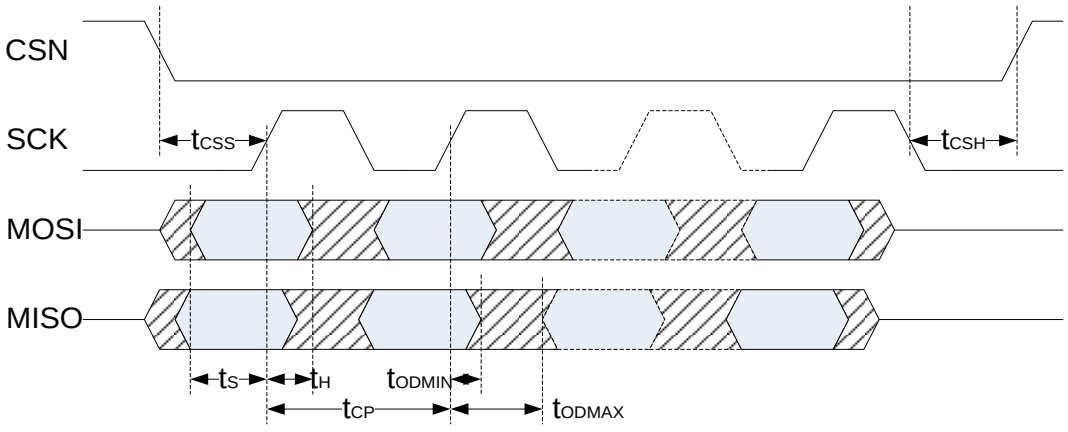


Table 6 SPI AC characteristics

Parameter	Condition	Min	Typ	Max	Unit
tCSS		1	-	-	tCP
tCSH		1	-	-	tCP
tCP		16	-	-	ns
tS		4	-	-	ns
tH		0	-	-	ns
tODMIN		3	-	-	ns
tODMAX		-	-	10	ns
Note: The reference clock edge of the tODMIN and tODMAX can be programmed to be the falling edge after the rising edge shown in the figure above.					

9 PACKAGING INFORMATION

Figure 1 Package view

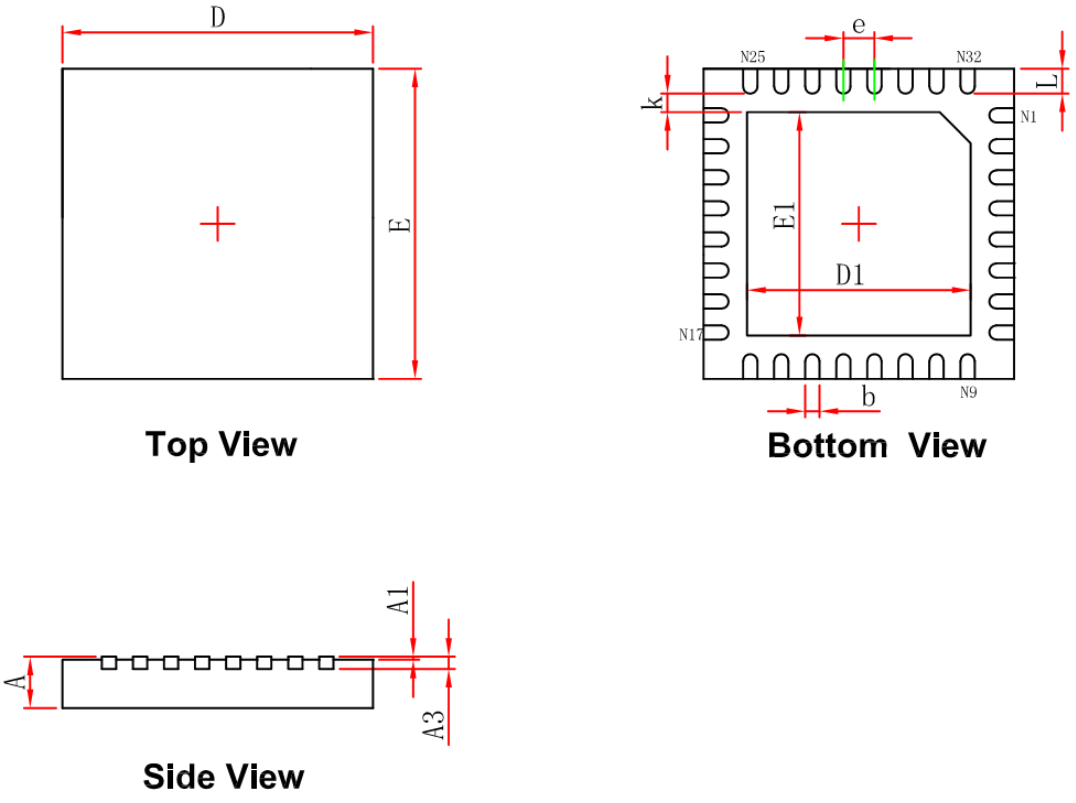


Table 1 Package size

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

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