# High efficiency, Low noise, Ultralow distortion, Constant large volume, Upgrade Seventh generation Class K Audio Amplifier

## FEATURES

- **Low noise：53μV**
- **Power amplifier overall efficiency 80%**
- **Ultra-low distortion：0.008%**
- **Speaker and Receiver two-in-one application**
  - **Receiver：1V/V，Vn=22uV，THD+N=0.025%**
  - **Receiver：3V/V，Vn=26uV，THD+N=0.025%**
- **Within Lithium battery voltage range, output power is maintained constant**
- **Selectable speaker-guard power level：0.6w，0.8W，1W，1.2W**
- No-crack-noise (NCN) technology
- Super TDD-Noise suppression
- Excellent pop-click suppression
- One wire pulse control
- High PSRR：-68dB（217Hz）
- ESD protection：±6kV (HBM)
- Small 0.4mm pitch 1.6mm×1.68mm CSP-14package

## APPLICATIONS

- **Smart phone**

## DESCRIPTION

AW87317 is designed to enhance smart mobile phone sound quality, which is a new high efficiency, low noise, ultra-low distortion, constant large volume, upgrading seventh generation class K audio amplifier. Using a new generation K-Chargepump technology, efficiency reaches 93%, power amplifier's overall efficiency is up to 80%, greatly prolong the mobile phone usage time. The AW87317 noise floor is as low as to 53μV, with 97dB high signal-to-noise-ratio(SNR). The ultra-low distortion 0.008% and unique no-crack-noise (NCN) technology brings high quality music enjoyment.

AW87317 has 0.6W, 0.8W, 1W and 1.2W four selectable speaker-guard output power levels, recommended using rated power of 0.5W and above speakers. AW87317 integrated unique NCN technology, the output power cannot drop along with lithium battery voltage lower down. Within lithium battery voltage range (3.3V--4.35V), output power is constant, preventing the voice becomes smaller and smaller during usage of cell phone.

AW87317 supports speaker and receiver two-in-one application. In receiver mode, the output noise is as low as to 22uV, amplifier is in class D mode, powered by VBAT.

AW87317 has built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. The AW87317 uses small 0.4mm pitch 1.6mmx1.68mm CSP-14 package.

## APPLICATION DIAGRAM

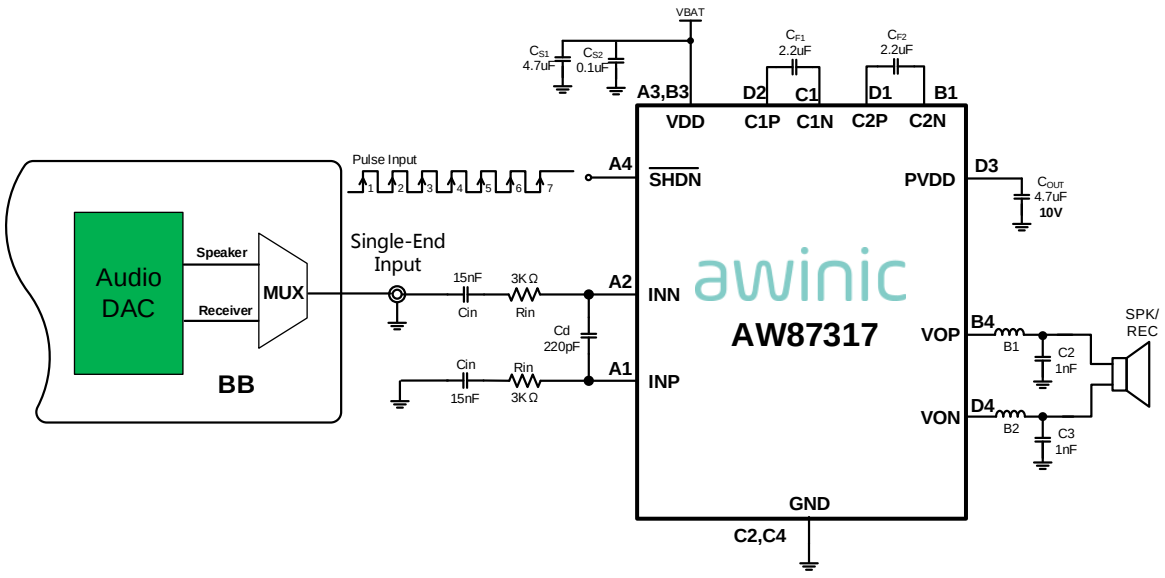


**Figure 1 AW87317 single-ended input application diagram**

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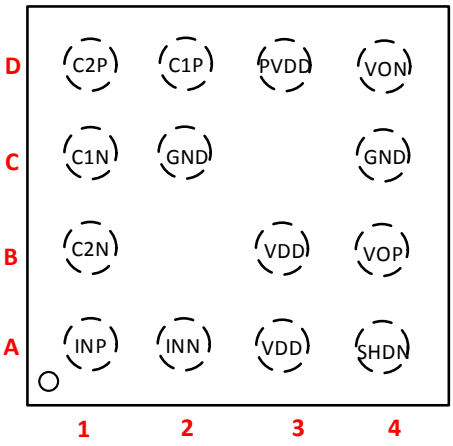
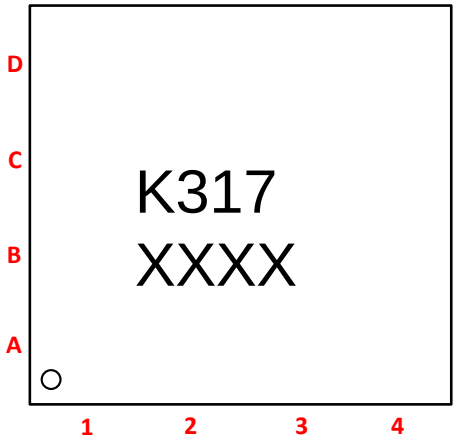
## PIN CONFIGURATION AND TOP MARK

AW87317CSR TOP VIEW




▲ Please notice the pin number

AW87317CSR MARKING




K317 – AW87317CSR
XXXX – Production tracking code

**Figure 2 AW87317 pin diagram top view and device marking**

## PIN DESCRIPTION

| Number | Symbol | Description |
|---|---|---|
| A1 | INP | Positive audio input terminal |
| A2 | INN | Negative audio input terminal |
| A3 | VDD | Power supply |
| A4 | SHDN | Chip power down pin，active low；one wire pulse control； |
| B1 | C2N | Negative side of the external charge pump flying capacitor C2 |
| B3 | VDD | Power supply |
| B4 | VOP | Positive audio output terminal |
| C1 | C1N | Negative side of the external charge pump flying capacitor C1 |
| C2，C4 | GND | Ground |
| D1 | C2P | Positive side of the external charge pump flying capacitor C2 |
| D2 | C1P | Positive side of the external charge pump flying capacitor C1 |
| D3 | PVDD | Boost charge pump output voltage |
| D4 | VON | Negative audio output terminal |

## AWINIC CLASS K FAMILY

| ITEM | TEST CONDITION | AW8736 | AW8737 | AW87317 | AW8738 |
|---|---|---|---|---|---|
| PVDD(V) | VDD=4.2V | 5.8 | 6.05 | 6.05 | 6.05 |
| Ouput noise(μV) | VDD=4.2V，f=20Hz to 20kHz，input ac grounded，8V/V,A-weighting | 125 | 52 | 53 | 40 |
| Efficiency(%) | $V_{DD}$=3.6V，Po=1.0W，$R_L$=8Ω+33μH | 75 | 80 | 80 | 83 |

## FUNCTIONAL DIAGRAM

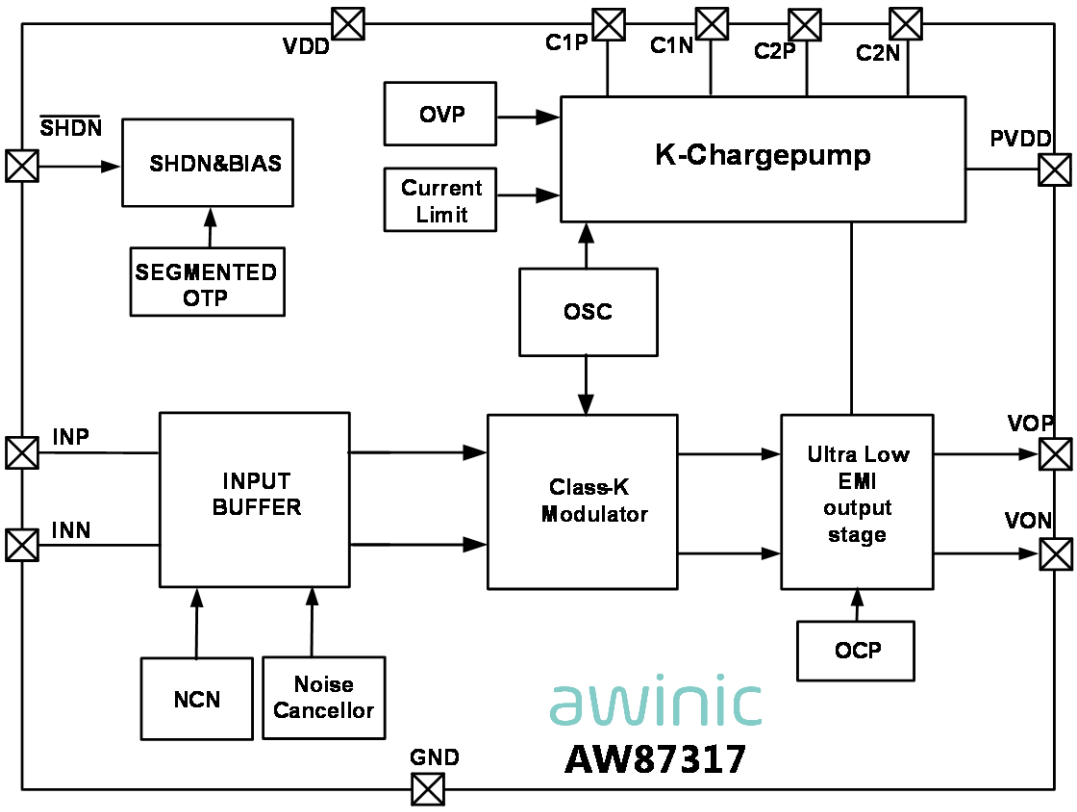



**Figure 3 AW87317 functional diagram**

## APPLICATION DIAGRAM

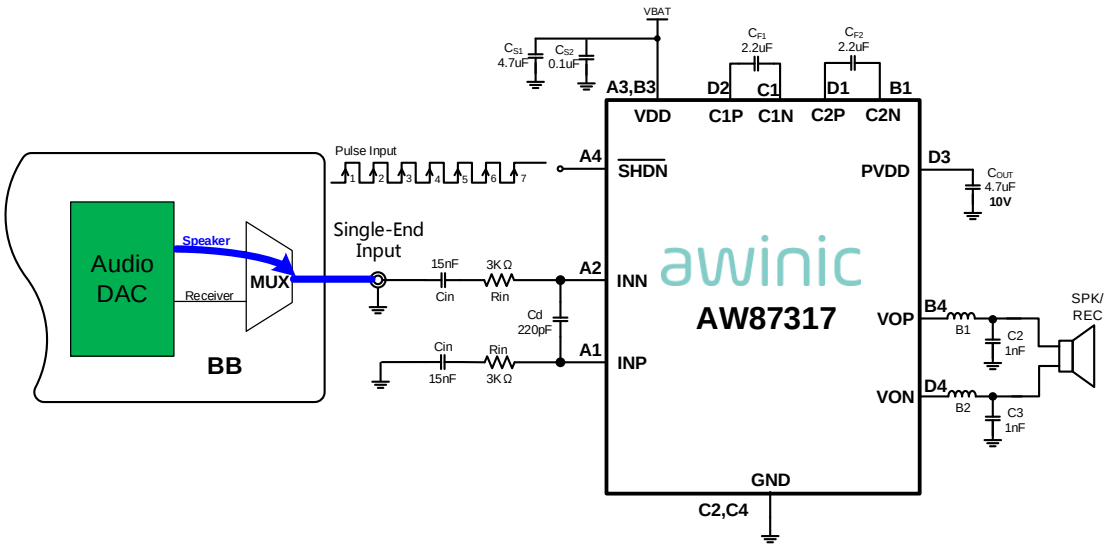



**Figure 4 AW87317 speaker mode application diagram (Note 1)**

***Note1：*** *when single-ended input，input audio signal can arbitrarily connect to one of INN，INP input terminal，the other terminal connects to ground through input capacitor and resistance.*

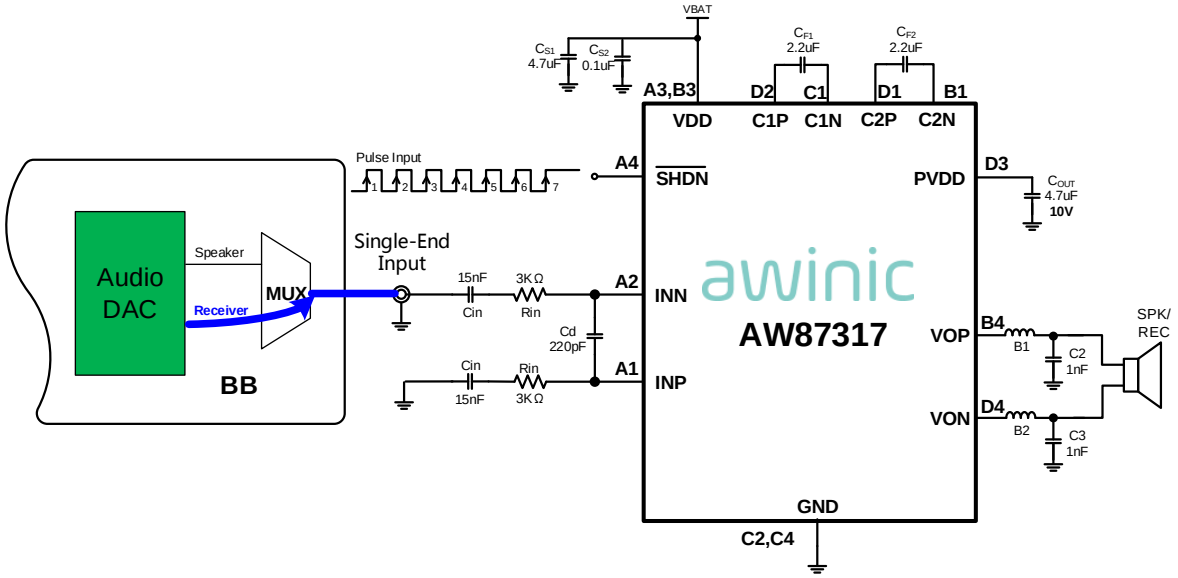
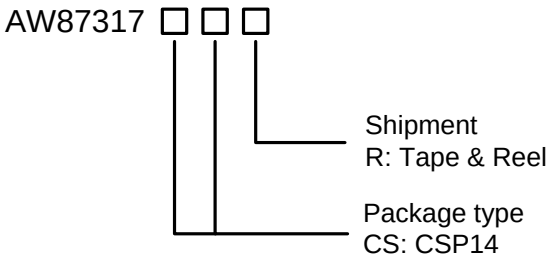



**Figure 5 AW87317 receiver mode application diagram**

## ORDERING INFORMATION

| Product Type | Operation temperature range | Package | Device Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AW87317CSR | -40℃～85℃ | CSP-14 | K317 | MSL1 | ROHS+HF | Tape and Reel 3000 pcs |




## ABSOLUTE MAXIMUM RATING(Note2)

| Parameter | Range |
|---|---|
| Supply Voltage VDD | -0.3V to 6V |
| Chargepump output voltage PVDD | -0.3V to 7V |
| VOP,VON | -0.3V to PVDD+0.3V |
| C1P ,C2P | -0.3V to PVDD+0.3V |
| C1N,C2N | -0.3V to VDD+0.3V |
| INP，INN Input Pin Voltage | -0.3V to VDD +0.3V |
| Package Thermal Resistance $\theta_{JA}$ | 84.9℃/W |

| | |
|---|---|
| Ambient Temperature Range | -40℃ to 85℃ |
| Maximum Junction Temperature $T_{JMAX}$ | 165℃ |
| Storage Temperature Range $T_{STG}$ | -65℃ to 150℃ |
| Lead Temperature（Soldering 10 Seconds） | 260℃ |
| ESD Rating（Note 3） | |
| HBM（human body model） | ±6KV |
| CDM | ±1.5KV |
| MM | ±250V |
| Latch-up | |
| Test Condition：JEDEC STANDARD NO.78D NOVEMBER 2011 | +IT：450mA<br>-IT：-450mA |

***Note 2：*** *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

***Note 3：*** *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883H Method 3015.8*

## MODE DESCRIPTION（TA=25℃,VDD=4.2V）

AW87317 audio amplifier outer input capacitor is Cin，outer input resist is Rin，inner input resist is 16.6KΩ，gain Av is 319.5K/(Rin+16.6K). Recommended typical application is：

1、 Cin=15nF，Rin=3KΩ，Av=16.3V/V；

2、 Cin=15nF，Rin=10KΩ，Av=12V/V；

| Mode | Enable Signal | Gain（V/V） | | NCN Power（W） | | NCN Function | Receiver Mode |
|---|---|---|---|---|---|---|---|
| | | Rin=3KΩ | Rin=10KΩ | RL=8Ω+ 33μH | RL=6Ω+ 33μH | | |
| Mode1 | | 16.3 | 12 | 1.2 | 1.6 | √ | |
| Mode2 | | 16.3 | 12 | 1 | 1.3 | √ | |
| Mode3 | | 16.3 | 12 | 0.8 | 1.0 | √ | |
| Mode4 | | 16.3 | 12 | 0.6 | 0.8 | √ | |
| Mode5 | | 1 | 1 | | | | √ |
| Mode6 | | 3 | 3 | | | | √ |
| Mode7 | | 16.3 | 12 | 1.75W@ THD=1% | 2.05W@ THD=1% | | |

# ELECTRICAL CHARACTERISTICS

Test condition：$T_A$=25℃，VDD=3.6V，RL=8Ω+33μH，f=1kHz（unless otherwise noted）

| Parameter | | Test conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 3.0 | | 5.5 | V |
| $V_{IH}$ | $\overline{SHDN}$ high input voltage | | 1.3 | | $V_{DD}$ | V |
| $V_{IL}$ | $\overline{SHDN}$ low input voltage | | 0 | | 0.35 | V |
| $\|V_{OS}\|$ | Output offset voltage | Vin=0V, $V_{DD}$=3.0V to 5.5V | -30 | 0 | 30 | mV |
| $I_{SD}$ | Shutdown current | $V_{DD}$=3.6V, $\overline{SHDN}$=0V | | | 1 | μA |
| $T_{TG}$ | Thermal AGC start temperature threshold | | | 150 | | ℃ |
| $T_{TGR}$ | Thermal AGC exit temperature threshold | | | 130 | | ℃ |
| $T_{SD}$ | Over temperature protection threshold | | | 160 | | ℃ |
| $T_{SDR}$ | Over temperature protection recovery threshold | | | 120 | | ℃ |
| $T_{ON}$ | Start-up time | | | 40 | | ms |
| **K-Chargepump** | | | | | | |
| PVDD | Output voltage | $V_{DD}$ =3.0V to 4V | | 1.5* VDD | | V |
| | | $V_{DD}$ >4V | | 6.05 | | V |
| Vhys | OVP hysteresis | $V_{DD}$ >4V | | 50 | | mV |
| $F_{CP}$ | Charge Pump frequency | $V_{DD}$=3.0V to 5.5V | 0.8 | 1.06 | 1.33 | MHz |
| $\eta_{CP}$ | Charge pump efficiency | $V_{DD}$=3.6V, $I_{load}$=200mA | | 93 | | % |
| $T_{ST}$ | Soft-start time | No load，COUT=4.7μF | 1 | 1.2 | 1.4 | ms |
| $I_L$ | Current limit when PVDD short to ground | | 200 | 300 | 400 | mA |
| **Class K power amplifier（Mode1-Mode4，Mode7）** | | | | | | |
| $I_q$ | Quiescent current | $V_{DD}$=4.2V，Vin=0，no load | | 10 | 15 | mA |
| η | Efficiency | $V_{DD}$=3.6V, Po=1.0W, $R_L$=8Ω+33μH | | 80 | | % |
| Fosc | Modulation frequency | $V_{DD}$=3.0V to 5.5V | 600 | 800 | 1000 | kHz |
| Av | gain | external input resistance=3kΩ | | 16.3 | | V/V |
| Vin | Recommend input voltage | $V_{DD}$=3.0V to 5.5V | | | 1 | Vp |
| Rini | Inner input resistance | Mode1~Mode4，Mode7 | | 16.6 | | kΩ |
| Fhin | Input high pass filter corner frequency | Cin=15nF，external input resistance=3kΩ | | 542 | | Hz |
| Pncn | Mode1 NCN output power | $V_{DD}$=4.2V, $R_L$=8Ω+33μH | 1.08 | 1.2 | 1.32 | W |
| | | $V_{DD}$=4.2V, $R_L$=6Ω+33μH | 1.44 | 1.6 | 1.76 | W |
| | | $V_{DD}$=4.2V, $R_L$=4Ω+15μH | 2.16 | 2.4 | 2.64 | W |
| | | $V_{DD}$=4.2V, $R_L$=3Ω+15μH | 2.16 | 2.4 | 2.64 | W |
| | Mode2 NCN output power | $V_{DD}$=4.2V, $R_L$=8Ω+33μH | 0.9 | 1 | 1.1 | W |
| | | $V_{DD}$=4.2V, $R_L$=6Ω+33μH | 1.17 | 1.3 | 1.43 | W |
| | | $V_{DD}$=4.2V, $R_L$=4Ω+15μH | 1.8 | 2 | 2.2 | W |

| Parameter | | Test conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$=4.2V, $R_L$=3Ω+15μH | | 2.16 | 2.4 | 2.64 | W |
| Pncn | Mode3 NCN output power | $V_{DD}$=4.2V, $R_L$=8Ω+33μH | | 0.72 | 0.8 | 0.88 | W |
| | | $V_{DD}$=4.2V, $R_L$=6Ω+33μH | | 0.9 | 1.0 | 1.1 | W |
| | | $V_{DD}$=4.2V, $R_L$=4Ω+15μH | | 1.44 | 1.6 | 1.76 | W |
| | | $V_{DD}$=4.2V, $R_L$=3Ω+15μH | | 1.8 | 2.0 | 2.2 | W |
| | Mode4 NCN output power | $V_{DD}$=4.2V, $R_L$=8Ω+33μH | | 0.54 | 0.6 | 0.66 | W |
| | | $V_{DD}$=4.2V, $R_L$=6Ω+33μH | | 0.72 | 0.8 | 0.88 | W |
| | | $V_{DD}$=4.2V, $R_L$=4Ω+15μH | | 1.08 | 1.2 | 1.32 | W |
| | | $V_{DD}$=4.2V, $R_L$=3Ω+15μH | | 1.44 | 1.6 | 1.76 | W |
| PSRR | Power supply rejection ratio | $V_{DD}$=4.2V, Vp-p_sin=200mV | 217Hz | | -68 | | dB |
| | | $V_{DD}$=4.2V, Vp-p_sin=200mV | 1kHz | | -68 | | dB |
| SNR | Signal-to-noise ratio | $V_{DD}$=4.2V, Po=1.75W, THD+N=1%, $R_L$=8Ω+33μH，Av=8V/V | | | 97 | | dB |
| Vn | Output noise voltage | VDD=4.2V, f=20Hz to 20kHz, input ac grounded，AV=8V/V | A-weighting | | 53 | | μVrms |
| | | VDD=4.2V, f=20Hz to 20kHz, input ac grounded, 12V/V | | | 58 | | μVrms |
| | | VDD=4.2V, f=20Hz to 20kHz, input ac grounded, 16V/V | | | 68 | | μVrms |
| THD+N | Total harmonic distortion+noise | $V_{DD}$=3.6V,Po=1W,$R_L$=8Ω+33μH,f=1kHz, Mode1 | | | 0.008 | | % |
| | | $V_{DD}$=3.6V,Po=1W,$R_L$=6Ω+33μH,f=1kHz,Mode7 | | | 0.008 | | % |
| $P_O$ | Mode7 output power | THD+N=10%, f=1kHz, $R_L$=8Ω+33μH, $V_{DD}$=4.2V | | | 2.15 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=8Ω+33μH, $V_{DD}$=4.2V | | | 1.75 | | W |
| | | THD+N=10%, f=1kHz, $R_L$=8Ω+33μH, $V_{DD}$=3.6V | | | 1.6 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=8Ω+33μH, $V_{DD}$=3.6V | | | 1.28 | | W |
| | | THD+N=10%, f=1kHz, $R_L$=6Ω+33μH, $V_{DD}$=4.2V | | | 2.52 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=6Ω+33μH, $V_{DD}$=4.2V | | | 2.05 | | W |
| | | THD+N=10%, f=1kHz, $R_L$=6Ω+33μH, $V_{DD}$=3.6V | | | 1.82 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=6Ω+33μH, $V_{DD}$=3.6V | | | 1.5 | | W |
| | | THD+N=10%, f=1kHz, $R_L$=4Ω+15μH, $V_{DD}$=4.2V | | | 2.8 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=4Ω+15μH, $V_{DD}$=4.2V | | | 2.4 | | W |
| | | THD+N=10%, f=1kHz，$R_L$=4Ω+15μH, $V_{DD}$=3.6V | | | 2.02 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=4Ω+15μH, $V_{DD}$=3.6V | | | 1.68 | | W |
| | | THD+N=10%, f=1kHz, $R_L$=3Ω+15μH, $V_{DD}$=4.2V | | | 2.63 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=3Ω+15μH, $V_{DD}$=4.2V | | | 2.35 | | W |
| | | THD+N=10%, f=1kHz，$R_L$=3Ω+15μH, $V_{DD}$=3.6V | | | 1.85 | | W |
| | | THD+N=1%, f=1kHz, $R_L$=3Ω+15μH, $V_{DD}$=3.6V | | | 1.65 | | W |
| **Receiver (Mode5-Mode6)** | | | | | | | |
| $I_q$ | Quiescent current | $V_{DD}$=4.2V，Vin=0，no load | | | 5 | 7.5 | mA |
| η | Efficiency | $V_{DD}$=3.6V, Po=0.8W, $R_L$=8Ω+33μH，Mode6 | | | 86 | | % |
| Fosc | Modulation frequency | $V_{DD}$=3.0V to 5.5V | | 600 | 800 | 1000 | kHz |

| Parameter | | Test conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Av | gain | external input resistance=3kΩ，Mode5 | | | 1 | | V/V |
| | | external input resistance=3kΩ，Mode6 | | | 3 | | V/V |
| Rini | Inner input resistance | Mode5 | | | 186.6 | | kΩ |
| | | Mode6 | | | 56.6 | | kΩ |
| Fhin | Input high pass filter corner frequency | Cin=15nF, external input resistance=3kΩ,Mode5 | | | 56 | | Hz |
| | | Cin=15nF, external input resistance=3kΩ,Mode6 | | | 178 | | Hz |
| Vn | Output noise voltage | VDD=4.2V，f=20Hz to 20kHz，input ac grounded，Av=1V/V | A-weighting | | 22 | | μVrms |
| | | VDD=4.2V，f=20Hz to 20kHz，input ac grounded，Av=3V/V | | | 25 | | μVrms |
| THD+N | Total harmonic distortion+noise | $V_{DD}$=4.2V,Po=0.1W,$R_L$=8Ω+33μH,f=1kHz，Mode5 | | | 0.025 | | % |
| | | $V_{DD}$=4.2V,Po=0.4W,$R_L$=8Ω+33μH,f=1kHz，Mode6 | | | 0.025 | | % |
| **One wire pulse control** | | | | | | | |
| $T_H$ | $\overline{SHDN}$ high level duration time | $V_{DD}$=3.0V to 5.5V | | 0.75 | 2 | 10 | μs |
| $T_L$ | $\overline{SHDN}$ low level duration time | $V_{DD}$=3.0V to 5.5V | | 0.75 | 2 | 10 | μs |
| $T_{LATCH}$ | $\overline{SHDN}$ turn on delay time | $V_{DD}$=3.0V to 5.5V | | 150 | | 500 | μs |
| $T_{OFF}$ | $\overline{SHDN}$ turn off delay time | $V_{DD}$=3.0V to 5.5V | | 150 | | 500 | μs |
| **NCN** (Note 4) | | | | | | | |
| $T_{AT}$ | Attack time | -13.5dB gain attenuation completed | | | 40 | | ms |
| $T_{RL}$ | Release time | 13.5dB gain release completed | | | 1.2 | | s |
| $A_{MAX}$ | Maximum attenuation | | | | -13.5 | | dB |

***Note 4：****Attack time points to 13.5dB gain attenuation time；Release time points to 13.5dB gain recovery time.*

# MEASUREMENT SETUP

AW87317 features switching digital output, as shown in Figure 6. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

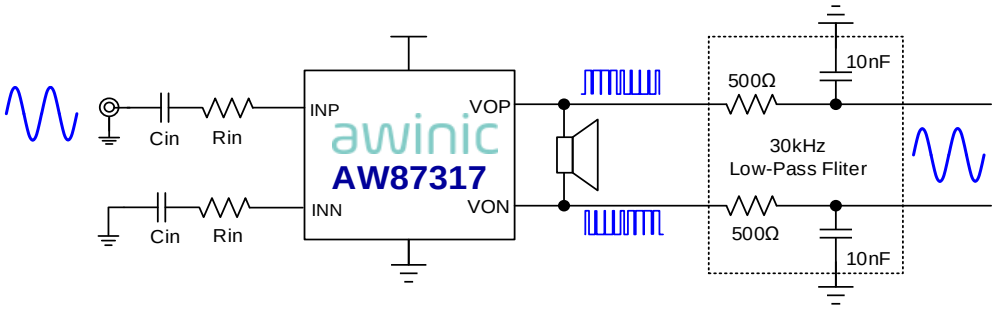



**Figure 6 AW87317 test setup**

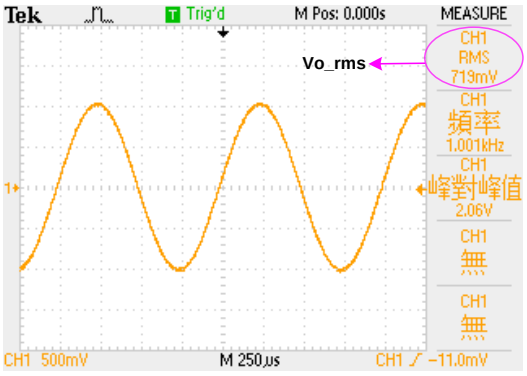
Low pass filter uses resistance and capacitor values listed in Table 1.

| $R_{filter}$ | $C_{filter}$ | Low-pass cutoff frequency |
|---|---|---|
| 500Ω | 10nF | 32kHz |
| 1kΩ | 4.7nF | 34kHz |

**Table 1 AW87317 recommended values for low pass filter**

### Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal as shown below:

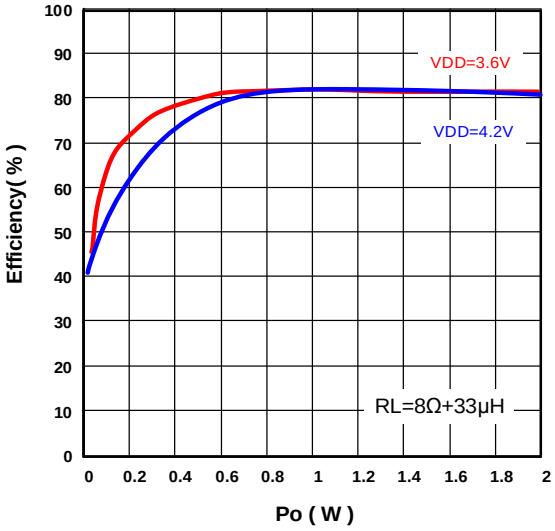



The power calculation of Speaker is as follows：

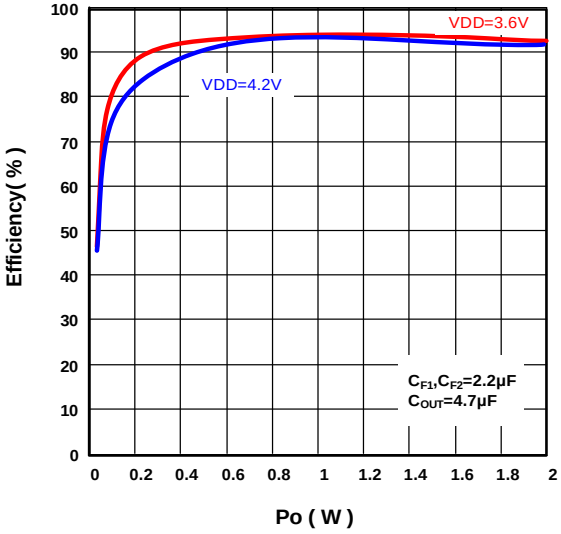
$$P_L = \frac{(Vo\_rms)^2}{R_L}$$ （$R_L$：load impedance of the speaker）

# TYPICAL CHARACTERISTICS

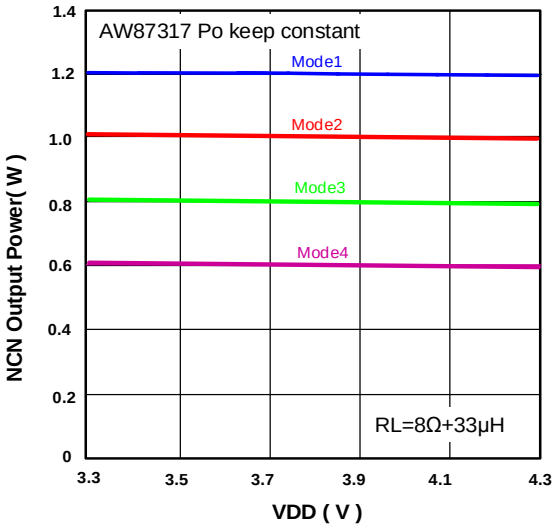
Efficiency vs Po



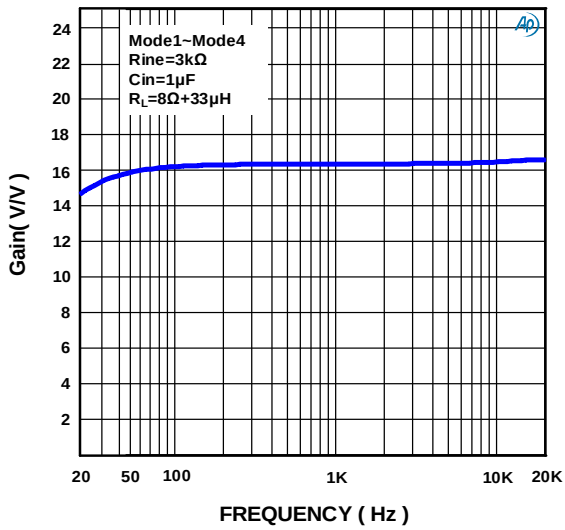

K-chargepump Efficiency



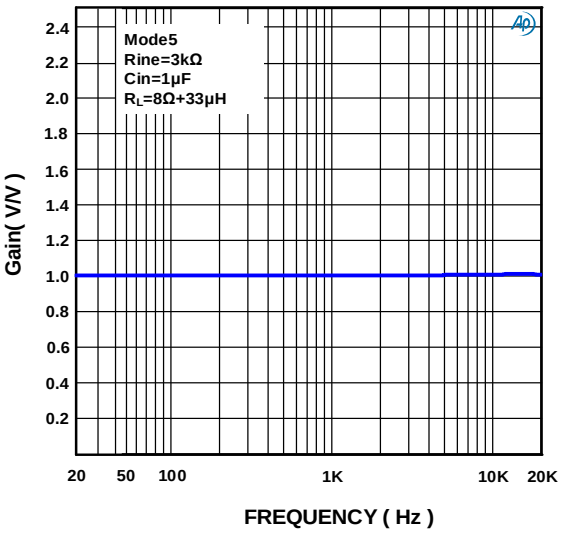

OUTPUT POWER vs VDD



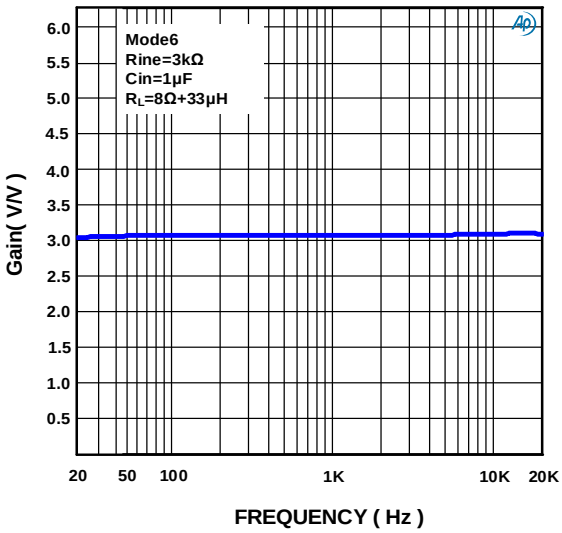

GAIN vs FREQUENCY



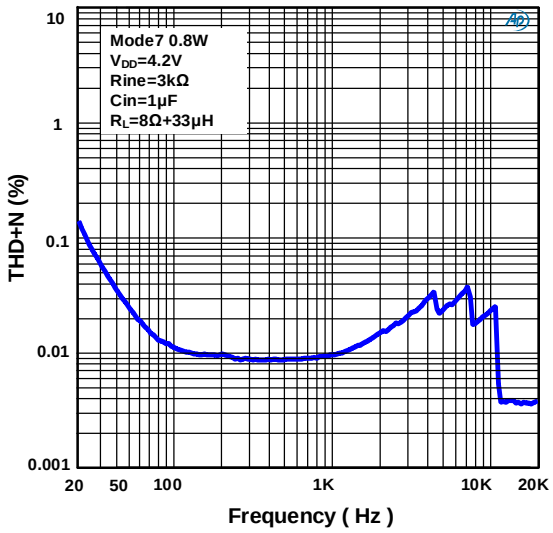

GAIN vs FREQUENCY



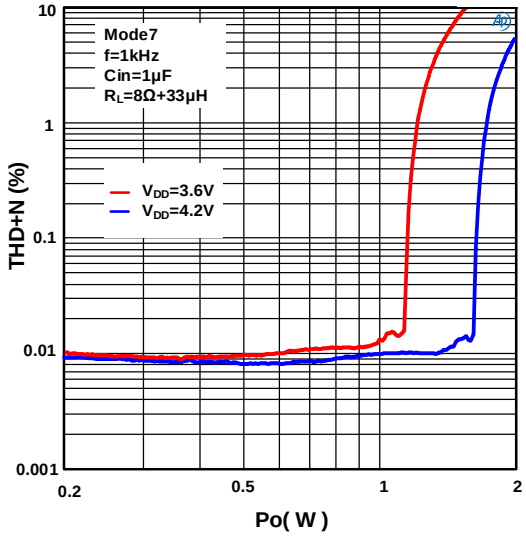

GAIN vs FREQUENCY



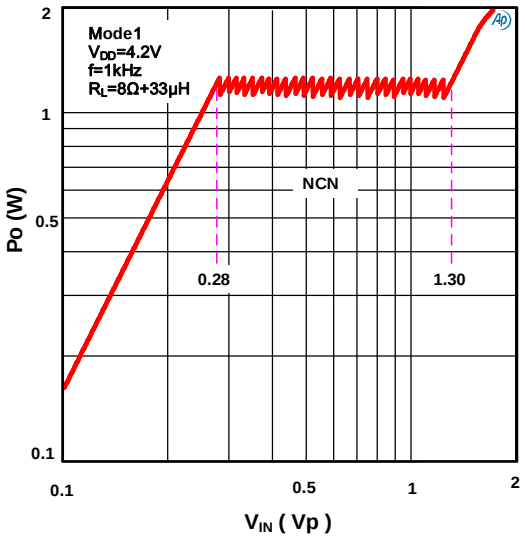
THD+N vs FREQUENCY



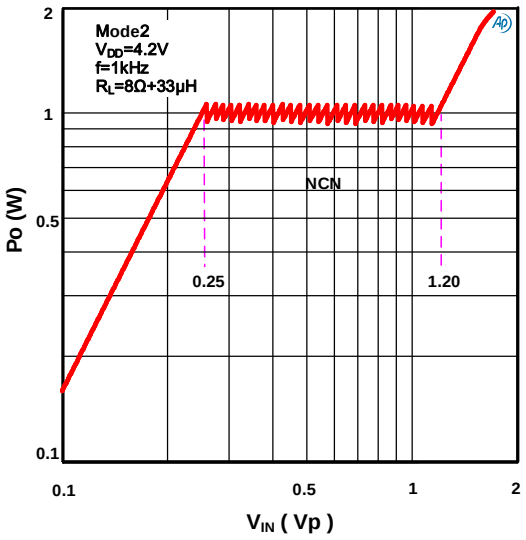

THD+N vs Po



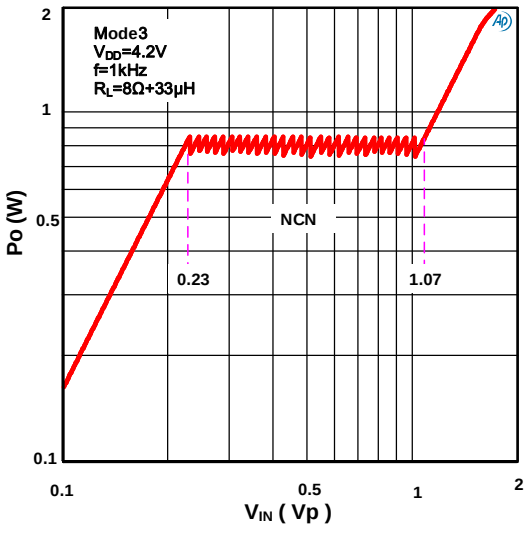

Po vs $V_{IN}$



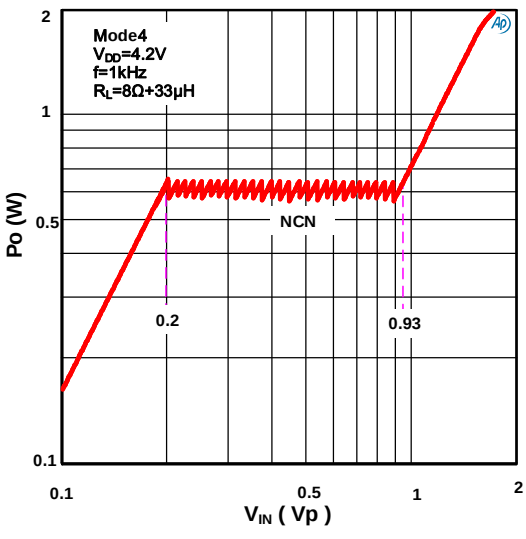

Po vs $V_{IN}$



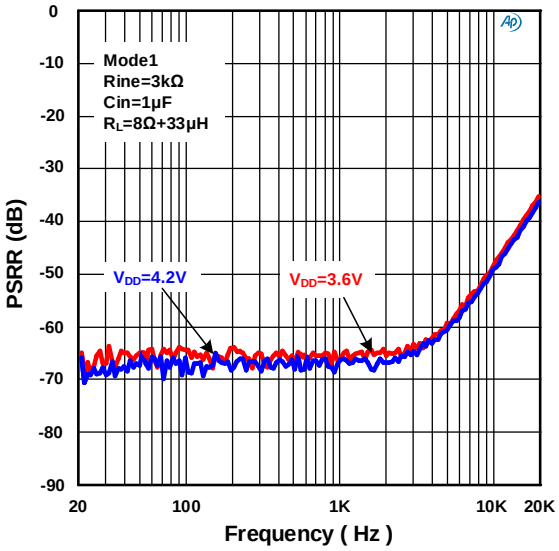

Po vs $V_{IN}$



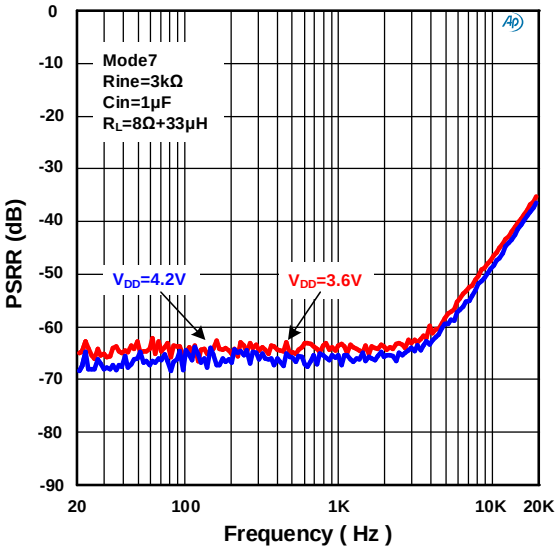

Po vs $V_{IN}$



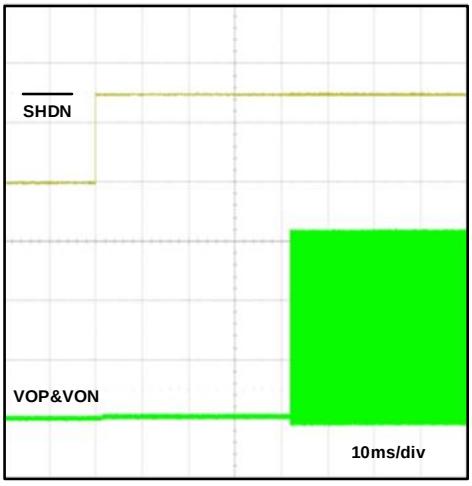
PSRR vs FREQUENCY



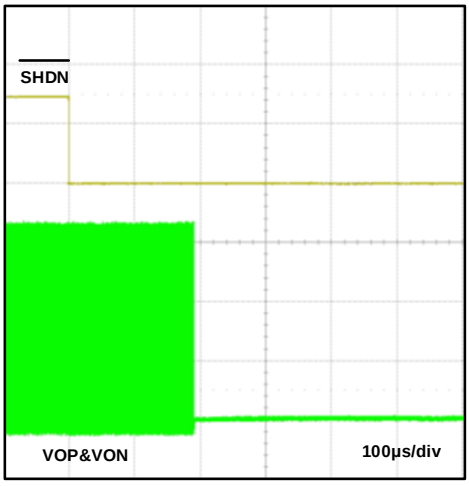

PSRR vs FREQUENCY



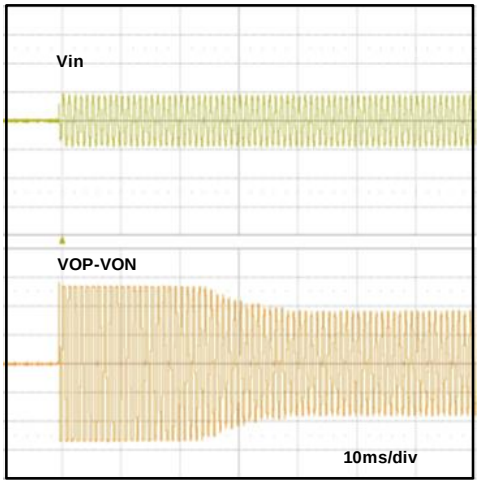

STARTUP SEQUENCE



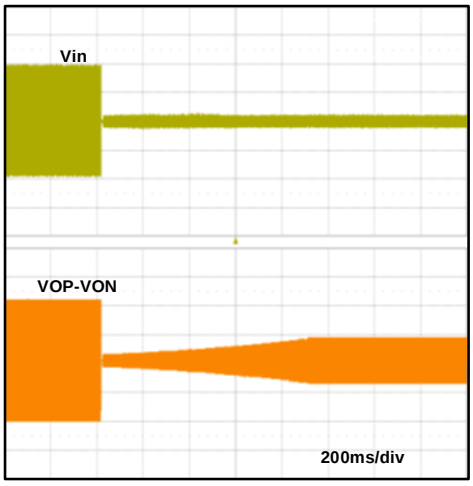

SHUTDOWN SEQUENCE




NCN ATTACK SEQUENCE




NCN RELEASE SEQUENCE



# DETAILED FUNCTIONAL DESCRIPTION

AW87317 is designed to enhance smart mobile phone sound quality, which is a new high efficiency, low noise, ultra-low distortion, constant large volume, upgrading seventh generation class K audio amplifier. Using a new generation K-Chargepump technology, efficiency reaches 93%, power amplifier's overall efficiency is up to 80%, greatly prolong the mobile phone usage time. The AW87317 noise floor is as low as to 53μV, with 97dB high signal-to-noise-ratio(SNR). The ultra-low distortion 0.008% and unique no-crack-noise (NCN) technology brings high quality music enjoyment.

AW87317 has 0.6W, 0.8W, 1W and 1.2W four selectable speaker-guard output power levels, recommended using rated power of 0.5W and above speakers. AW87317 integrated unique NCN technology, the output power cannot drop along with lithium battery voltage lower down. Within lithium battery voltage range (3.3V--4.35V), output power is constant, preventing the voice becomes smaller and smaller during usage of cell phone.

AW87317 supports speaker and receiver two-in-one application. In receiver mode, the output noise is as low as to 22uV, amplifier is in class D mode, powered by VBAT.

The AW87317 built in excellent pop-click noise suppression circuit, effectively avoids pop-click noise during shutdown, wakeup, and power-up/down operation of AW87317.

The AW87317 uses awinic proprietary TDD-Noise suppression technology and EMI suppression technology, effectively restrain TDD-Noise and EMI interference.

AW87317 has built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. The AW87317 uses small 0.4mm pitch 1.6mmx1.68mm CSP-14 package. The AW87317 is specified over the industrial temperature range of -40℃ to 85℃.

## CONSTANT OUTPUT POWER

In the mobile phone audio applications, the NCN function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually, leads to smaller and smaller music volume. So, it is hard to provide high quality music within the battery voltage range. The AW87317 uses unique second generation NCN technology, within lithium battery voltage range(3.3V--4.35V), output power is constant, the output power cannot drop along with lithium battery voltage lower down. Even if the battery voltage drops, AW87317 can still provide high quality large volume music enjoyment. AW87317 has seven operation modes, first four modes have NCN function, the output power level is 1.2W,1W,0.8W,0.6W, respectively.

## Second Generation NCN technology

In audio application, output signal will be undesirable distortion caused by too large input and power supply voltage down with battery, and clipped output signal may cause permanent damage to the speaker. The traditional NCN function adjusts system gain automatically to generate desired output by detecting the "Crack" distortion of output signal, makes the output audio signal maintain smooth, not only can effectively avoid overloading output power to the damage of speaker, at the same time bring the constant shock of high quality music enjoyment. The traditional NCN function is shown below in figure 7.

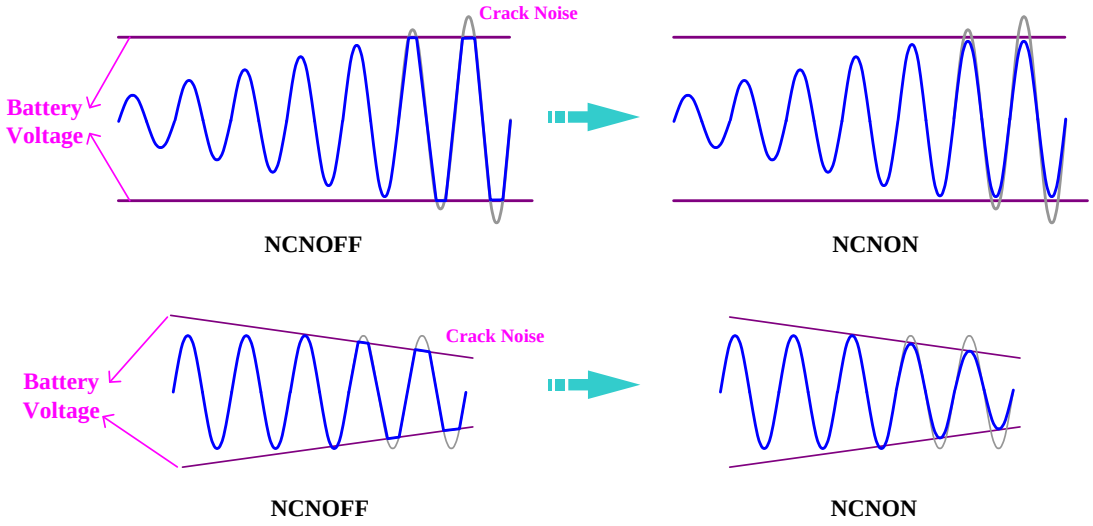



**Figure 7 Traditional NCN Operation Principle**

AW87317 adopts Awinic unique second generation NCN technology, the output signal is free from limitation of power rail. When battery voltage drops, NCN output signal will not distort, output amplitude remains unchanged, keeping constant output power, as shown in figure 8. Even if the battery voltage drops, AW87317 can still provide high quality large volume music enjoyment.

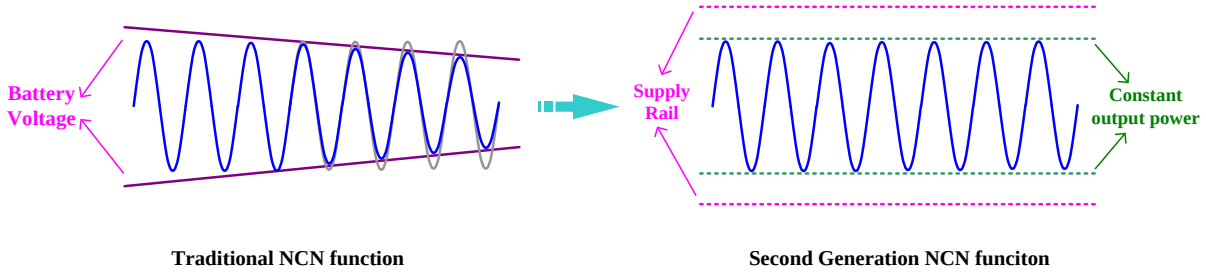



**Figure 8 Second generation NCN Operation Principle**

***Attack time***

Attack time is the time it takes for the gain to be attenuated -13.5dB once the audio signal exceeds the NCN threshold. Fast attack times allow the NCN to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the NCN cycles quickly. Slower attack times cause the NCN to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function. According to mobile phone and portable equipment audio features, attack time of AW87317 is set to be 40ms, effectively keeping the music rhythm, and at the same time eliminating the crack distortion, protecting the speaker.

***Release time***

Release time is the time it takes for the gain to return to its normal level once the audio signal returns below the NCN threshold. A fast release time allows the NCN to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time makes the music smooth and soft, it is better to suppress the crack distortion, but longer release time will make music sounds “boring” ,lack of impact.

According to mobile phone and portable equipment audio features, release time of AW87317 is set to be 1.2s.

## K-Chargepump

AW87317 adopts a new generation of charge pump technology：K -Chargepump structure, it has high efficiency and large driving ability, working frequency is 1.1MHz，built in soft start circuit, current limiting control loop and over-voltage-protection(OVP) loop, guaranteeing system stable and reliable operation.

***High Efficiency***

AW87317 uses K-chargepump structure，booster output voltage PVDD is 1.5 times of supply voltage VDD, the ideal efficiency can reach 100%. K-chargepump efficiency is the ratio of output power to input power, that is

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\%$$

For example, in an ideal M times chargepump, the input current $I_{IN}$ is M times of output current $I_{OUT}$，the efficiency formula can be written as：

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\% = \frac{V_{OUT} * I_{OUT}}{V_{IN} * M * I_{OUT}} * 100\% = \frac{V_{OUT}}{M * V_{IN}} * 100\%$$

M is charge pump work mode variable (1.5 times), VOUT is charge pump output voltage, VIN is power supply voltage, IOUT is load current. For K-chargepump, the output voltage is 1.5 times of the input voltage, due to the charge pump internal switch loss and IC static current loss, the actual efficiency will be up to 93%. Therefore, K-chargepump booster technology can greatly improve the power efficiency.

***Charge Pump Structure***

Figure 9 is charge pump basic principle diagram, the charge pump used in AW87317 has seven switches, the output voltage PVDD is 1.5 times as input voltage VDD through seven switches timing control.

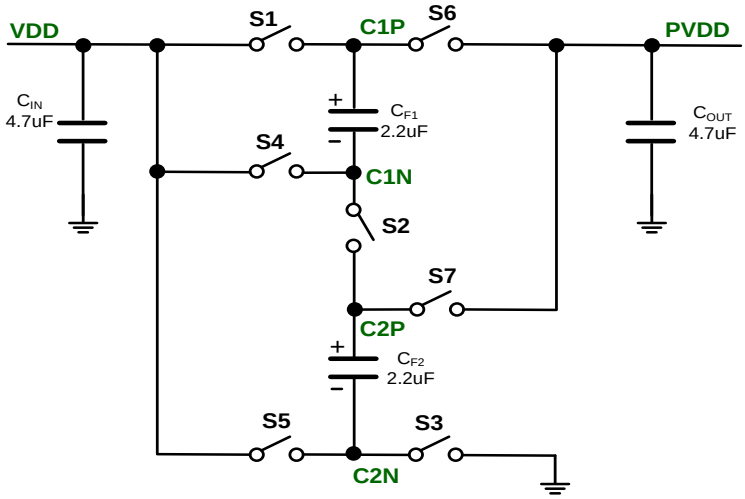



**Figure 9 Charge Pump Principle Diagram**

The operation of the charge pump has two phases. In Φ 1, as shown in figure 10, switches S1, S2 and S3 are closed, VDD charges to the flying capacitor CF1 CF2.

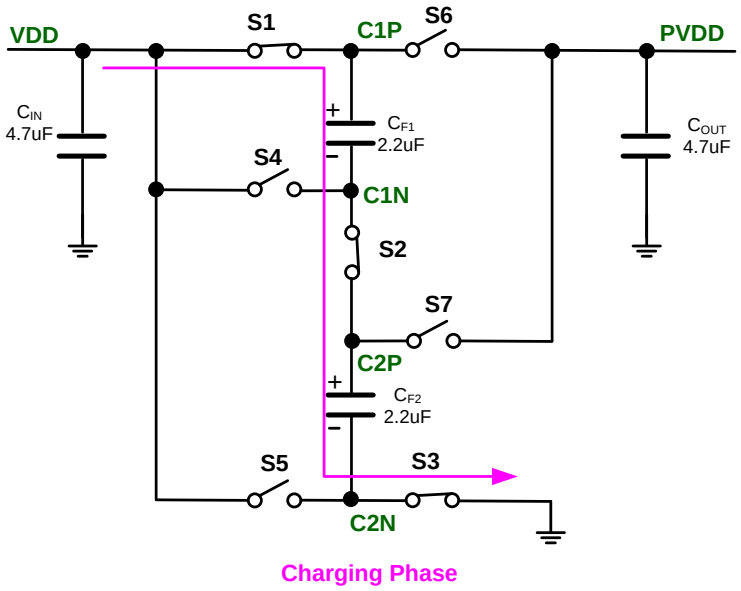



**Figure 10 Φ1: Flying Capacitor Charging**

In Φ 2, as shown in figure 11: switches S1, S2 and S3 are disconnected, switches S4, S5, S6 and S7 are closed. Because the voltage across the capacitor can't mutation, so the voltage on flying capacitor CF1 CF2, is added to the VDD, which make PVDD risen to a higher voltage.

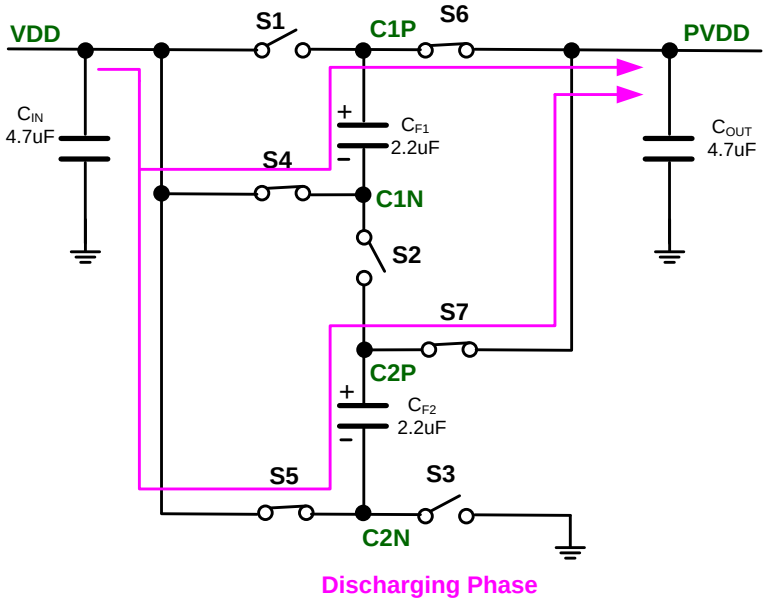



**Figure 11 Φ2: Flying capacitor charge transfer to the output capacitance $C_{OUT}$**

### *Soft start*

K-chargepump has integrated soft start function in order to limit supply power inrush current during start-up. The supply current is limited to be 350 mA, and the soft start time is 1.2 ms.

### *Current Limitation Control*

K-chargepump has integrated the current limitation control loop. In normal operation, when the heavy load or a situation that make charge pump flow through very large current, the current limitation control loop will control charge pump maximum output current capacity, that is 2A.

***Over Voltage Protection(OVP)Control***

K-chargepump's output voltage PVDD is a multiple of the input voltage VDD, which provide a high voltage rail for internal power amplifier circuits, allowing the amplifiers provide greater output dynamic range in the lithium battery voltage range, so as to realize the large volume, high quality class K audio enjoyment. K-chargepump has integrated the over voltage protection control loop, when the input voltage VDD is greater than 4V, the output voltage PVDD is no longer a multiple of VDD, but is controlled by over voltage protection(OVP) loop and is stable in 6.05V, and the hysteresis voltage is about 50mV.

## Speaker & Receiver two-in-one application

AW87317 mode5, mode6 are receiver modes, the gain can be optional, 1V/V and 3V/V, respectively, which make the application flexible. Receiver modes use speakers' signal path, which has ultra-low distortion and a strong driving ability. So it is suitable for high definition voice application. Another advantage is that there is no need of additional external components, less system cost and PCB layout space.

In Figure 5 typical application, input capacitance Cin=15nF, input resistance Rine=3kohm, speaker mode gain is about 16.3V/V, the input high-pass corner frequency is at 544Hz; When receiver mode gain is 1V/V, the output noise of receiver is 22uV， the input high-pass corner frequency is at 56Hz. AW87317 can achieve speaker and receiver two-in-one application without changing any hardware.

## One-wire pulse control

One wire pulse control technology only needs a single GPIO port to operate the chip, complete a variety of functions, it is very popular in the area of the GPIO port shortage and portable systems.
When the control signal line is longer, because of the signal integrity or radio frequency interference problem, it will produce the narrow glitch signal. Awinic one wire pulse control technology integrated the Deglitch circuit in internal control pin, which can effectively eliminate the influence of the glitch signal, as shown in figure 12.

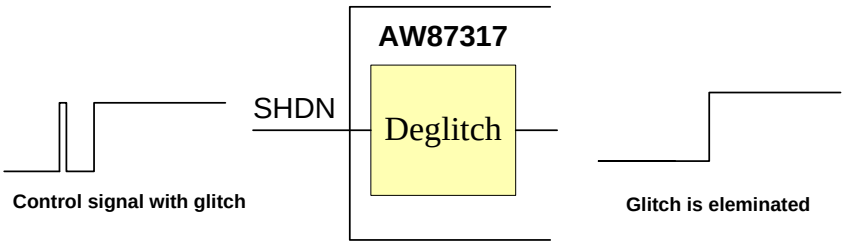



**Figure 12 Awinic Deglitch function diagram**

The traditional one wire pulse control technology still receives pulse signal from control port when chip is startup, so when the master control chip (such as mobile phone BB) sends wrong pulse during normal operation, the system will enter into error states. AW87317 uses one wire pulse latch technology, after the master control chip has sent pulses, the state will be latched, no longer receive the latter mis-sending pulse signals, as shown in figure 13.

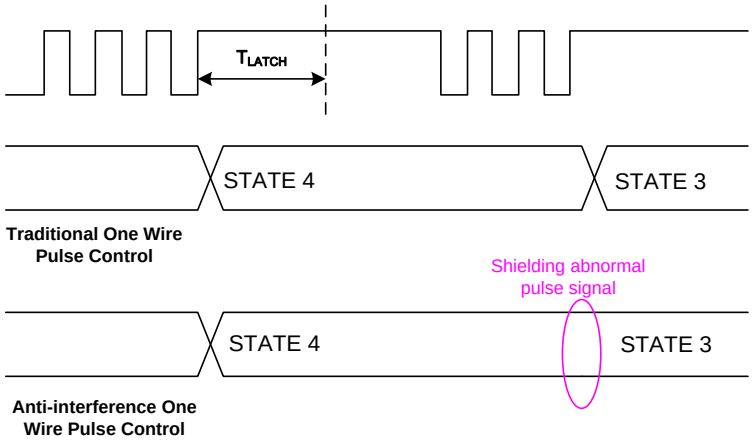



**Figure 13 Anti-interference One Wire Pulse Control Function Diagram**

***One Wire Pulse Control***

AW87317 select each mode through the detection of number of the pulse signal rising edge of SHDN pin, as shown in figure 14: When SHDN pin pull high from shutdown mode, there is only a rising edge, AW87317 enter into mode 1,NCN output power is 1.2W; When high-low-high signal set to SHDN pin, there are two rising edges, AW87317 enter into mode 2, NCN output power is 1W; When there are three rising edges, AW87317 enter into mode 3,NCN output power is 0.8W; When there are four rising edges, AW87317 enter into mode 4,NCN function is turned off; AW87317 has four operation modes, the number of the rising edges does not allow more than four.

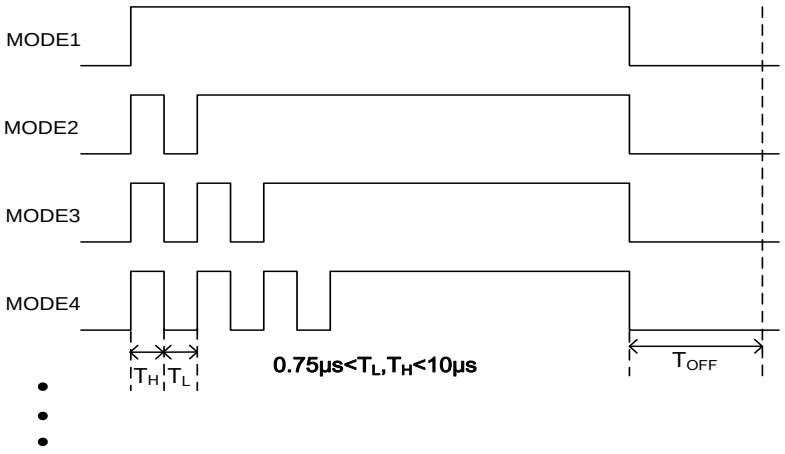



**Figure 14 One Wire Pulse Control**

When AW87317 needs to work in different mode, PIN SHDN should be pull low longer than $T_{OFF}$ first(recommended 1ms) which make the AW87317 shut down, Then send series pulse make the AW87317 enter into right mode, as shown in figure 15.

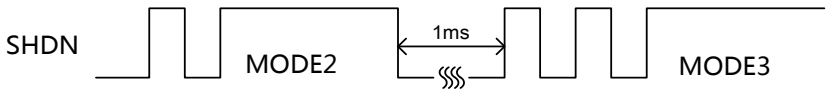



**Figure 15 One Wire Pulse Control Switching Sequence**

## RNS(RF TDD Noise Suppression)

GSM radios transmit using time-division multiple access with 217Hz intervals. The result is an RF signal

with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers.

In RF applications, improvements to both layout and component selection decrease the AW87317's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the AW87317. Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the AW87317. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane.

Some RF energy will couple onto audio traces regardless of the effort to prevent this phenomenon from occurring, form audible TDD Noise。The AW87317 features a unique RNS technology, which effectively reduces RF energy, attenuate the RF TDD-noise, an acceptable audible level to the customer.

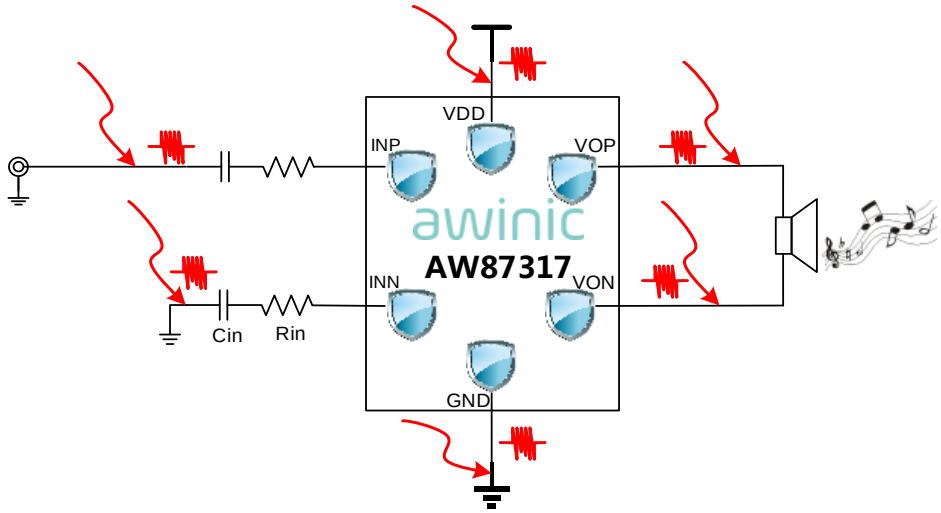



**Figure 16 RF Radiation coupling schematic diagram**

## Filter-Free Modulation Scheme

The AW87317 features a filter-free PWM architecture that reduces the LC filter of the traditional Class-D amplifier, increasing efficiency, reducing board area consumption and system cost.

## EEE

The AW87317 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth.

## Pop-Click Suppression

The AW87317 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

## Protection Function

When a short-circuit occurs between VOP/VON pin and VDD/GND or VOP and VON, the over-current circuit shutdown the device, preventing the device from being damaged. When the condition is removed, the AW87317 reactivate itself. When the junction temperature is high, the over-temperature circuit shutdown the device. The circuit switches back to normal operation when the temperature decreases to safe levels.

# APPLICATION INFORMATION

**External Input Resistor-$R_{ine}$（Gain setting）**

The AW87317 is a differential audio amplifier. The IC integrates two internal input resistors, which is $R_{ini}$=16.6kΩ. Take external input resistor $R_{ine}$=3kΩ for an example, gain setting as follows：

Class K mode： $A_V = \frac{319.5k\Omega}{R_{ine}+R_{ini}} = \frac{319.5k\Omega}{3k\Omega+16.6k\Omega} = 16.3V/V$

Receiver 1V/V mode： $A_V = \frac{190k\Omega}{R_{ine}+R_{ini}} = \frac{190k\Omega}{3k\Omega+186.6k\Omega} = 1V/V$

Receiver 2V/V mode： $A_V = \frac{190k\Omega}{R_{ine}+R_{ini}} = \frac{190k\Omega}{3k\Omega+56.6k\Omega} = 3.2V/V$

**Input Capacitor-$C_{in}$（input high-pass cutoff frequency）**

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. The input capacitors and input resistors form a high-pass filter with the corner frequency:

$$f_H(-3dB) = \frac{1}{2*\pi*R_{intotal}*C_{in}}(Hz)$$

Setting the high-pass filter point high can block the 217Hz GSM noise coupled to inputs. Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise.

Take typical application in Figure 1 as an example:

$$f_H(-3dB) = \frac{1}{2*\pi*R_{intotal}*C_{in}}(Hz) = \frac{1}{2*\pi*19.6k\Omega*15nF}(Hz) = 542Hz$$

Take 1V/V receiver mode application as example，the input high-pass corner frequency is：

$$f_H(-3dB) = \frac{1}{2*\pi*R_{intotal}*C_{in}}(Hz) = \frac{1}{2*\pi*189.6k\Omega*15nF}(Hz) = 56Hz$$

**Differential input filter capacitor Cd (input low-pass cutoff frequency)**

Input differential input filter capacitor and input resistor together to form a low-pass filter, could be used to attenuate high frequency components of the input signal. When the musical sounds screechy, this low-pass filter can be appropriately attenuate the high frequency part of the input signal, so that the music signal sounds soft and comfortable. -3dB cutoff frequency of the low-pass filter is as follows:

$$f_L(-3dB) = \frac{1}{2*\pi*(R_{ini}//R_{ine})*2*C_d}(Hz)$$

With input resistance Rine = 3kΩ, differential capacitance 220pF,for example, the low-pass cutoff frequency is as follows:

$$f_L(-3dB) = \frac{1}{2*\pi*(R_{ini}//R_{ine})*2*C_d}(Hz) = \frac{1}{2*\pi*2.54k\Omega*2*220pF}(Hz) = 142.5kHz$$

**Supply Decoupling Capacitor（$C_S$）**

The AW87317 is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW87317 is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

**Flying Capacitor（$C_F$）**

The value of the flying capacitor ($C_F$) affects the load regulation and output resistance of the charge pump. A $C_F$ value that is too small degrades the device's ability to provide sufficient current drive. Increasing the value of $C_F$ improves load regulation and reduces the charge pump output resistance to an extent. A 2.2μF@6.3V upper capacitor is recommended.

**Output Capacitor（$C_{OUT}$）**

The output capacitor value and ESR directly affect the ripple at PVDD. Increasing $C_{OUT}$ reduces output ripple. Likewise, decreasing the ESR of $C_{OUT}$ reduces both ripple and output resistance. A 4.7μF@10V capacitor is recommended.

**Optional Ferrite Bead Filter**

The AW87317 passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from amplifier to speaker, placed as close as possible to the output pin.

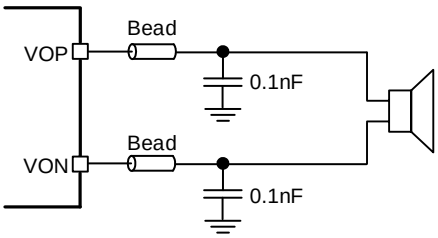
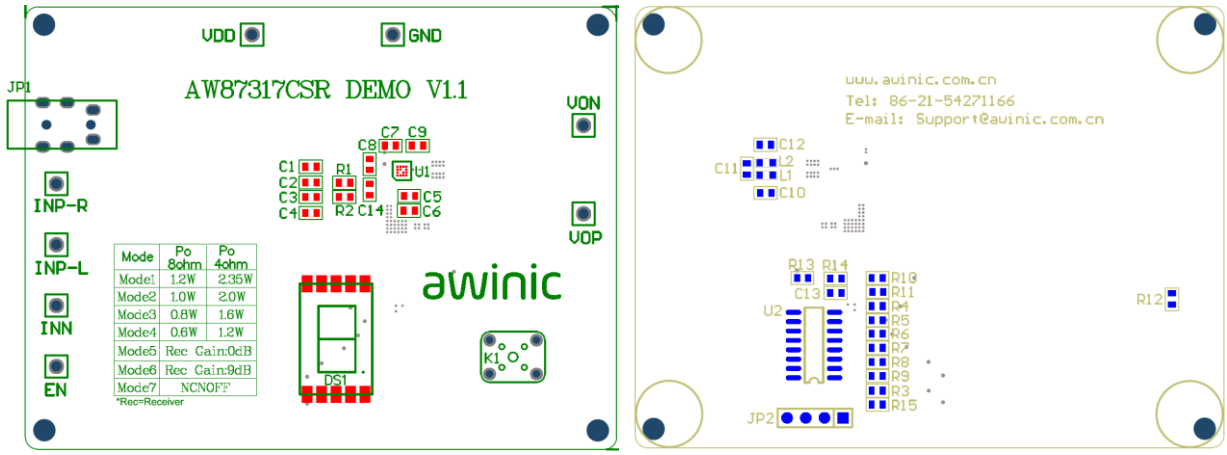


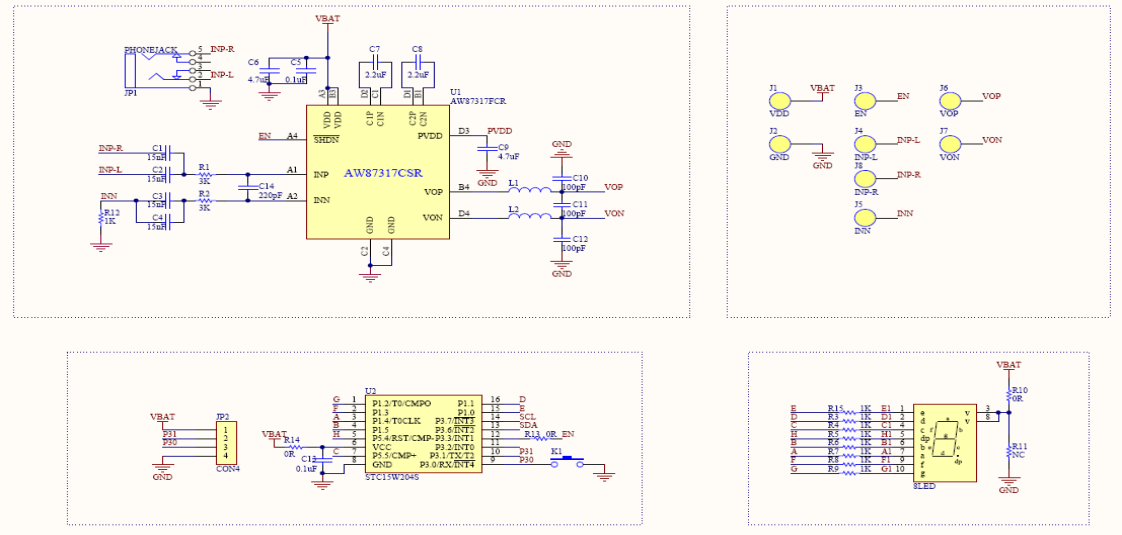

**Figure 17 Ferrite Chip Bead and capacitor**

## DEMO PCB




Top Layer　　Bottom Layer

## DEMO PCB SCHEMATIC



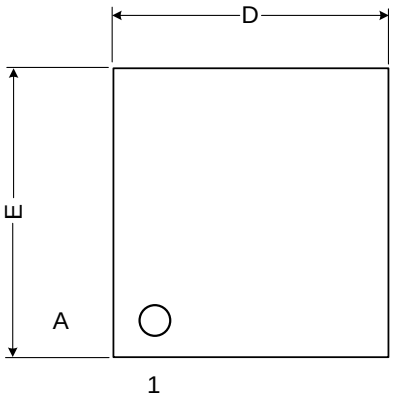

## PCB AND DEVICE LAYOUT CONSIDERATION

In order to obtain excellent performance of AW87317, PCB layout must be carefully considered. The design consideration should follow the following principles:

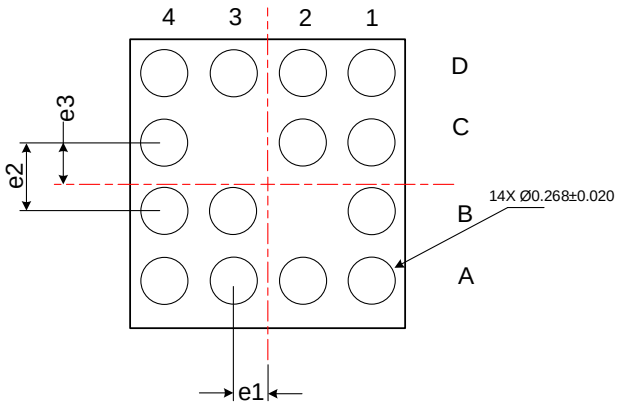
1. Try to provide a separate short and thick power line to AW87317, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to power supply pin.
2. The flying capacitors $C_{F1}$，$C_{F2}$ should be placed as close as possible to C1N, C1P and C2N, C2P, so the same to the output capacitor $C_{OUT}$, it should be close to PVDD pin. The connection from capacitor to PVDD pin should be short and thick.
3. The input capacitors and resistors should be close to AW87317 INN and INP input pin, the input line should be parallel to suppress noise coupling.
4. The beads and capacitor should be placed near to AW87317 VON and VOP pin. The output line from AW87317 to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.

# PACKAGE DESCRIPTION

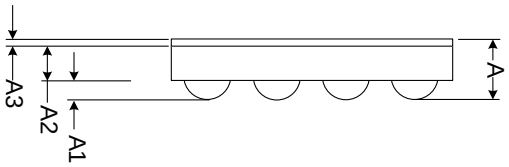
TOP VIEW




BOTTOM VIEW



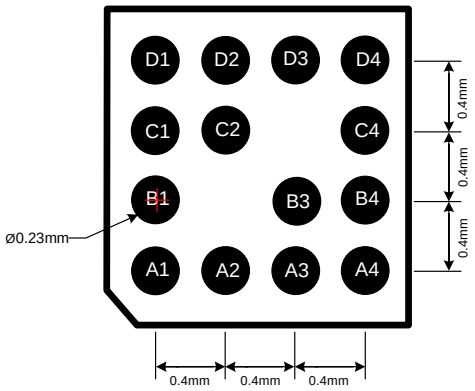

SIDE VIEW




| Symbol | NOM | Tolerance |
|---|---|---|
| A | 0.575 | ±0.055 |
| A1 | 0.195 | ±0.020 |
| A2 | 0.340 | ±0.025 |
| A3 | 0.040 | ±0.010 |
| D | 1.600 | ±0.025 |
| E | 1.680 | ±0.025 |
| e1 | 0.200 | NA |
| e2 | 0.400 | NA |
| e3 | 0.240 | NA |

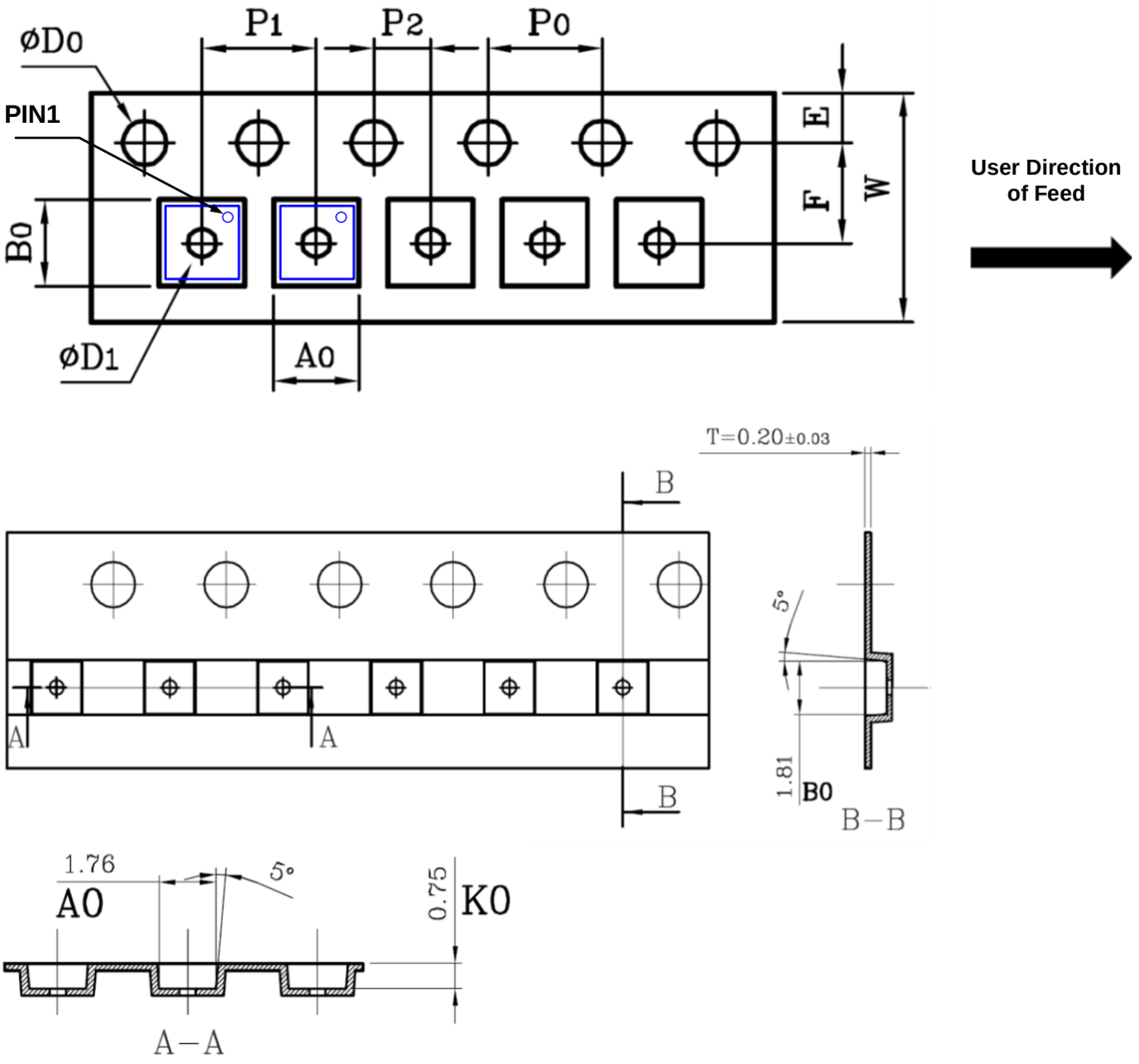
Unit: mm

LAND PATTERN

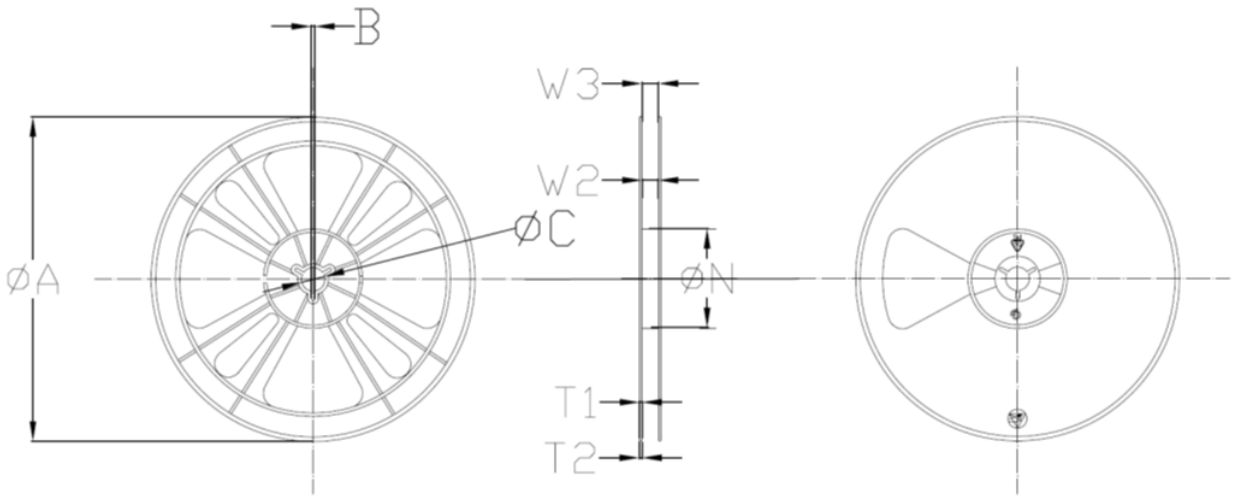


## TAPE DESCRIPTION

| PRODUCT SIZE (UNIT：mm) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| SPEC | W | P1 | E | F | D0 | D1 | P0 | P2 | 10P0 |
| SIZE | 8.00 $^{+0.30}_{-0.10}$ | 4.0±0.1 | 1.75±0.1 | 3.5±0.05 | 1.50 $^{+0.10}_{-0}$ | 0.5±0.05 | 4.0±0.1 | 2.0±0.05 | 40±0.2 |
| SPEC | A0 | A1 | B0 | B1 | K0 | K1 | T | | |
| SIZE | 1.76±0.05 | | 1.81±0.05 | | 0.75±0.05 | | 0.20±0.03 | | |



## REEL DESCRIPTION



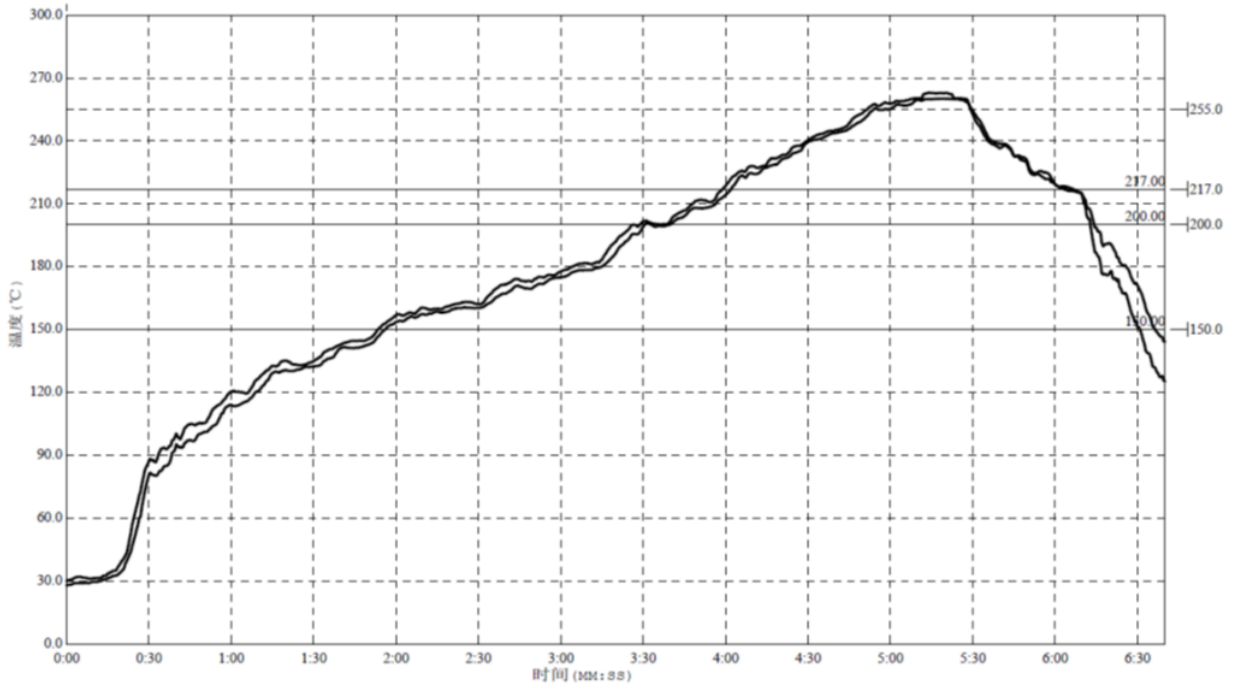

Unit: mm

| Item | Value&Tolerance |
|---|---|
| A | 179±1.0 |
| B | 2.0±0.1 |
| C | 13.5±0.2 |
| N | 54.8±0.2 |
| W2 | 9.0±0.2 |
| W3 | 9.2±1.0 |
| T1 | 1.2±0.2 |
| T2 | 1.5±0.2 |

Note：

1. Surface resistivity: $10^5$ to $10^{11}$ ohms/sq.
2. Restriction criterion of hazardous substance for packing material follow GP-M001.

## REFLOW




| Reflow Note | Spec |
|---|---|
| Average ramp-up rate (217℃ to peak) | Max. 3℃/sec |
| Time of Preheat temp. (from 150℃ to 200℃) | 60-120sec |
| Time to be maintained above 217℃ | 60-150sec |
| Peak Temperature | >260℃ |
| Time within 5℃ of actual peak temp | 20-40sec |
| Ramp-down rate | Max. 6℃/sec |
| Time from 25℃ to peak temp | Max. 8min |

# VERSION INFORMATION

| Version | Date | Description |
|---|---|---|
| V1.0 | 2015-10-16 | AW87317CSR datasheet V1.0 |
| V1.1 | 2017-09-25 | Add LAND PATTERN description, tape and reel description, add PIN1 direction in tape, add reflow curve. |
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