White LED Driver with Flexible Digital and PWM Brightness Control in Small Package

FEATURES

- 2.7 to 5.5V Input Voltage Range
- 38V Over-voltage Protection for up to 10 LEDs in Series
- Innovative CDC Output Drive Technology, Significantly Improve EMI Performance
- 200mV Reference Voltage
- Flexible Digital and PWM White LED Brightness Control
- Support EMI performance programmable under 1-wire/PWM mode
- Minimum PWM Dimming Duty Cycle: 1%
- 600kHz Switching Frequency
- Over-current and Over-temperature Protection
- Built-in Soft-start Limits Inrush Current
- Ultra Small 2mm*2mm TDFN-6L package

APPLICATIONS

- Mobile Phones
- Portable Media Players
- GPS Receivers

GENERAL DESCRIPTION

The AW9961 is a white LED driver with integrated boost converter. With an internal 40V switch FET, the AW9961 drives up a string of up to 10 LEDs in series. The boost converter runs at 600kHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allows for the use of small external components.

The default white LED current is set with the external sense resistor R_{SET}, and the feedback voltage is regulated to 200mV, as shown in the typical application. During the operation, the LED current can be controlled by using the 1-wire digital interface through the CTRL pin. Alternately, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the AW9961 does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED over-voltage protection that disables the AW9961 to prevent the output from exceeding the absolute maximum ratings during open LED conditions.

AW9961 sets a built-in EMI performance register, which can be configured under either 1-wire or PWM mode.

TYPICAL APPLICATION CIRCUIT

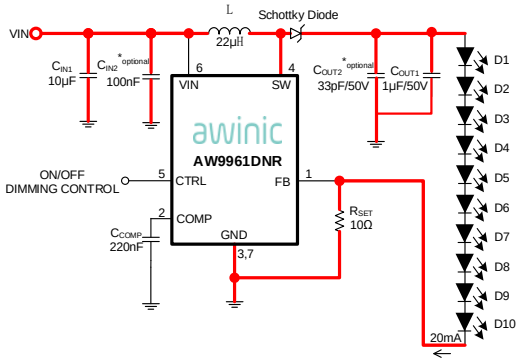

Figure 1 Typical Application Circuit of AW9961

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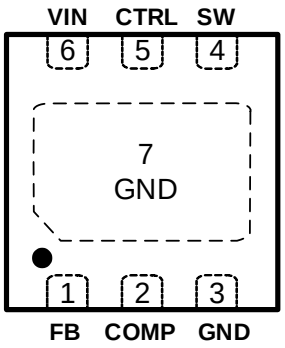
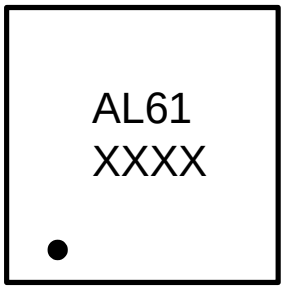
PIN CONFIGURATION AND TOP MARK

AW9961DNR TOP VIEW



AW9961DNR MARKING



AL61——AW9961DNR
XXXX——Manufacture Data Code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	FB	Feedback pin for current. Connect the sense resistor from FB to GND.
2	COMP	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the regulator.
3	GND	Ground.
4	SW	This is the switching node of the IC. Connect the inductor between the VIN and SW pin. This pin is also used to sense the output voltage for open LED protection.
5	CTRL	Control pin of the boost regulator. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.
6	VIN	The input supply pin for the IC. Connect VIN to a supply voltage between 2.7 and 5.5V.
7	GND	Exposed pad should be soldered to PCB board and Connected to GND.

FUNCTIONAL BLOCK DIAGRAM

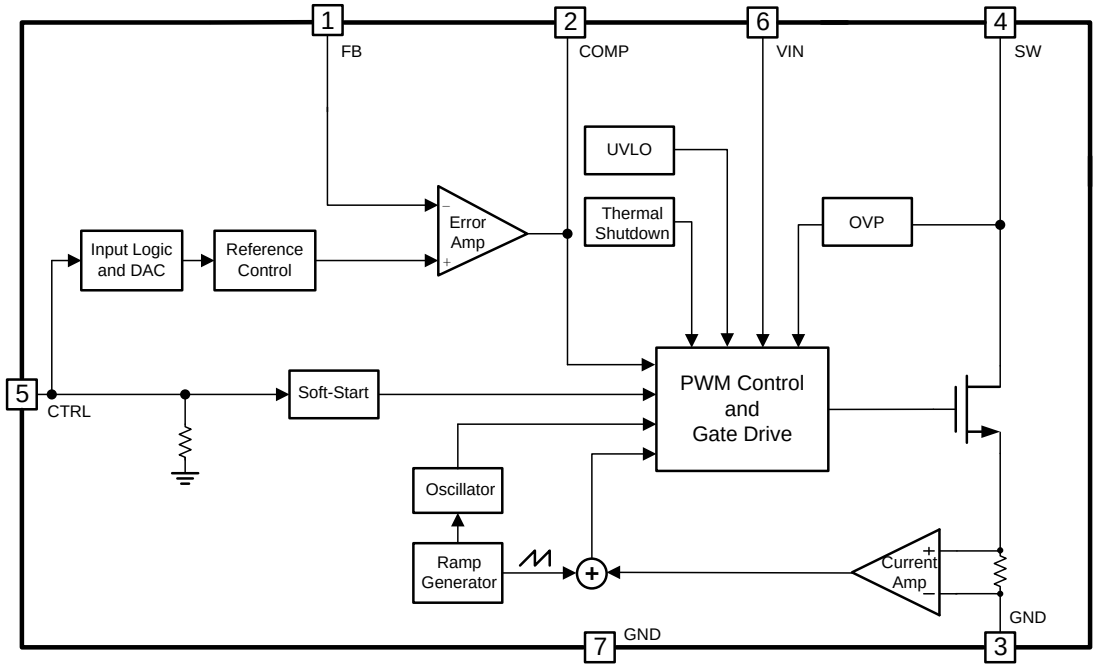


Figure 3 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION CIRCUITS

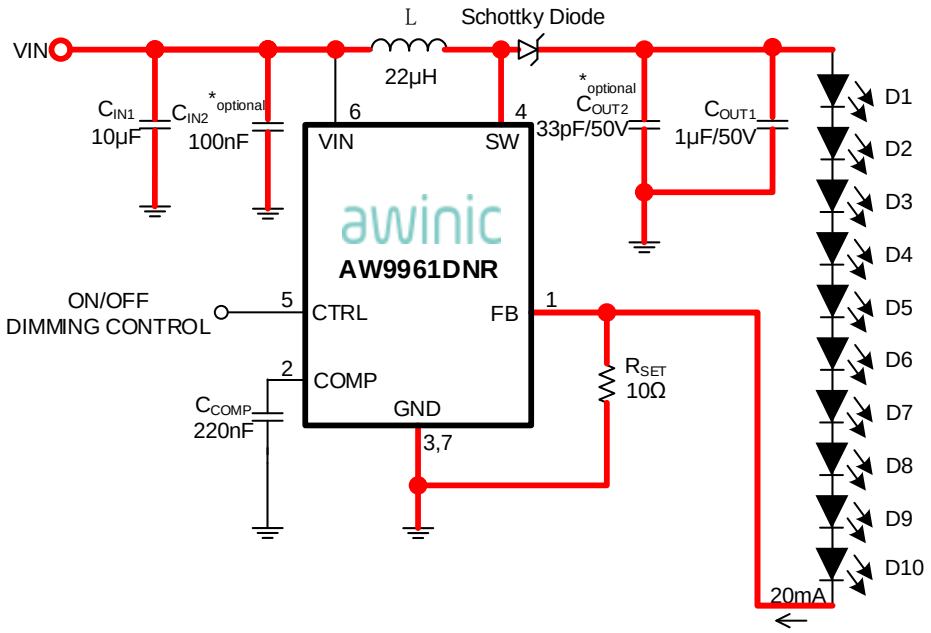


Figure 4 Typical Application of AW9961

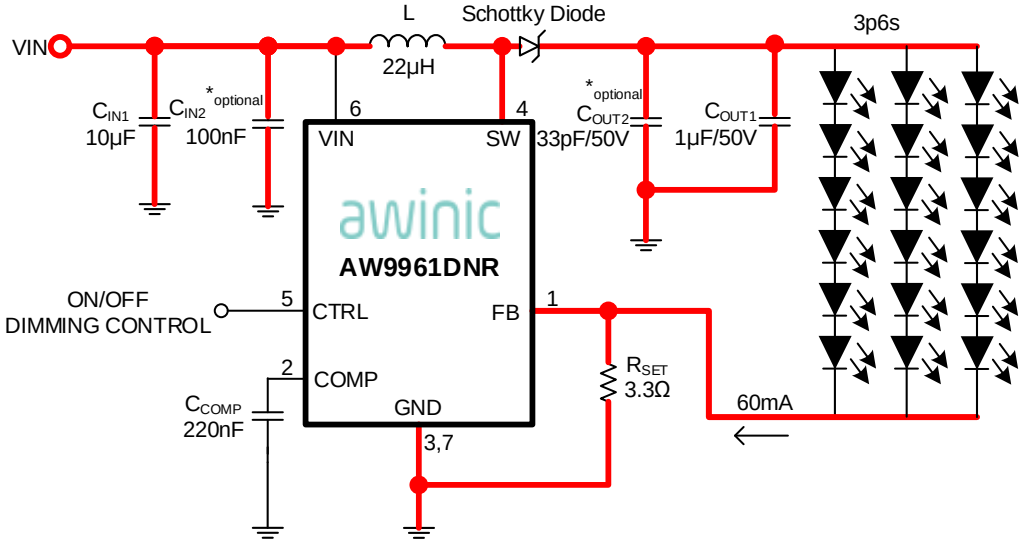


Figure 5 Drive 18 White LEDs for Large Screen Display

Notice for Typical Application Circuits:

1：Recommended device for AW9961:

L:TDK VLCF5020T-220MR75-1

C_{IN1}: Murata GRM188R61C106MA73

C_{IN2}: Murata GRM155R61C104K

C_{OUT1}: Murata GRM21BR71H105KA

C_{OUT2}: Murata GRM1555C1H330GA

Schottky Diode: ONsemi MBR0540T1

2：C_{IN2} and C_{OUT2} are recommended to use in parallel with the input capacitor and output capacitor to suppress high frequency noise.

3：Red lines are high current paths, reference to the section APPLICATION INFORMATION.

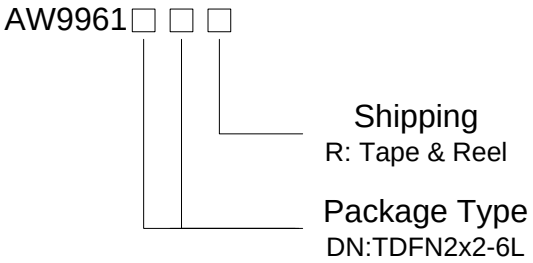
4：The capacitors (C_{IN1}, C_{IN2}, C_{OUT1}, C_{OUT2} and C_{COMP}) should be placed as close to the pins of the IC as possible.

5：Minimize trace lengths between the IC and the inductor, the Schottky diode and the output capacitor, keep these traces short, direct, and wide.

6：Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9961DNR	-40℃～85℃	TDFN2x2-6L	AL61	MSL3	ROHS+HF	3000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS	RANGE
Supply voltage range VIN(NOTE 2)	-0.3V to 6V
Voltage on FB,CTRL and COMP(NOTE 2)	-0.3V to 6V
Voltage on SW(NOTE 2)	-0.3V to 40V
Junction-to-ambient thermal resistance θ_{JA}	120℃/W
Operating free-air temperature range	-40℃ to 85℃
Maximum Junction temperature T_{JMAX}	160℃
Storage temperature T_{STG}	-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)	260℃
ESD(NOTE 3)	
ALL PINS HBM (human body model) (NOTE 4)	±6000V
ALL PINS CDM (charge device model) (NOTE 5)	±2500V
ALL PINS MM (machine model) (NOTE 6)	±300V
Latch-up(NOTE 7)	
Latch-up current maximum rating per JEDEC standard	+IT：250mA -IT：-250mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *All voltage values are with respect to network ground terminal.*

NOTE3: This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. AWINIC recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883H Method 3015.8.

NOTE5: Test Condition: JEDEC EIA/JESD22-C101E.

NOTE6: Test Condition: JEDEC EIA/JESD22-A115.

NOTE7: Test Condition: JEDEC STANDARD NO.78D NOVEMBER 2011.

ELECTRICAL CHARACTERISTICS

Test Condition: T_A = 25℃, VIN = 3.6V, V_{CTRL} = VIN (Unless otherwise specified).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
VIN	Input voltage range		2.7		5.5	V
I_Q	Operating quiescent current	VFB = 1V		0.9	1.4	mA
I_{SD}	Shutdown current	V_{CTRL} = GND, VIN=4.2V		0.1	1	μA
V_{UVLO}	Under-voltage lockout threshold	VIN falling	1.85	2	2.25	V
V_{HYS}	Under-voltage lockout hysteresis			150		mV
ENABLE AND REFERENCE CONTROL						
V_{CTRL_H}	CTRL logic high voltage	VIN = 2.7V to 5.5V	1.5			V
V_{CTRL_L}	CTRL logic low voltage	VIN = 2.7V to 5.5V			0.3	V
R_{CTRL}	CTRL pull down resistor			600		kΩ
t_{OFF}	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
t_{1W_DET}	Digital 1-wire brightness detection time(NOTE 1)	CTRL pin low	260			μs
t_{1W_DELAY}	Digital 1-wire brightness detection delay		100			μs
t_{1W_WIN}	Digital 1-wire brightness detection window time	Measured from CTRL pin	1			ms
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		195	200	205	mV
V_{REF_PWM}	Voltage feedback regulation voltage under brightness control	f_{PWM} = 10 kHz, duty cycle = 25%	46	50	54	mV
		f_{PWM} = 10 kHz, duty cycle = 10%	16	20	24	mV
I_{FB}	Voltage feedback input bias current			0.1	1	μA
f_S	Oscillator frequency		500	600	700	kHz
D_{MAX}	Maximum duty cycle		90%	95%		
POWER SWITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN = 3.6V		0.36	0.65	Ω
		VIN = 3.0V			0.7	Ω
I_{L_NFET}	N-channel leakage current	V_{SW} = 35V, T_A = 25℃			1	μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OCP AND OVP						
I_{LIM}	N-channel MOSFET current limit		0.6	1.1	1.7	A
V_{OVP}	Open LED overvoltage protection threshold	Measured on the SW pin	36	38	40	V
t_{REF}	VREF filter time constant			480		μs
DIGITAL 1-WIRE COMMAND TIMING						
t_{START}	Start time of program stream		2			μs
t_{EOS}	End time of program stream		2		360	μs
t_{H_LB}	High time low bit	Logic 0	2		180	μs
t_{L_LB}	Low time low bit	Logic 0	$2\times t_{H\_LB}$		360	μs
t_{H_HB}	High time high bit	Logic 1	$2\times t_{L\_HB}$		360	μs
t_{L_HB}	Low time high bit	Logic 1	2		180	μs
V_{ACKNL}	Acknowledge output voltage low	Open drain, R_{PULLUP} = 15kΩ to VIN		0.1		V
$t_{VALACKN}$	Acknowledge valid time	See(NOTE 2)			2	μs
t_{ACKN}	Duration of acknowledge condition	See(NOTE 2)			512	μs
PWM DIMMING TIMING						
f_{PWM}	Frequency of PWM dimming		10		100	kHz
t_{H_PWM}	High time of PWM dimming signal	f_{PWM}=10kHz	1			μs
		f_{PWM}=100kHz	100			ns
THERMAL SHUTDOWN						
T_{OTP}	Thermal shutdown threshold			165		℃
T_{HYS}	Thermal shutdown threshold hysteresis			16		℃

NOTE1: *To select 1-wire digital interface mode, the CTRL pin has to be low for more than t_{1W_DET} during t_{1W_WIN}.*

NOTE2: *Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open drain output, line needs to be pulled high by the host with resistor load.*

TYPICAL CHARACTERISTICS

Table 1 TABLE OF FIGURES

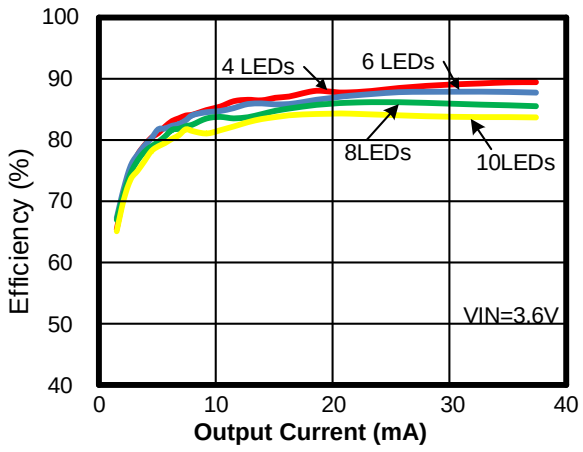


Fig7. EFFICIENCY Vs. OUTPUT CURRENT

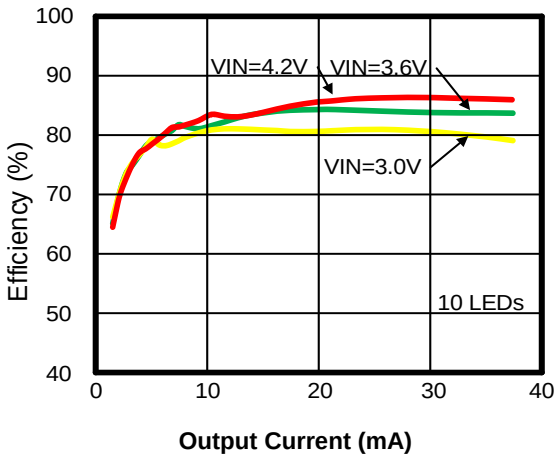


Fig8. EFFICIENCY Vs. OUTPUT CURRENT

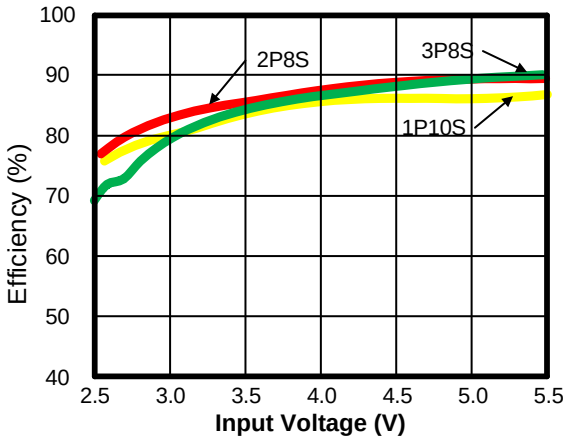


Fig9. EFFICIENCY Vs. INPUT VOLTAGE

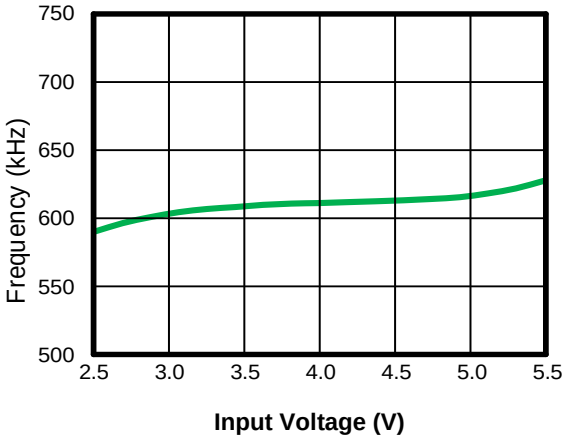


Fig10. FREQUENCY Vs. INPUT VOLTAGE

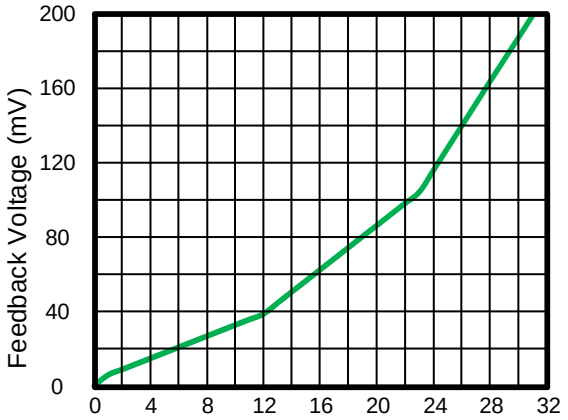


Fig11. FEEDBACK VOLTAGE Vs. 1-WIRE DIMMING STEP

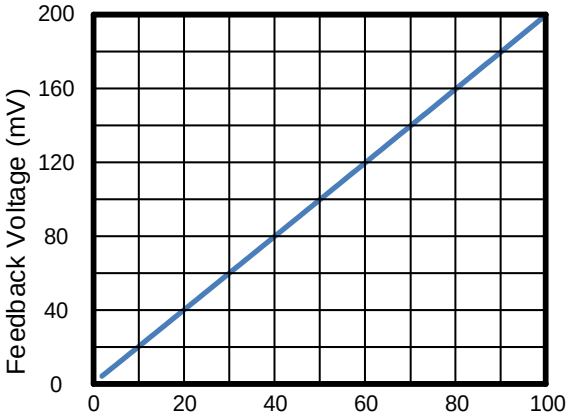


Fig12. FEEDBACK VOLTAGE Vs. PWM DUTY CYCLE

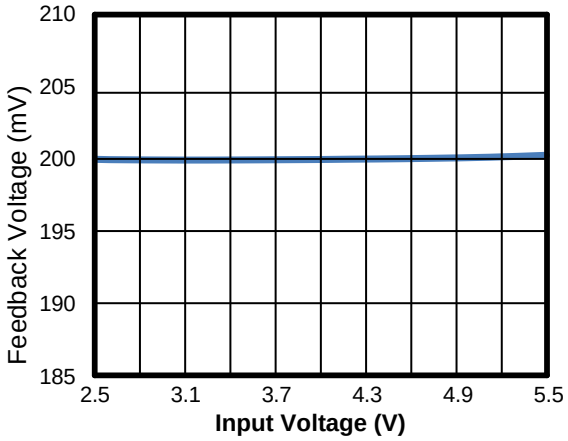


Fig13. FEEDBACK VOLTAGE Vs. INPUT VOLTAGE

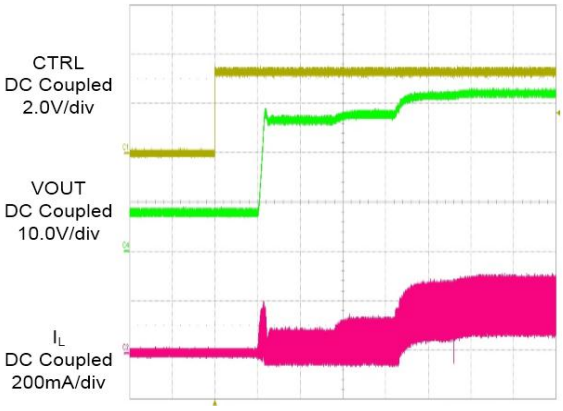


Fig14. SOFT-START WAVEFORM

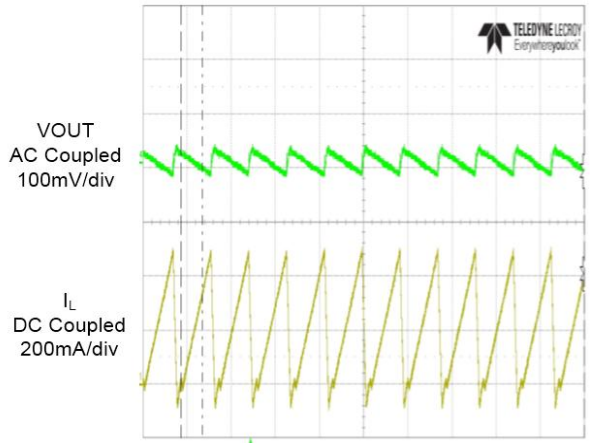


Fig15. SWITCHING WAVEFORM

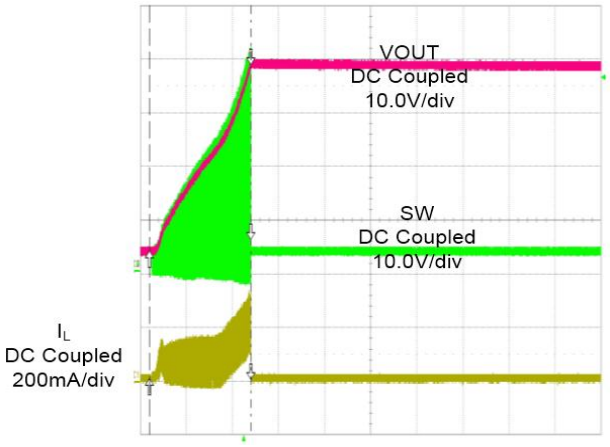


Fig16. OPEN LED PROTECTION

DETAILED FUNCTIONAL DESCRIPTION

The AW9961 is a high efficiency, high output voltage boost converter in small package size. The device is ideal for driving up to 10 white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40V/1.0A switch FET and operates in pulse width modulation (PWM) with 600kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control. Therefore, slope compensation is added to the current signal to allow stable operation for duty cycle larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

SOFT START-UP

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage. This ensures that the output voltage rises slowly to reduce the input current. See the start-up waveform of a typical example.

OPEN LED OVER-VOLTAGE PROTECTION

Open LED over-voltage protection circuitry prevents IC damage as the result of white LED disconnection. The AW9961 monitors the voltage at the SW pin during each switching cycle. The circuitry turns off the switch FET as soon as the SW voltage exceeds the V_{OVP} threshold for 8 clock cycles. The switch will switch after about 50ms. When the above condition is met, the protection circuitry will work again.

SHUTDOWN

The CTRL input is used to enable or disable the AW9961. Pulling the CTRL pin higher than 1.5V will enable the device. The AW9961 has an internal shutdown delay circuitry, when the CTRL pin is held low for an amount of time longer than 3.0ms, the AW9961 will enter shutdown mode and the input supply current for the device is less than 1μA. Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

UNDER-VOLTAGE LOCKOUT

An under-voltage lockout prevents operation of the device at input voltage below typical 2V. When the input voltage is below the under-voltage threshold, the device is shut down and the internal switch FET is turned off. If the input voltage rises by under-voltage lockout hysteresis, the IC restarts.

CURRENT PROGRAM

The FB voltage is regulated by a low 200mV reference voltage. The LED current is programmed externally using a current sense resistor in series with the LED string. The value of the RSET can be calculated by the following equation:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \qquad (1)$$

Where:

I_{LED} = output current of LEDs

V_{FB} = regulated voltage of FB

R_{SET} = current sense resistor

LED BRIGHTNESS DIMMING MODE SELECTION

The CTRL pin is used for the control input for both dimming modes, PWM dimming and the 1-wire dimming. The dimming mode for the AW9961 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter 1-wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time that the IC starts from the shutdown mode.

1. Pull the CTRL pin high to enable the AW9961, and to start the 1-wire detection window.
2. After the digital 1-wire brightness detection delay (t_{1W_DELAY}, 100μs) expires, drive the CTRL pin low for more than the digital 1-wire brightness detection time (t_{1W_DET}, 260μs).
3. The CTRL pin has to be low for more than digital 1-wire brightness detection time before the digital 1-wire brightness detection window (t_{1W_WIN}, 1ms) expires. Digital 1-wire brightness detection window starts from the first CTRL pin low to high transition.

The IC immediately enters 1-wire mode once the above three conditions are met. The 1-wire mode communication can start before the detection window expires. Once the dimming mode is programmed, it cannot be changed without another start up. This means the IC needs to be shut down by pulling the CTRL pin low for 2.5ms and restarts. See the *Dimming Mode Detection and Soft-start* (See FIGURE 17) for a graphical explanation.

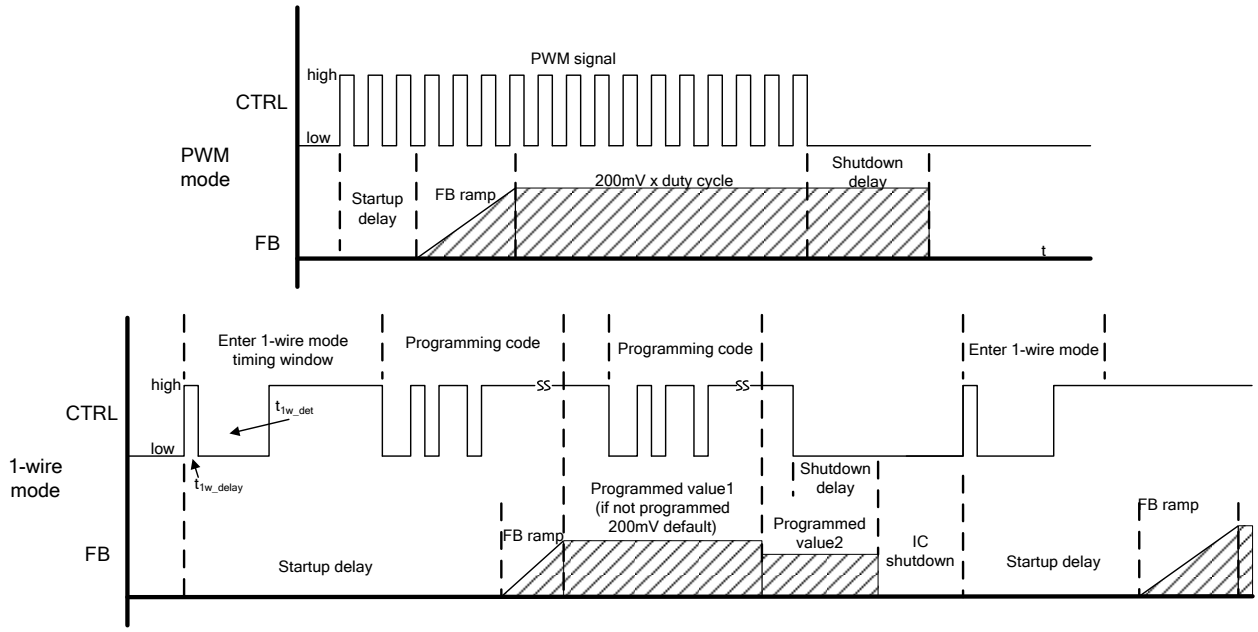


Figure 17 Dimming Mode Detection and Soft Start PWM Brightness Dimming

PWM BRIGHTNESS DIMMING

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage, it achieves LED brightness dimming. The relationship between the duty cycle and the FB voltage is given by the following equation:

$$V_{FB} = Duty \times 200mV \qquad (2)$$

Where:

Duty = duty cycle of the PWM signal

200mV = internal reference voltage

As shown in the FIGURE 18, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, AW9661 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 10kHz to 100kHz. The requirement of minimum dimming frequency comes from the digital 1-wire brightness detection delay and detection time specification in the dimming mode selection. Since the CTRL pin is logic only pin, adding external RC filter applied to the pin does not work.

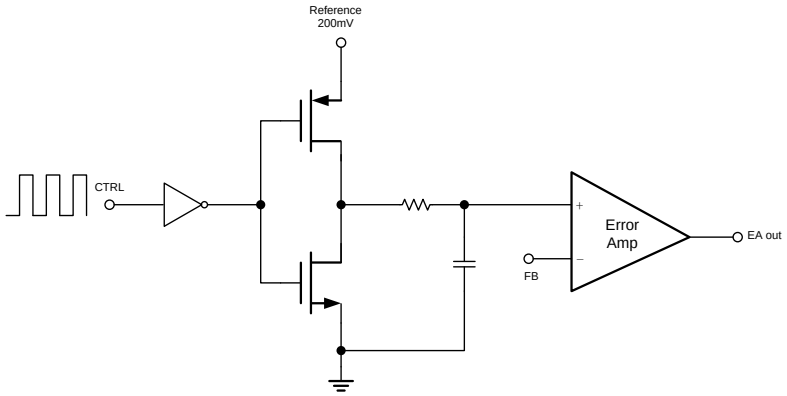


Figure 18 Block Diagram of Programmable FB Voltage Using PWM Signal

DIGITAL 1-WIRE BRIGHTNESS DIMMING

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The AW9961 adopts the 1-wire digital interface for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See TABLE 2 for the FB pin voltage steps. The default step is full scale when the device is first enabled (V_{FB} = 200mV). The programmed reference voltage is stored in an internal register. The shutdown mode clears the register value and reset it to default.

1-wire digital interface is a simple but flexible single pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. TABLE 3 and FIGURE 19 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72H. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the “Request for Acknowledge” condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of 1-wire digital interface compared with other single pin interface is that its bit detection is in a large extent independent from the bit transmission rate.

Table 2 Selectable FB Voltage

	FB voltage (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

Table 3 1-wire Digital Interface Bit Description

Byte	Bit Number	Name	Transmission Direction	Description
Device Address Byte(72 hex)	7	DA7	IN	0 MSB device address
	6	DA6		1
	5	DA5		1
	4	DA4		1
	3	DA3		0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address
Data Byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open drain output, line needs to be pulled high by the host with a pull-up resistor. This feature can only be used if the master has an open drain output stage. In case of a push-pull output stage acknowledge condition may not be requested.

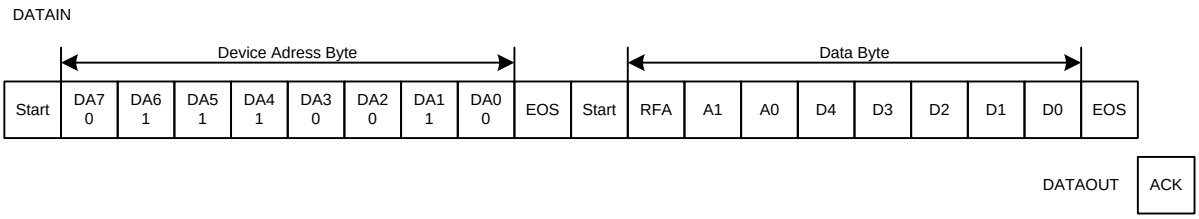


Figure 19 Digital 1-wire Interface Protocol Overview

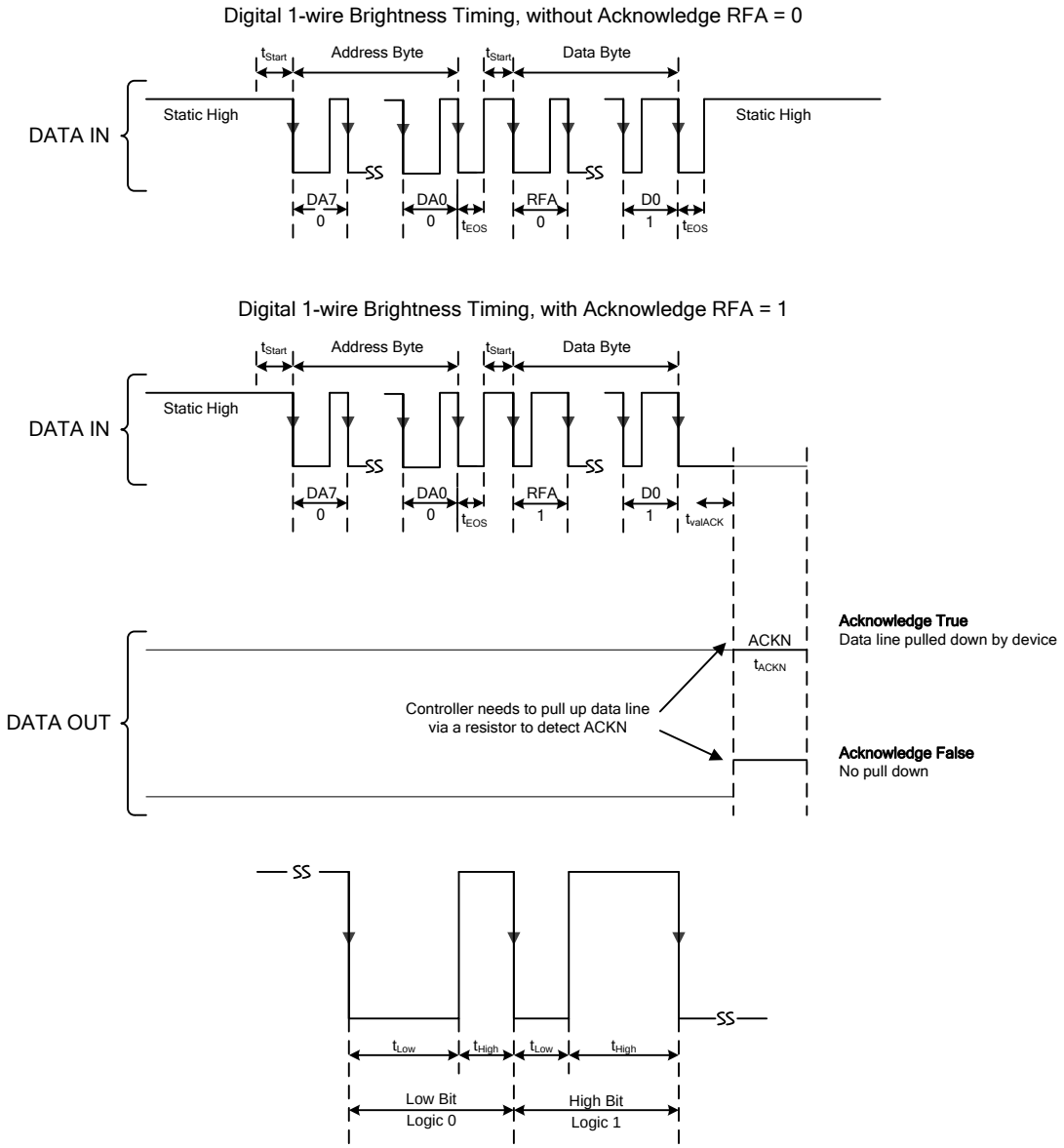


Figure 20 Digital 1-wire Interface Bit Coding

All bits are transmitted MSB first and LSB last. FIGURE 20 shows the protocol without acknowledge request (Bit RFA = 0), and the protocol with acknowledge (Bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{START} (2µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End of Stream condition for at least t_{EOS} (2µs).

The bit detection is based on a logic detection scheme, where the criterion is the relation between t_{Low} and t_{High}. It can be simplified to:

High Bit: $t_{High} > t_{Low}$, but with t_{High} at least 2 x t_{Low}, see FIGURE 20.

Low Bit: $t_{Low} > t_{High}$, but with t_{Low} at least 2 x t_{High}, see FIGURE 20.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{High} and t_{Low}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.

- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time t_{ACKN}, which is 512μs maximum then the Acknowledge condition is valid after an internal delay time t_{valACK}. This means that the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after t_{valACK} and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

Note that the acknowledge condition may only be requested in case the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CTRL line to limit the current to 500μA is recommended to for such cases as:

- an accidentally requested acknowledge, or
- to protect the internal ACKN-MOSFET.

EMI CONTROL BITS

To adjust the EMI(electromagnetic interference) issue arisen by the periodic change of inductor current, AW9961 sets an EMI control register EMI_CTL<1:0>, of which default value is 00. By configuring the EMI bits, the EMI performance can be adjusted. EMI control register is detailed in the table below.

Table 4 EMI Control Register Description

Register	A1	A0	D4	D3	D2	D1	D0	Default
PROTECT	1	1	0	1	0	1	0	0
EMI_CTL	1	0	-	-	-	EMI_CTL<1>	EMI_CTL<0>	00

Note that the EMI_CTL register cannot be written unless the PROTECT register has been written firstly. And the PROTECT bits sequence which needs to be followed is fixed to “1101010”, from A1 to D0. The PROTECT register would be cleared automatically when the next write operation happens.

Among all of the EMI bits configuration, “00” has been set for default condition. The other three conditions would be described in terms of EMI performance/ efficiency compared to default status as follows: 01(EMI worst, efficiency best), 10(EMI best, efficiency worst), 11(EMI better, efficiency worse).

AW9961 supports the EMI adjustment under either 1-wire or PWM brightness dimming mode, and the register should be configured by means of 1-wire interface protocol in both modes. While there are still some differences between the two configure methods, below are more details:

1-wire Mode

Under 1-wire mode, EMI_CTL register can be configured in the same way as dimming register. **FIGURE 21** shows a timing diagram for EMI adjustment under 1-wire mode.

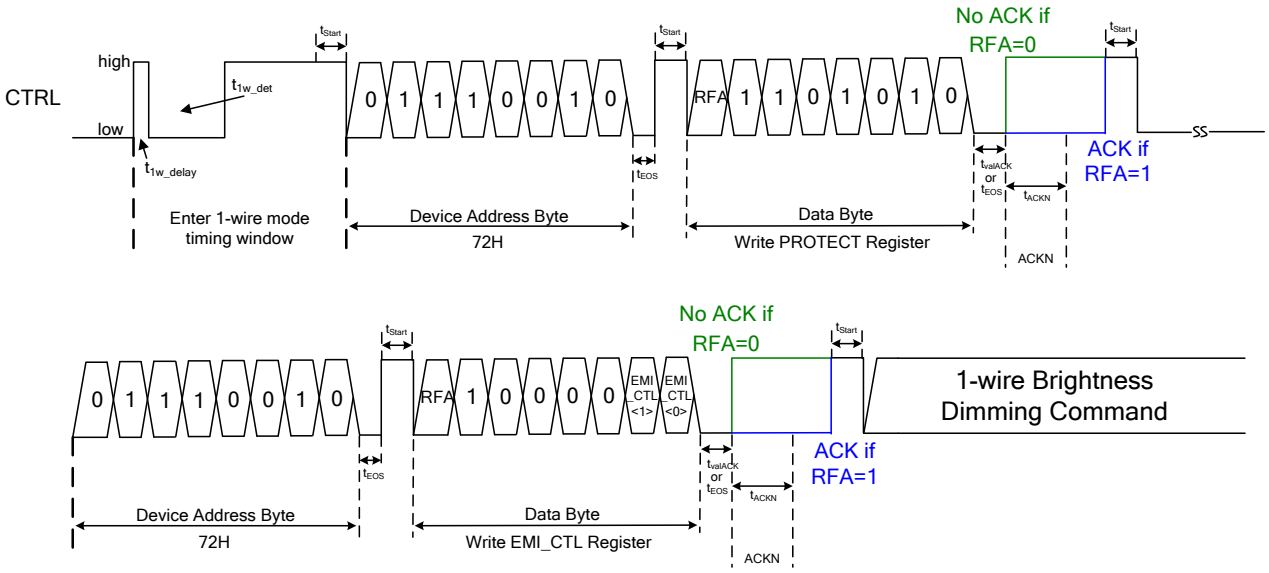


Figure 21 EMI_CTL Register Configuration Timing under 1-wire Mode

PWM Mode

In PWM mode, EMI_CTL register configuration would be implemented with the 1-wire interface protocol, while there are some different timing requirements from those under 1-wire mode at the CTRL pin: Firstly, Host should pull the CTRL pin high for 2~3ms when enabling the chip, to avoid making confusion with the mode detection window. On the other hand, no ACK would be applied at the CTRL pin unless the following sequence is satisfied:

a) PROTECT register be configured correctly only one time (non-repetitive)

b) EMI_CTL bits be configured correctly

c) the RFA bit of EMI_CTL Data Byte has been set to request an acknowledge. See **FIGURE 22**.

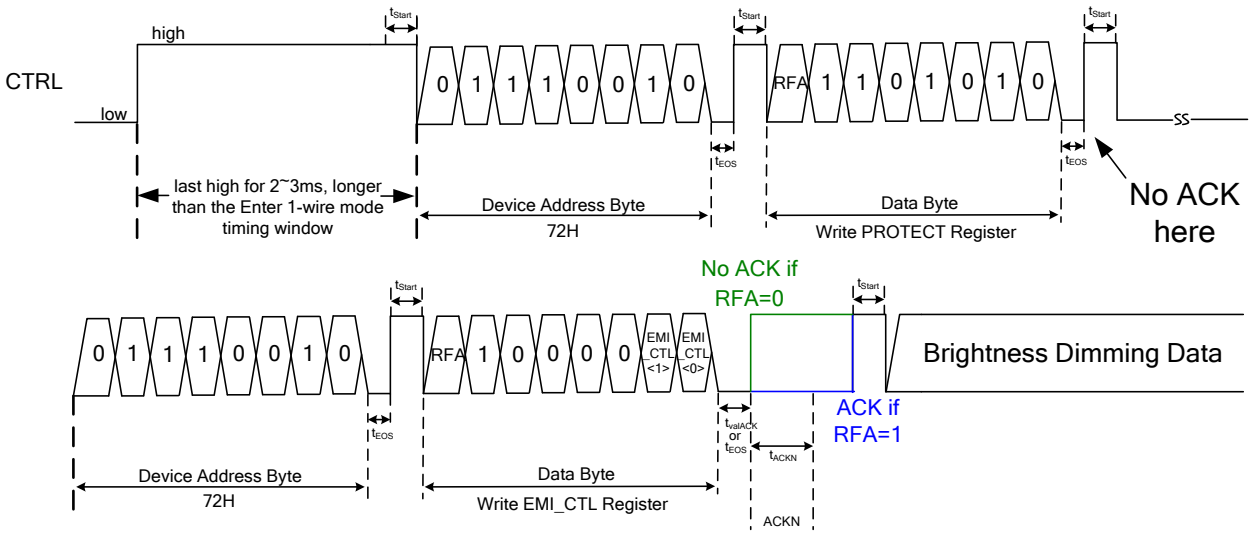


Figure 22 EMI_CTL Register Configuration Timing under PWM Mode

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of is exceeded 165℃. The device is released from shutdown automatically when the junction temperature decreases by 16℃.

APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT

The over-current limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current. Therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{L \times F_s \times (\frac{1}{V_{OUT} + V_F - V_{IN}} + \frac{1}{V_{IN}})} \quad (3)$$

Where:

I_P = inductor peak to peak ripple

L= inductor value

V_F = Schottky diode forward voltage

F_S = switching frequency

V_{OUT} = output voltage of the boost converter. It is equal to the sum of V_{FB} and the voltage drop across LEDs.

$$I_{out\_max} = \frac{V_{IN} \times (I_{lim} - I_P / 2) \times \eta}{V_{OUT}} \quad (4)$$

Where:

I_{out_max} = maximum output current of the boost converter

I_{lim} = over-current limit, for worst case calculation the minimum value has to be chosen.

η= efficiency

INDUCTOR SELECTION

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by equation 3, pause the inductor DC current given by:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{out}}{V_{IN} \times \eta} \quad (5)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous

PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10μH to 22μH inductor value range is recommended. A 22μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. TABLE 5 lists the recommended inductor for the AW9961. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

AW9961 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10μH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

Table 5 Recommended Inductors for AW9961

Part Number	L (μH)	DCR Max (Ω)	Saturation Current (mA)	Size (L x W x H mm)	Vendor
VLCF5020T-220MR75-1	22	0.4	750	5 x 5 x 2.0	TDK
LQH3NPN100NM0	10	0.3	750	3 x 3 x 1.5	Murata
A997AS-220M	22	0.4	510	4 x 4 x 1.8	TOKO
CDH3809/SLD	10	0.3	570	4 x 4 x 1.0	Sumida

SCHOTTKY DIODE SELECTION

The high switching frequency of the AW9961 demands a high-speed rectification for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED over-voltage protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for AW9961.

COMPENSATION CAPACITOR SELECTION

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the AW9961. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the AW9961. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1μF Y5V or Z5U capacitor could have a capacitance of only 0.1μF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the AW9961.

The compensation capacitor C_{COMP} (see the application circuit), connected from COMP pin to GND, is used to stabilize the feedback loop of the AW9961. Use 220nF X5R or X7R ceramic capacitor for C_{COMP}.

INPUT AND OUTPUT CAPCCITORS SELECTION

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{out}}{V_{OUT} \times F_S \times V_{ripple}} \qquad (6)$$

Where, V_{ripple} = peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I_{out} \times R_{ESR} \qquad (7)$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a resonant frequency in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

An X5R or X7R capacitor of 10μF is recommended for input side. The output requires a X5R or X7R capacitor in the range of 0.47μF to 4.7μF. A 100nF capacitor and a 33pF capacitor are recommended to use in parallel with the input capacitor and the output capacitor to suppress high frequency noise.

The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. For example, if use the output capacitor of 0.1μF, a 470 nF compensation capacitor has to be used for the loop stable.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

POWER DISSIPATION

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the AW9961. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined by using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{\theta_{ja}}$$

Where, T_{Jmax} is the Maximum Junction Temperature, T_A is the maximum ambient temperature for the application. θ_{ja} is the thermal resistance junction-to-ambient given in Power Dissipation Table.

The AW9961 comes in a thermally enhanced TDFN package. Compared with the TSOT package, the TDFN package has better heat dissipation. This package includes a thermal pad that improves the thermal capabilities of the package. The θ_{ja} of the TDFN package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered directly to the analog ground on the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit(IC).

Using thermal vias underneath the thermal pad as illustrated in the layout example.

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the IC supply ripple.

Connect the exposed paddle to the PCB ground plane using at least two vias. The input and the output bypass capacitors should be placed as close to the IC as possible. Minimize trace lengths between the IC and the inductor, the diode and the output capacitor; keep these traces short, direct, and wide.

A recommended PCB Layout is shown in FIGURE 23. In order to dissipate the package heat, the package thermal pad must be connected to a large copper area on the ground plane underneath using multiple vias.

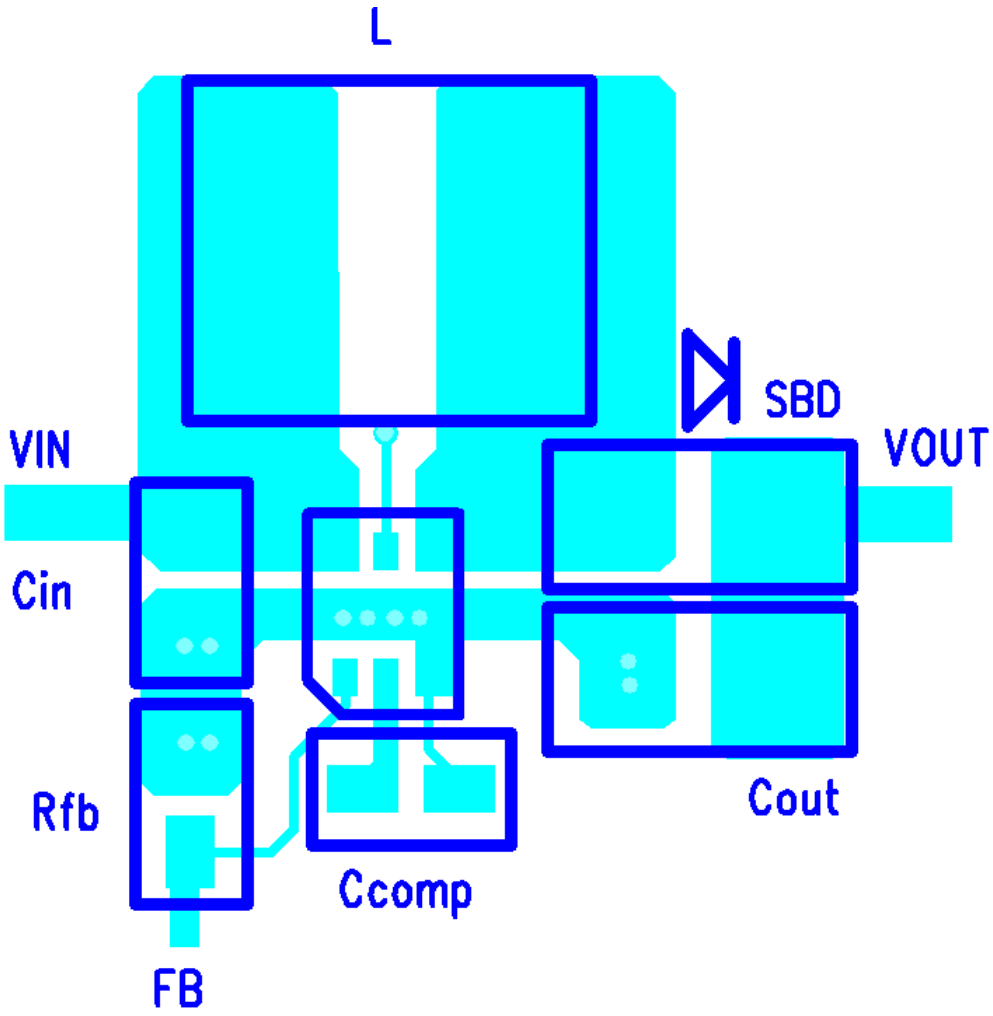
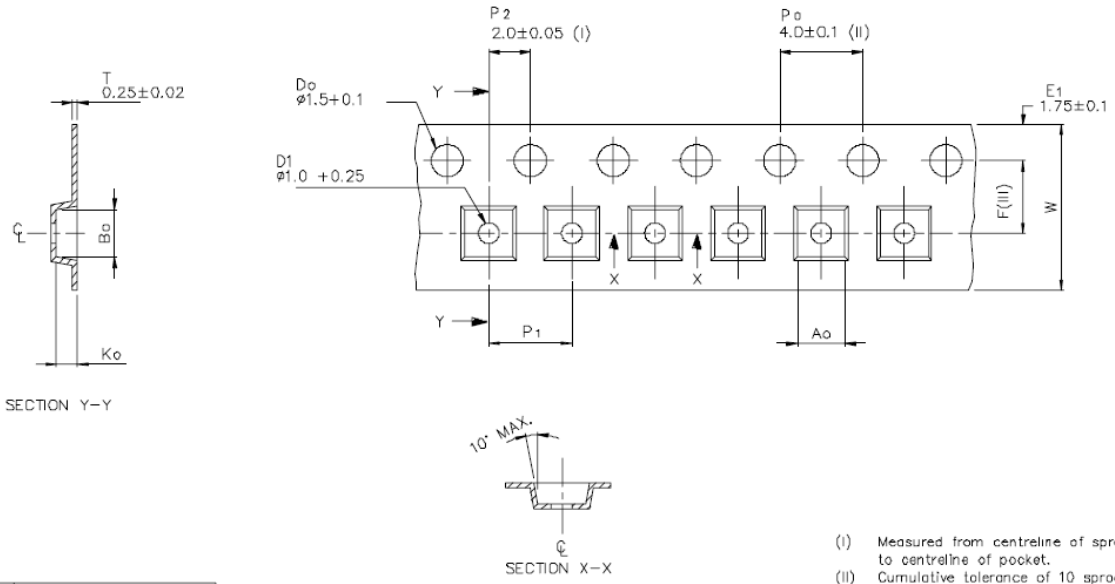


Figure 23 Recommended PCB Layout

TAPE AND REEL INFORMATION

Carrier Tape

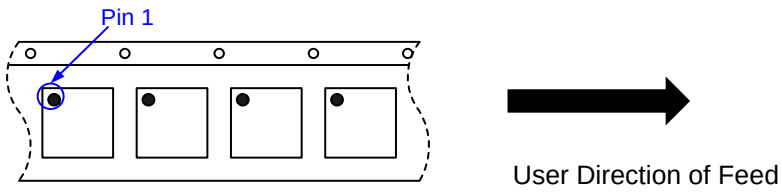


Ao	2.30 +/−0.05
Bo	2.30 +/−0.05
Ko	1.00 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +0.3/−0.1

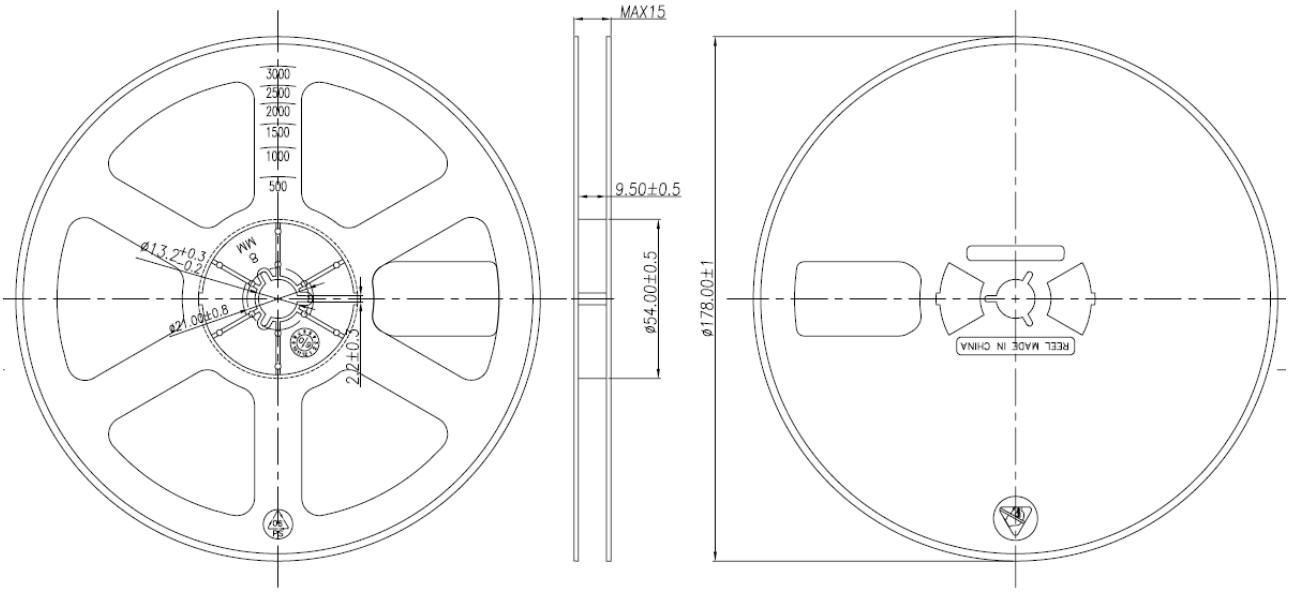
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^9 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

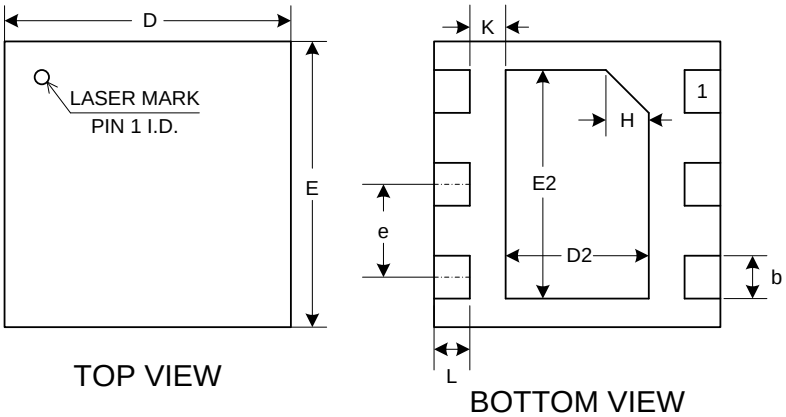
Pin1 Direction

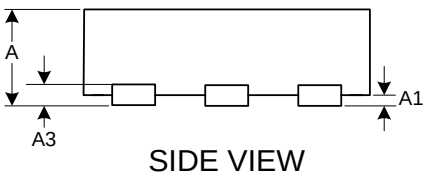


Reel



PACKAGE DESCRIPTION



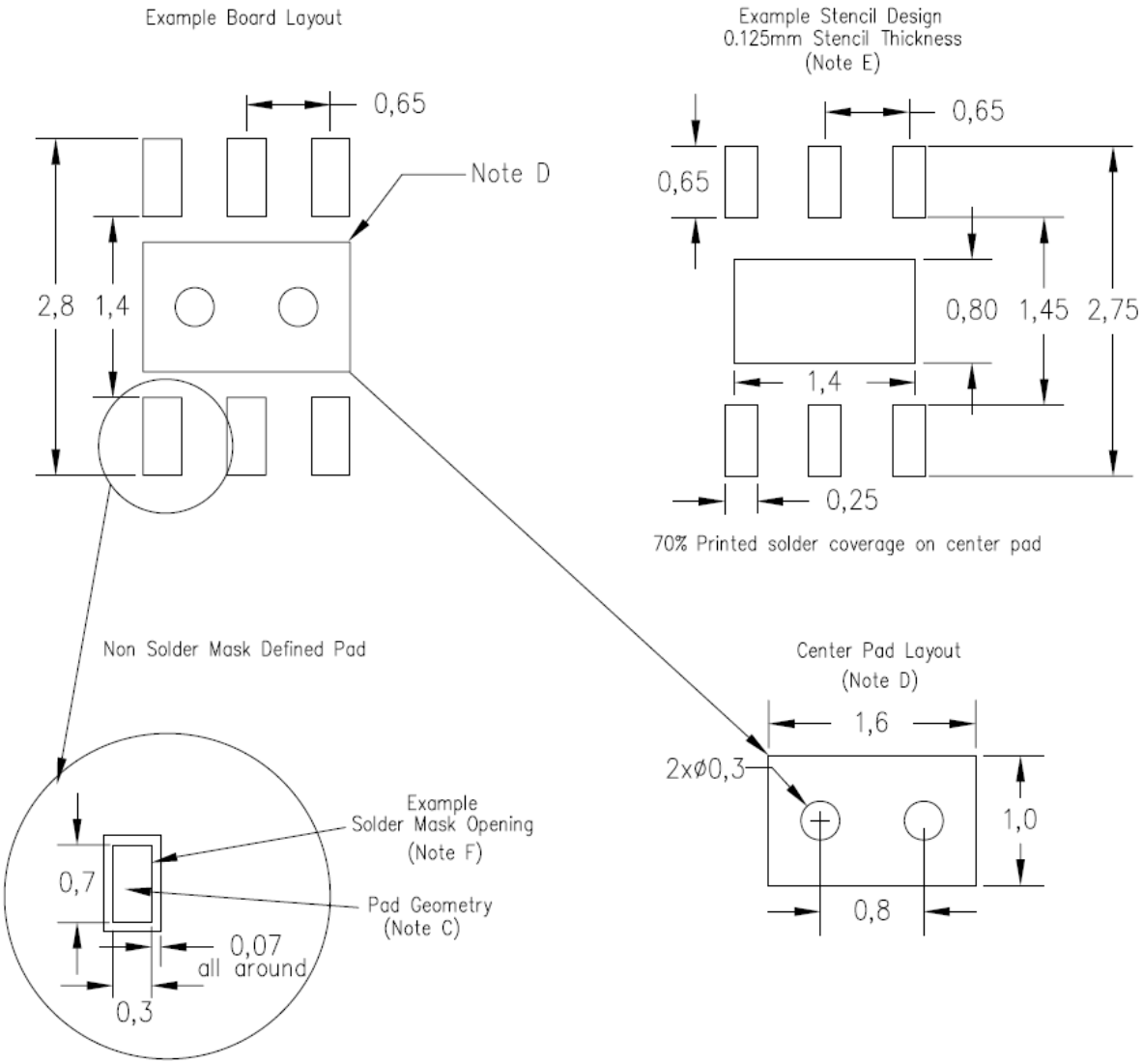


COMMON DIMENSIIONS
(UNITS OF MEASURE=MILLIMETER

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	1.50	1.60	1.70
e	0.55	0.65	0.75
K	0.15	0.25	0.35
L	0.20	0.25	0.30
H		0.20REF	

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-229
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

LAND PATTERN DATA



NOTE A: *All linear dimensions are in millimeters.*

NOTE B: This drawing is subject to change without notice.

NOTE C: Publication IPC-7351 is recommended for alternate designs.

NOTE D: This land pattern is designed to be soldered to a thermal pad on the board.

NOTE E: Laser cutting aperture with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.

NOTE F: Customers should contact their board fabrication site for solder mask tolerances.

REFLOW

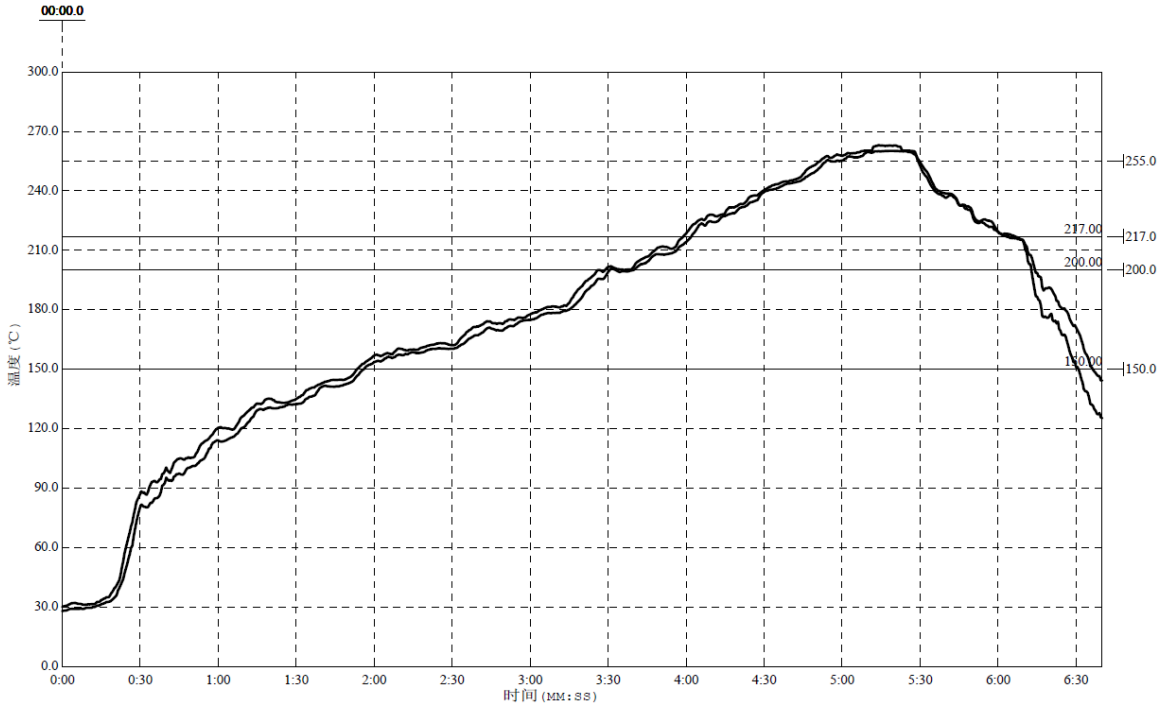


Figure 24 Package Reflow Oven Thermal Profile

Reflow Note	Spec
Average ramp-up rate (217℃ to Peak)	Max. 3℃/sec
Time of Preheat temp.(from 150℃ to 200℃)	60-120sec
Time to be maintained above 217℃	60-150sec
Peak Temperature	>260℃
Time within 5℃ of actual peak temp	20-40sec.
Ramp-down rate	Max. 6℃/sec
Time from 25℃ to peak temp	Max. 8min.

REVISION HISTORY

Vision	Date	Change Record
V0.9	August 2014	Datasheet V0.9 Released
V1.0	March 2015	Datasheet V1.0 Released
V1.1	May 2015	1、 Refreshed C_{IN} information 2、 Refreshed Figure 5 3、 Added EMI_CTL register and configuration description.
V1.1.1	June 2015	1、 Added Figure 6 2、 Corrected some literal mistakes.
V1.1.2	November 2015	1、 Added PWM DIMMING TIMING information in the Electrical Characteristics 2、 Corrected some literal mistakes.
V1.1.3	May 2016	1、 Updated UVLO parameters.
V1.1.4	May 2016	1、 Updated Manufacture data code.
V1.1.5	June 2017	1、 Added Pin1 indicating information 2、 Updated characteristic part.
V1.1.6	November 2017	1、 Added MSL Level 2、 Added User Direction of Feed
V1.1.7	January 2018	1、 Delete the Chinese introduction of the first page 2、 Added Environmental Information
V1.2	January 2018	1、 Changing the threshold of θ_{JA} from 65℃/W to 120℃/W 2、 Delete the picture of the external PWM Dimming network

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