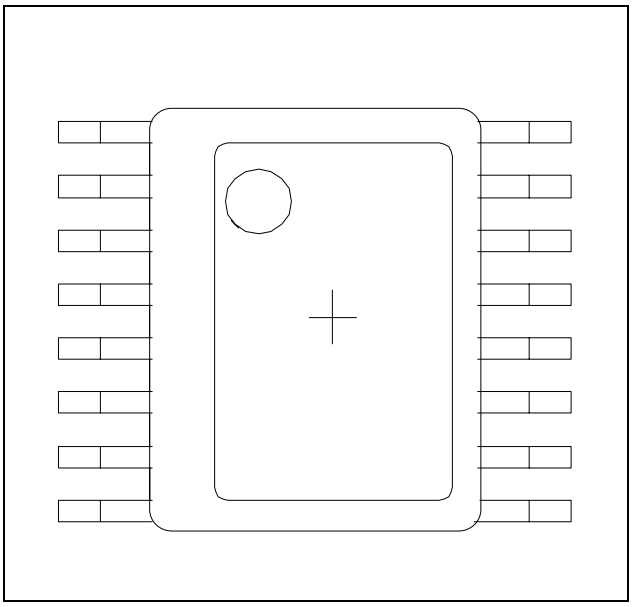
AWT1902
TX POWER MMIC
Advanced Product Information
Rev 3

DCS1800/PCS1900 GaAs 4.8 V Single Supply Power Amplifier IC

DESCRIPTION

The AWT1902 is a 3 stage monolithic Power Amplifier IC suited for DCS 1800 (1710-1785) and PCS1900 (1850-1910) cellular telephone applications



FEATURES

- High Output Power
- High Efficiency
- Built in Pulse Control
- 16 Pin SSOP Plastic Package.
- 50Ω Input Impedance
- Low Cost
- Single Supply

1. Maximum Ratings

Static sensitive electronic devices. Do not operate or store near strong electrostatic, fields. Take proper ESD precautions.

PIN	RATING	NOTES
Pin 1 - V_{D1}	+7.5V max., 0 V min.	
Pin 2 - V_{REF}	+ 5V max., 0 V min.	If V_{REF} is kept high and not pulsed, the amplifier may draw very high currents and permanent damage may occur.
Pin 3 - RF_{IN}	+ 12 dBm max.	AC coupled only, do not apply DC voltage.
Pin 5 - V_{DB}	+ 7.5V max., 0 V min.	
Pin 6 - V_{SS}_IN	- 7.5 V	V_{SS}_IN must be between -3V and -5V to allow proper operation.
Pin 8 - V_{DC}	+ 7.5V max., 0 V min.	
Pin 9 - V_{D2}	+ 7.5V max., 0 V min.	
Pin 12,13,14 - V_{D3}, RF_{OUT}	+ 7.5V max., 0 V min.	

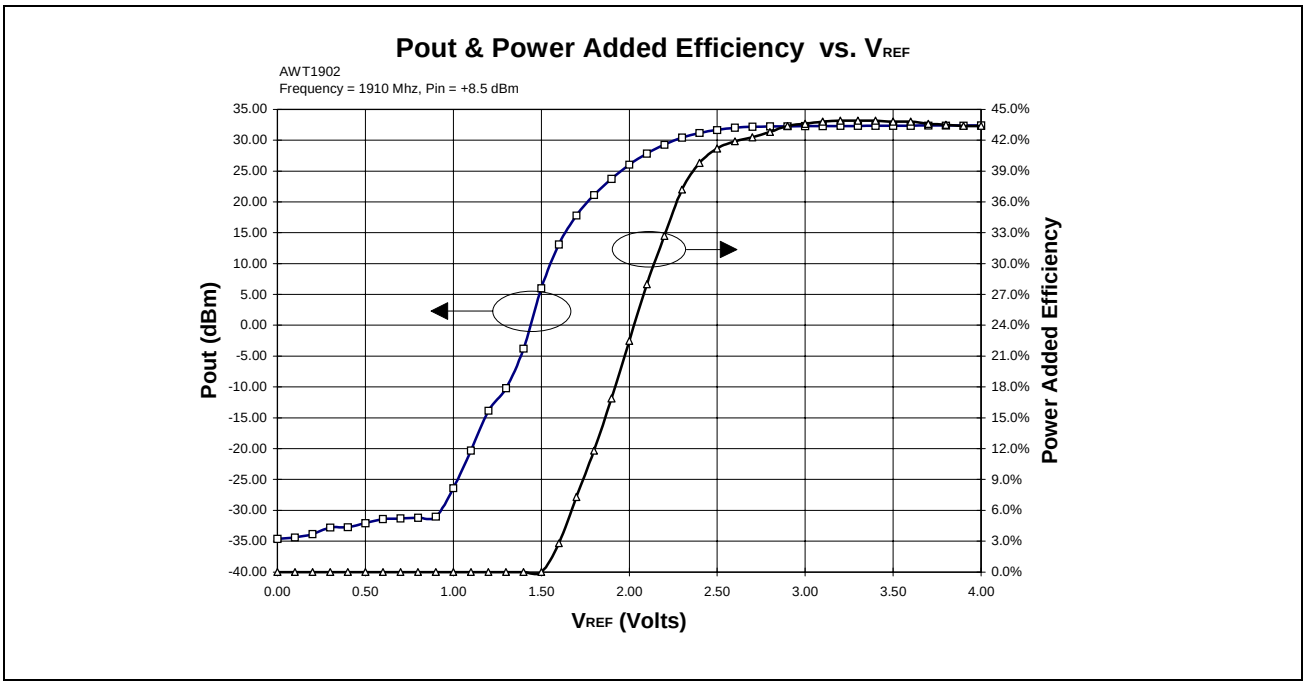
2. ELECTRICAL CHARACTERISTICS:(1)

(Pin = + 8.5 dBm, V_D= + 4.8 V_{DC}, V_{REF} Pulsed @ 577 µS/12.5% Duty, 0.5V - 3.6V max.
External clock or V_{SS} = - 4V. Tc = 25^{O}C, Zo= 50Ω.

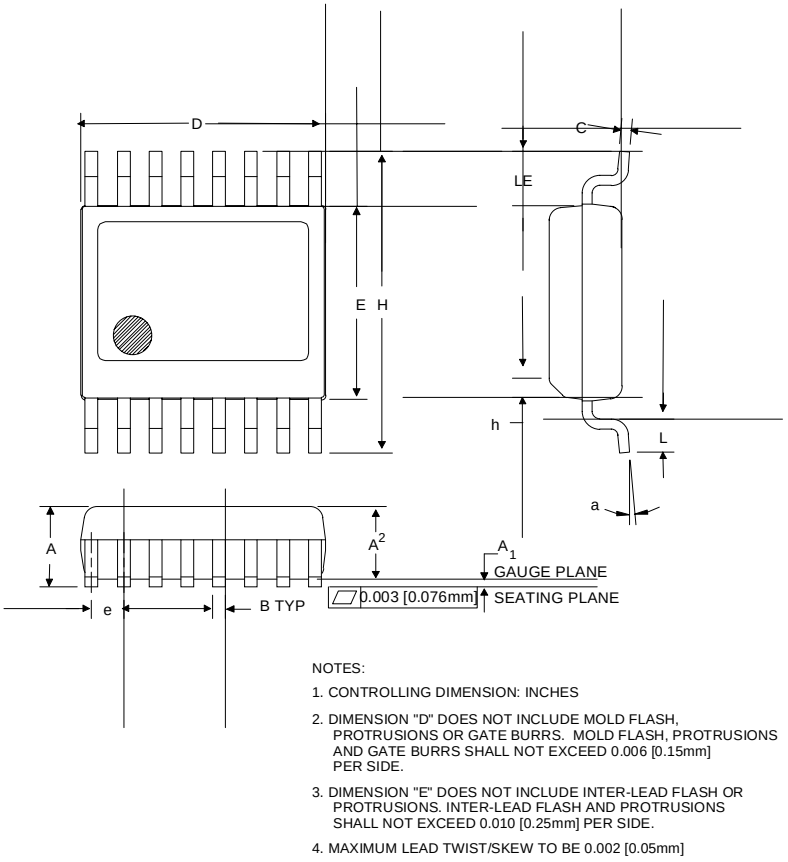
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	PARAMETER
Frequency(2) DCS OR PCS	fo	1710 1850		1785 1910	MHz
Power Output @ V_{REF} = 3.6V	P_{OUT}		32		dBm
Power Added DCS Efficiency or @ P_{OUT} = 32 dBm PCS	PAE		45 40		%
Harmonics	2fo 3fo		- 35 - 40		dBc
Stability: < -80 dBc, all spurious outputs relative to desired signal			6:1		VSWR load, all phase angles, P_{OUT} ≤ 32dBm V_{DS} = + 4.8V Zs = 50 Ω
Input Return Loss	RTN_{IN}		10		dB
Temp		-20		+70	

1. As measured in ANADIGICS test fixture.
2. Operating frequency band is dependent on external matching, see page 5 for test fixture schematic.

3. DATA



4. Package Outline and Pin Description



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A_1	0.004	0.008	0.10	0.20	
A_2	0.052	0.062	1.32	1.57	
B	0.008	0.012	0.20	0.30	
C	0.006	0.009	0.15	0.25	
D	0.189	0.196	4.80	5.00	2
E	0.149	0.157	3.78	3.99	3
e	0.025 BSC		0.63 BSC		4
H	0.228	0.246	5.79	6.25	
h	0.014	0.016	0.36	0.41	
L	0.016	0.032	0.41	0.81	
LE	0.039	—	0.99	—	
a	0	8	0	8	

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE 0.002 [0.05mm]

Pin	Signal	Description
1	V_{D1}	1st stage drain supply (4.8V)
2	V_{REF}	Output Power control, Should be set to level that corresponds to the desired output power . Pulse control voltage (V_{REF}, 0 to 3.6V)
3	RF_{IN}	RF power input
4	GND	RF and DC Ground
5	VDB	Bias circuit supply (+ 4.8V, 3-4 mA)
6	CB/V_{SS}_IN	CB and Negative Supply (- 4.4 V)
7	CA	CA
8	N/C	
9	V_{D2}	2_{ND} stage drain supply (+ 4.8 V)
10,11	GND	RF and DC Ground
12,13,14	V_{D3}/RF_{OUT}	3_{RD} stage drain supply and RF_{OUT}
15,16	GND	RF and DC Ground

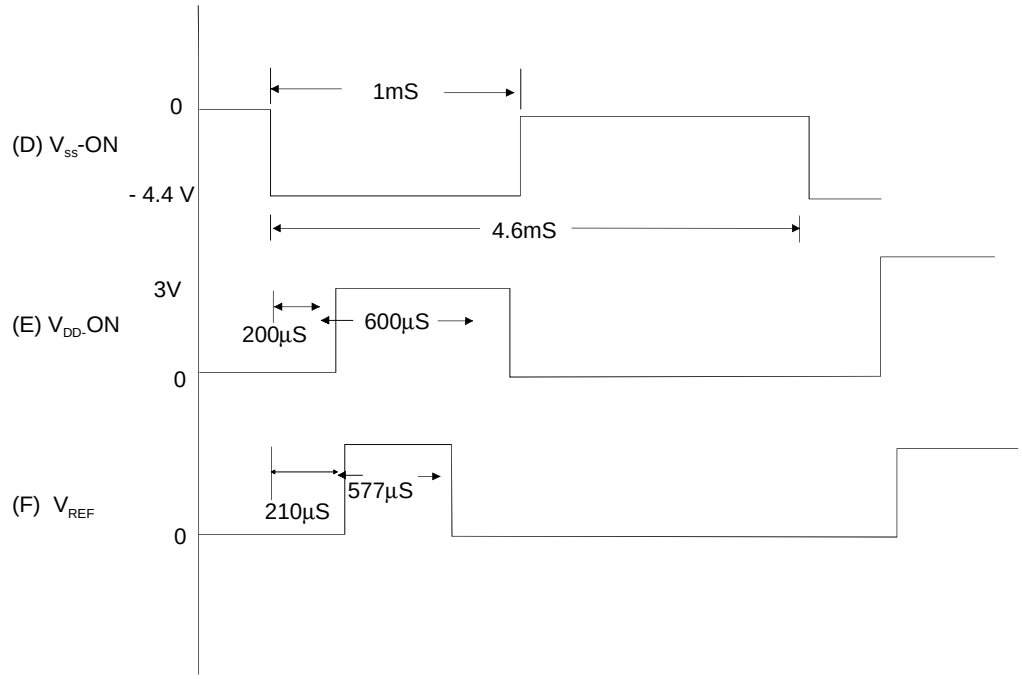
5. Power Amplifier Evaluation Test Fixture Operation Procedure.

Power Up: Dual supply operation, (for Single Supply operation please contact ANADIGICS).

A. Begin by setting all power supplies to zero volts.
B. Set the RF input power level to +8.5 dBm
C. Set V_{DC} and V_{BAT} to + 4.8 volts.
D. Apply a periodic square wave (PRF=217Hz, pulse width = 1m Sec, amplitude = -4.4V) to V_{SS}-ON. (pin 6).
E. Apply a synchronized periodic square wave (PRF=217Hz, pulse width = 600 μSec, pulse delay = 200μSec, amplitude = 3V) to V_{DD}_ON. This signal turns on the pass transistor, which then applies positive voltage (VBAT) to the drains of the amplifier.
F. Pulse V_{REF} (power control) with a synchronized periodic square wave (PRF=217Hz, pulse width = 577 μSec, pulse delay = 210μsec), and adjust its' amplitude for a desired output power ($0V < V_{REF} < 3.6V$). Make sure that the pulse generator is properly terminated, otherwise, you may apply as much as twice the generator voltage to the V_{REF} pin.

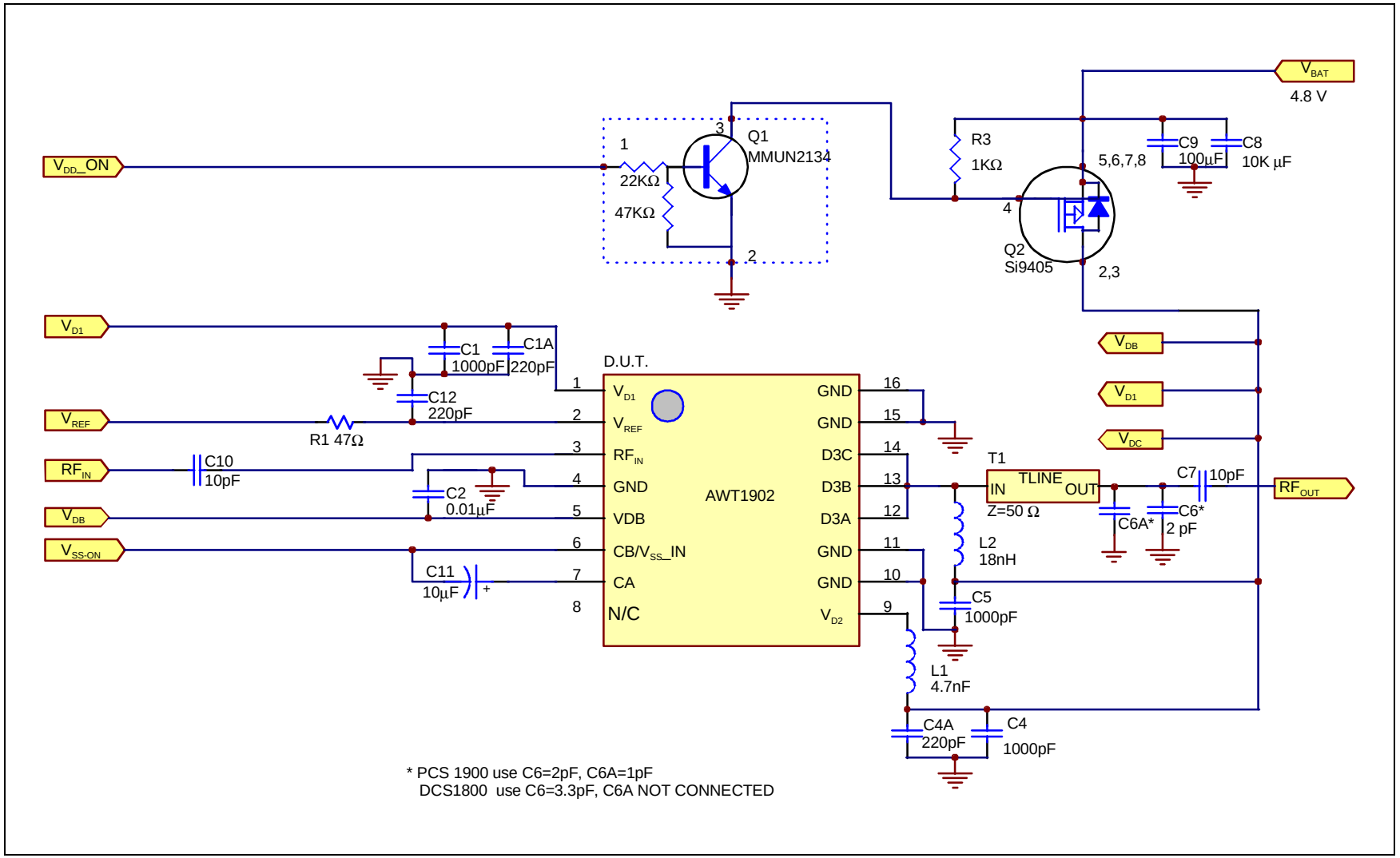
Note: The square wave signals in steps E and F are synchronized to the square wave signal in step D. Furthermore, the pulse widths and delays in steps D through F, (timing sequence), should be tailored for each system application. The important point to remember, is to ensure that negative voltage is always present during the time the power amplifier is operating (positive voltage applied to drains). Please see timing diagram shown below.

Power Down
To power down the device follow the above procedure in reverse order.



AWT1902 Evaluation Test Fixture Timing Diagram

AWT1902 Evaluation Test Fixture Schematic



COMPONENT	VALUE	SIZE
C1,C4,C5	1000 pF	0603
C1A,C4A,C12	220 pF	0603
C7,C10	10 pF	0805
C6	* 2 pF	0603
C6A	*1 pF	0603
C8	10,000 μF	-
C9	100 μF	-
C2	0.01 μF	2410
L1	4.7 nH	0603
L2	18 nH	1008
R1	47 ohms	0603
R3	1K ohms	0603
T1	Z_O = 50	
Q1	MMUN2134	MOTOROLA
Q2	SI9405	SILICONIX

* PCS1900 use C6 = 2pF, C6A = 1pF, DCS1800 use C6 =3.3pF, C6A Not Connected